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The Mechanical Performance of Sn-Pb Solder Joints on LTCC Substrates

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Abstract

The assembly of ceramic components often use soldering technologies to attach metal structures to the ceramic base material. Because many suitable solder alloys do not readily wet-and-spread on ceramics, a metallization layer is deposited on the latter to support wetting and spreading by the molten solder for completion of the joint. The metallization layer must be sufficiently robust to retain its integrity though the soldering process as well as not negatively impact the long-term reliability of the joint. A study was performed to evaluate the mechanical properties of solder joints made to a 0.200Ti/W-4.0Cu-2.0Pt-0.375Au (μm) thin film metallization deposited on low-temperature co-fired ceramic (LTCC) base materials. The solder joints were made with the 63Sn-37Pb solder (wt.%, abbreviated Sn-Pb). A pin pull test was developed to measure the tensile strength of the solder joint as a function of soldering parameters. Failure mode analysis was a critical metric for assessing the roles of interfaces, bulk solder, and the ceramic on mechanical performance. The Sn-Pb solder joints experienced a nominal strength loss with increased severity of the soldering process parameters. The strength decline was attributed to changes in the solder joint microstructure and not a direct degradation to the thin film structures.

Key words: Thin film conductor, low-temperature co-fired ceramic, pin pull strength, soldering process conditions.

Introduction

Ceramic substrates have traditionally been specified for printed circuit boards (PCBs) that must meet the performance requirements of radio-frequency (RF) electronics or to minimize the thermal mechanical fatigue (TMF) degradation of solder joints belonging to large ceramic components (e.g., capacitors, filters, etc.). Today, these PCBs are also being targeted for use in high-temperature electronics that provide in-situ monitoring of oil, gas, and geothermal wells (Fig. 1). Down-hole temperatures are typically 150 – 200°C, but can peak at 300°C. Similar conditions exist for the very high reliability electronics that are aboard deep-space probes exploring the planet, Venus, or the Sun [1 – 3].

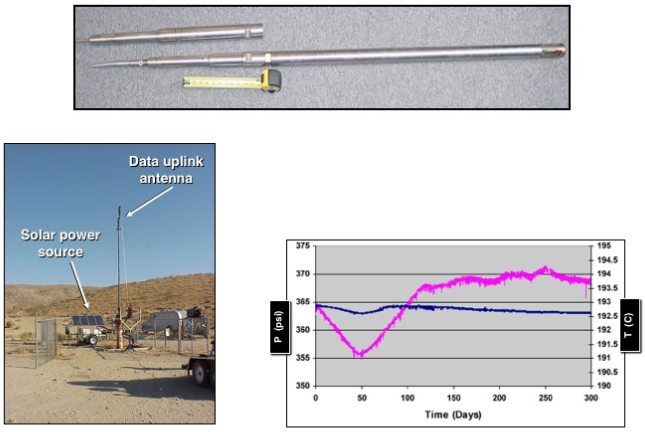

Figure 1 Photographs show the Navy/Sandia Coso down-hole tool and test site. The graph shows the extreme pressure and temperature conditions under which the tool operated without failure for nearly one year.

Electronics based on ceramic PCBs are referred to as *hybrid microcircuits (HMCs)*. Traditionally, HMCs used an alumina ceramic substrate, an example of which, is shown in Fig.2a. Traces and bond pads were created from pastes that were a combination of metal particles, typically Ag, Au-Pd, or Au-Pt-Pd alloy; a glass frit; and organic binders. The circuit pattern was formed by printing the paste through a screen or stencil sheet that duplicated that pattern. Once the paste was printed on the ceramic surface, it was dried to drive off the organic binder and then fired at 850 – 900°C for 15 – 30 min in air. The firing step sintered the metal particles together to form an electrically conductive layer; it also caused the glass frit to melt and diffuse to the metal layer/ceramic surface where it bonded the two materials together. Lastly, the ceramic substrate was assembled with components using the same solder processes as are used with traditional laminate PCBs, creating the HMC assembly shown in Fig. 2b.

Alumina substrates are generally limited to having circuitry on one or both surfaces because of the difficulty of creating internal conductor layers. Signal transmission between the two sides is achieved by edge clips or holes that are mechanically drill through the substrate. If the substrate is sufficiently thin (< 0.5 mm), the holes can be formed by laser drilling. The hole or *via* walls were covered with the same thick film conductor

and fired to create a continuous electrical path. These "through-ceramic" holes provide adequate reliability for the circuit; but, they can add significant manufacturing costs to the product.

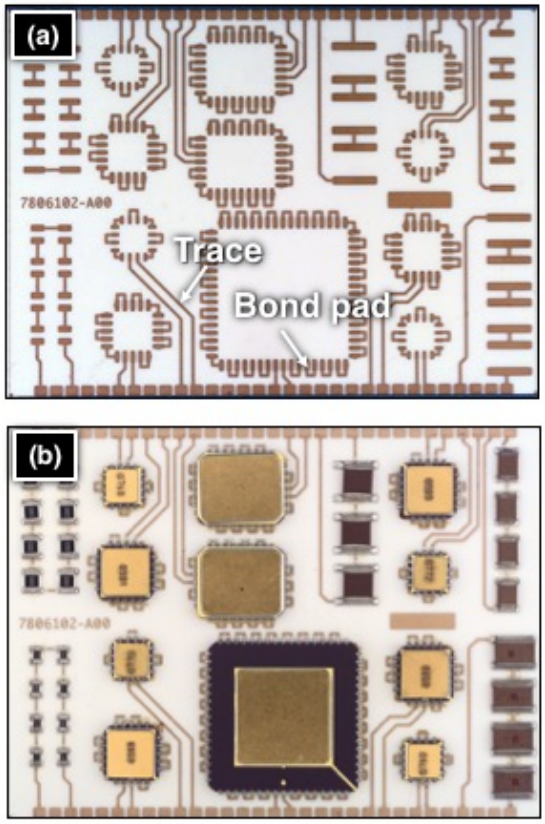

Figure 2 (a) Photograph shows an alumina substrate having traces and pads formed from a Au-Pt-Pd thick film. (b) HMC assembly is shown with the components soldered to the bond pads.

Unfortunately, even the above two-layer HMC technology based on screen printed, thick film conductors, has reached its engineering limits with respect to supporting the further miniaturization and increased functionality of electronic products. The answer to the two-layer limitation was the development of low-temperature, co-fired ceramic (LTCC) substrate technology. The LTCC ceramic attains a multilayer construction similar to laminate PCBs using the stack-up of individual "tape" layers, each having a thick film, circuit pattern printed and dried on it. The layers, which include vias that connect them together, are pressed and fired at elevated temperatures (800 – 850°C) to complete a bond that is both electrically conductive and mechanically strong.

Although LTCC provided an answer to the need for multiple substrate layers, thick film conductor technology has become the bottleneck towards further miniaturization of HMC electronics. The screen printing-drying-firing process has reached its limits with respect to providing minimum line widths and spacings that can support solder processes and provide interconnections that meet long-term reliability requirements. The reliability limitation became particularly apparent in the development of thick film/LTCC PCBs for multi-chip module (MCM) sub-assemblies [4].

An alternative approach is to replace thick film conductors with thin film layers. The thin films are deposited by physical vapor deposition (PVD) techniques – evaporation or sputtering. The glass adhesion layer is replaced with a thin film metallization such as titanium (Ti) or chromium (Cr). On top of the adhesion layer is deposited the *solderable finish*. The solderable finish is the layer to which the solder joint is made. Common solderable finishes include copper (Cu), nickel (Ni), and platinum (Pt). The solderability of the layer is maintained by adding a *protective finish* on top of it. Often-used protective finishes include gold (Au), silver (Ag), and tin (Sn). While the adhesion layer is typically only fractions of a micron thick, the other layers can have thicknesses that vary over several microns, depending upon the soldering process, signal transmission properties, and long-term reliability requirements.

The particular advantage of thin film conductors is that the corresponding circuit pattern can be made with increasingly finer features to support further miniaturization. Circuit definition can be achieved by one of three methodologies: (a) shadow masks, (b) photoimaging as is similarly used in the microelectronics industry, and (c) laser ablation. The use of shadow masks provides a rapid means to define the metallization pattern. However, its drawback is a limitation on feature definition due to the combination of minimum mask feature dimensions and proximity of the mask to the substrate surface.

The photoimaging process can realize considerably finer lines and spaces. Ultraviolet light passes through a glass mask to define the pattern on a photosensitive film or *resist* covering the thin film metallization. The unexposed film is removed by chemicals; the exposed metallization is removed by plasma etching, leaving behind the desired circuit pattern under the exposed photosensitive layer. The latter layer is removed by a different chemical removal step. Drawbacks include capital equipment costs; time duration to plasma etch away the thin film, which increases with the latter's thickness. Also, prolonged etching times can expose the substrate surface to temperatures of 150 – 200°C.

The third technique is laser ablation [5]. The particularly advantage comes with thicker film layers because it reduces both process time and temperature rise at the substrate while still providing feature resolution equivalent to that of photoimaging techniques. Besides capital equipment costs, its other drawbacks include metal and substrate spatter as well as surface micro-cracks and general roughness that may impact high-frequency, RF signal performance. See Fig. 3 for an example of a laser ablated surface.

Hybrid microcircuit products have been developed at Sandia National Laboratories using a thin film-on-LTCC technology. The metallization stack was as follows: 0.200 µm Ti adhesion layer, 4.0 µm copper (Cu) signal layer, 2.0 µm Pt solderable finish, and 0.250 µm Au protective finish. The relatively thick

metallization required plasma etching as the photo definition process. Titanium was selected as the adhesion layer based upon its success on alumina ceramics. An extensive study was conducted that is similar to that reported below, which examined the adhesion strength of the Ti-Cu-Pt-Au system when soldered with the 63Sn-37Pb solder (wt.%, abbreviated Sn-Pb) and 95.5Sn-3.9Ag-0.6Cu (SAC396) Pb-free solder [6]. The thin films withstood exposure to molten solder as well as long-term, solid-state aging at temperatures as high as 170°C and time periods as long as 200 days.

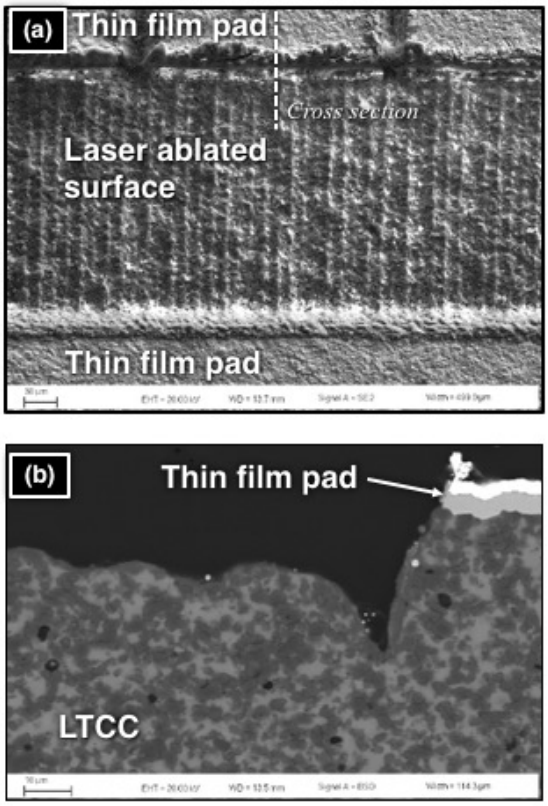

Figure 3 (a) SEM photograph shows laser ablated, LTCC surface used to define the thin film pads. (b) SEM image shows the cross section between the ablated (left) and non-ablated (right) region; the latter is under the thin film.

Nevertheless, the microanalysis of metallographic cross sections uncovered localized separations between the Ti layer and the LTCC, specifically, at the Ti/SiO_2 interface. This anomaly was sensitive to the conditions of the LTCC surface, which were difficult to control as part of the overall process. As a result of these findings, a task was initiated to explore alternative adhesion layers having improved bonding to the LTCC surface. Candidate layers included chromium (Cr), zirconium (Zr), silicon (Si), and the titanium/tungsten (Ti/W) alloy. Chromium, Zr, and Si can be deposited by evaporation. The deposition of Ti/W layer required establishing a new radio-frequency (RF) sputtering capability. This report describes the results of a study, the goal of which was to assess the processibility and long-term reliability of the 0.200 Ti/W – 4.0 Cu – 2.0Pt – 0.375Au metallization for Sn-Pb solder joints made to LTCC.

A second degradation scenario is the effect of *solid-state aging* on the joint strength. The results from those tests and microanalyses will not be presented in this report in the interest of brevity. Those findings will be provided in a follow-on text.

Experimental Procedures

Materials

The thin film stack used in this study was as follows:

- 0.200Ti/W – 4.000 Cu – 2.000 Pt – 0.375 Au (μm)

The Ti/W film served as the adhesion layer. The Ti/W ratio was determined to be $Ti_{1.5}/W_{3.5}$ using spectral analysis techniques, the details of which, are provided in the results section. The Cu layer supported electrical signal conduction. The Pt layer served as the solderable finish. The 0.375 μm thick Au layer was the protective finish. The Ti/W film was deposited by RF sputtering. The Cu and Pt layers were also deposited by RF sputtering in the same chamber without a break in the vacuum condition. The Au layer was evaporated on the Pt layer in a second chamber. The limited oxidation of the Pt layer allowed the test pieces to be exposed to the air environment prior to the Au deposition. Initial attempts were made to deposit the Ti/W film by RF sputtering; break the vacuum; and move the test pieces into the evaporation system to deposit the Cu, Pt, and Au layers. However, the Cu layer exhibited very poor adhesion to the Ti/W film using this process sequence.

The LTCC substrates were fabricated using Dupont™ 951 tape (Dupont is a registered trademark of the E.I. Dupont de Nemours Corp., Wilmington, DE). The test vehicle and pin used to perform the pull test are shown in Fig. 4. The post-fired substrate thickness was 0.914 mm. The test specimen had an x-y footprint of 25.4 mm x 25.4 mm. The substrates were not subjected to additional surface preparation steps (e.g., polishing) other than those routinely performed at the manufacturer. This surface condition is typically the starting point from which a thin film circuits were created with the LTCC substrate. A pattern of nine test sites was used to assess thin film adhesion. The pattern was created by sputtering the Ti/W layer through an aperture mask followed by the Cu and Pt then lastly, evaporation of the Au layer through the same mask.

Copper pins were soldered to each pad using the 63Sn-37Pb solder (wt.%, abbreviated Sn-Pb). A specially designed fixture held the LTCC substrate and pins for the soldering process (Fig. 5). Solder paste was dispensed onto each pad and the substrate was placed onto the fixture base plate (Fig. 5a). The Cu pins were fed through a frame that held them in an upright position. The frame was attached to the base plate after which, the pins were lowered onto the solder paste deposit (Fig. 5b). The entire assembly was placed into the furnace to complete the soldering

process. Once the fixture had cooled to room temperature, the test specimen – substrate-plus-soldered pins – was cleaned of flux residues and inspected for solder joint quality (Fig. 5c).

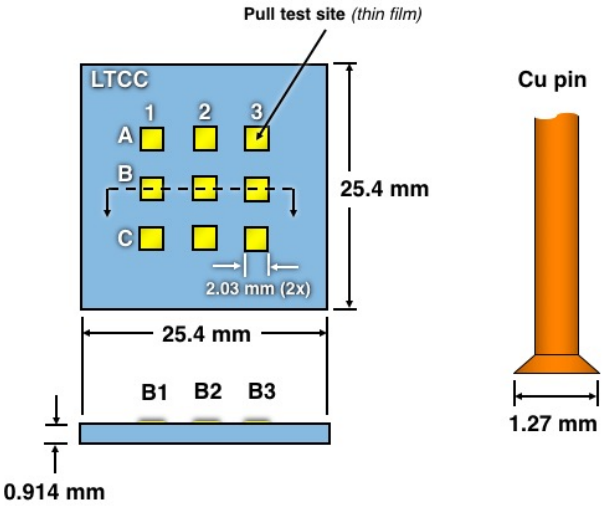

Fig. 4 LTCC pull test specimen and the Cu pin

This study evaluated the solder joint strength as a function of the *soldering process*. Potential degradation mechanisms include (a) incomplete dissolution of the Au layer; (b) excessive leaching of the Pt layer that exposed the Cu layer to dissolution by molten solder; and (c) excessive intermetallic compound (IMC) layer development between the solder and Pt thin film layer. In addition, exposure of the Ti/W-Cu-Pt-Au to the high temperatures of the soldering process could potentially lead to delamination between individual layers or an adhesion loss between the Ti/W layer and LTCC surface.

The soldering process variables included exposure time to the molten solder and the molten solder temperature. The time durations were:

- 15s, 60s, and 120s.

These values took into account the range of automated soldering processes. The molten solder temperatures, which are listed below, were likewise based upon typical soldering assembly processes:

- 215°C, 240°C, 260°C, and 290°C

Duplicate samples were fabricated and tested for each combination of solder temperature and time duration.

All pull tests were performed in a mechanical test frame. The displacement rate was 10 mm/min. Eight of the nine solder joints were pull tested per sample, leaving one joint for cross section and microanalysis. The pull strength was represented by the mean and the standard deviation of the sixteen (16) data points.

Failure mode analysis was also performed on the test samples. There were four predominant failure modes were:

- *Solder failure:* crack path that remains in the solder and/or associated IMC layers;
- *Thin film delamination*: a separation of the Ti/W layer from the LTCC surface.
- *Thin film peeling*: separation along the interface(s) between layers within the thin film stack.
- *Divot failure*: loss of bulk LTCC from under the joint area

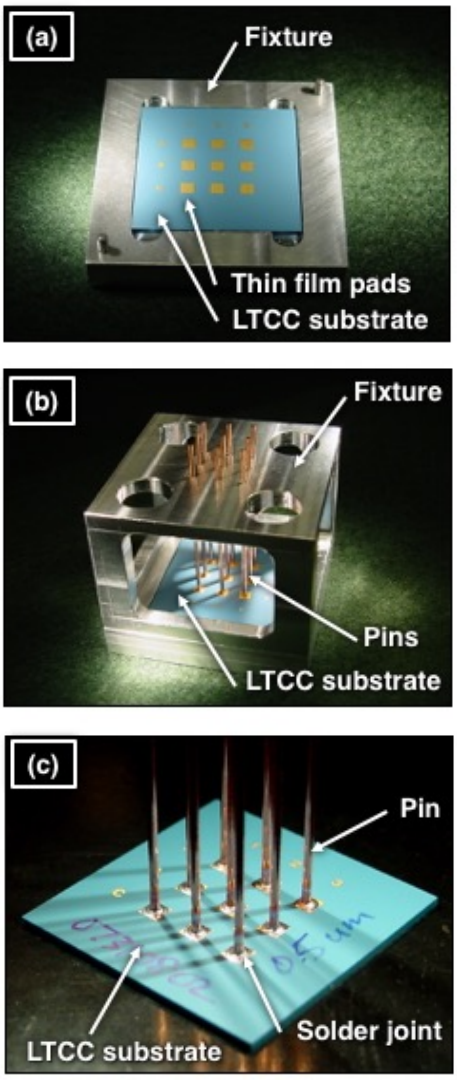

Fig. 5 (a) LTCC substrate is located into the base plate of the fixture. (b) Fixture is assembled with the LTCC substrate; solder paste; and pins in place. The entire assembly would be placed into the furnace to make the joints. (c) Photograph of the final test specimen.

Scanning electron microscope images will be presented that illustrate these failure modes in the discussion, below.

The failure mode analysis methodology began with each pull-tested site being assigned one of the four failure modes that predominated the fracture surface. A further discrimination was not made between minor failure modes because, in general, there was one mode that controlled the fracture for each pin pull test. The failure modes were added up and the percentage determined by dividing that count by sixteen (16), which is the total number of test sites.

Results and Discussion

Spectral analysis of the Ti/W-Cu-Pt-Au thin film

The Ti/W-Cu-Pt-Au thin film was evaluated using scanning transmission electron microscopy (STEM). The specimen was prepared by the focused ion-beam (FIB) cutting process using Ga ions. The STEM image is shown in Fig. 6. The Cu and Pt layers developed with largely columnar grain structures. A small demarcation line was observed near the top of the Pt layer. The columnar grain structure appeared to be continuous across the line, which implies that the source of the artifact did not significantly interrupt the deposition process and, as such, did not introduce a material defect in the Pt layer.

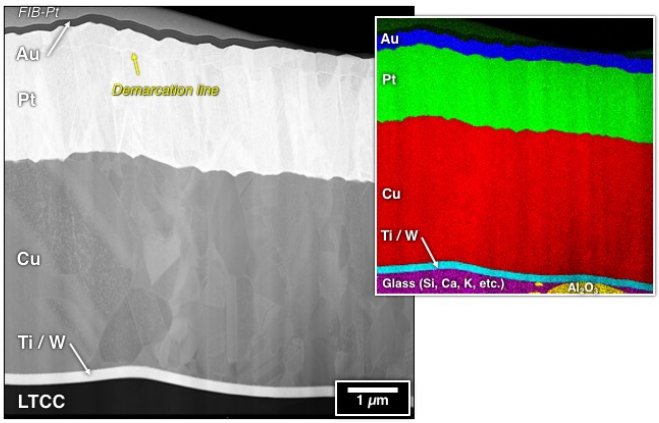

Fig. 6 STEM image shows the as-deposited, Ti/W-Cu-Pt-Au layer. A faint demarcation line is identified in the layer. The inset picture is the annular spectral image that identifies the elements by color, including the different phases in the LTCC.

The inset picture is an annular spectral image that identified the elemental construction of the layer: blue, Au; green, Pt; red, Cu; cyan, Ti/W; magenta, the silica-based glass component of the LTCC; and yellow, the alumina particles also within the LTCC base material. An important observation is that the Ti/W layer exhibits excellent adhesion to the silica-based, glass component of the LTCC base material, which was a shortcoming of the Ti adhesion layer. Besides a potentially improved intrinsic interaction between the Ti/W layer and glass, the higher energy, RF deposition process may also have contributed to an improved adhesion performance by partially sputtering the LTCC surface. Interdiffusion was also absent between the individual layers. Lastly, quantitative data, which were obtained from this analysis, determine the Ti/W layer composition to be $Ti_{1.5}/W_{3.5}$.

A high magnification image is shown in Fig. 7 of the Ti/W layer. A faint demarcation line was also observed, which as was the case with the Pt layer, above, was likely caused by a brief interruption of the deposition process. Although the gray tone implies a slightly lower material density, discontinuities such as voids and cracks were not associated with the demarcation line. General porosity was limited to less than 5 nm size. The layer had excellent adhesion to the LTCC substrate. Excellent adhesion was also confirmed between the Cu and Ti/W layers.

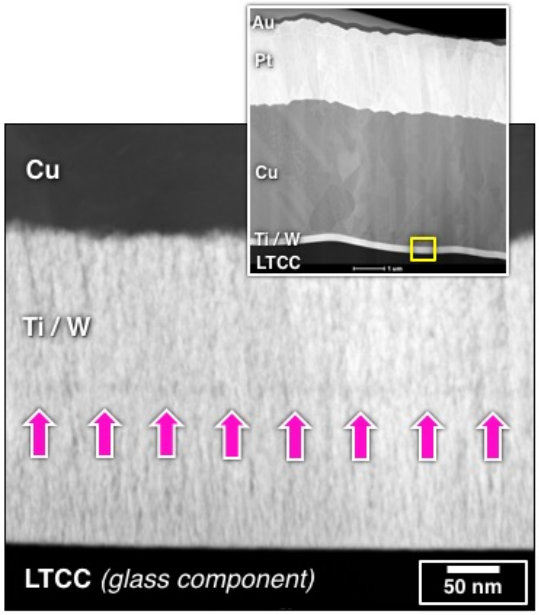

Fig. 7 High magnification, STEM image shows Ti/W-Cu-Pt-Au layer at the location of the film. A faint demarcation line is identified in the Ti/W layer by the magenta arrow.

Effect of soldering process parameters on *pull strength*

The pull strength data are shown in Fig. 8 as a function of the process temperature. The blue circles, magenta squares, and red diamonds represent the 15s, 60s, and 120s data, respectively. The pull strengths are presented in load (lb.). Tensile stresses were calculated at minimum and maximum load values bounding the data. The very high pull strengths reflect the plain strain effect resulting from the confined geometry created by the thin gap and the wide footprint of the joint. The strength enhancement is demonstrated, by comparing the data in Fig. 8 with the tensile strength of bulk Sn-Pb solder, which is 5.8 – 7.3 ksi (40 – 50 MPa) at a similar displacement rate [7]. A minor, yet statistically significant difference, was observed between the 15 s interval versus the 60s and 120s soldering times, but for only the 240°C and 260°C soldering temperatures. The short error bars indicate the excellent reproducibility of the strength values.

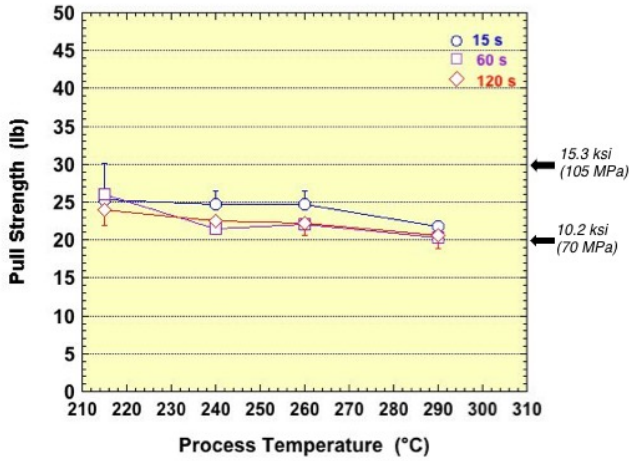

Fig. 8 Pull strength is shown as a function of process temperature for each of the three process time intervals. The tensile stresses were calculated for the 20 lb. and 30 lb. loads to illustrate these limiting cases – those values are shown at the right of the graph.

Effect of soldering process parameters on *failure mode*

The failure mode results are presented in Fig. 9 for the test vehicles assembled by soldering for 15 s. At the soldering temperature of 215°C, 50% of the test sites exhibited failure within the solder joint (blue bar); the remainder of the failures were evenly split (25%) between thin film delamination at the Ti/W-LTCC interface (yellow bar) and fracture by the LTCC divot mode (red bar).

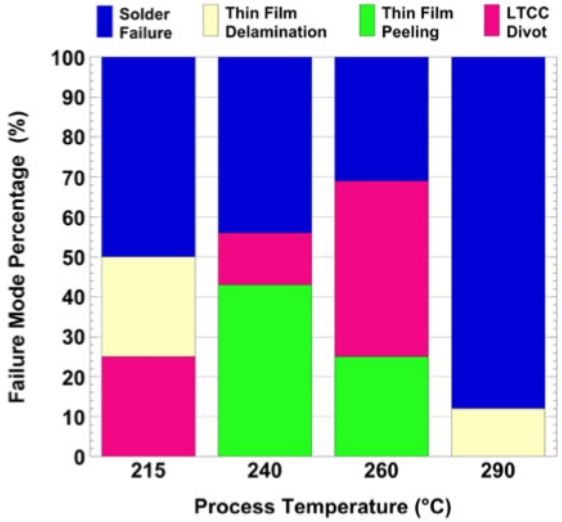

Fig. 9 Bar chart shows the percentage of the observed failure modes as a function of solder temperature for a soldering time of 15 s. Each of the four failure modes is distinguished by the color of the bar per the legend above the plot.

An increase of the soldering temperature to 240°C introduced the thin film peeling mode, which replaced the thin film delamination mode and a portion of the solder failure and LTCC divot modes. The thin film peeling mode remained at the higher soldering temperature of 260°C, but to a lesser degree as the LTCC divot mode increased in frequency. The LTCC divot failures have been attributed to residual stresses caused by the mismatch of coefficients of thermal expansion (CTE) between the Cu pin, Sn-Pb solder, and LTCC [6]. This point will be further discussed later in the report. Lastly, when the soldering temperature was raised to 290°C, ninety-percent (90%) of the test sites showed solder failures; the remaining failures were thin film delamination at the Ti/W-LTCC interface.

The failure mode data in Fig. 9 were compared to the pull strength data in Fig. 8. The pull strengths remained essentially unchanged across the 215°C, 240°C, and 260°C soldering temperatures. Yet, a significant variation occurred to the failure modes. This trend implies that, by-and-large, the intrinsic strengths were similar between the microstructural features associated with each failure mode.

When the soldering temperature was raised to 290°C, ninety-percent (90%) of the test sites showed the solder failure mode; the remaining failures were thin film delamination of the Ti/W-LTCC interface. The increased presence of the solder failure mode was accompanied by a small decrease of pull strength as shown in Fig. 8. This trend implies that, in the event that there is a strength loss by the solder joints, the likely culprit can be found in the solder joint microstructure and not the adhesion properties accompanying the thin film layers.

At this point, an analysis is made of the physical metallurgies that characterized each of the failure modes in Fig. 9. The solder failure (blue bar) is illustrated by the scanning electron microscope (SEM) images in Fig. 10. Figures 10a and 10b show the fracture surfaces on the LTCC pad and pin sides of the solder joint, respectively. This joint was made using the process conditions of 215°C and 15 s. Three distinctive regions were identified on the fracture surfaces by the letters: "A,", "B", and "C." Their physical metallurgies were determined with the assistance of the energy dispersive x-ray (EDX) technique.

Region A had a relatively smooth topography in Fig. 10. That topography resulted from intergranular fracture as shown by the higher magnification SEM image in Fig. 11. The accompanying EDX elemental maps indicate that the fracture surface was comprised primarily of Au, Cu, and Sn. Although intermittent areas showed only the Sn signal (white circles), by-and-large, the fracture surface showed all three elements to overlap with one-another (cyan circles). The same surface topography and elemental distributions were repeated on the pin side of the fracture (region A, Fig. 10b).

The failure mode morphology of region A resulted from fracture *through* the $(Cu, Au)_xSn_y$ intermetallic compound (IMC) layer that formed at the solder/Cu pin interface. The Au layer, which topped the thin film stack on the LTCC substrate, dissolved into the molten Sn-Pb solder. While the solder was molten, as well as following solidification, a driving force developed for Au to diffuse to the solder/Cu interface where it was incorporated into the IMC layer. Note that the contribution by solid-state diffusion had taken place *at room temperature*.

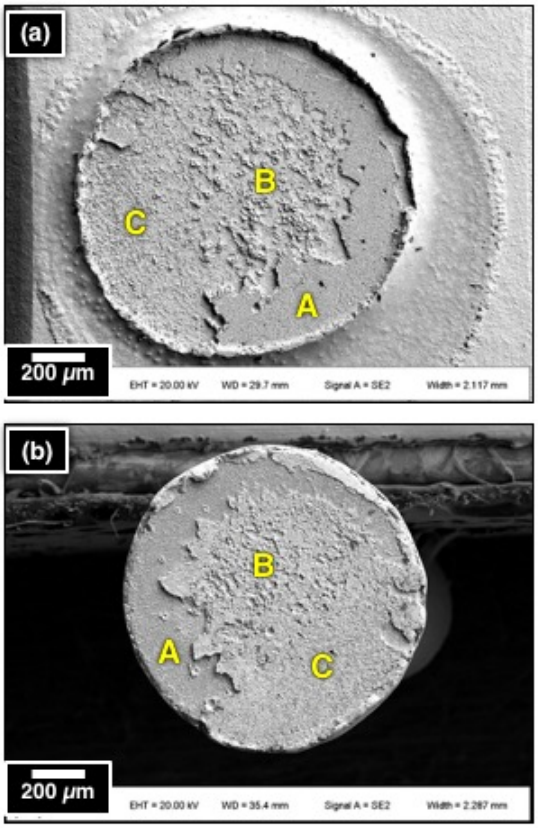

Fig. 10 SEM photographs show the solder failure mode, fracture surfaces belonging to (a) the thin film pad on the LTCC substrate and (b) the corresponding pin. The letters "A," "B," and "C" denote the three surface topographies. The soldering process parameters were 215°C and 15 s

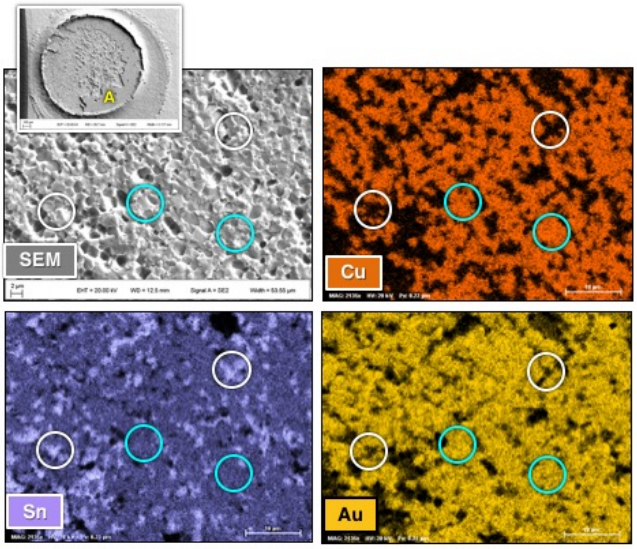

Fig. 11 High magnification, SEM image of the region A (see the inset picture) is shown, together with the EDX maps of Cu, Sn, and Au that predominated the fracture surface (process conditions: 215°C and 15 s). These data were obtained from the pad (LTCC) side of the failure.

The regions B and C were very similar. Their relative heights versus that of region A in Fig. 10 indicated that the fracture surface was closer to the solder/thin film interface. The primary difference between regions B and C was that region B included a greater percentage of failure within the ductile Sn-Pb solder that generated the cup-and-cone fracture surface relief. Therefore, further discussion of this fracture behavior will focus on region C.

A high magnification, SEM image is shown in Fig. 12 of the region C. The EDX maps show the fracture surface to be comprised predominantly of Pt and to a lesser extent, Sn. Lead (Pb) was also observed, which reflected an intermittent fracture in the adjacent, Sn-Pb solder. At first glance, the data suggest that fracture occurred along a Pt_xSn_y IMC layer that formed at the solder/Pt interface after the Au had been dissolved away. However, the yellow circles show that there is *minimal coincidence* between the Pt and Sn signals, which implies that the fracture path did not have a significant association with a Pt_xSn_y IMC layer.

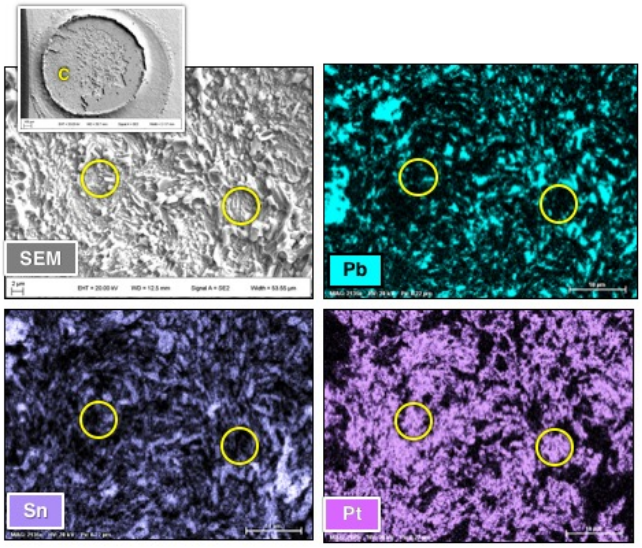

Fig. 12 High magnification, SEM image of the region C (see the inset picture) is shown, together with the EDX maps of Sn, Pt, and Pb on the fracture surface (process conditions: 215°C and 15 s). These data were obtained from the *pad (LTCC) side* of the failure.

In order to confirm the above hypothesis, SEM and EDX data were analyzed of the region C on the *pin side* of the fracture. Those results are shown in Fig. 13. *Platinum was not detected on the fracture surface.* However, there was a significant Au presence. The Pb signal (white circles) is due to localized fracture in the adjoining Sn-Pb solder field as noted earlier. The remaining fracture surface was comprised primarily of overlapping Sn and Au signals. These findings, when coupled with those of the fracture surface on the pad side (Fig. 12) indicate that the Au was not fully dissolved from atop the Pt layer by the molten solder. Rather, some Au remained and reacted with Sn to form a Au_uSn_v IMC layer. The C-region failure mode originated from fracture along the interface

between the Au_uSn_v IMC layer and the Pt layer. Given that region C comprises a significant fraction of the solder failure surface, Au_uSn_v IMC/Pt interface fracture does not necessarily indicate that the latter poses an intrinsic weakness to the joint.

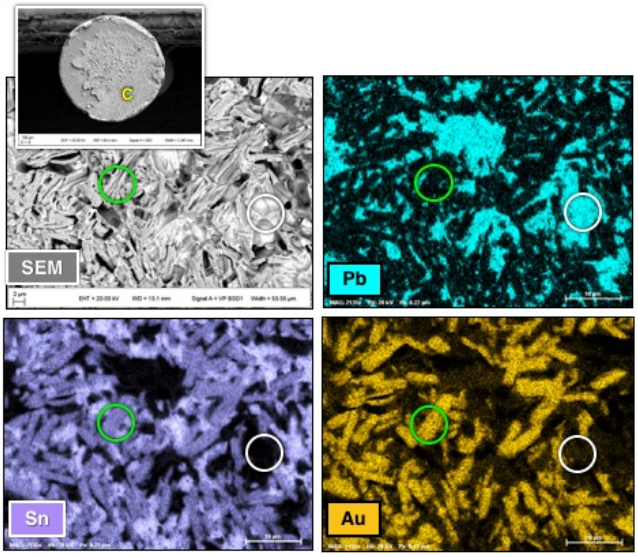

Fig. 13 High magnification, SEM image shows the region C (see the inset picture) together with the EDX maps of Sn, Au, and Pb (process conditions: 215°C and 15 s). These data were obtained from the *pin side* of the failure.

The divot failure mode is illustrated by the complementary SEM images in Fig. 14. Failure initiation occurred in the bulk LTCC material, which is indicated by the letter A in both images. As the LTCC fracture expanded from the pad center (Fig. 14a), it transitioned into a the "fractal" pattern (B) that is the combination of thin film delamination and thin film peeling. As the crack approached the outer edge of the joint, a second transition took place whereby separation was entirely thin film delamination (C). This behavior was documented as an "LTCC divot" failure mode because it predominates the LTCC fracture. Also, given the rapid nature of the LTCC fracture, the remaining fracture surface may not reflect the intrinsic failure mode of the joint in the absence of the LTCC fracture.

The thin film peeling failure mode is illustrated by the SEM images in Fig. 15 and, specifically, location A. This sample was fabricated at 240°C and 15 s. The LTCC pad and pin sides of the fracture are shown in (a) and (b), respectively. A small divot (B) and associated "fractal pattern" (C) were observed in both images. However, the latter fracture paths were secondary to the thin film peeling mode.

The fracture surface appeared to be relatively featureless at the magnifications used in Fig. 15. A high magnification, SEM image is shown of the fracture surface in Fig. 16 (LTCC side). The corresponding EDX maps, together with those from the pin side of the fracture, confirmed that failure took place at the Ti/W – Cu interface. Residual Cu was not observed on the exposed Ti/W film to within the detection limits of the EDX technique.

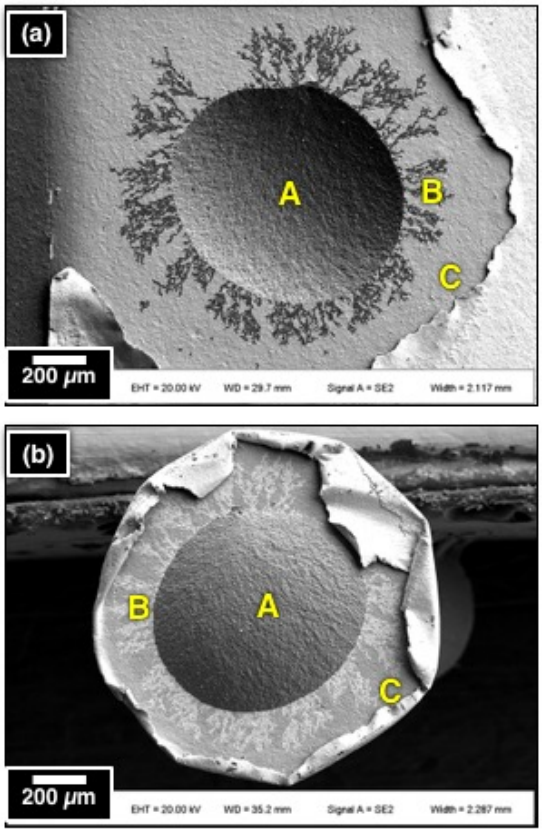

Fig. 14 SEM photographs show the complementary fracture surfaces of (a) the thin film pad on the LTCC substrate and (b) the pin that together illustrate the "LTCC divot" failure mode. The A region is the divot, itself; the B region is a fractal pattern comprised of a mixture of both the "thin film peeling" and "thin film delamination" failure modes The C region is solely the thin film peeling mode. The soldering process parameters were 215°C and 15 s.

At the higher magnification level of Fig. 16, the fracture surface showed significant relief. The Ti/W layer is only 0.200 μm thick so that it replicates the surface topography of the LTCC substrate. The limited thickness of the Ti/W layer also permitted the x-ray signal to sample the chemistry of the LTCC underneath it. The protrusions of the film correspond to the alumina phase of the LTCC (Al map). The glass phase is represented by the Ca signal because the Si signal, which would be generated by the primary constituent of the glass material, silica (SiO_2), is overlapped by the W line of the Ti/W film.

The failure mode percentage data appear in Fig. 17 that were obtained from test sites soldered for 60s. The thin film peeling appeared at the soldering temperature of 215°C; it was no longer observed at 260°C as recorded at 15 s (Fig. 9). The failure mode percentages were nearly identical at 240°C. At the soldering temperatures of 260°C and 290°C, there was a significant increase of the solder failure mode at the expense of the other three modes. This trend implies that, with increasing soldering temperature, the interfaces associated with the thin film structures and the bulk LTCC (divots) had lesser roles in

the fracture behavior while the solder joint microstructural features – bulk solder and IMC reaction layers – had greater effects on mechanical performance.

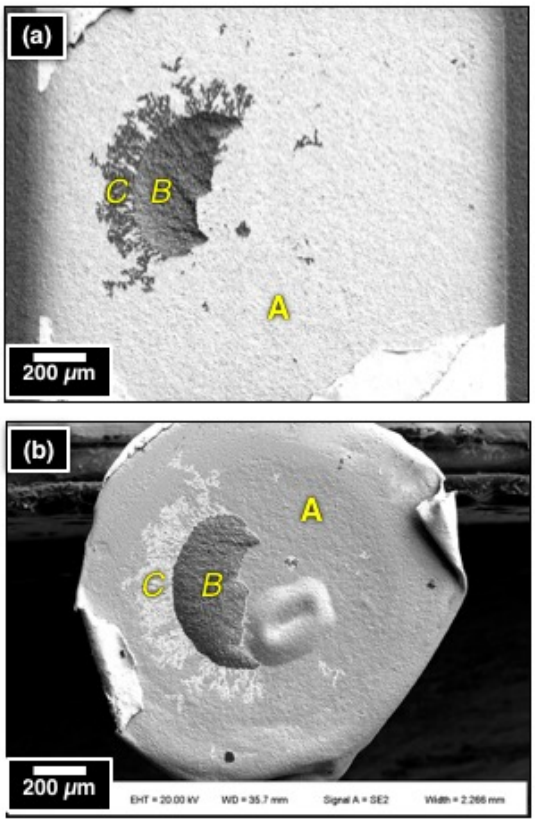

Fig. 15 SEM photographs show the complementary fracture surfaces of the (a) thin film pad on the LTCC substrate and (b) the pin showing the "thin film peeling" failure mode. The A region identifies the film peeling mode. The secondary fracture paths were the LTCC divot (B) and the fractal patterns of thin film delamination and thin film peeling (C). The soldering process parameters were 240°C and 15 s.

The details of the fracture surface morphologies associated with the failure modes in Fig. 17, were generally similar to those discussed in association with Figs. 10 – 16.

The failure mode data in Fig. 17 (60 s) were compared to the pull strength results in Fig. 8. The pull strength decreased slightly between 215°C and 240°C, which happened to coincide with the increase of the thin film peeling mode from 12% to 50%. However, nearly the same failure mode percentages were observed at 240°C, 15 s (Fig. 9), but without the lower pull strength associated with 240°C and 60 s data (Fig. 17). Thus, a conclusive correlation cannot be drawn between low solder joint strength and the thin film peeling mode. A similar conclusion can be made with respect to the thin film delamination failure mode. At the soldering temperature of 215°C, increasing the soldering time from 15 s to 60 s caused this failure mode to increase from 25% to 38%. Yet, the pull strength did not change, significantly, between those same conditions. In summary, the analysis of failure mode data, which were obtained for 15 s (Fig. 9) and 60 s (Fig. 17), when compared to the pull strength results (Fig. 8), indicated that a direct correlation cannot be made between the failure mode and strength metrics for the soldering temperatures, 215°C, 240°C, and 260°C soldering temperatures. This trend implies, once again, that the particular fracture paths associated with each failure mode have similar intrinsic strengths.

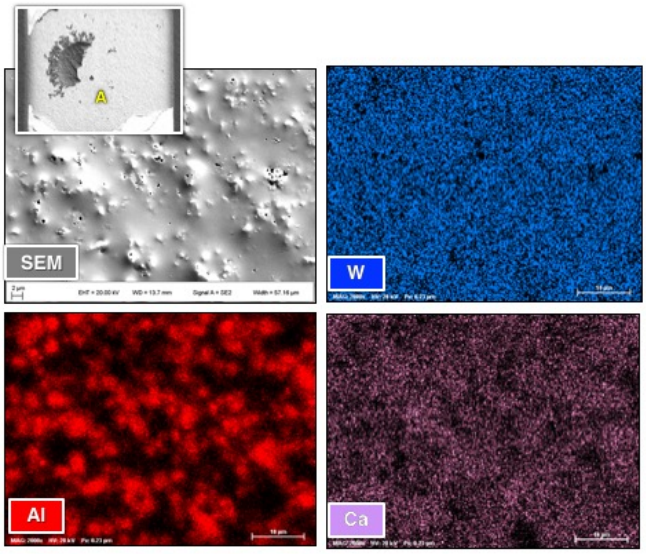

Fig. 16 High magnification, SEM image of the region A (see the inset picture) is shown, together with the EDX maps of W, Al, and Ca (process conditions: 240°C and 15 s). These data were obtained from the LTCC pad side of the failure.

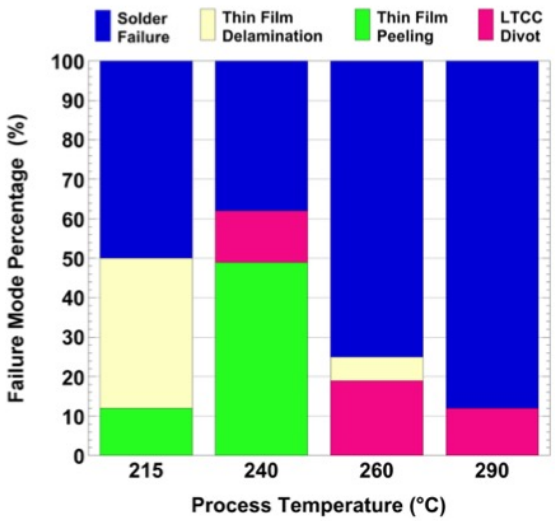

Fig. 17 Bar chart shows the percentage of the observed failure modes as a function of solder temperature for a soldering time of 60 s.

However, the failure mode data in Fig. 17 (60 s) for the 290°C soldering temperature, like that in Fig. 9 (15 s), showed a reduce pull strength and 88% occurrence of the solder failure mode. This comparison indicates that changes to the Sn-Pb solder and associated IMC reaction layers, which control the solder joint failure mode, have the ability to reduce the pull strength of the

joint. Moreover, those features are expressly a function of the soldering conditions.

The details of the fracture surface morphologies associated with the failure modes in Fig. 17, were generally similar to those described with respect to Figs. 10 – 16.

The failure mode percentages are shown in Fig. 18 for the longest soldering time of 120 s. The thin film peeling mode was observed at the soldering temperatures of 215°C and 240°C; it increased at the former temperature and decreased at the latter temperature when compared to the 60 s solder time results in Fig. 17. Moreover, the solder failure mode increased, significantly, at the two lowest soldering temperatures when compared to either of the two shorter soldering times. At the higher soldering temperatures of 260°C and 290°C, the solder failure mode retained its dominance at 120 s as was the case at 60 s. But, there was also an increased frequency of LTCC divot failures with the longer soldering time.

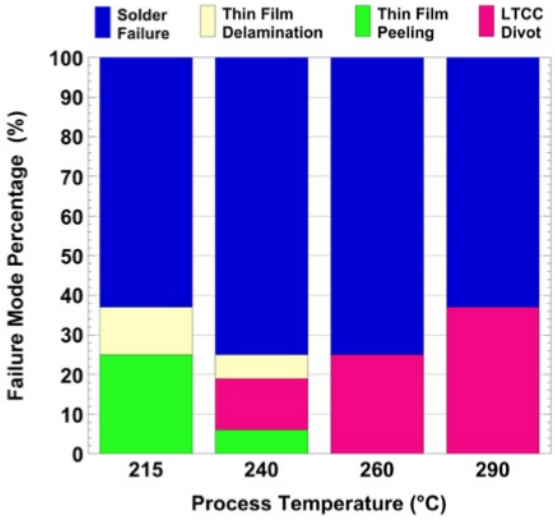

Fig. 18 Bar chart shows the percentage of the observed failure modes as a function of solder temperature for a soldering time of 120 s.

The failure mode trends in Fig. 18 were compared to the pull strength data in Fig. 8. A reduced pull strength was observed at 215°C that coincided with the increased prevalence of the solder failure mode. The pull strength was unchanged at the soldering temperatures of 240°C and 260°C as was also the case for the dominance of the solder failure mode. In addition, the increased frequency of LTCC divots between these temperatures was not reflected by a change to the pull strength. A slight drop of pull strength was observed at 290°C. However, the slight increase of the LTCC divot failure mode (Fig. 18) cannot be confidently asserted as the cause. Rather, the solder failure mode with its dependence on the Sn-Pb microstructure and IMC layers likely caused the drop in the pull strength.

A closer examination was made of the fracture surfaces associated with the four failure modes between soldering process conditions. Even at higher magnifications, the details of the fracture surface morphologies changed very little for the thin film delamination, thin film peeling, and LTCC divot modes as a function of either soldering temperature or time. Therefore, the "appearance" and "disappearance" of these three failure modes versus the soldering parameters are not correlated to intrinsic changes to the thin film layers, their interfaces, or the properties of the bulk LTCC.

On the other hand, the fracture surfaces associated with the solder failure mode did change as a function of the soldering parameters in two manners. First, the proportion of the fracture area represented by region A (Fig. 10) increased with severity of the soldering conditions. Recall that region A results from separation in the IMC layer that formed at the solder/Cu pin interface. This trend is illustrated in Fig. 19, which shows the surfaces on the pad (LTCC) side of the fracture path for the range of soldering conditions: (a) 215°C, 15 s; (b) 215°C, 60 s; and (c) 290°C, 120 s. Note that region A has increased at the expense of the combined regions, B plus C.

Second, the details of the fracture surface topography belonging to region A changed as a function of soldering conditions. This behavior is illustrated in Fig. 20, which shows the region A fracture surface generated by the following soldering parameters: (a) 215°C, 60 s and (b) 290°C, 120 s. The smooth topography in Fig. 20a has changed to a rougher topography in Fig. 20b. The latter surface was attributed to an increased growth of the $(Cu, Au)_xSn_y$ IMC layer caused by the prolonged exposure to molten solder.

A review was made of the EDX data, the goal of which was to determine whether the topographical changes to region A as illustrated in Fig. 20, were likewise accompanied by chemistry changes to the associated $(Cu, Au)_xSn_y$ IMC layer. *A decrease was observed in the Au signal relative to that of Cu with the increased severity of the soldering conditions*. In the absence of cross section analyses, it could only be hypothesized that the higher soldering temperature allowed the Au to reach a higher concentration in the Sn-Pb solder, which reduced its concentration in the $(Cu, Au)_xSn_y$ IMC layer formation. Because the reduction in the Au content of the IMC layer would cause the latter to become *less* brittle, the increased propensity for fracture at this interface (region A) was attribute to the increased thickness of the IMC layer.

In summary, the solder failure mode, the propensity of which increased with the severity of the soldering conditions, was correlated to the reduction in solder joint pull strength. Furthermore, the loss of pull strength was associated with an increased proportion of the fracture surface occurring at the solder/pin interface (region A). The reduce pull strength of the latter interface coincided with a thickening of the $(Cu, Au)_xSn_y$ IMC layer taking place at the region A fracture surface. It is important to reiterate that the strength loss observed in Fig. 8 was relatively small and certainly would not portend a degradation to the performance or long-term reliability of the joint.

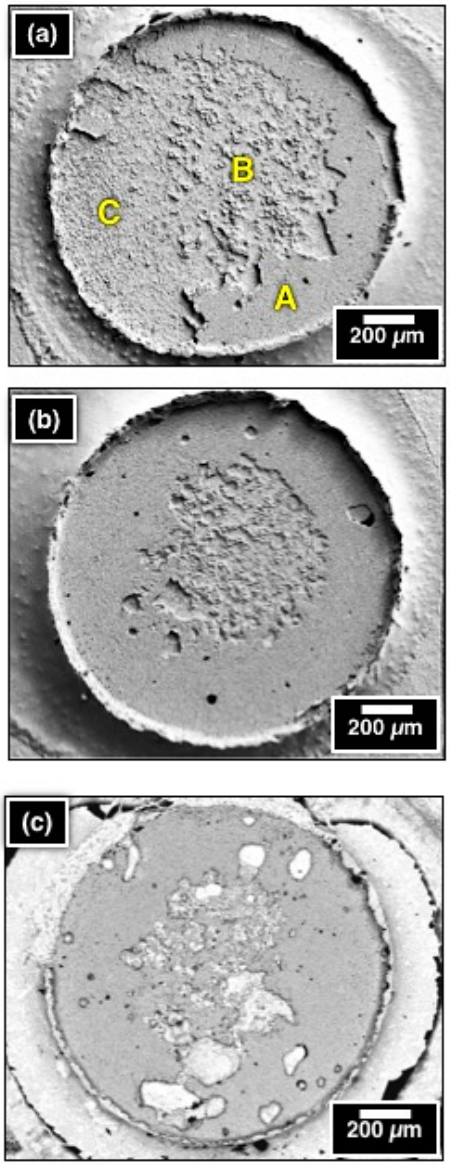

Fig. 19 SEM photographs illustrate the changes to the fracture surfaces and, specifically the proportions of regions A, B, and C as a function of soldering process conditions: (a) 215°C, 15 s; (b) 215°C, 60 s; and (c) 290°C, 120 s.

Program goal: a robust thin film technology

The long-term objective of this program was to develop a robust thin film technology for LTCC-based electronic products. Although the solder failure mode appeared to control the pull strength of the Sn-Pb joints, it required the presence of the Cu pin. A Cu base material may not always be present in an HMC solder joint. Therefore, additional consideration was given to the other three failure modes in order to understand their individual behaviors.

Once goal was to ascertain the ability of the Ti/W adhesion layer to withstand the range of soldering process conditions required to assemble HMC products. In the case of the *thin film delamination mode*, the SEM and EDX analyses showed that the Ti/W film, like its Ti counterpart, exhibited a slightly better bond to the alumina phase (particles) than to the silica-based glass phase of the LTCC material. Nevertheless, these differences of adhesion were subtler than was the case of the Ti layer and, as such, did not significantly impact the solder joint pull strength.

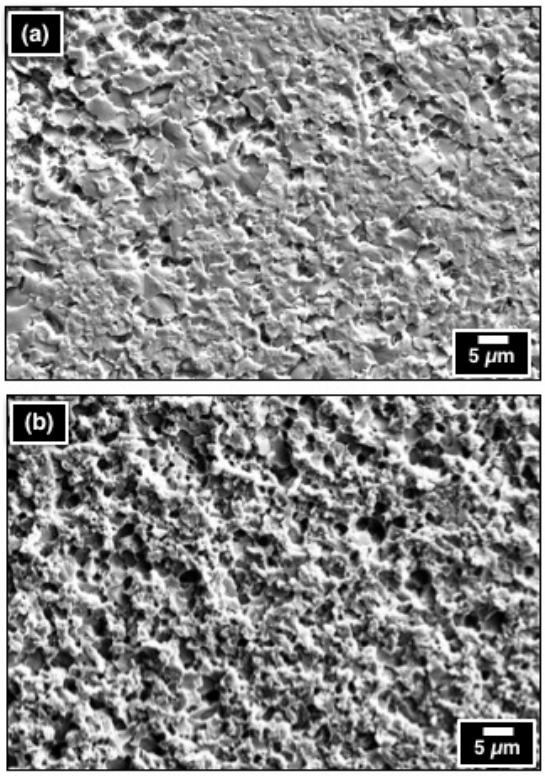

Fig. 20 SEM photographs shows an increased roughness to the fracture surface topography if region A as a function of soldering conditions: (a) 215°C, 60 s and (b) 290°C, 120 s.

The *thin film peeling failure mode* represented a separation between the Ti/W adhesion layer and the Cu layer. Although depositing the Cu layer without breaking vacuum improved its adhesion to the Ti/W surface, this measure reduced, but did not completely eliminate, its occurrence. Interestingly, thin film peeling appeared to diminish with increased severity of the soldering process conditions. This trend suggests that the additional thermal exposure improved adhesion at the interface between the Cu and Ti/W layers. Perhaps an ancillary thermal treatment would increase the bond strength of that interface. Nevertheless, the thin film peeling fracture path was not sufficiently pervasive nor weak enough to pose a risk to the mechanical strength of the solder joint.

Lastly, *the LTCC divot failure mode* occurred persistently in the pull tests, but without an obvious trend as a function of soldering process parameters. Moreover, the occurrence of LTCC divots did *not* correlate with the pull strength trends. Clearly, the strength of the LTCC ceramic was, at least, comparable to the intrinsic strengths of the structures that contributed to the other three failure modes.

Further consideration was given to the LTCC divot failure mode. The tensile strength of LTCC is in the range of 39 – 51 ksi, which exceeds the nominal stresses generated by the pull loads in Fig. 8 by nearly three-fold [8]. The failure mode analysis did not indicate that the test substrates contained a repeatable flaw in the LTCC material. Therefore, a stress concentration must have been generated in the substrate such that, when combined with the stresses of the pull test, caused the total stress in the LTCC to exceed its intrinsic strength.

The hypothesis was mentioned earlier that residual stresses can result from the mismatch of CTE values between LTCC (5 – 8 ppm/°C) and those of either the Sn-Pb solder (21 ppm/°C) or the Cu pin (17 ppm/°C) [7, 9]. Radial *tensile* stresses are generated under the solder joint footprint *after its solidification* as the Sn-Pb alloy and Cu pin contracted to a greater degree than did the LTCC material. A detailed finite element analysis was outside the scope of this study. Nevertheless, it is hypothesized that the pull load placed on the joint superposed additional tensile stresses on the pre-existing residual stresses so that the total tensile stress exceeded the local tensile strength of the LTCC, resulting in the divot failure mode.

The CTE mismatch residual stresses can only develop after solidification of the solder (183°C). Per se, the residual stresses were not sensitive to the specific soldering temperatures because they exceed 183°C because the Sn-Pb alloy would still be molten and could not support a mechanical load. The same trend was observed with the LTCC divot failure mode – that is, its occurrence was largely insensitive to the soldering temperature. This correlation supports the premise that residual stresses, which arose only after the Sn-Pb solder had solidified at 183°C, contributed to the divot formation. Also, the LTCC divot failure mode was not sensitive to soldering time. The latter observation, when coupled to the soldering temperature insensitivity, implies that the strength of the LTCC material was not explicitly degraded by the harshness of the overall soldering conditions so as to be a cause of the divots. Lastly, the residual stresses and LTCC divot failure mode were not of a magnitude or prevalence, respectively, to control the solder joint performance and/or reliability.

Conclusions

1. A study was undertaken to develop a 0.200Ti/W-4.0Cu-2.0Pt-0.375Au (μm, abbreviated Ti/W-Cu-Pt-Au) thin film metallization system to serve as the conductor on low-temperature, co-fired ceramic (LTCC) substrates for high-reliability hybrid microcircuit (HMC) electronic products.

2. A pin pull test was used to assess the tensile strength of solder joints made to the Ti/W-Cu-Pt-Au thin film with the 63Sn-37Pb (wt.%) filler metal. The assembly process, which attached Cu pins to the thin film pads, was based on the matrix of the soldering temperatures of 215°C, 240°C, 260°C, and 290°C and soldering times of 15 s, 60 s, and 120 s.

3. The pull strengths were well in excess of calculated values based on the tensile strength of Sn-Pb solder due to the plain strain effect of the solder joint geometry. The strength values experienced a modest loss from 25 lb. to 21 lb. between 215°C and 290°C. Strength differences were within the experimental error as a function of soldering time at either of these temperatures. At 240°C and 260°C, strengths were slightly higher at 15 s versus 60 s and 120 s, but only just outside the error bars of the respective data sets.

4. Failure modes were dominated by fracture within the solder joint and specifically, at the solder/thin film or solder/Cu pin interfaces. The slight loss of pull strength was correlated to an increased prevalence of failure in the $(Cu, Au)_xSn_y$ intermetallic compound (IMC) layer at the solder/Cu pin interface.

5. The thin film delamination and thin film peeling failure modes had a negligible role because they did not correlate to the trends in the pull strength. The thin film peeling failure mode, which was caused by separation along the interface between the Ti/W and Cu layers, appeared to actually diminish with increased severity of the soldering process.

6. The LTCC divot failure mode was also a minor contributor to the fracture behaviors. Its occurrence shifted slightly to the higher soldering temperatures, but without a consistency that could be correlated to the pull strength data. The divots were attributed to the presences of tensile residual stresses generated by the CTE mismatch of the materials after solidification of the Sn-Pb solder joint.

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