

Quantum dots with split enhancement gate tunnel barrier control

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We introduce a silicon metal-oxide-semiconductor quantum dot architecture based on a single polysilicon gate stack. The elementary structure consists of two enhancement gates separated spatially by a gap, one gate forming a reservoir and the other a quantum dot. We demonstrate, in three devices based on two different versions of this elementary structure, that a wide range of tunnel rates is attainable while maintaining single-electron occupation. A characteristic change in slope of the charge transitions as a function of the reservoir gate voltage, attributed to screening from charges in the reservoir, is observed in all devices, and is expected to play a role in the sizable tuning orthogonality of the split enhancement gate structure. The all-silicon process is expected to minimize strain gradients from electrode thermal mismatch, while the single gate layer should avoid issues related to overlayers (e.g., additional dielectric charge noise) and help improve yield. Finally, reservoir gate control of the tunnel barrier has implications for initialization, manipulation and readout schemes in multi-quantum dot architectures.

Silicon (Si) quantum dots (QDs) are strong contenders for the realization of spin qubits.^{1,2} Silicon germanium heterostructure (Si/SiGe) platforms with integrated micromagnets³ have produced the highest performance qubits,⁴⁻⁶ with fidelities over 99.9%,⁷ while metal-oxide-semiconductor (MOS) platforms have also achieved fault tolerant fidelities.⁸

Most of the high performance systems mentioned above are enhancement mode devices comprising at least two layers of control gates. The overlapping gates ensure strong confinement and the highest electrostatic control over regions surrounding the QDs. These current multi-stack devices have therefore achieved excellent tunability, thanks in part to an independent control of reservoirs, dots and tunnel barriers through respectively dedicated gates. On the other hand, single-layer enhancement mode devices are being explored for ease of fabrication and potentially higher yield, in both Si/SiGe and MOS systems.⁹⁻¹³ In particular, all-silicon MOS single-layer devices are expected to avoid thermal mismatch and additional dielectric charge noise from overlayers.^{14,15} These single-layer devices generally use a single gate to form a source-dot-drain channel, relying on constrictions and lateral depletion gates to shape the confinement potential.^{9,16} Reservoir filling, dot charge occupation and tunnel rates are therefore controlled differently than in multi-gate stack architectures. Various architectures and methods of tunnel barrier control impact tunability differently, and understanding those differences will influence choices of multi-QDs initialization, manipulation and readout schemes, including automatic tuning procedures,^{17,18} as well as reproducibility, versatility and scalability of devices.¹⁹

Here we explore a single gate stack structure featuring a split gate for dot and reservoir formation. The tunnel barrier is

simply formed by the gap between the dot and reservoir gates. We investigate, in all-silicon MOS devices based on this elementary structure, how tunnel barrier control can be achieved by modulation of the reservoir gate voltage. The operation principle is studied in two variations of the layout, emphasizing some intrinsic effects brought by the use of a reservoir gate for tunnel control, in contrast with the more frequent method of control using a dedicated barrier gate directly on top of the barrier. We also define a control orthogonality metric with significance for tunability and versatility of quantum dot devices and use it to compare a split gate QD device to a multi-stack device from the literature. Finally, we conclude by examining single-electron regime characteristics and valley splitting tuning in the split gate devices.

The elementary single-gate stack structure we explore consists of a quantum dot enhancement gate, AD, and a reservoir enhancement gate, AR, separated by a gap, as shown in Fig. 1(a). We refer to this base unit of design as the *split enhancement gate* structure. Devices are fabricated using the Sandia National Laboratories MOS quantum dot process,^{20,21} which is described in detail in the Supplementary Material. The gate stack consists of a 10 000 Ω -cm n-type silicon float zone substrate, a 35 nm SiO₂ gate oxide and a degenerately As-doped 100 nm thick polysilicon gate (shown in Fig. 1(a)). The polysilicon nanostructure is defined by a single electron-beam lithography and dry etching step. The gate oxide properties have been characterized in Hall bars fabricated on the same starting gate stack as the nanostructures. Peak mobility, percolation density,^{20,22} scattering charge density,^{20,23} interface roughness and interface correlation length²⁴ were extracted for the wafers used for each of the devices and are described in the Supplementary Material.

In this study, we look at two different layouts of split enhancement gate devices. We examine a single-lead layout (devices A1 and A2), where a single reservoir is connected to a dot, and a double-lead layout (device B), where the dot

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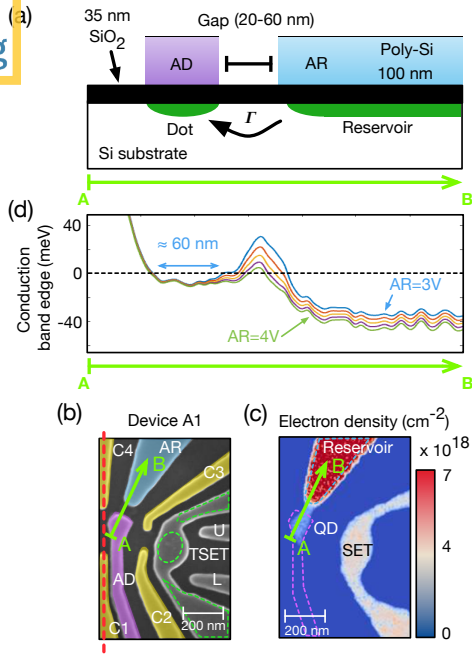


FIG. 1. (a) Schematic transverse cut of the split enhancement gate tunnel barrier devices. AR is the reservoir enhancement gate, and AD is the dot enhancement gate. (b) False-color scanning electron micrograph (SEM) of single-lead split-enhancement gate device A1. C1, C2, C3, and C4 are confinement gates. The gate TSET forms the SET channel, and U and L help define its source and drain barriers. A mirror structure, on the left side of the dotted red line, not shown for clarity, includes gates AD', AR', C2', C3', TSET', U', and L'. (c) Simulated electron density, representing approximately 20 electrons in the dot. (d) Simulated conduction band edge profile (smoothed traces) along the green arrow A-B from (a), (b), (c) and (d), for V_{AR} varying from 3 to 4 V with 0.25 V increments, with other parameters kept constant. Small amplitude modulations in the potential result from the mesh resolution used for those particular simulations and the associated sub-optimal interpolation routine.

is connected in series to reservoirs to enable transport measurements, in addition to charge sensing. Devices A1 and A2 present the same layout, with only differences in scale and spacing (see Table I in the Supplementary Material). For all devices, measurements are performed using a proximal SET as a charge sensor with standard lock-in or RF reflectometry techniques.²⁵ Details on the measurements and a list of all voltages employed are given in the Supplementary Material.

To illustrate the split enhancement gate tunnel barrier structure and its operation, we have performed Thomas-Fermi numerical simulations²⁶ of device A1, as shown in Fig. 1(b), using the corresponding MOS structure and operating gate voltages as input parameters. Figure 1(c) shows the simulated electron density at the Si/SiO₂ interface when the device is experimentally set in a ~ 20 electrons regime. As expected, a reservoir is formed under gate AR, and a quantum dot under the tip of gate AD, separated by the tunnel barrier region. Some form of tunnel barrier control using the reservoir gate voltage, V_{AR} , is suggested by variations of the potential along the dot-reservoir axis (Fig. 1(d)). Indeed, as a function of V_{AR} , the tunnel barrier potential height and width are modified, while the QD conduction band edge stays fairly constant

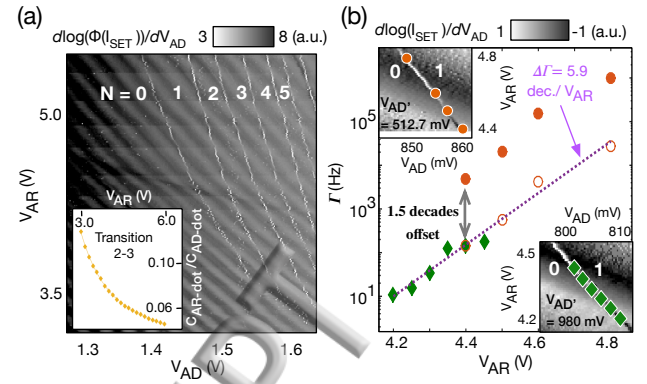


FIG. 2. (a) Stability diagram of AD vs AR in the few-electron regime for the single-lead device A2. The data was processed through a 5th order Butterworth digital filter and a Hilbert transform to extract the phase $\phi(\text{SET})$ of the signal and minimize the appearance of the background's SET's Coulomb oscillations (darker, more horizontal features). Charge occupation N in the dot is indicated for each region between the transitions (thin white and more vertical features). Bottom left inset: capacitance ratio $C_{AR\text{-dot}}/C_{AD\text{-dot}}$ as a function of V_{AR} extracted from the $N = 2 \rightarrow 3$ charge transition's slope. (b) Reservoir-dot tunnel rate as a function of V_{AR} for the $N = 0 \rightarrow 1$ transition in device A1. The green (diamonds) data points are obtained via full counting statistics of single-shot traces²⁸ while the orange (circles) data points are extracted from pulse spectroscopy.²⁹ Hollow orange circles are the orange filled circle data points translated by ≈ 1.5 decades. The dotted line is an exponential fit to green and hollow orange data points, yielding a slope $\Delta\Gamma$. Top left inset: zoom on the region of the stability diagram corresponding to the orange data points, with the left dot accumulation gate AD' at 512.7 mV. Bottom right inset: Zoom on the region of the stability diagram corresponding to the green data points, with $V_{AD}' = 980$ mV.

relative to the Fermi level of the reservoir, indicating some form of *tuning orthogonality* between charge occupation of the QD and tunnel rate to the reservoir (similar quantities are evoked in Ref.¹⁹). A sufficient tuning orthogonality would allow simultaneously for a wide range of tunnel rates Γ and the ability to regularly tune these devices to the single electron regime. We therefore investigate this characteristic for a QD based on a split enhancement gate structure employing the reservoir gate as a knob.²⁷

Figure 2(a) shows how the QD occupancy can be tuned down to the single electron regime in device A2 (similar to device A1 except for scale, see Supplementary Material). The single electron occupation was confirmed with spin filling from magnetospectroscopy, and yields an 8 meV charging energy for the last electron. The effect of V_{AR} on the tunnel rate is qualitatively visible from the charge transitions, which go from a "smooth" appearance at high V_{AR} , when Γ is high compared to the measurement rate, to a speckled appearance at low V_{AR} , when Γ is of the order of the measurement rate or lower.³⁰

We observe a gradual decrease of the AR gate capacitance to the dot, $C_{AR\text{-dot}}$, as the reservoir fills up with electrons, as shown in the inset of Fig. 2(a) (assuming $C_{AD\text{-dot}}$, the capacitance of the AD gate to the dot, stays constant). The capacitance ratio $C_{AR\text{-dot}}/C_{AD\text{-dot}} = -1/m$ is extracted from the slope m of the transition $N = 2 \rightarrow 3$ in the stability

diagram.¹ A similar dependence of the capacitance ratio is also observed in numerical simulations, but the agreement is only qualitative, due in part to the limitations of the semi-classical simulation. We attribute this visible curvature in the dot transitions to a screening effect of the reservoir gate potential, induced by the accumulated charges in the reservoir. This specific effect therefore seems to be caused by the use of an enhancement gate connected to a ohmic contact as a tuning knob.

Device A1 also exhibits a comparable behavior as a function of the AR and AD gate voltages (see Supplementary Material). We measured the dot-reservoir tunnel rate as a function of the voltage on gate AR for device A1, along the $N = 0 \rightarrow 1$ charge transition, as V_{AR} was compensated with V_{AD} to preserve the charge state, as shown in Fig. 2(b). Two data sets (diamond and filled circles) were taken at different voltages on a surrounding gate, $V_{AD'}$. The 467 mV difference results in a 1.5 decades global offset in tunnel rates. We subtract this offset (hollow circles) to extract a single exponential dependence of Γ with V_{AR} .^{32,33}

From the slope of the exponential fit, we extract a gate response of $\Delta\Gamma = 5.9 \pm 0.7$ decades/ V_{AR} , defined as the variation in dot-reservoir tunnel rate induced by a change of 1 V on gate AR, when compensated by gate AD to keep the dot chemical potential fixed. More useful for comparison between devices is when we remove the device geometry specific capacitance by converting to change in chemical potential, $\Delta\mu_{dot}$. We define the following metric:

$$\beta_{AR,AD} = \Delta\Gamma_{AR,AD} / \Delta\mu_{dot}, \quad (1)$$

where $\Delta\Gamma_{AR,AD}$ is the change in tunnel rate induced by the change in voltage on AR (and compensated by AD), $\Delta\mu_{dot}$ is the change in chemical potential caused by gate AR (equal to the chemical potential compensated by gate AD), and we call $\beta_{AR,AD}$ the *tuning orthogonality*. For device A1, the above analysis leads to $\beta_{AR,AD} = 0.9 \pm 0.3$ decade/meV, using the gate lever arm $\alpha_{AR} \sim 0.007$ meV/mV (from $\alpha_{AD} \sim 0.22$ meV/mV). We note that the chemical potential of the QD does not actually shift for a given tunnel rate variation here, since there is a second gate compensating the chemical potential shift from the first. Therefore, care must be taken in interpreting this ratio: it does not represent the effect of a single gate on the tunnel rate, but rather the interplay of two gates acting in opposite direction on the two quantities, with unequal contributions.

Taken individually, more positive voltages on gates AD and AR would both tend to decrease the barrier height and width, as one would expect and as shown in the conduction band edge simulations of Fig.1(d). But if one wants to keep the dot occupation fixed, and shift from high to low tunnel rates, gates AD and AR have to be swept in opposite directions. Our measurements indicate that in this case the lever of gate AR on the tunnel barrier still overcomes the opposite effect of gate AD. Furthermore, we speculate that the screening effect from charges under AR contributes to this efficiency, as it reduces the lever of gate AR on the dot occupation, but on the tunnel barrier, such that less compensation on AD is necessary to maintain charge occupation than if no screening effect was present.

The quantity $\beta_{1,2}$ can be estimated for other designs in the literature, for any pair of gates 1 and 2 used to tune the tunnel

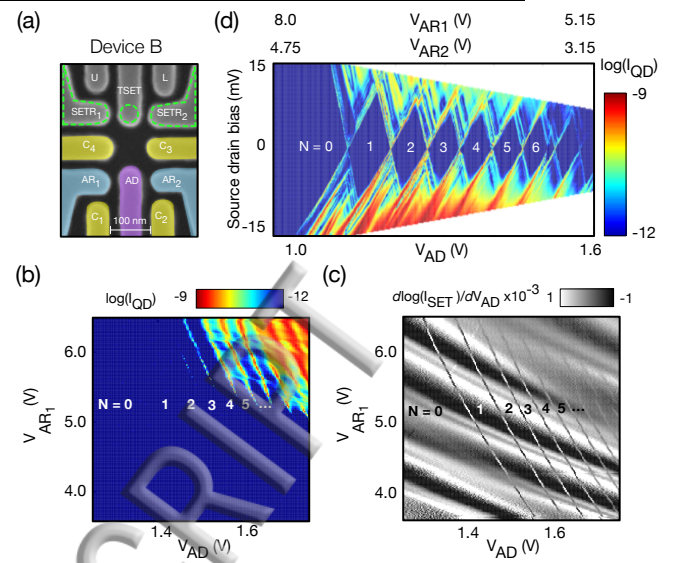


FIG. 3. (a) SEM of a two-lead single quantum dot device, device B. C1, C2, C3 and C4 are confinement gates, AD is the dot accumulation gate, and AR1 and AR2 are the source and drain reservoir accumulation gates, respectively. A mirror structure above is operated as a SET for charge sensing. (b) Stability diagram in transport of AD vs AR_1 . (c) Stability diagram in charge sensing corresponding to the transport diagram in (b). (d) Coulomb diamond measurement corresponding to a stability diagram of AD vs AR_1 and AR_2 . The small diamond after electron #6 is due to a donor ionization³⁶ (see fabrication details in the Supplementary Material).

rate and compensate for changes in the dot occupation, respectively. For comparison, we estimate $\beta_{BG,AD} = 1.4 \pm 0.5$ decades/meV for the case of a dedicated barrier gate BG compensated by the dot accumulation gate AD equivalent in a Si/SiGe device.³⁴ This indicates a tuning orthogonality that can reach the same order of magnitude as dedicated barrier gate devices in multi-stack architectures. The single-layer split enhancement gate layout could therefore provide a wide operation range³⁵ for single-electron QD devices. Details on the calculations as well as assumptions leading to the metric β and its limitations are provided in the Supplementary material.

The double-lead layout also supports transport down to the last electron and exhibits a typical split enhancement gate behavior. Figure 3(a) shows device B, where transport is through a QD under gate AD with source and drain reservoirs under gates AR_1 and AR_2 . A mirrored structure can be operated as a SET charge sensor, correlating the transport transitions (Fig. 3(b)) with charge sensed measurements (Fig. 3(c)).

In Fig. 3(b), the tunnel rate ranges from the life-time broadened regime at high V_{AR} , corresponding to a ~ 3 GHz tunnel rate^{34,37} to slower than can be detected by the charge sensor, ~ 8 Hz. The slight curvature in the dot and SET transitions of Fig. 3(d) is ascribed to a similar screening effect as in the single lead devices, although it is not as pronounced. This demonstrates that two neighboring barriers in series can be tuned relatively orthogonally (i.e., crosstalk is not a prohibitive issue), and that the split enhancement gate concept can be applied in several layouts.

In Fig. 3(d), V_{AR1} and V_{AR2} are adjusted simultaneously to symmetrize the tunnel barriers on the source and drain side of the QD, giving rise to Coulomb diamonds.³⁸ The notable

difference in voltage ranges applied on AR_1 and AR_2 is attributed mainly to asymmetry in the voltages applied on the neighboring gates on the left and right side of the device, although small variations in width of the dot-reservoir gap could also contribute to the difference. The precise effect of the dot-reservoir gap width on the tuning orthogonality and general efficiency remains to be studied in detail.

The addition energy of the last electron and the first orbital energy are extracted from the Coulomb diamonds of Fig. 3(d), yielding approximately $E_{add} = 11$ meV and $\Delta E = 3$ meV, respectively. A classical capacitance between the QD and the AD gate of 2.9 aF is estimated (e.g., $C_{AD} = e/\Delta V_{AD}$ with $\Delta V_{AD} = 56$ meV the voltage applied on gate AD to go from the $N = 0 \rightarrow 1$ charge transition to the $N = 1 \rightarrow 2$ transition in Fig. 3(b)). The classical capacitance can be associated with a circular 2D QD below the gate and is used to estimate a QD radius of ~ 30 nm, using $\epsilon_r = 3.9$ for the SiO_2 and neglecting small errors due to the electron offset from the SiO_2 interface and depletion of the polysilicon. The orbital energy also provides an estimate of QD size. Following Ref.,³⁴ we can extract an effective length of a confining 2D box ($\pi r^2 = L^2$) and using $\Delta E = \frac{3\hbar^2\pi^2}{2m^*L^2} = 3$ meV, we obtain a similar dot size, $r \sim 25$ nm, using $m^* = 0.19 m_e$. These estimated dot sizes and energies are similar to the ones obtained in multi-stack accumulation mode quantum dot devices.^{34,39}

Finally, an investigation of the spin filling and singlet-triplet energy splitting in our silicon QDs using magnetospectroscopy^{34,40,41} indicates that the valley splitting is linearly tunable with the vertical electric field ($8.1 \pm 0.6 \mu\text{eV}/\text{MV}$ in the double-lead device) and is tunable over a range of ~ 75 -250 μeV (see the Supplementary Material for details).

In conclusion, we explored a split enhancement gate architecture implemented in single-lead and double-lead layouts of polysilicon MOS QD devices. The single-electron regime was reliably achieved in three different devices. Using the reservoir enhancement gate to modulate the tunnel rate and compensating with the dot enhancement gate, we found a tuning orthogonality $\beta_{AR,AD} \approx 0.9$ decade/meV in one of the single-lead devices. We argue that the notable tuning orthogonality, which is comparable to what can be achieved in devices with a dedicated barrier gate in multi-stack architectures, is boosted by the screening effect arising from the use of an enhancement gate as a tuning knob. In addition, a strongly confined quantum dot with charging energies up to 11 meV and orbital energy of 3 meV was observed in the device with smallest features, corresponding to a ~ 30 nm radius QD. Linear tunability of the QD's valley splitting was also observed up to 250 μeV .

SUPPLEMENTARY MATERIAL

Section I of the Supplementary Material provides details on the samples fabrication. Section II describes experimental details and devices characteristics. Section III presents a discussion on the tuning orthogonality metric, and Section IV is dedicated to the study of the valley splitting tuning in the split enhancement gate devices.

ACKNOWLEDGMENTS

We gratefully recognize conversations with J. K. Gamble about early split gate designs, and J. Dominguez for supporting preparation of the devices. We acknowledge technical support from M. Lacerte, R. Labrecque, and M. Lapointe-Major, and helpful discussions with J. Camirand Lemyre, L. Schreiber and J. Klos. This work was supported by the Natural Sciences and Engineering Research Council of Canada (NSERC) and the Canada Foundation for Innovation (CFI). This research was undertaken thanks in part to funding from the Canada First Research Excellence Fund. This work was performed, in part, at the Center for Integrated Nanotechnologies, an Office of Science User Facility operated for the U.S. Department of Energy (DOE) Office of Science. Sandia National Laboratories is a multimission laboratory managed and operated by National Technology and Engineering Solutions of Sandia, LLC, a wholly owned subsidiary of Honeywell International, Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525. This paper describes objective technical results and analysis. Any subjective views or opinions that might be expressed in the paper do not necessarily represent the views of the U.S. Department of Energy or the United States Government.

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