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Supplementary Material for "Quantum dots with split enhancement gate tunnel barrier control"

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I. SAMPLES FABRICATION

The fabrication is composed of two phases. The first phase is run in a 0.35 micron CMOS silicon foundry, and the second phase is performed in another fabrication area that provides more flexibility in processing, particularly the e-beam lithography used for the nanofabrication. Three different devices are presented in this work. We describe the process flow for devices A1 and A2. Significant differences in the structure are noted for device B.

Phase 1 (silicon foundry): The initial material stack is fabricated using a 0.35 micron silicon foundry process at Sandia National Laboratories. The starting material is a 150 mm diameter float zone <100> n-type silicon wafer with a room temperature resistivity of 10 000 Ω-cm. Device B used a p-type float zone substrate with a 99.95% Si^{28} enriched epitaxy layer instead. A 35 nm thermal silicon oxide is grown at 900°C with dichloroethene (DCE) followed by a 30 min, 900°C N_2 anneal. The next layer deposited is a 100 nm amorphous silicon layer followed by a $5\times10^{15}\mathrm{cm}^{-2}$, 10 keV arsenic implant at 0° tilt. Device B used a 200 nm layer and the implant energy was 35 keV with the same dose. The amorphous layers are crystallized later in the process flow to form a degenerately doped poly-silicon electrode. In the silicon foundry, the poly-Si is patterned and etched into large scale region, a "construction zone" around $100\ \mu\mathrm{m}\times100\ \mu\mathrm{m}$ in size, that will later be patterned using e-beam lithography to form the nanostructure.

After etching, Ohmic implants are formed using optical lithography and implantation of As at $3\times10^{15}\mathrm{cm}^{-2}$ density at 100 keV. An oxidation anneal of 900°C for 13 min and an N_2 soak at 900°C for 30 min follows the implant step and serves the multiple purposes of crystallizing, activating and uniformly diffusing the dopants in the poly-Si while also forming a SiO_2 layer (10-25 nm) on the surface of the poly-Si. This SiO_2 layer, forms the first part of the hard mask layer used for the nanostructure etch in the construction zone. The second part of the hard mask is a 20 nm Si_3N_4 layer (35 nm for device B). An 800 nm thick field oxide is subsequently deposited using low pressure chemical vapor deposition (CVD), tetraethoxysilane (TEOS) or high density plasma CVD for device B. The field oxide is planarized using chemical mechanical polishing (CMP) leaving approximately 500 nm over the silicon and 300 nm over the poly-Si. Vias are etched to the conducting poly-Si and n^+ Ohmics at the silicon surface. The vias are filled with Ti/TiN/W/TiN. The tungsten is a high contrast alignment marker for subsequent e-beam lithography steps. Large, approximately $100\ \mu\mathrm{m}\times100\ \mu\mathrm{m}$ windows aligned to the construction zones are then etched in the field oxide to expose the underlying hardmask and poly-Si construction zone for nanostructure patterning. The last processing step for the devices in the silicon foundry is a 450°C forming gas anneal for 90 min.

Phase 2 (separate nano-micro fabrication facility): The wafers are removed from the silicon foundry and subsequently diced into smaller parts, leading to 10 mm × 11 mm dies, containing each 4 complete QD devices. The nanostructure are patterned using electron beam lithography and a thinned ZEP resist. The pattern is transferred with a two-step etch process. First, the SiN and SiO_2 hard mask layers are etched with a CF_4 dry etch, and O_2 clean then strips the resist *in-situ*. The second etch step is to form the poly-Si electrodes, which is done with an HBr dry etch in the same chamber. The poly-Si etch is monitored using end-point detection in a large scale etch feature away from the active regions of the device. Wet acetone and dry O_2 cleans are used to strip the residual resist after the poly-silicon nanostructure formation. After the wet strips of the tungsten vias, a lift-off process is used for aluminum formation of bond pads to contact the Ohmics and poly-silicon electrodes.

The last step is a 400°C, 30 minute forming gas anneal. For device B, after polysilicon etch, a second e-beam lithography and implant step was done to place donors near the QD region. The device was sent out for implant, $4\times10^{11}\mathrm{cm}^{-2}$ Phosphorus at 45 keV. After the implant step, the photoresist was stripped with acetone and then the metal and residual organics were stripped from the surface using peroxide and RCA cleans. The device was subsequently metallized using an Al lift-off process similar to devices A1 and A2.

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II. DEVICES AND EXPERIMENTAL PARAMETERS

This appendix provides supplementary information on the devices and experiment's parameters presented in the main text.

Experiments are performed in two distinct laboratories, Université de Sherbrooke (devices A1 and A2) and Sandia National Laboratories (device B), in dilution refrigerators sustaining electronic temperature of 125 mK and 160 mK, respectively. In the limited testing of standard measurements, the samples are found to be robust to thermal cycles (i.e., little threshold shift) and no devices were visually altered by the long-distance shipping (e.g., damage from electrostatic discharge was not observed). The devices are also electrically stable, with the drift of the quantum dot chemical potential in device B characterized as approximately 5.3 $\pm$ 0.5 μeV standard deviation over a 150 hour period.

Table I compares the characteristic of devices A1, A2, and B. Table II exposes the experimental parameters for all measurements shown or mentionned in the main text for devices A1 and A2 (single-lead devices), while Table III does the same for device B.

A statement concerning device A1 is helpful to the full comprehension. The full range AD vs AR stability diagram for device A1 is not shown in the main text for the sake of clarity. Indeed, features not related to the split enhancement gate operation principles, and attributed to an irregularly shaped confinement potential under gate AD, were presents in the full-range stability diagrams of device A1 (see Fig. 1(b) of the Supp. Mat.). This effect could be mitigated, but only up to a certain point, by applying more negative voltages on gates C1 and C2. The stability diagram of device A2 however is much cleaner owing to its smaller features compared to A1, but experimental setup constraints at that time prevented us to repeat the tunnel rate measurements on device A2, hence why we rely on qualitative analysis only for this device. We emphasize that with the appropriate confinement, both devices qualitatively exhibit the same tunnel rate modulation and bending of the charge transitions, which, as stated in the main text, we believe is intrinsic to the split enhancement gate tunnel barrier.

Figure 1(b) of the Supp. Mat. illustrates the effect of an insufficient and irregular confinement of the dot in device A1. Figures 1 (c)-(f) show how the smaller features of device A2, combined to an increasingly more negative voltage on gate C1, lead to more regular dot transitions, and the clean diagram shown in Fig. **??** (a) of the main text. This observation is in agreement with the clean and regular transitions witnessed for device B (Fig. **??**(d)), which possesses even smaller features than device A2 (see Table I).

III. TUNING ORTHOGONALITY

When designing a QD device, it is of interest to provide local control of important device properties, with the surface gate voltages often serving as the control knobs. One oft used parameter is gate lever arm α, which describes the efficacy of a gate voltage on the QD chemical potential level μ. The lever arm is defined as

$$\Delta\mu_i = \alpha_i \Delta V_i \tag{1}$$

where there is a unique α_i for each gate i. In a similar spirit, a parameter describing the controllability of the QD-reservoir tunnel rate can be defined as

$$\Delta\Gamma_i = \beta_i' \Delta V_i \tag{2}$$

While α is always positive by definition, β' can be positive or negative, depending on if gate i increases or decreases the reservoir-QD tunnel rate with a positive voltage change. For example, for a QD under gate AD, gate AR increases the tunnel rate with increasing voltage, while gate AD$'$ decreases the tunnel rate with increasing voltage (Fig. 2(b) of the main text). Geometric arguments can typically be made to estimate the sign of β' by considering whether a positive voltage change on a gate is pulling the dot towards or away from the reservoir.

Of particular interest for designing QDs is the ability to tune the tunnel rates to the QD while only imparting a minimal change in the QD chemical potential, which denotes a high degree of tuning orthogonality between the two properties. Good orthogonality facilitates emptying the QD (fewer gate compensations are required to obtain $N = 1$) and tuning the reservoir coupling with minimal effect on the shift in the charge stability diagram (quicker optimization of relaxation and coherence times). For a single gate, the orthogonality between the tunnel rate and the chemical potential tunability is optimized by maximizing the ratio $\frac{\Delta\Gamma_i}{\Delta\mu_i} = \frac{\beta_i'}{\alpha_i} \equiv \beta_i$. We rewrite this in an analogous form to the lever arm:

$$\Delta\Gamma_i = \beta_i \Delta\mu_i \tag{3}$$

To obtain β_i, one must measure the change in both tunnel rate and chemical potential for a change on the gate voltage ΔV_i. In practice, this is impossible because a change in a single voltage moves the QD level out of resonance with the Fermi level, and a change in tunnel rate cannot be determined. Thus, one must consider the effect of two gate voltages changing and compensating each other such that the QD chemical potential is always in resonance with the Fermi level. Continuing the analogy with the lever arm, we assume that the total change in tunnel rate is simply the sum of the contributions of each gate that has changed. For two gates 1 and 2, this results in

$$\Delta\Gamma_{1,2} = \Delta\Gamma_1 + \Delta\Gamma_2 = \beta_1\alpha_1\Delta V_1 + \beta_2\alpha_2\Delta V_2 \tag{4}$$

As the chemical potential has not changed, we have the additional constraint

$$\Delta\mu_{1,2} = \Delta\mu_1 + \Delta\mu_2 = \alpha_1\Delta V_1 + \alpha_2\Delta V_2 = 0 \tag{5}$$

Combining Eq. 4 and Eq. 5, we can define the two-gate tunnel rate orthogonality parameter as

$$\beta_{1,2} \equiv \beta_1 - \beta_2 = \frac{\Delta\Gamma_{1,2}}{\Delta\mu_1} \tag{6}$$

TABLE I. Measured devices characteristics. Devices A1 and A2 present the same layout, differing only in the spacing between the gates and the width of the gates (A2 gates are more closely packed than A1 gates). For comparison, we label the devices by the distance between gates AD and C2, and the distance between AD and AR tips (see Fig 1(c) /hlof the main text).

Device	**A1**	**A2**	**B**
Reservoirs	Single lead	Single lead	Double lead
Device dimensions	AD-C2: 60 nm, AD-AR: 100 nm, AD width: 100 nm	AD-C2: 25 nm, AD-AR: 30 nm, AD width: 75 nm	AD-C2: 30 nm, AD-AR: 20 nm, AD width: 50 nm
Mobility	4560 $\mathrm{cm}^2/\mathrm{V/s}$	4560 $\mathrm{cm}^2/\mathrm{V/s}$	11600 $\mathrm{cm}^2/\mathrm{V/s}$
Interface roughness	2.4 Å	2.4 Å	1.8 Å
Percolation density	$6.0 \times 10^{11}\mathrm{cm}^{-2}$	$6.0 \times 10^{11}\mathrm{cm}^{-2}$	$1.6 \times 10^{11}\mathrm{cm}^{-2}$
Scattering charge density	$7.6 \times 10^{10}\mathrm{cm}^{-2}$	$7.6 \times 10^{10}\mathrm{cm}^{-2}$	$5.2 \times 10^{10}\mathrm{cm}^{-2}$
Interface correlation length	26 Å	26 Å	22 Å
Wafer type	10 000 Ω-cm, n	10 000 Ω-cm, n	10 000 Ω-cm, p*
Polysilicon gate stack thickness	100 nm	100 nm	200 nm
Silicon gate oxide thickness	35 nm	35 nm	35 nm

*Device B contains a 99.95% Si^{28} enriched epitaxy layer.

TABLE II. Experimental parameters for various data sets of the main text, for devices A1 and A2.

Data	**Fig 1d**	**Fig 2a**	**Fig 2b, top inset**	**Fig 2b, bottom inset**	**Fig 4b**
Device	A1	A2	A1	A1	A2
AD	1.75 V	1.25 to 1.65 V	0.840 to 0.870 V	0.790 to 0.820 V	1.25 to 1.40 V
AR	3.0 to 6.0 V	3.0 to 6.0 V	4.4 to 4.9 V	4.2 to 4.5 V	6.5 V
C1	-1.0 V	-3.0 V	-1.0 V	-1.0 V	-1.0 V
C2	-3.0 V	-1.4 V	-3.0 V	-3.0 V	-3.0 V
C3	-1.0 V	-1.4 V	-1.0 V	-1.0 V	-1.0 V
C4	-1.0 V	-1.0 V	-1.0 V	-1.0 V	-1.0 V
TSET	2.59 V	2.0 V	2.45V	2.59 V	2.0 V
U	-1.32V	-1.4 V	-3.19 V	-2.32V	-1.4 V
L	-2.06 V	-1.4 V	-1.75V	-2.06V	-1.4V
AD'	0.980V	0V	0.5127 V	0.980 V	0V
AR'	7.0 V	0 V	7.0 V	7.0 V	0V
C2'	-3.0 V	0 V	-1.0 V	-1.0 V	0 V
C3'	-1.0 V	0 V	-1.0 V	-1.0 V	0 V
TSET'	0 V	0 V	0 V	0 V	0 V
U'	0V	0 V	0 V	0 V	0 V
L'	0 V	0 V	0 V	0 V	0 V
Details	Thomas-Fermi numerical simulations.	Charge sensing, $f_{\mathrm{LI}} = 16.4$ Hz (lock-in frequency), $\mathrm{V_{SD}} = 100\ \mu$V (source-drain voltage).	Pulse spectroscopy, measured by charge sensing, $f_{\mathrm{LI}} = 19$ Hz, $\mathrm{V_{SD}} = 100\ \mu$V.	Single-shot measured by RF reflectometry, carrier wave $f = 180$ MHz, bandwidth of 326 kHz.	Charge sensing, $f_{\mathrm{LI}} = 16.4$ Hz, $\mathrm{V_{SD}} = 100\ \mu$V.

which is directly attainable from the measurements in Fig. **??**(b). From the data, we extract a slope of $\frac{\Delta\Gamma_{AR,AD}}{\Delta V_{AR}} = 5.9 \pm 0.7$ decades/$\mathrm{V_{AR}}$, describing the change in tunnel rate induced by a change in both $\mathrm{V_{AR}}$ and $\mathrm{V_{AD}}$. With a lever arm $\alpha_{AR} \sim 0.007$ eV/V, we determine $\beta_{AR,AD} = 0.9 \pm 0.3$ decades/meV.

For comparison, we extract $\beta_{1,2}$ for a multilayer enhancement mode Si/SiGe device which uses a dedicated barrier gate located directly on top of the tunnel barrier, sandwiched between the reservoir and QD gates (Zajac *et al.*[1]). Information on the tunnel rates are determined from the stability diagram

TABLE III. Experimental parameters for various data sets of the main text, for device B. All measurements are made with a Lock-In frequency of 492.6 Hz and a source drain bias of 50 μ V rms.

Data	**Fig 3b and 3c**	**Fig 3d**	**Fig 4a**	**Fig 4b**
Device	B	B	B	B
AD	1.2 to 1.8 V	0.9 to 1.6 V	1.8 V	1.21 to 1.8 V
AR1	3.0 to 7.0 V	5.15 to 8.0 V	5.0 V	5.0 V
AR2	3.5 V	3.15 to 4.75 V	3.0 V	3 to 3.1 V
C1	-2.7 V	-1.5 V	-6.7 to -5.3 V	-6.7 to -0.76 V
C2	-4.0 V	-3.0 V	-3.0 V	-3.0 V
C3	-0.26 V	0 V	-0.26 V	-0.26 V
C4	-4.2 V	-4.2 V	-4.2 V	-4.2 V
TSET	2.61 V	0 V	2.53 V	2.53 V
SETR1	2.5 V	0 V	2.5 V	2.5 V
SETR2	2.5 V	0 V	2.5 V	2.5 V
U	-1.5 V	0 V	-4.8 V	-4.8 V
L	-4.8V	0V	-0.92V	-0.92 to -1.26 V

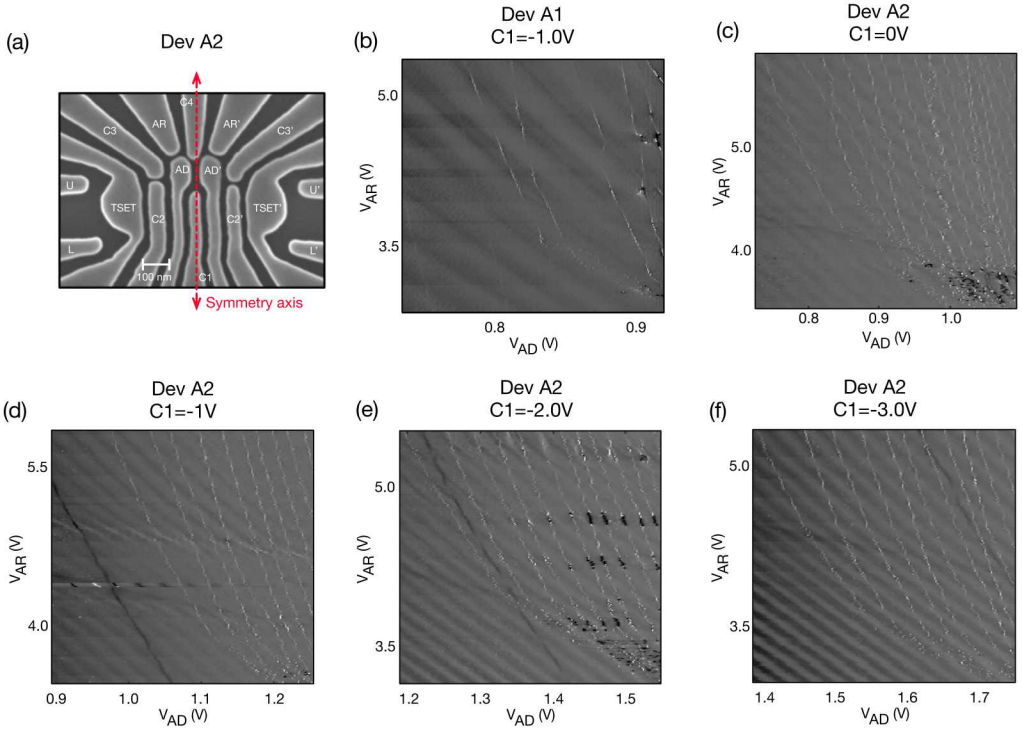

FIG. 1. (a) SEM of single-lead device A2. The device has a symmetry axis between the two quantum dots. Experiments on device A2 involved the formation of a single quantum dot, on the left side of the device only (under AD).(b) Wide range stability diagram for device A1 corresponding to bottom right inset of Fig. 2(a) in the main text. The pale charge transitions on the left-hand side are transitions in the left QD, which was activated for this measurement serie. The large features of device A1 and the small negative voltage on C1 are responsible for the irregularities in the right dot transitions (right hand side). (c), (d), (e), (f) Stability diagrams for device A2, with all parameters kept the same except for C1 gate voltage. A more negative voltage on C1 leads to more regular quantum dots, as expected.

of the tunnel barrier gate LB1 and the QD gate L1 (Fig. 2a of Zajac *et al.*[1]). To more easily compare this data to our device, we relabel LB1→BG and L1→AD. The voltage ranges studied show transition rates ranging from the measurement sample rate (assumed to be at least 10 Hz) to the lifetime broadened regime ($\frac{k_B T_e}{h} = 800$ MHz for a reported electron temperature of $T_e = 40$ mK). This provides two coordinates $(\Gamma, \mathrm{V_{BG}})$ to estimate the tunnel rate orthogonality, for which we find $\Delta\Gamma_{BG,AD} = \frac{7.9\mathrm{decades}}{0.4\mathrm{V_{BG}}} = 19.8\,\mathrm{decades/V_{BG}}$. From the reported lever arms and capacitance ratio for the QD and barrier gates, we determine $\alpha_{BG} = 0.022$ eV/V, and thus $\beta_{BG,AD} = 1.4 \pm 0.5$ decades/meV.

The definition of $\beta_{1,2}$ lends itself to compare other devices and geometries as well, as $\beta_{1,2}$ is independent of geometry specific information like capacitances. The concept of $\beta_{1,2}$ can also be extended to optimize QD devices for other characteristics which may be useful for qubit operation. For example, on can similarly define a parameter that describes the orthogonality between a double-QD coupling and the double-QD detuning, or a double-QD coupling and the valley splitting.

IV. VALLEY SPLITTING TUNING

In this section, we examine the spin filling and singlet-triplet energy splitting in our silicon QDs using magnetospectroscopy.[1–3]

The first 4 charge transitions from device B are shown as a function of transverse magnetic field, at $\mathrm{V_{AD}}$=1.8 V, in 2(a). The first transition shows a shift in chemical potential consistent with a lowering of energy due to increasing Zeeman splitting. The inflection point at $B = B_{ST}$ in the $N = 1 \rightarrow 2$ charge transition indicates the magnetic field at which the singlet-triplet (ST) transition occurs in the quantum dot.[4,5] The magnetospectroscopy for the $N = 2 \rightarrow 3$ transition has an inflection at the same B-field as the $N = 1 \rightarrow 2$ transition. This is consistent with a simple model for which there are two valleys and the 2^{nd} valley is loaded with a 3^{rd} electron as spin down. The inflection point again marks the crossing of the spin up of the lower valley with the spin down of the upper valley. The 4^{th} electron then loads always spin up, also suggesting that the next orbital energy is well offset from this lower manifold, which is indeed consistent with the order of 3 meV estimate from the Coulomb diamonds. This spin filling also indicates a relatively small Coulomb repulsion relative to orbital energy spacing.[6]

The magnetospectroscopy measurements are repeated for different $\mathrm{V_{AD}}$, compensating with the confinement gate C1 to maintain charge occupation. We estimate the single particle valley splitting from $E_{VS} = g\mu_B B_{ST}$, assuming $g = 2$, for devices A2 and B (2(b)). For device B, we extract a linear tunability of E_{VS} with the accumulation gate voltage of 231 ± 15 μ eV/V, the error range corresponding to a 95% confidence interval on the fit. Roughly approximating the vertical electric field as $\Delta F_Z = \Delta \mathrm{V_{AD}}/t_{ox}$, where t_{ox} is the gate oxide thickness, 35 nm here, we convert this tunability to 8.1 ± 0.6 μeV m/MV. The linear trend is qualitatively consistent with theory and recent observations in MOS QDs.[4,8]

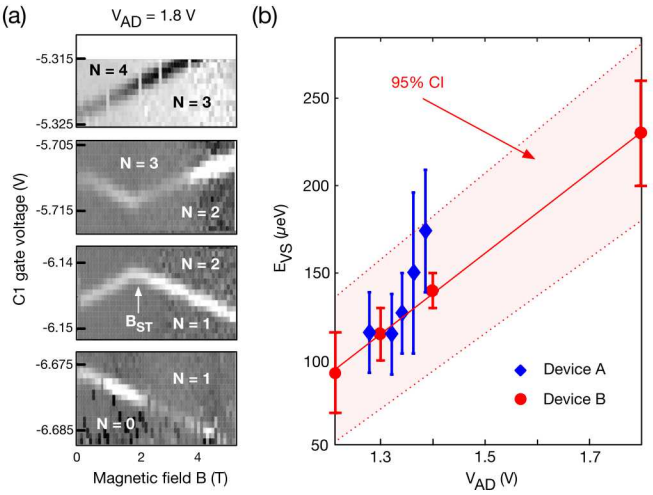

FIG. 2. (a) In-plane magnetospectroscopy measurements for device B, for transitions $N = 0 \rightarrow 1$, $1 \rightarrow 2$, $2 \rightarrow 3$, and $3 \rightarrow 4$, from a stability diagram similar to Fig. 3(c) of the main text, at $\mathrm{V_{AD}}$=1.8 V. A lever arm of 31 ± 4 μ eV/mV is inferred assuming g=2, within 15% of the lever arm extracted from Coulomb peak width temperature dependence.[7] B_{ST} indicates the magnetic field at which the singlet-triplet transition occurs. (b) Extracted valley splitting E_{VS} as a function of the dot accumulation gate voltage $\mathrm{V_{AD}}$. The diamonds (blue) data points are for device A2 (single-lead, Fig. 1), and the circles (red) data points are for device B (two-leads, Fig. 3(a) of the main manuscript). Dashed red line indicates the fit for the valley splitting tunability of device B, and the 95% confidence range (CI) is indicated by the red filled region.

For device A2, although the measurements were too noisy to extract a convincing tunability fit, all data points are located into the confidence interval for device B's tunability. We note that differences in valley splittings between devices A2 and B would be expected from variations in electrostatic environments (e.g., gate layout and dimensions, distribution of voltages to reach single electron occupation and threshold voltages) and in interface roughness, approximately 20% different between the two samples.[8]

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