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Extraction and Comparison of Interface Trap Formation During BTI Stress in SiC Power MOSFETs Using Subthreshold Characteristics

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Purpose

- Silicon Carbide (SiC) devices are theoretically superior to Si for power electronics applications
- Reliability concerns have limited implementation
  - High interface trap density
  - V_{th} instability at elevated temperature and biases
- Evaluation of interface trap density on vertical SiC power MOSFETs difficult without MOS capacitors and processing information from the manufacturer
- The increase in interface trap density after stress can be extracted solely from subthreshold I-V curves

Outline

- Introduction
- Method Overview
- Extraction with an Assumed Doping Density
  - Normalizing Energy Levels and ΔD_{IT}
- Sensitivity Analysis
  - Doping Concentration
  - Threshold Voltage
  - Oxide Capacitance
- Improvements in ΔD_{IT} for SiC MOSFETs
- Conclusions

Gate Oxide Reliability Has Limited the Adoption of SiC MOSFETs

Critical gate oxide interfacial region

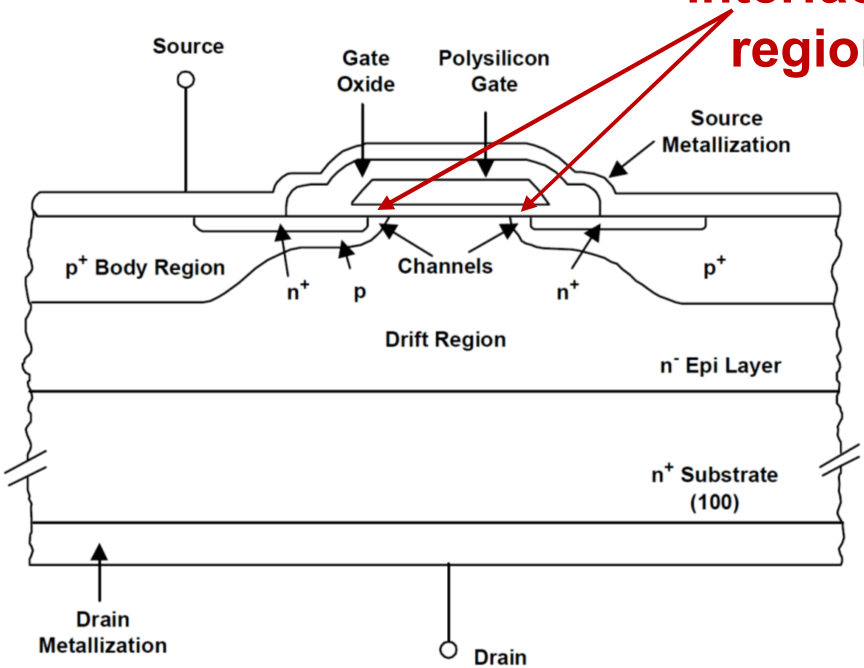


Diagram source: International Rectifier, "Power MOSFET Basics"

Charge injection due to small band offset at SiO_2/SiC interface enhances V_T shift

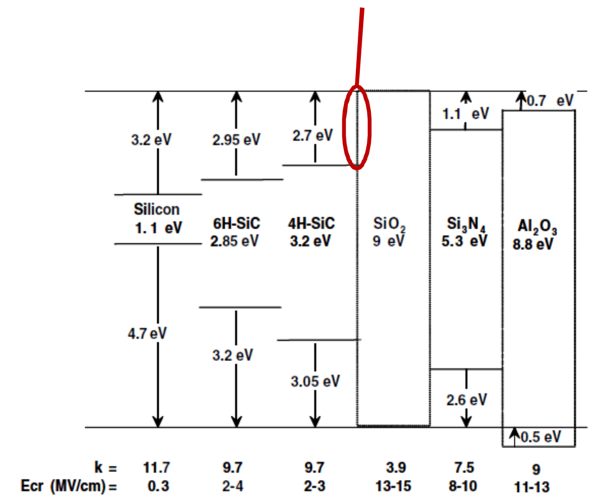


Fig. 1. Dielectric constants, and critical electric fields of various semiconductors (Si, 6H-SiC, 4H-SiC) and dielectrics (SiO_2, Si_3N_4 and Al_2O_3). Conduction and valence band offests of these are also shown with respect to SiO_2.

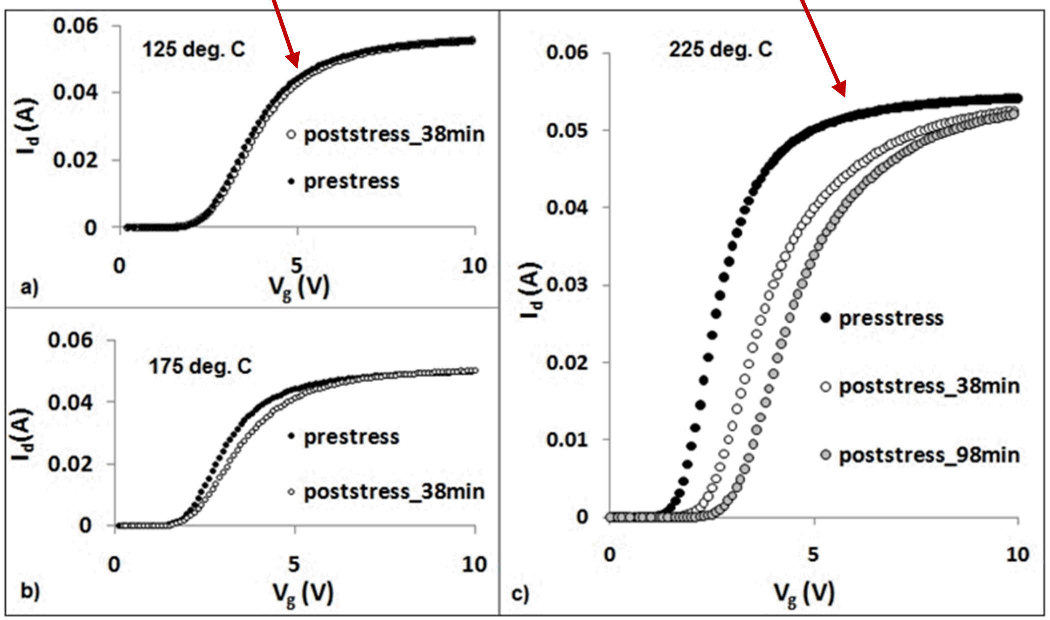
R. Singh, *Microelectronics Reliability* 46, 713 (2006).

The typical SiC power MOSFET structure (vertical DMOS) is not ideal for charge pumping since there is no body tie

Bias-Temperature Stress: ΔV_{th} and Increase in MOS Interface State Density

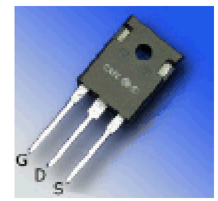
Minimal degradation at rated temp (125˚C)

Severe degradation at high temp



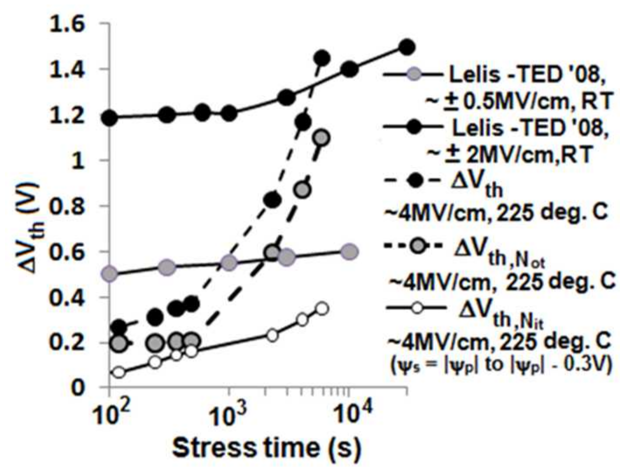
Stress: V_{GS} = +20 V, V_{DS} = 0.1 V

S. DasGupta et al., *Appl. Phys. Lett.* 99, 023503 (2011).



TO-247-3

Commercial 1200 V SiC MOSFET



Evolution of interface and bulk trapping components vs. time

Method Details

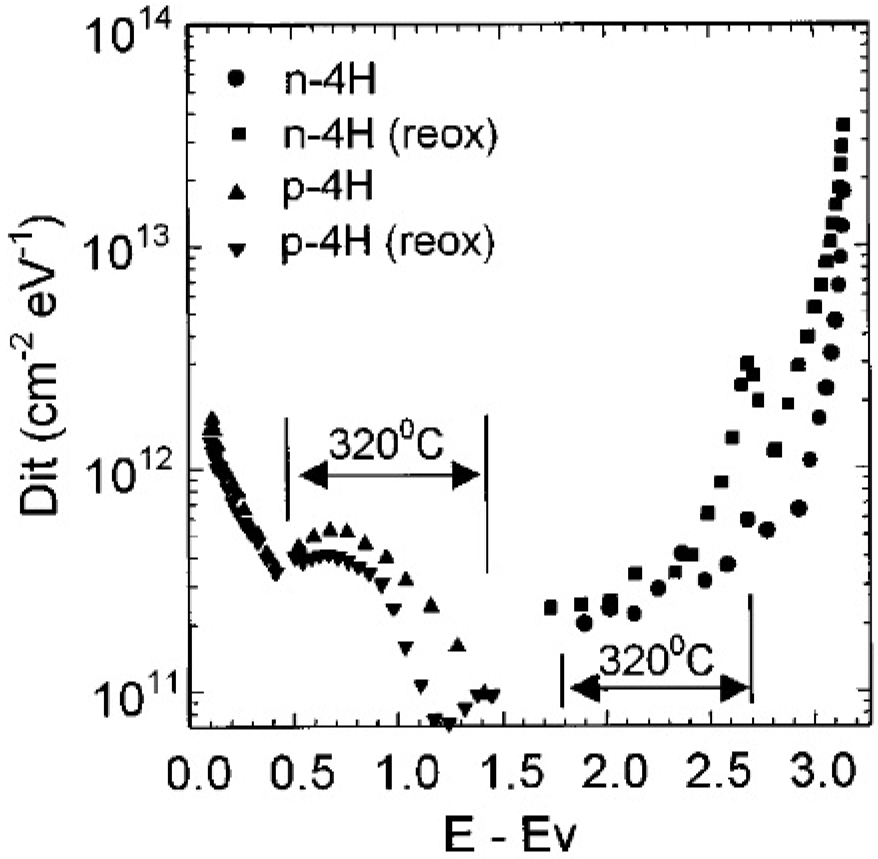
- **High interface trap densities cause a change in subthreshold slope**
  - **Modulates the fraction of V_G that determines the barrier between source and drain**

- $\boldsymbol{S} = \ln(\mathbf{10})\,\frac{\boldsymbol{kT}}{\boldsymbol{q}}\left(\mathbf{1} + \frac{\boldsymbol{C_d}+\boldsymbol{C_{it}}}{\boldsymbol{C_{ox}}}\right)$

D_{IT} at the Band Edges

- SiC has D_{IT} profiles that rise sharply towards the band edges

- This causes the subthreshold slope to vary with gate voltage
  - Enables extraction of D_{IT} profiles



G. Y. Chung et al., *Appl. Phys. Lett.* 76, 1713 (2000).

Method Overview

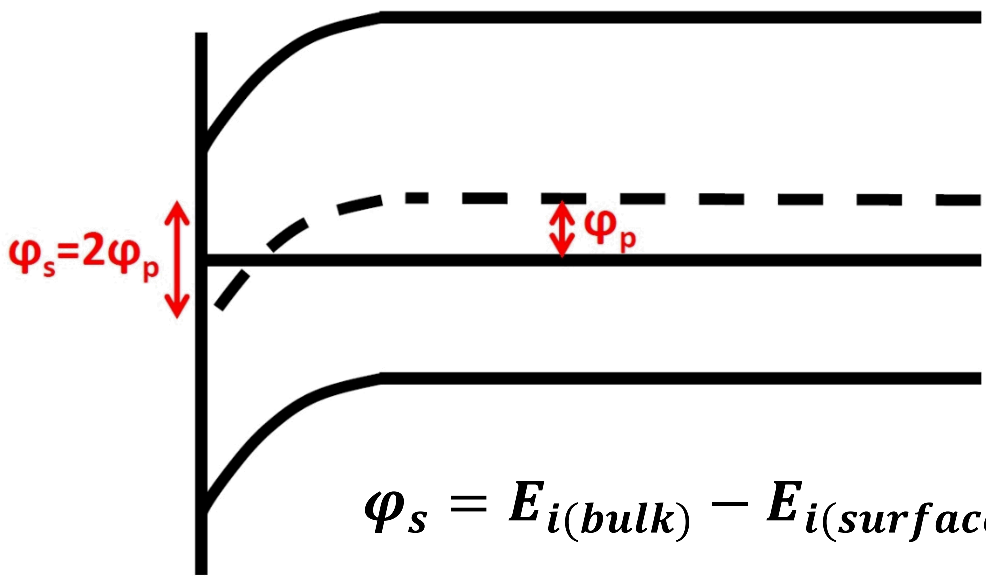
1) Establish a relationship between gate voltage and surface potential

2) Solve for changes in V_{IT} (voltage term for the contribution of trapped interfacial charge) for small intervals of surface potential

3) Solve for D_{IT} over these intervals based on ΔV_{IT} and construct a D_{IT} profile

Gate Voltage and Surface Potential

- Drain current can be related to surface potential via:
- $$I_D = I_{D0}(V_D)\frac{e^{\beta\varphi_s}}{\sqrt{\beta\varphi_s}}$$
  - Effectively relates V_G to φ_s (band bending)

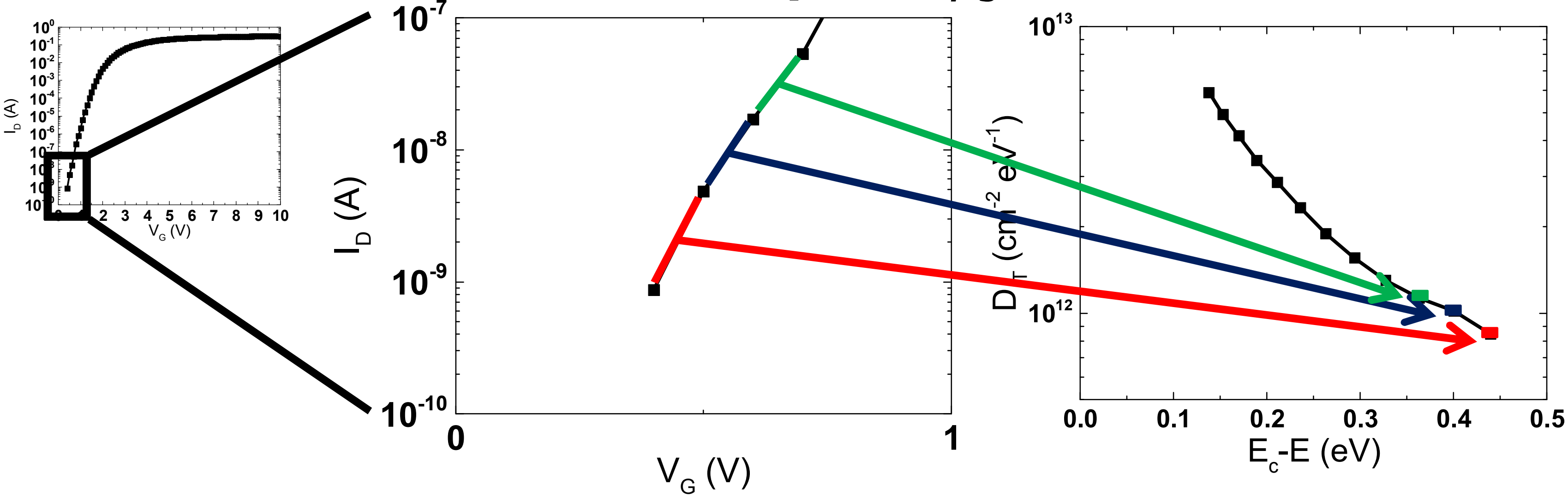


$$\varphi_s = E_{i(bulk)} - E_{i(surface)}$$

- Solve for I_{D0} at threshold
  - Determine I_{th} from I-V curve
  - Surface potential at threshold known in relation to doping

Calculating D_{IT}

- **Using V_G and φ_s, V_{FB}+V_{IT} can be solved for:**
- $(V_{FB} + V_{IT}) = V_G - \varphi_s - \frac{a}{\beta}\sqrt{\beta\varphi_s - 1}$
- **(V_{FB}+V_{IT}) is solved for at each point**
- **D_{IT} is calculated over the intervals between points via:** $D_{IT} = \frac{C_i}{q} \times \frac{\Delta V_{IT}}{\Delta\varphi_s}$



Example Calculation

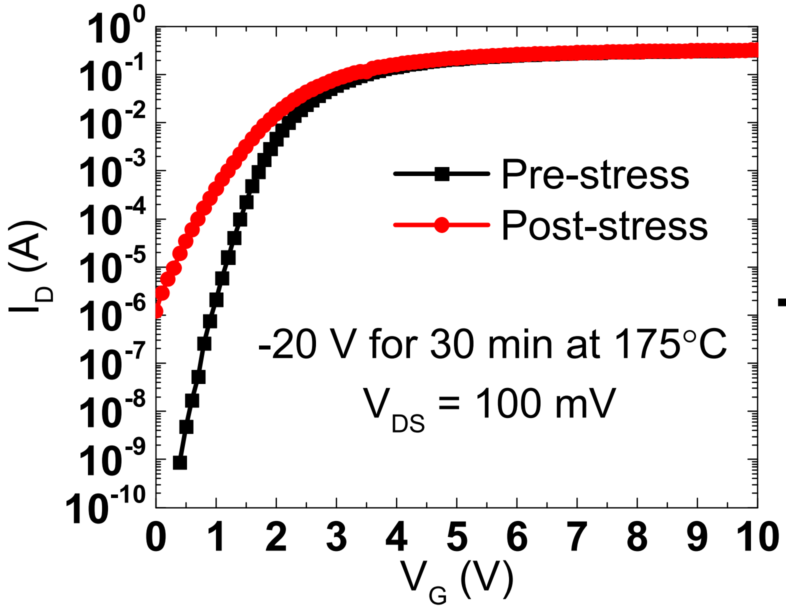
- Analysis of stresses performed on commercially available parts
- No knowledge of process parameters
  - Doping concentration assumed
- Three steps
  - Extraction
  - Normalization
  - Subtraction

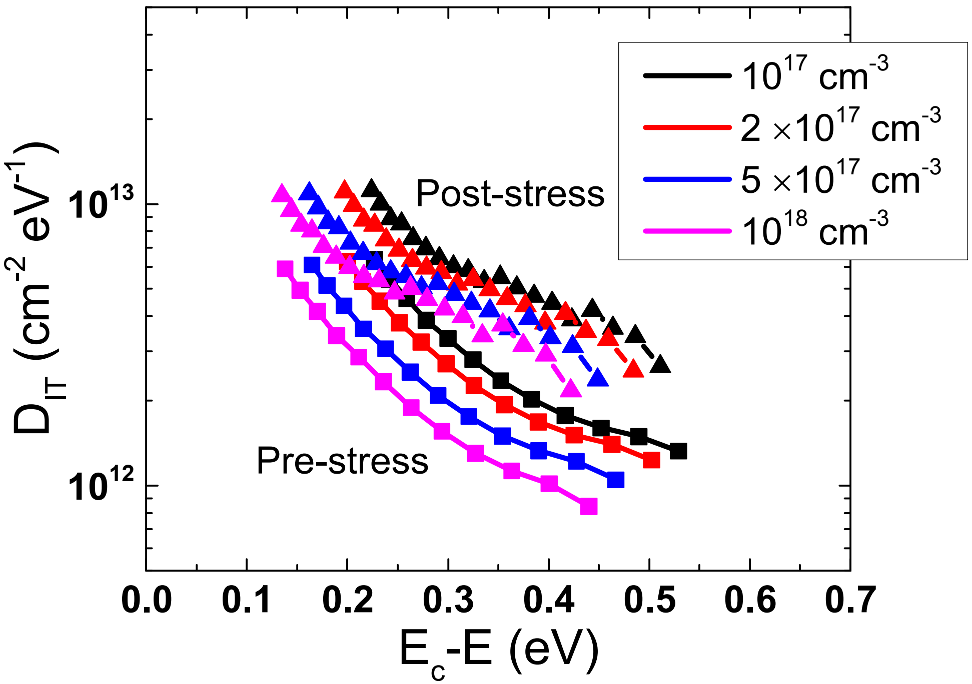
Extraction → Normalization → Subtraction

Extraction with Assumed Doping

Extraction → Normalization → Subtraction

- I-V curves for a SiC power MOSFET



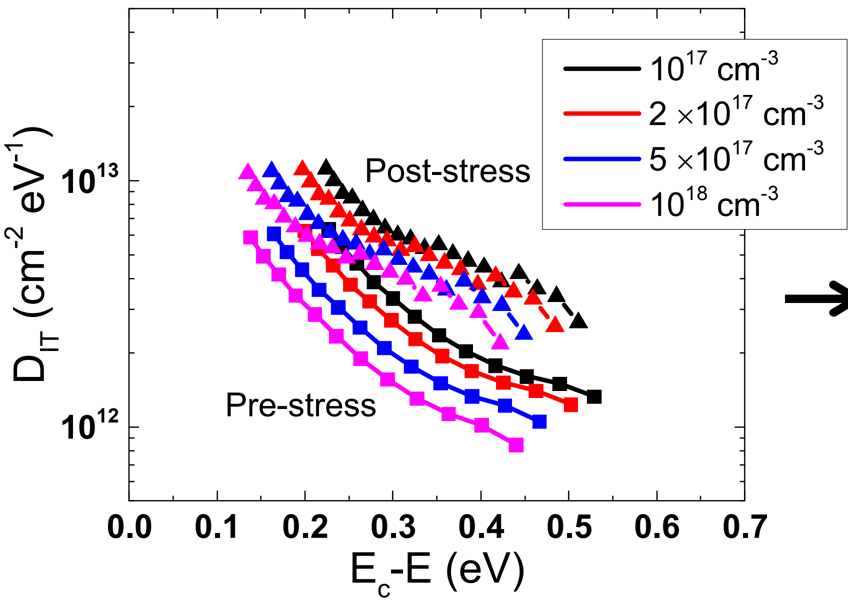


- Variation in assumed doping values causes shifts in the D_{IT} profiles

Normalizing the Energy Level

Extraction → **Normalization** → Subtraction

- **Varying the assumed doping changes the bulk potential, altering φ_s at V_{th}**



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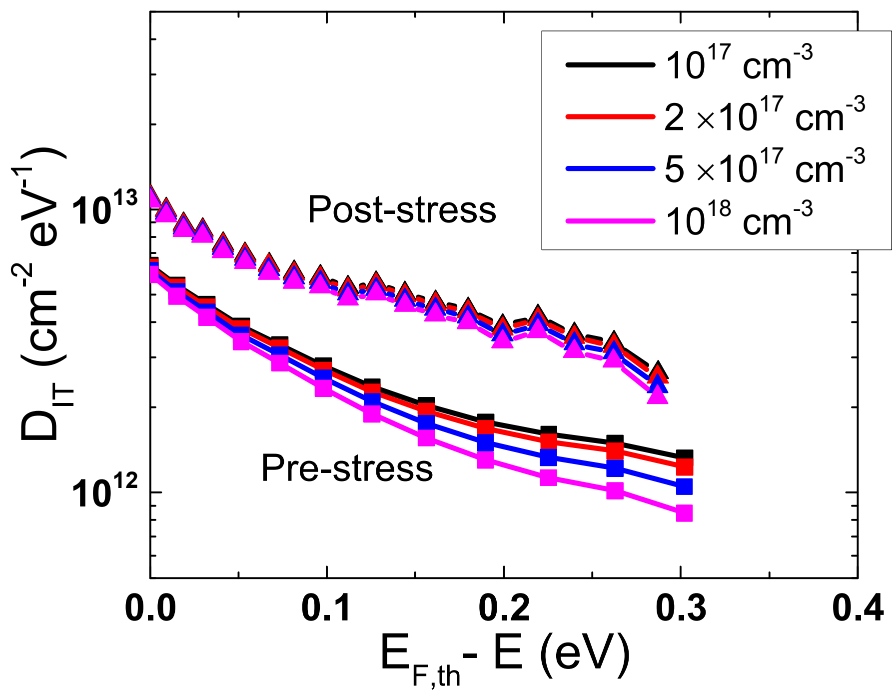
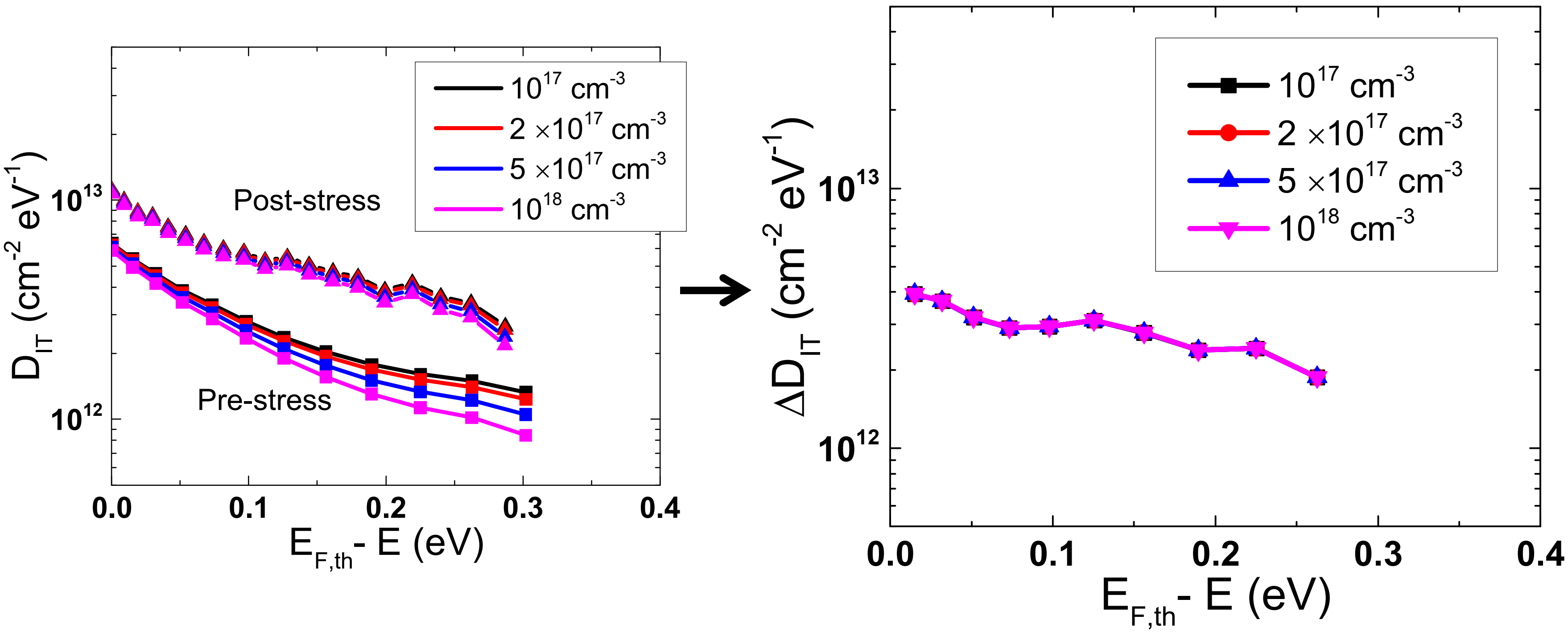


- ***D_{IT}* profiles can be aligned by normalizing the energy level to the Fermi level**

ΔD_{IT} Profiles

Extraction → Normalization → **Subtraction**

- **Variations in assumed doping cause changes in calculated D_{IT} concentrations**



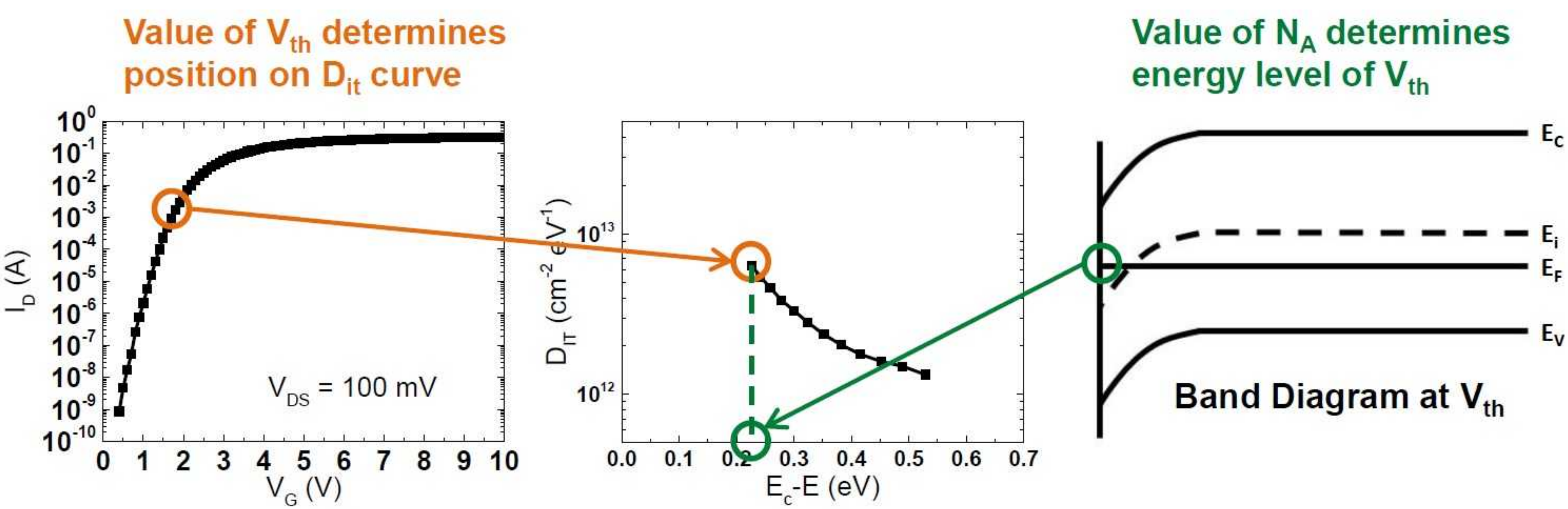
- **ΔD_{IT} profiles are independent of assumed doping concentration when referenced to $E_{F,th}$**

Sources of Uncertainty

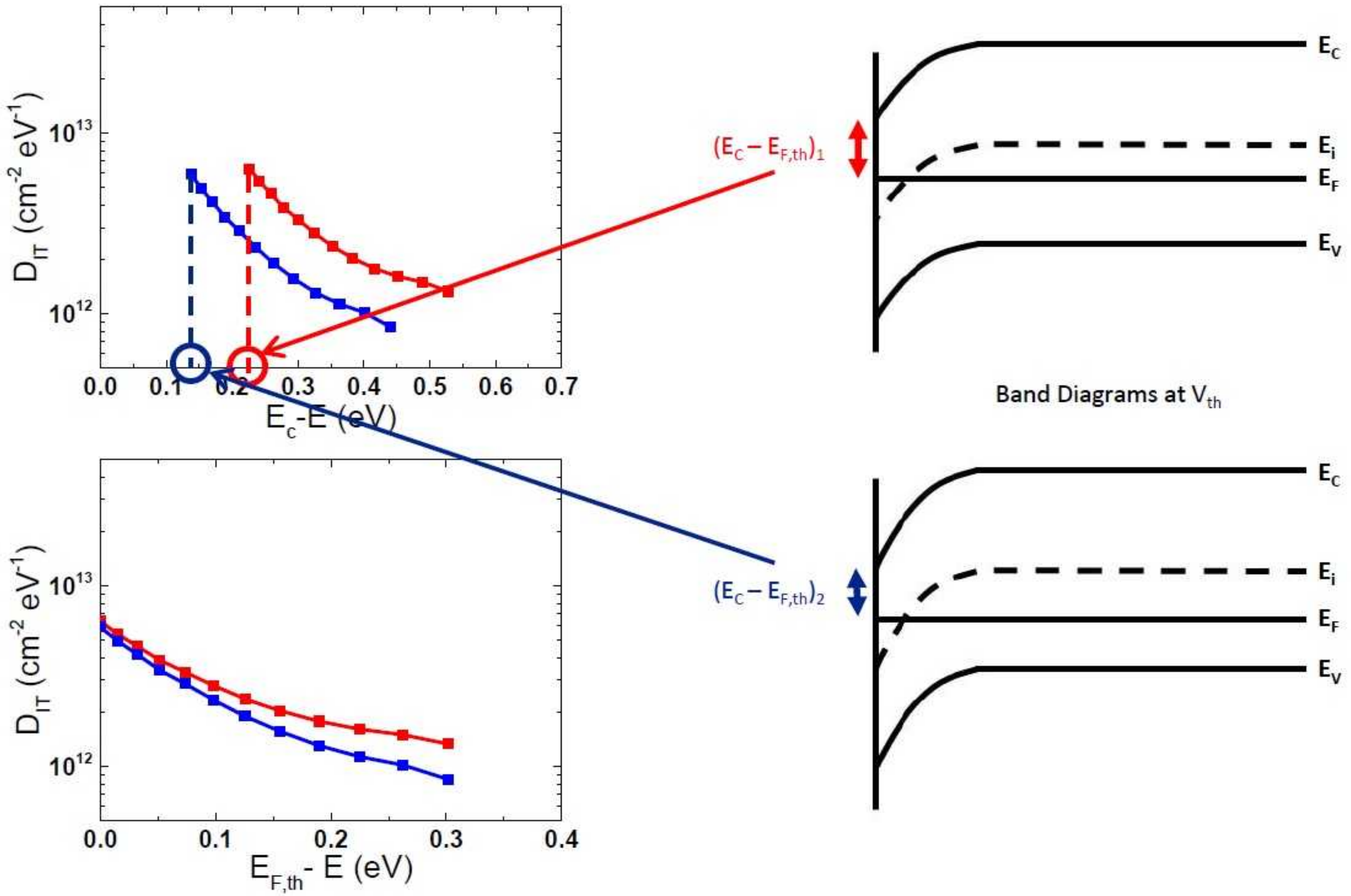
- **Doping**
  - Doping is required to calculate parameters like bulk potential
- **Threshold voltage**
  - There are multiple ways to extract threshold voltage that can yield different voltages
- **Oxide thickness (capacitance)**
  - The insulator capacitance is used to calculate V_{IT} and D_{IT}

Doping and Threshold Voltage Dependence

- **Assumed doping primarily alters the energy level at which V_{th} is set**
- **The choice of threshold voltage affects D_{IT} concentration at that energy level**

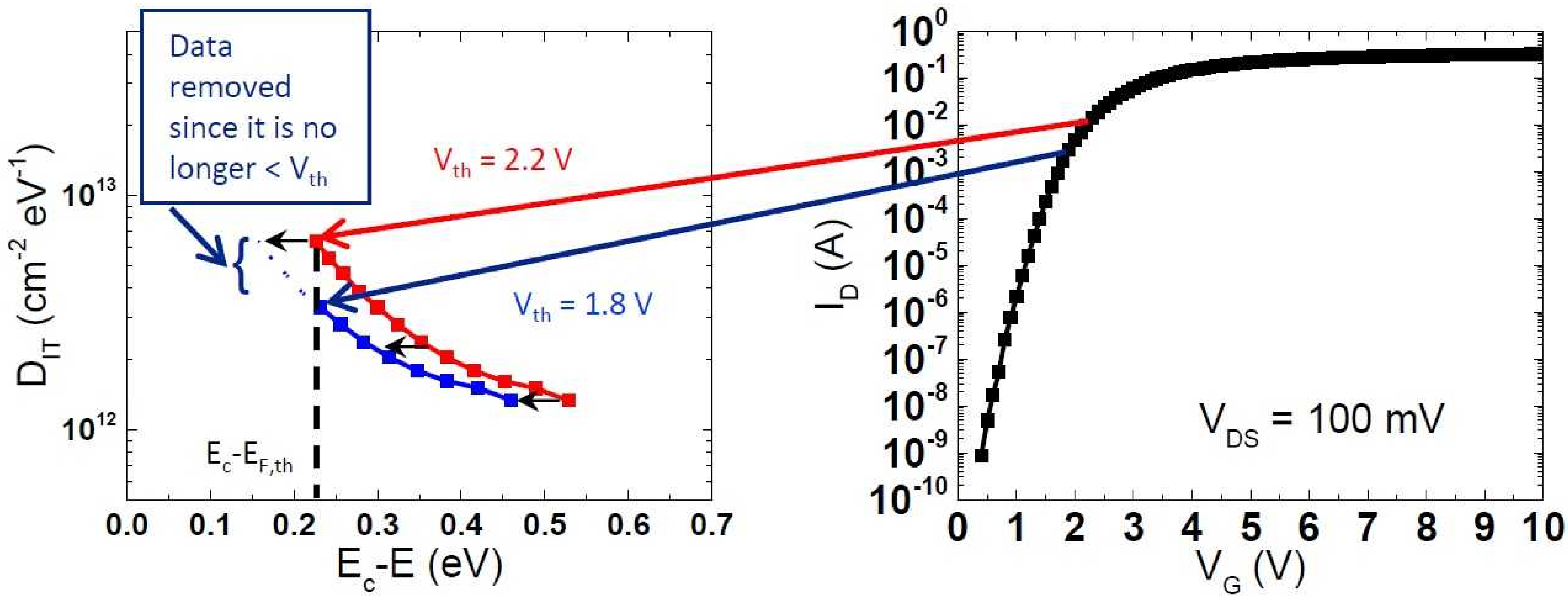


Doping Dependence



- **Varying doping varies $E_{F,th}$ → Normalize to $E_{F,th}$**
  - **Using ΔD_{IT} eliminates magnitude changes**

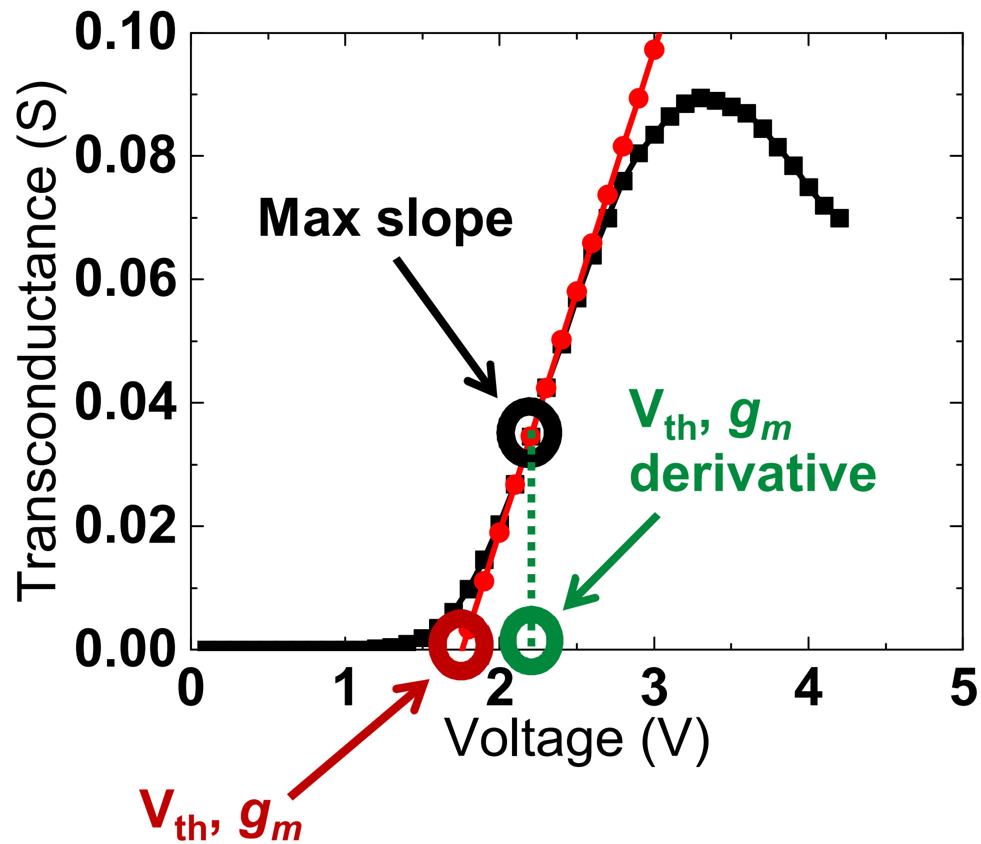
Threshold Voltage Dependence



- **The choice of V_{th} determines the value of D_{IT} at threshold**
  - **Varying V_{th} effectively shifts the curve and removes data for voltages above V_{th}**

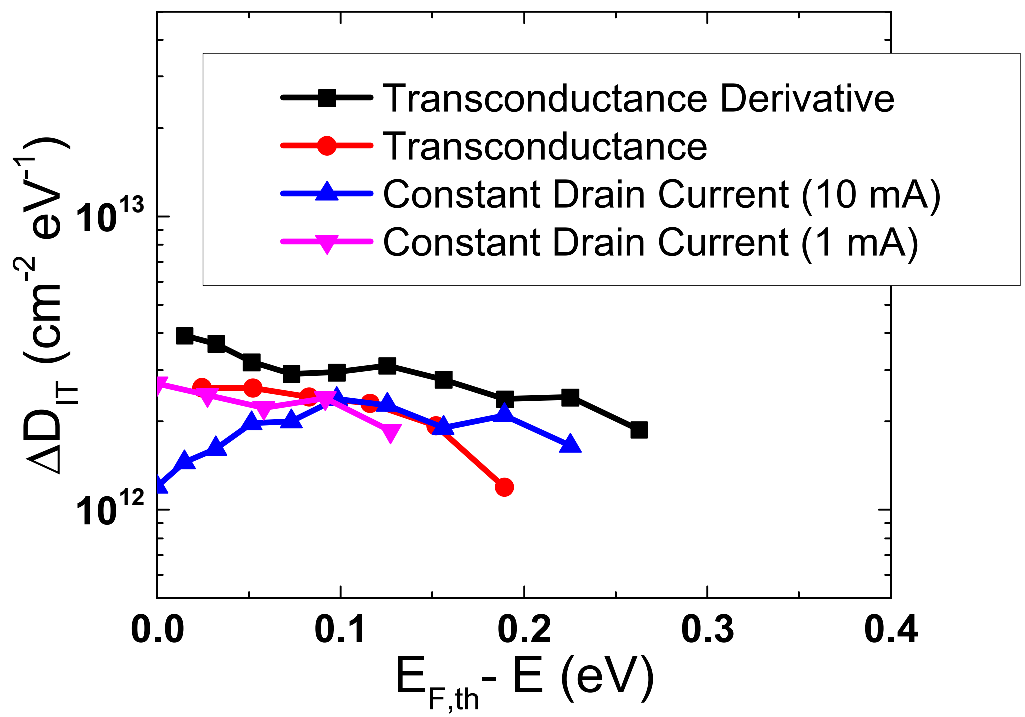
Threshold Voltage Extraction Methods

- Transconductance Derivative
  - Unaffected by series resistance and mobility degradation
- Transconductance
- Constant Current



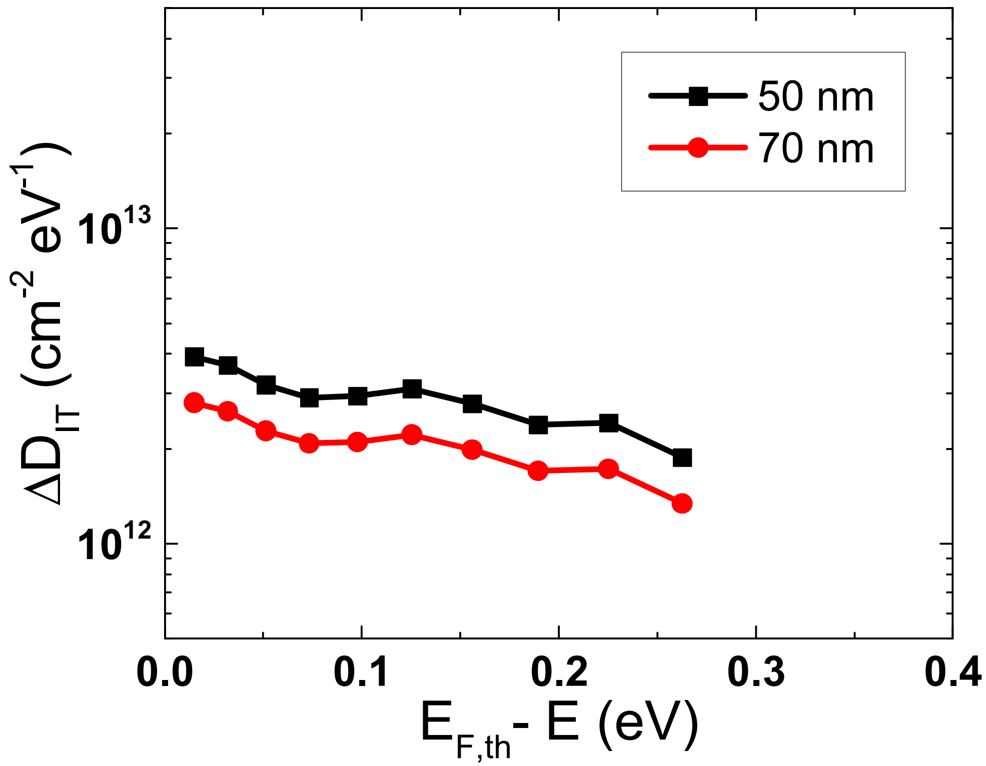
ΔD_{IT} Profiles for Varying V_{th} Extractions

- g_m derivative method and g_m method show similar trends
- Constant current (1 mA) uses lower V_{th}
  - Less points used
- 10 mA results are unphysical
  - Constant current may not be accurate method for these devices



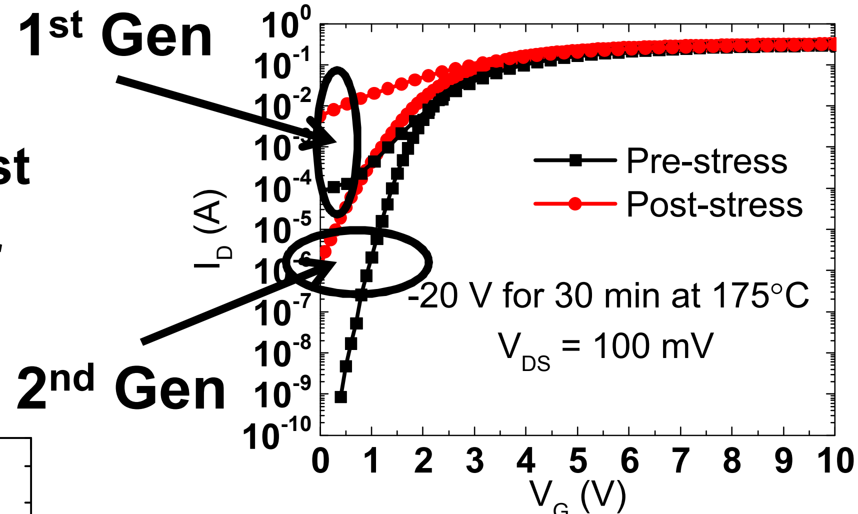
Capacitance Dependence

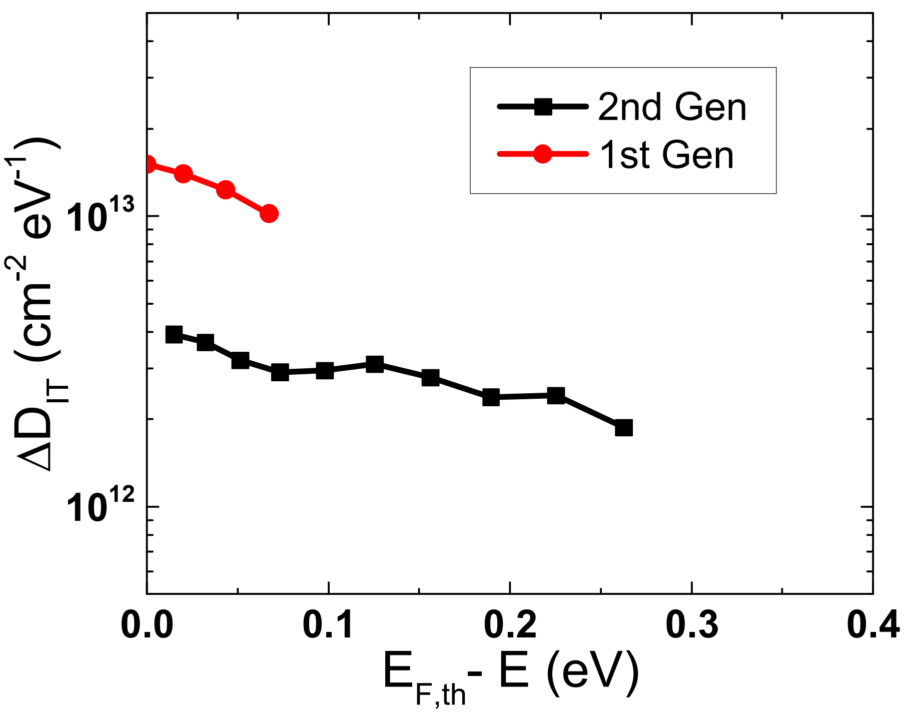
- Calculated ΔD_{IT} varies with oxide capacitance
  - Oxide thickness
- ΔD_{IT} changes by the ratio of the assumed C_{ox}
  - 70nm/50nm = 1.4
- Typical oxide thickness range small



ΔD_{IT} Comparison Between SiC MOSFET Generations

- D_{IT} has been reduced from the 1st to 2nd generation of SiC MOSFETs





- Less information for 1st gen
  - Equivalent voltage sweep covers fewer energies due to D_{IT}
  - Fewer I-V data points

Conclusions

- ΔD_{IT} profiles can be extracted from SiC MOSFETs using subthreshold I-V curves
  - Independent of assumed doping
  - No MOS capacitors needed
  - Impact of oxide thickness is minimal if the range is small
  - Can calculate D_{IT} values with additional information
- The choice of threshold voltage extraction method must be considered carefully
  - Constant current method may be of limited use
- This method provides a fast and easy way to evaluate the effects of BT stress on SiC MOSFETs