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Bottom-up STM-fabricated Si:P devices

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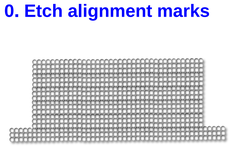
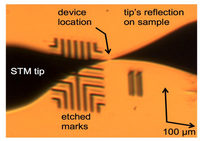
Scanning tunneling microscopy (STM) has been used to fabricate, bottom-up, simple planar Si:P devices with single-atom scale precision. We would like to expand the scope of the devices that can be made bottom-up using this process by developing:

1. **Faster writing, to enable more complex devices with more contacts**
2. **Engineered interfaces, to enable 3D device stacks**
3. **Better alignment, to enable more complex multi-step fab processing, including both the above**

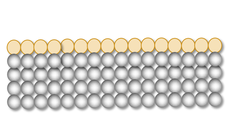
Recipe for single-atom-scale donor devices in Si, a la UNSW (Simmons & co.)

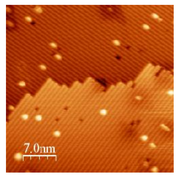
0. Etch alignment marks



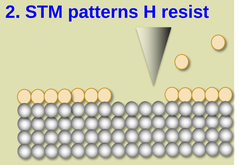


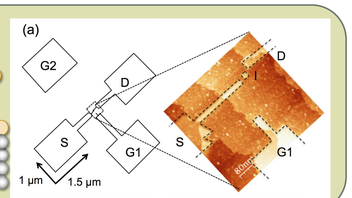
1. Clean Si (100) surface & H-passivate



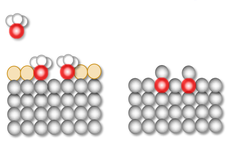


2. STM patterns H resist





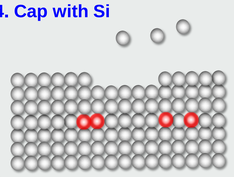
3. Dose with PH3, incorporate



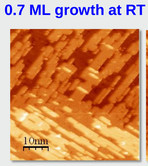
4K Hall measurements

Device #	e⁻ density n_e 10^{14} /cm²	e⁻ mobility cm²/Vs
1	1.7	25
2	1.5	20
3	1.8	26

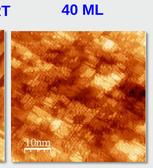
4. Cap with Si



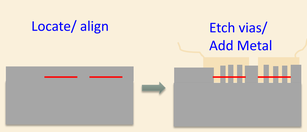
0.7 ML growth at RT

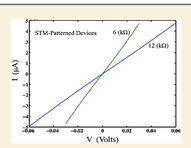


40 ML



5. Find and contact buried device



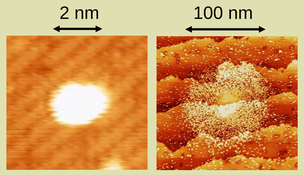


Transport at 4K confirming Ohmic contacts

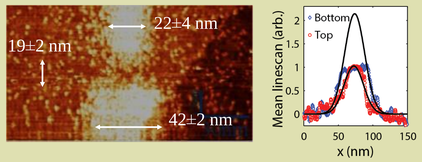
Rapid nanoscale patterning using STM field emission

STM depassivation of hydrogen is atomically precise, slow. Can you write faster? What are relevant design rules for other modes?

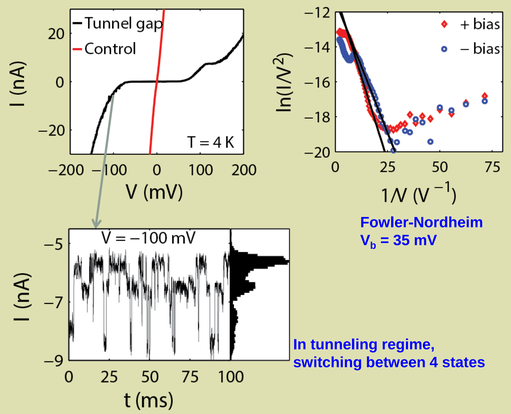
	Tunneling	Field emission
z	0.5 nm	10 nm
V	5 V	50 V
Speed	50 nm/s	2 µm/s
Precision	0.5 - 2 nm	10-100 nm



Level of blowout in H depassivation



4K transport data demonstrates tunneling



Fowler-Nordheim V_b = 35 mV

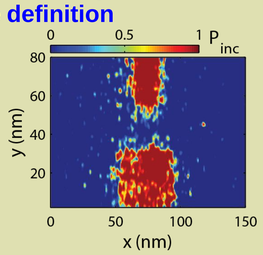
In tunneling regime, switching between 4 states

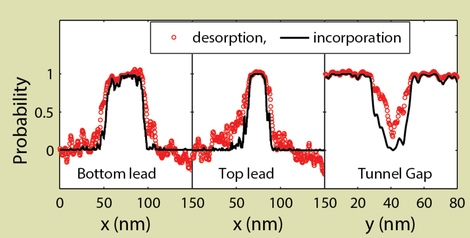
P incorporation chemistry enhances device definition

Phosphorus incorporation requires 3 adjacent dimers; probability is 1 for 6 dimer chain

$$P_{inc} = P_6 + (1 - P_6) * [P_5 + (1 - P_5) * \{P_4 + (1 - P_4) * P_3\}]$$

Fuechsle, Thesis (2012)

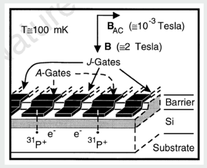




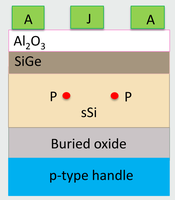
Development of vertical stack for 2Q operations

Current process produces 2D donor-based nanostructures

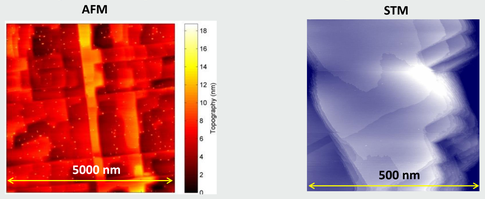
Would like to build a 3D device stack with an interface to pull electrons to for an exchange operation



Kane, Nature (1998)

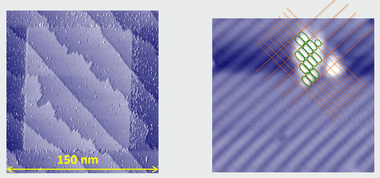


1. Can you prepare a clean sSOI(100) surface?

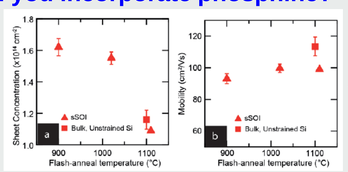


Relaxation of strain?

2. Can you do STM-based H lithography?

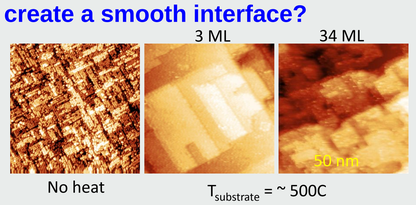


3. Can you incorporate phosphine?



Lee, Nanotech. (2014)

4. Can you create a smooth interface?

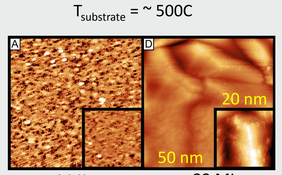


No heat

$T_{substrate}$ = ~ 500C

Strain matched

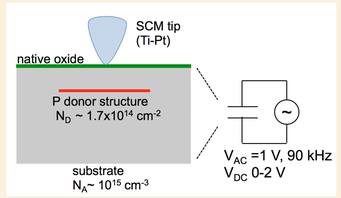
20 % Ge



Higher occurrence of atomic defects
Shallow (2-3 nm) islands

5. Can you make contact using the same via etch & metal deposition? **In progress**

SCM registration and alignment of buried Si:P device layer

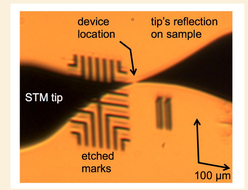


Need to locate buried device *ex situ* to wire it up.

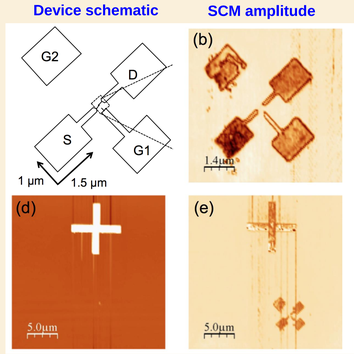
Scanning Capacitance Microscopy (SCM) measures local variations in doping via MOS *dC/dV*, and can detect 10^{15} cm^{-3} variation

Ex-situ alignment of buried device

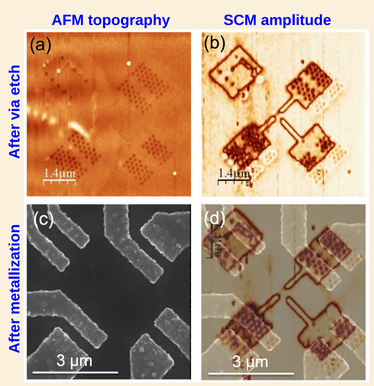
- **Optical location of tip precise to ~ 10 µm**
- **Lay down metal alignment cross**



- **SCM locates buried device with respect to metal alignment mark to ~ 100 nm**
- **Etch vias, deposit metal contacts**



Ability to see multiple layers at once



Verify aligment of buried device, vias, contact metal

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