6/16/2014

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SAND2014-15082PE

3D IC's For Space Applications

June 16, 2014

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Mixed Signal ASIC/SoC Products

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505-284-0153

Exceptional service in the national interest

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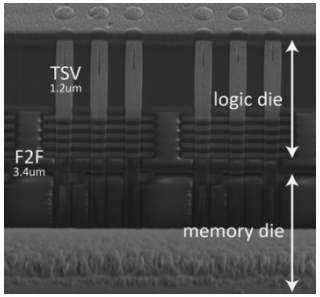

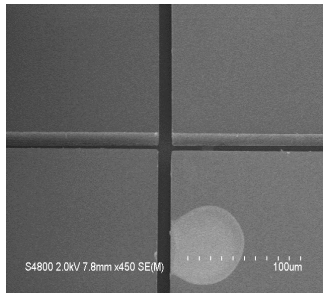

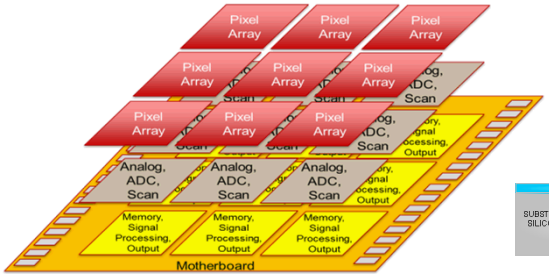

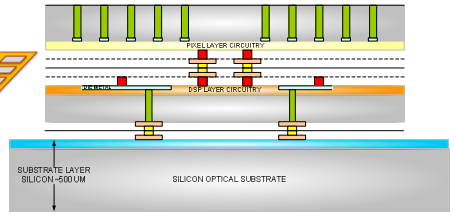

U.S. DEPARTMENT OF ENERGY

National Nuclear Security Administration

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Outline

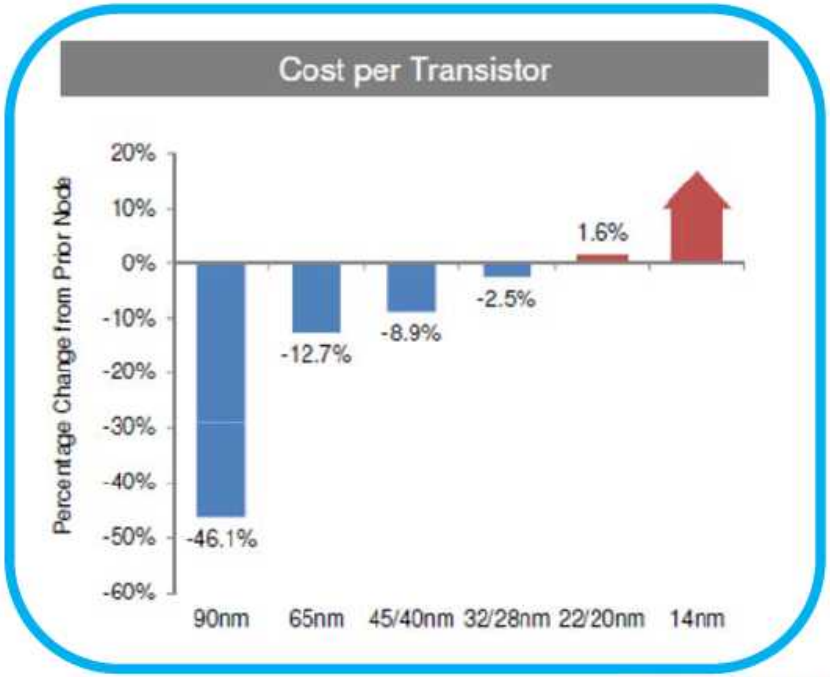
- Commercial Motivation
- 3D Processing Overview
- Commercial Trends & Adoption
- Space Based Applications & Qualifications
- Sandia Sensor Applications

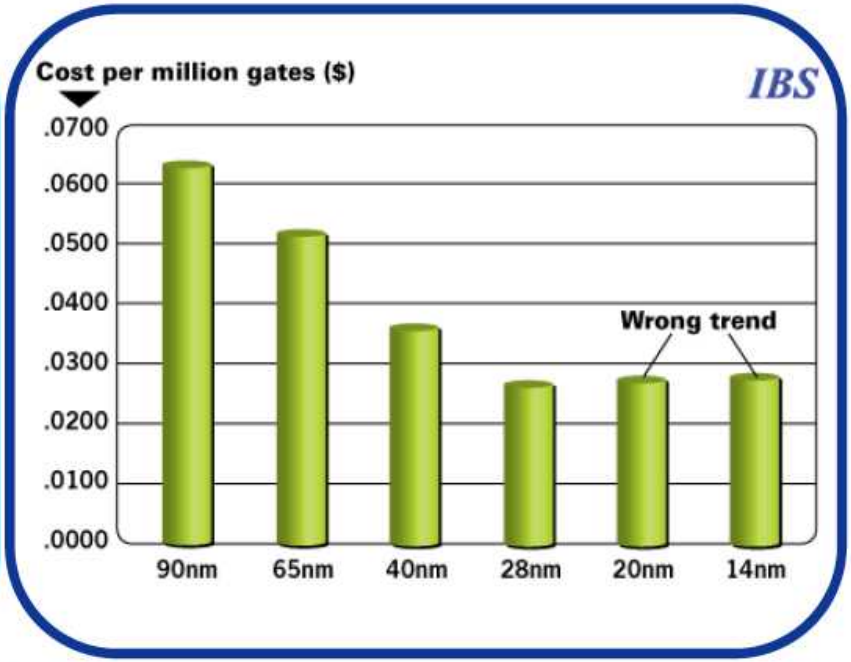
Limited 3D Commercial Adoption

- Limited by additional cost of 2.5D/3D fabrication
  - Through Silicon Via's (TSV)
    - Bosch Etch
    - Liner Deposition and Metal Fill
  - Bonding
    - Thermal Compression
    - Covalent
    - Eutectic
  - TSV Exposure
    - Backgrinding and Thinning
- Requires specialized processing, tools, materials research
- Additional yield loss in handling and process steps
- New design and test paradigms
- Lack of fully defined standards

Transistor Cost Growing

For the first time in history cost per transistor has increased





Sources: IBS and Nvidia

Transistor cost is pushing applications that don't require density/speed improvement to consider 2.5D/3D as a more cost effective solution.

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3D PROCESSING OVERVIEW

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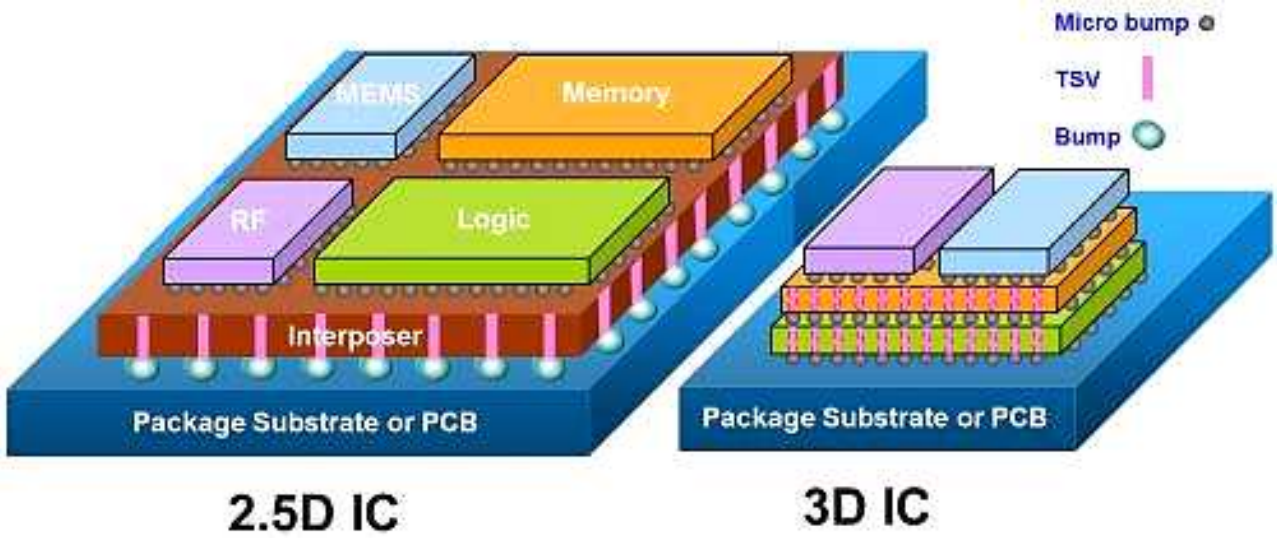
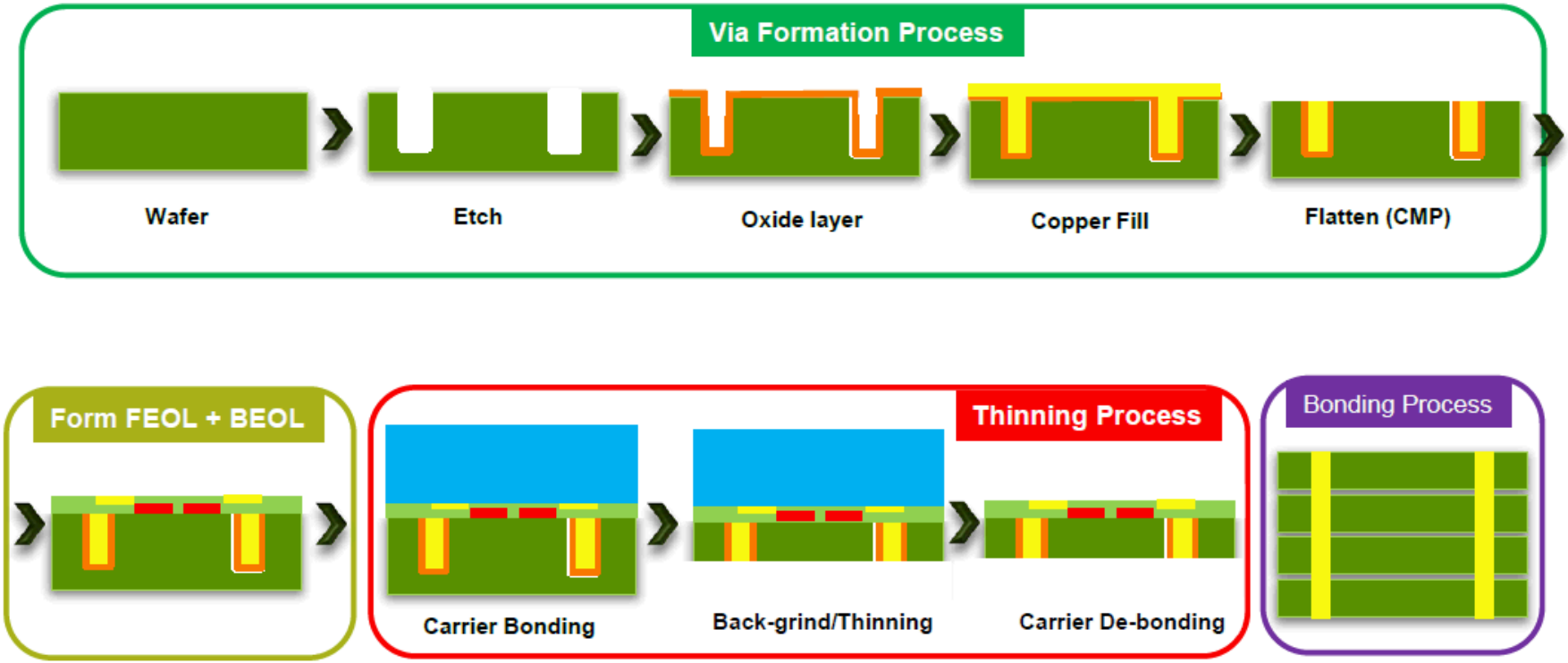
2.5D, 3D, 5.5D Integration

- 2.5D - Interposer Only Design
- 3D - vertically integrated IC's
- 5.5D - 3D + 2.5D, joke at DAC 2012 panel but very valid approach (think hybird memory cube combined with FPGA)



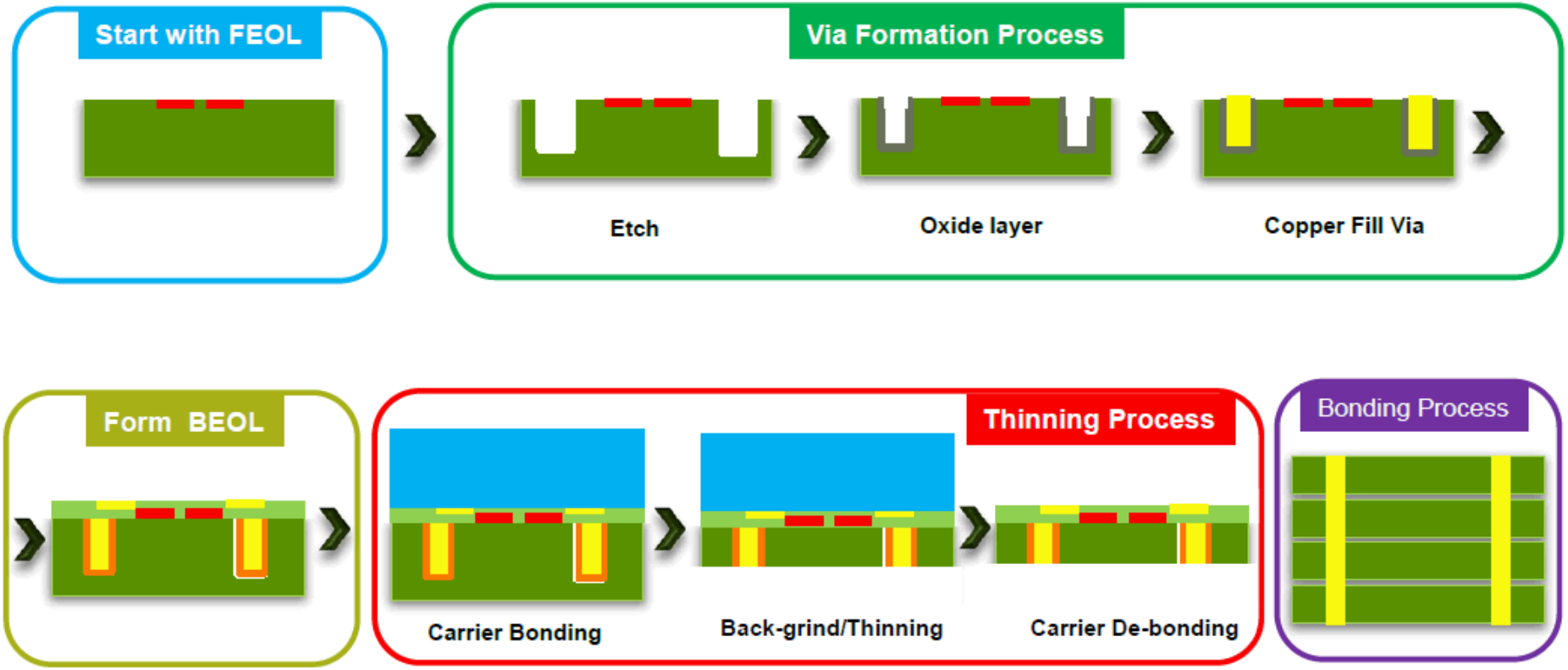
TSV First Approach (Before FEOL)

TSV inserted BEFORE any front end of line (FEOL) processing



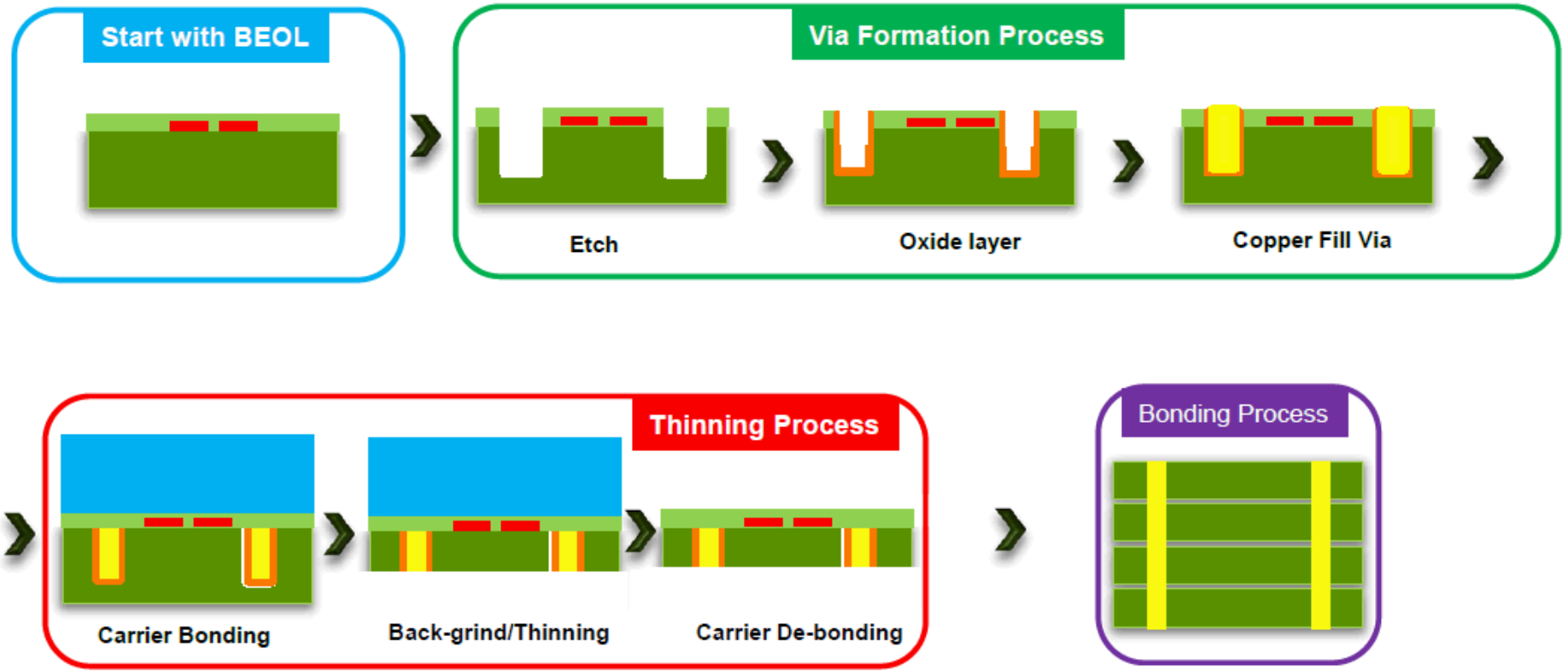
TSV Middle Approach

TSV inserted after FEOL processing but before back end of line (BEOL)
Note: This could also be done after a first few metal layers

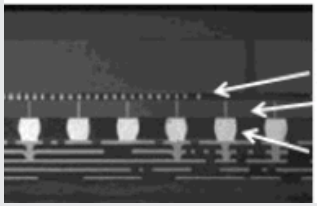
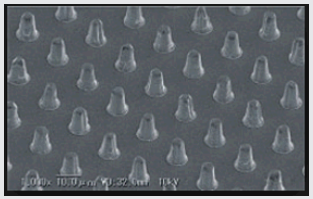
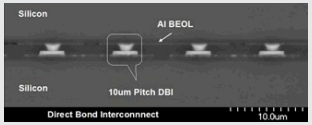


TSV Last Approach

TSV inserted after FEOL and BEOL. Both front side and backside TSV approaches are being explored (contact metal 1 or contact last metal)



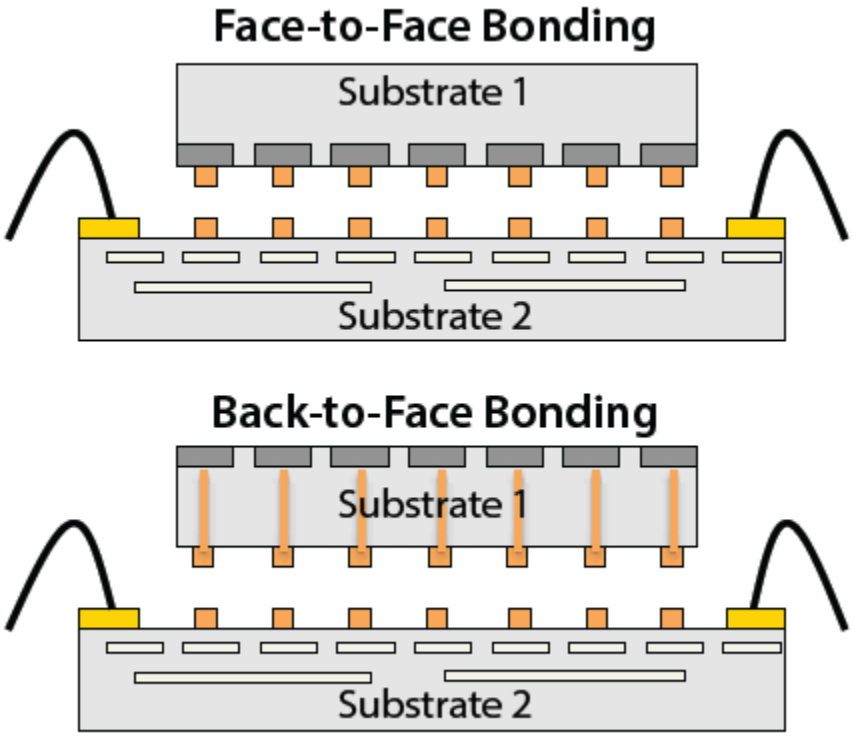
Bonding Technology

	C4	µBump	Indium Bump	DBI (Ziptronics®)
Density	Low	Moderate	Moderate	High
Minimum Pitch	300µm	150-20µm	10-15um	3µm
Method	D2D, D2W	D2D, D2W	D2D	W2W, D2W
Underfill	Yes	Yes	Yes	No
Maturity	High	High	High	Moderate
Images				

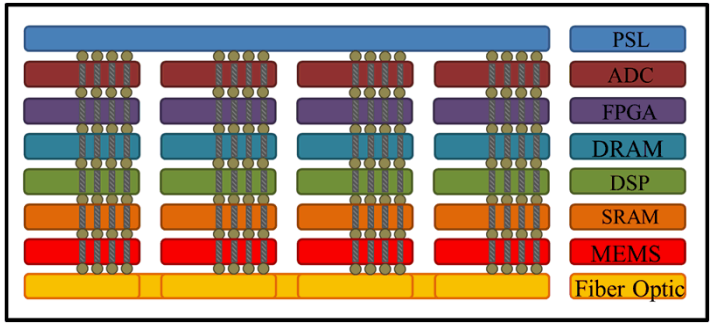
W2W = Wafer To Wafer Bonding
D2W = Die To Wafer Bonding
D2D = Die To Die Bonding

Bonding Surfaces

- Face-to-face limited primarily by bonding technology
  - Does not require TSV for 2-layers
- Face-to-back (or back-to-back) limited by bonding **AND** TSV pitch



3D Integration Considerations
Custom u-Systems & Heterogeneous Integration



- Layer-to-Layer Interconnect Density
- TSV Requirements (diameter, pitch)
- Stacked Alignment Accuracy
- Tiling Accuracy Placement Requirements
- Wafer Level vs. Die Level Requirements & Assembly
  - Most High Density Processes Require Wafer-To-Wafer Bonding
    - Wafer level processing required to define TSV's and interconnect layers
    - Wafer level processing required to thin wafer backside to reveal TSV's
  - Wafer Level Fabrication At Advanced Technology Nodes Can Be Cost Prohibitive
  - Costs Are More Manageable Using Multi-Project Wafer (MPW) Runs
    - Wafer contains designs for other users; Only die are ultimately available, which can complicate 3D processing approach
    - Circuitry must be partitioned to contain interconnect density

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COMMERCIAL TRENDS & ADOPTION

Commercial 3D Status

Company	3-D	2.5-D	Production	On-Shore	Notes
Intel	Yes	Yes	No	Yes	No public products released, but multiple research thrusts
IBM	Yes	Yes	No	Yes	MPW demonstrations in SOI.
Global	Yes	Yes	No	Yes	Functional at 20nm node. TSV-Middle approach, 6µm TSV diameter
Tezzaron (Novati)	Yes	Yes	No	Yes	Multiple approaches. Via First, Via Middle, 1-2um diameter. Low Volume
MIT Lincoln Labs	Yes	Yes	No	Yes	Low Volume specialized functionality. Integrated PDK for 3 layers, 3µm TSV diameter.
TSMC	Yes	Yes	Yes	No	2.5D high volume, Xilinx Virtex 7 FPGA
IMEC	Yes	Yes	?	No	TSV-last 10-5µm diameter. µBump bonding
Samsung	Yes	Yes	Yes	Yes/No	32nm off-shore. TSV at 32nm node currently used in DDR3 with 2.5D technology. FinFet is onshore in Texas.
Chartered	Yes	Yes	?	No	Uses Tezzaron as TSV partner. 130nm node demonstrated. <3µm TSV diameter. TSV-first approach.

Commercial Applications

- FPGA
  - Xilinx Virtex-7 & UltraScale
- Memory
  - Micron – Hybrid Memory Cube
  - AMD – High Bandwidth Memory
  - Tezzaron – DiRAM4
- CMOS Imagers
  - Sony
  - Toshiba

Xilinx

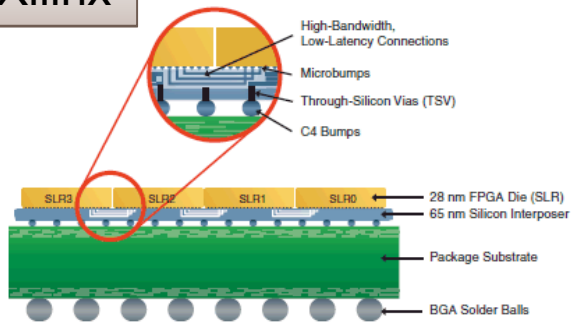
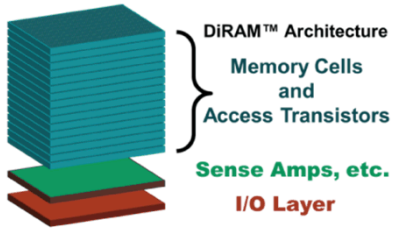


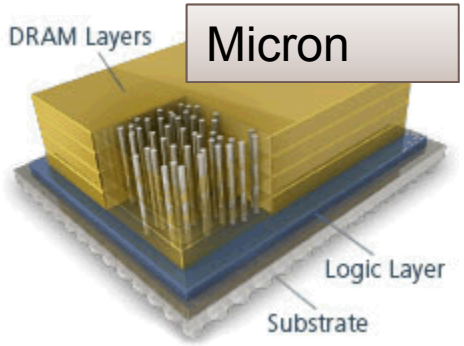
Figure 1: **Virtex®-7 2000T FPGA Enabled by SSI Technology**

Micron

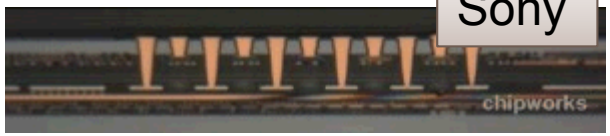
Dis-Integrated 3D RAM Architecture



Micron



Sony



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3D Standards

Activity on 3D-IC Standards

- 3DS-IC Standards Committee
  - Bonded wafer pair task force
  - Inspection and metrology task force
  - Thin wafer carrier task force

- 3D-IC Working Group

- 3D-IC Enablement Program
  - Joint alliance with Sematech, SIA and SRC
  - Administered by Sematech's 3D-IC Interconnect program

- Multiple Chip Packages Committee
- Solid State Memories Committee
- Silicon Devices Reliability Qualification Committee
  - Just released *3D-IC Chip Stack with TSVs* (JEP158)

- Intimate Memory Interconnect Standard

- 3D-Test Working Group
  - P1838 Standard for test access architecture for 3D-IC stacked circuits

Courtesy: Wally Rhines, Mentor Graphics

Commercial Trends

- 2.5D will continue to see extended use and will dominate market first
  - Easy adoption (evolutionary not revolutionary)
- 3D Drivers
  - High performance processors to overcome bandwidth limitations and improve power performance
  - Mixed-signal designs in which analog functionality does not benefit from node shrink (cost savings)
  - Higher cost of adoption, requires new paradigm in design
  - Heterogeneous integration may offset cost of adoption long-term
- Applications drive development
  - High Density Interconnect:
    - Pixelated sensors require high density, small pitch millions of connections
    - Can tolerate less than 100% functionality (a dead pixel is “ok”).
  - Low/Medium Density Interconnects:
    - High performance processors and custom heterogeneous solutions will drive low/medium density solutions.
    - Requires high yield and will tolerate larger interconnects.

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SPACE BASED APPLICATIONS & QUALIFICATIONS FOR 3D

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Space Applications

- Pixelated Sensors
- Micro-fluidics for cooling
- Additional silicon AREA for fault-tolerant design
  - Smaller PCB foot-print
  - TMR distributed across layers?
  - A/B side circuitry redundancy stacked vertically?
- Power management
  - Lower power
  - Increased performance
- Heterogeneous Integration
  - Various materials integrated together (CTE must be considered)
  - Each design aspect targeted to specific technology node

Space Qualification

- Operational Temperature
  - Military -55 to 125C
  - Extreme: -200C to 200C (or more?)
- Reliability
  - Aging
  - Vibration
  - Shock
  - Thermal Stresses (CTE mismatches)
- Radiation
  - SEL, TID, SEU's
- Out gassing
  - New material development may not be space friendly

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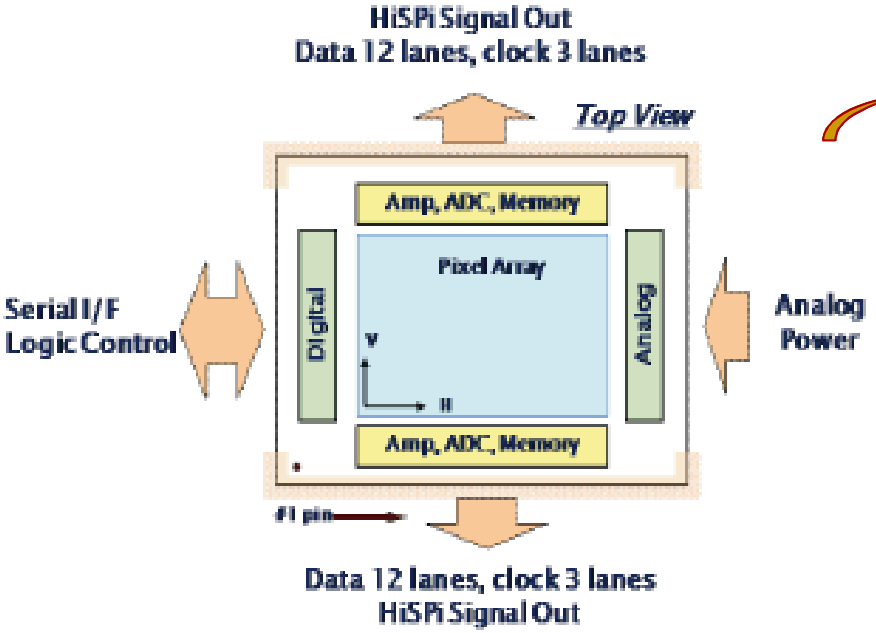
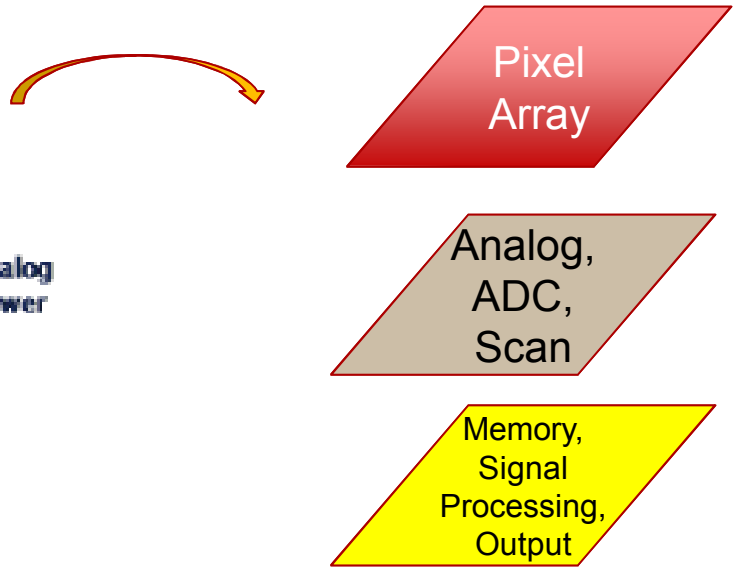
SANDIA SENSOR APPLICATIONS

High-Speed Access To Small Pixel Regions



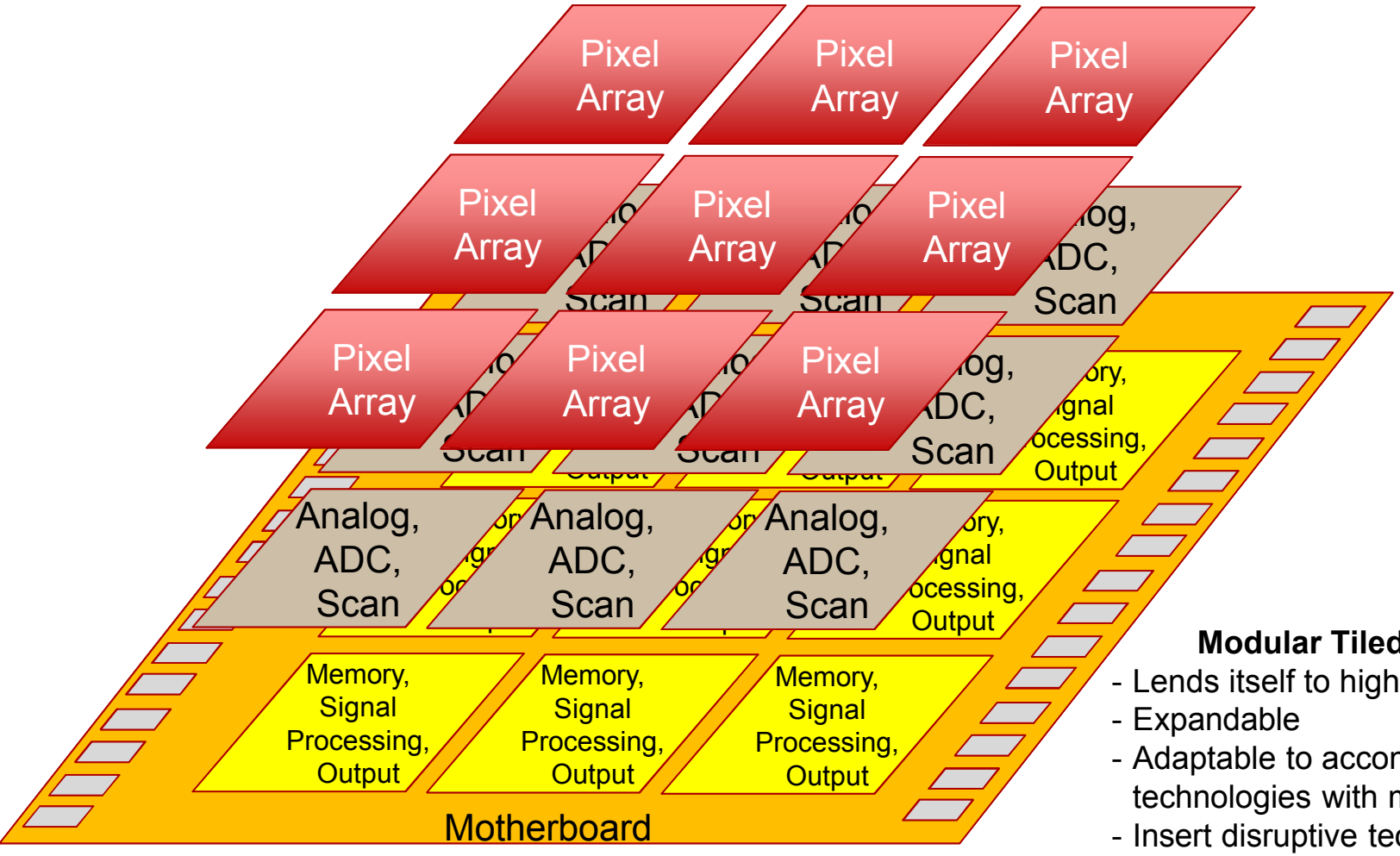
Consumer Imager Single Silicon Layer



FPA Concept Multiple Silicon Layers

FPA architecture allows highly parallel processing of pixels

Tiling Allows Building Large FPAs From Smaller Tiles

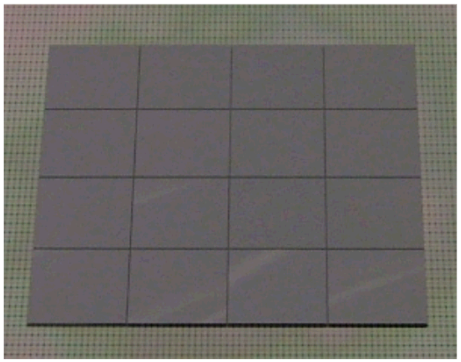


Modular Tiled Structure

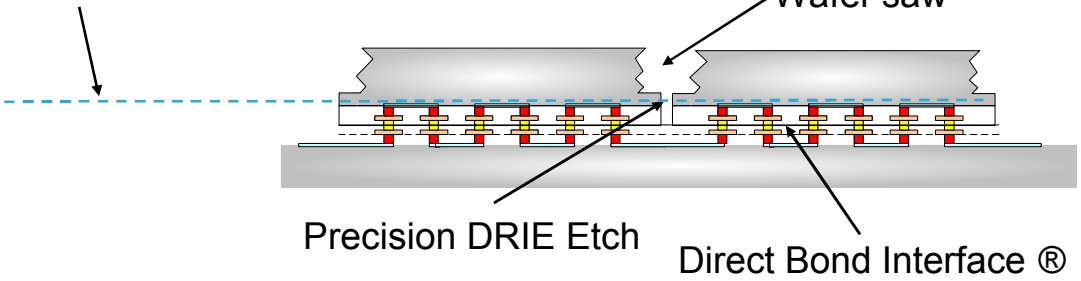
- Lends itself to higher yields
- Expandable
- Adaptable to accommodate latest technologies with minimal redesign
- Insert disruptive technology

HTS-MEO FPA Tiling Process

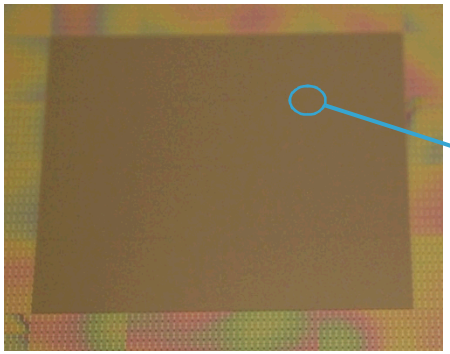
Tiled Assembly before Planarization
Large Wafer Saw Gaps are visible



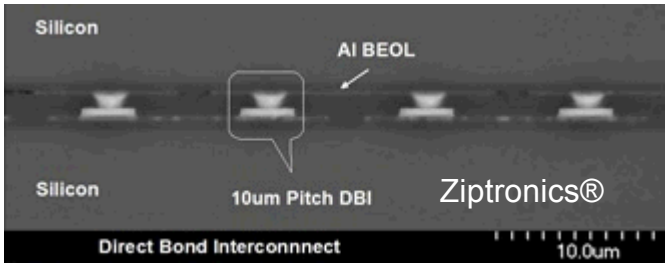
Planarize

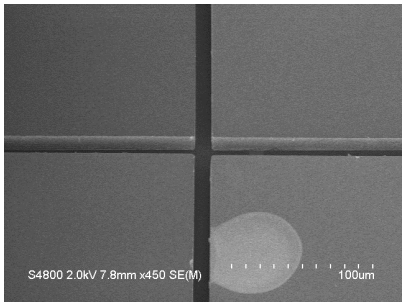


Tiled Assembly after Planarization
Precision 10um gaps are not visible



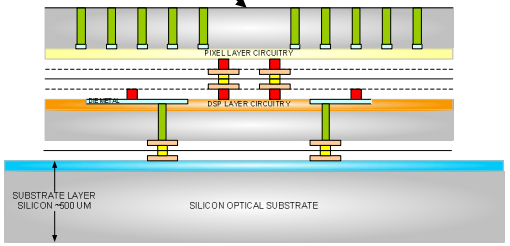
Planarize





Precision DRIE Tiles
10um +/2um gaps

Planarization will reveal
contacts to pixels



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QUESTIONS?

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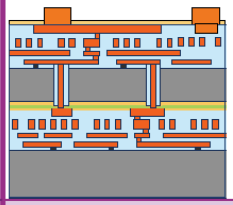
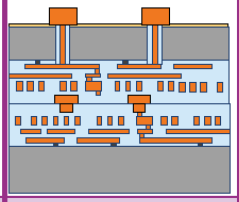
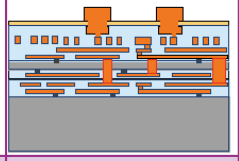
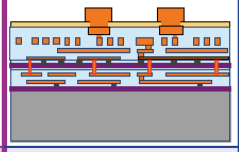
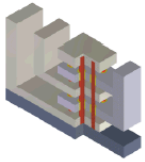
BACKUP

IMEC Roadmap

3D ROADMAP

	3D-SIC	3D-SOC		"Monolithic"	3D-IC
wiring level	Global	Semi-global	Intermediate	Local	FEOL
2-tier stack			2nd FEOL before stacking 	2nd FEOL after stacking 	Multi-tier FEOL 
TSV Pitch	10 ⇒7 ⇒5 µm	10 ⇒7 ⇒5 µm	"TSV" after stack	"TSV" after stack	No TSV
Contact Pitch: *Rel. density:*	µbump pitch: 40 ⇒20 ⇒10 µm 1 ⇒ 4 ⇒16 Cu TSV –Cu pad: 10 ⇒ 7 ⇒5 µm 16 ⇒ 33 ⇒64	5⇒ 1 ⇒ 0.5 µm 64⇒1.610³⇒6.410³ *(Overlay 2nd tier defined by W2W alignment/bonding)*	1 µm ⇒ 0.5 µm 1.610³⇒ 6.410³	200 ⇒100 nm 410⁴ ⇒ 1.610⁵ *(Overlay 2nd tier defined by litho scanner alignment)*	< 100 nm >1.610⁵
Stacking Method	D2D, D2W (W2W) B2F / F2F N>2 tiers	W2W (D2W) F2F N=2 tiers	W2W Device layer–to-wafer stacking F2F N>2 tiers	W2W Si layer-to-wafer statcking 2nd Tier Device fab. after stacking	Monolithic Device-level stacking

imec 3D SYSTEM INTEGRATION PROGRAM 5

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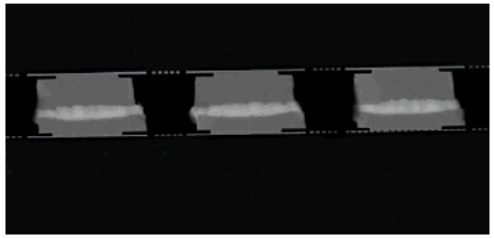
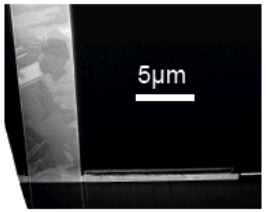
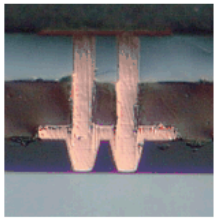
BUMPING APPROACHES

- Cu/Sn µbump bonding:
  - Cu/Sn Transient-Liquid-Phase, TLP, (250°C)
  - diffusion bonding (<200°C)
  - Pitch Scaling : 40→20→10µm
  - Bump planarisation
- Cu/Cu bonding :
  - High T Thermo-compression bonding
  - Low T Cu/Cu "insertion bonding'
- Cu oxide removal & prevention
- No-flow & wafer-level, pre-applied underfill







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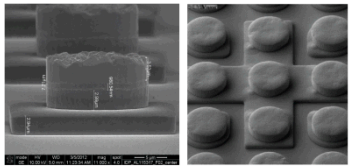
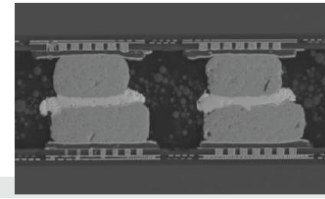
20

Break N
Click here

Bonding Approaches

- Cu/Sn uBump
- TABLE/PIctures





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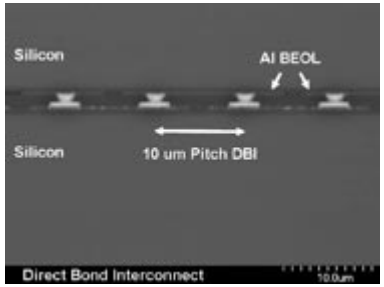

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