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Radiation Effects Microscopy in Microelectronic devices Using a Heavy Ion Nuclear Microprobe

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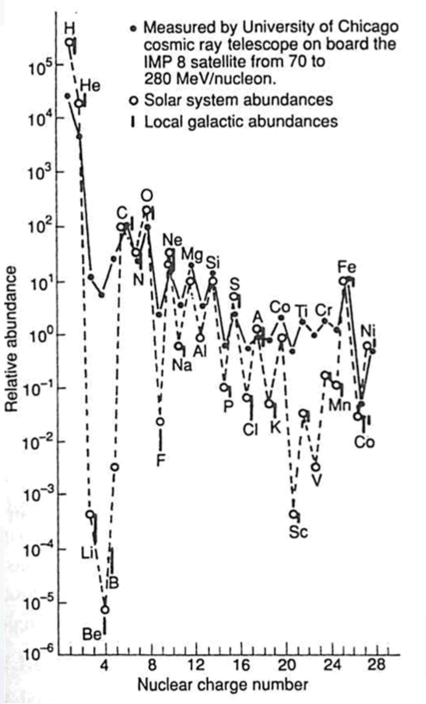
Overview

- **Radiation environments**
- **Fundamental damage mechanisms**
- **Single Event Effects**
- **Examples**
  - Single Event Burnout in HBTs
  - Single Event Effects in Memristors
- **Modeling SEEs**
- **Limitation of the the heavy ion microprobe**

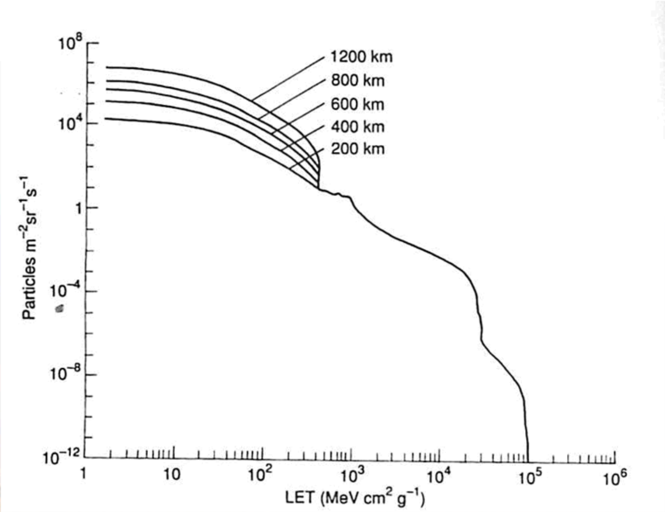
Radiation environments

- Space
- High-energy physics experiments
- Nuclear reactors
- Natural environments
- Processing-induced radiation

Space (TID and SEE)



- Protons (several hundreds of MeV) and electrons (few MeV) trapped in the Van Allen belt
- Heavy ions trapped in the magnetosphere
- Galactic cosmic rays, protons and heavy ions, up 100s of GeV
- Proton and heavy ions from solar flares, > 100 MeV



Holmes-Siedle, A. and L. Adams, *Handbook of Radiation Effects,* 2002, New York: Oxford University Press Inc.

High-energy physics experiments

- Protons and electrons with 100s of GeV energy
- The primary hadron-hadron interactions produce high flux of charged particles, gamma rays, and neutrons
- Up to 1.6×10^{14} 1 MeV neutron/cm^2 equivalent integrated fluence
- Displacement damage, detector degradation

Fusion and fission reactors

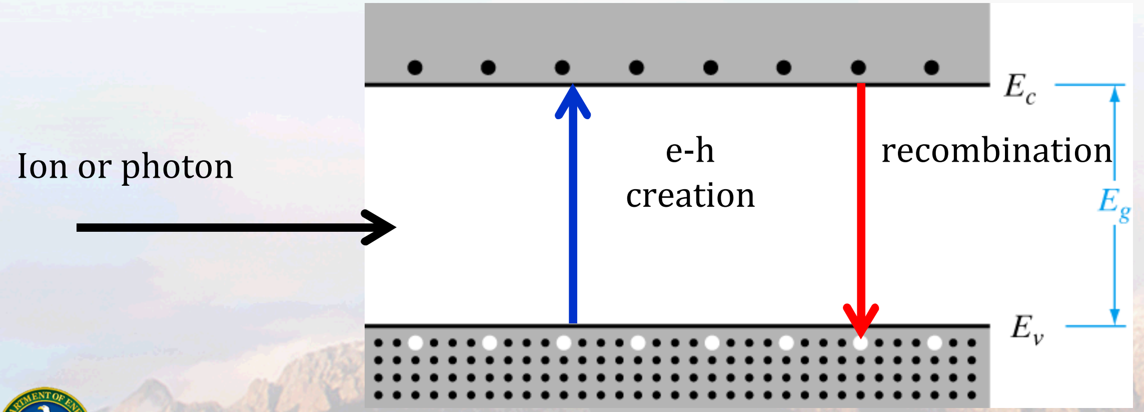
- Reactor core, environment of the reactor, accidents
- Neutrons, gamma rays, and hydrogen isotopes (fusion)
- Significantly higher fluences than in space environments
- Displacement damage and TID

Natural environment and processing

- Alpha radiation from radioactive impurities (U and Th)
- Alpha particles from $^{10}B(n,\alpha)^{7}Li$ reaction in BPSG
- Terrestrial neutrons
- Ion implantation, lithography, sputtering, ion milling, plasma etching, etc.

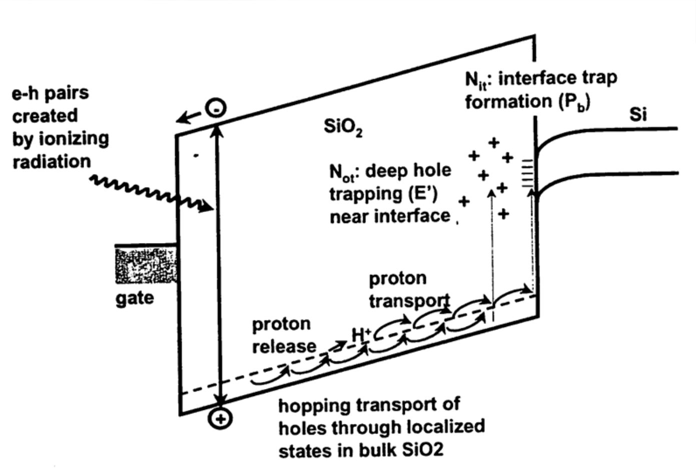
Fundamental damage mechanism

- Ionization (removing or exciting electrons of atoms, creating electron-hole pairs)
  - Energy necessary to create an e-h pair $f{\cdot}E_g$, 3.62 eV for Si, 17-18 eV for SiO_2
  - Photocurrent (SEE) (Gunn theorem)
  - Trapped charge (bulk or interface) (TID) in MOS devices



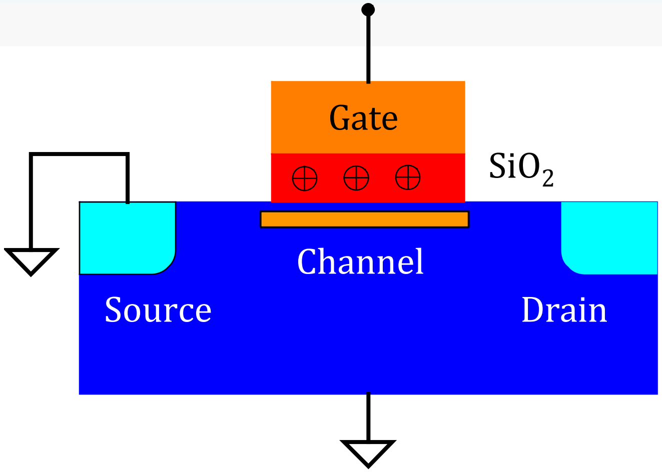
$$I_i = -q\mathbf{v}\frac{\partial \mathbf{E}}{\partial V_i}$$

How TID affects devices?



Schwank, J.R., *Total dose effects in MOS devices*, in 2002 IEEE NSREC Short course note book, 2002

- Holes get trapped in the oxide
- Holes move by “hopping” toward the SiO_2/Si interface
- Released hydrogen moves to the interface and forms interface traps

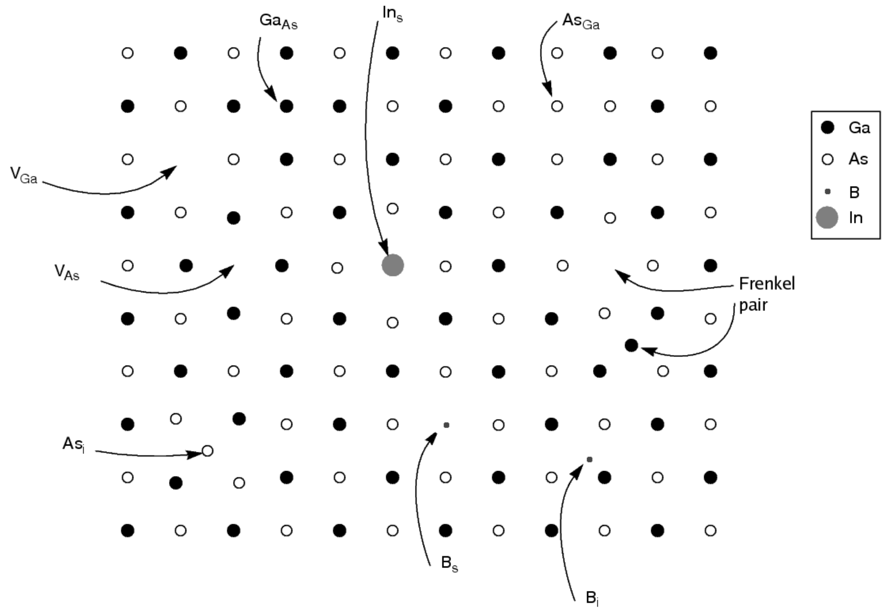


The extra charge in the oxide will add extra voltage to the gate voltage and the transistor will be switched on at lower voltage or even at zero gate bias. Also, it increases the leakage current from the PS.

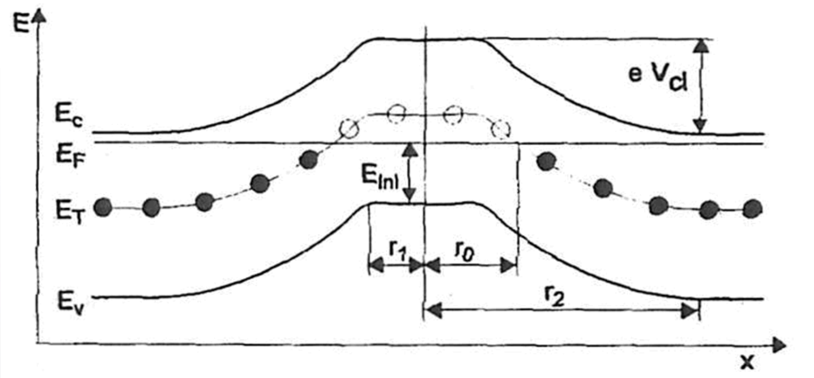
Problems occurs not only in MOS devices but also with SOI and all other devices that have field oxide.

Displacement damage

- Recoils with enough energy leave the lattice site and can create permanent defects
- Vacancies, interstitials, anti-sites, clusters
- Carrier lifetime is decreased due to recombination in defects (SRH)
- Clusters distort the energy band locally



Wikipedia



Damage cluster

Simoen, E. and C. Claeys, *Radiation Effects in Advanced Semiconductor Materials and Devices*. Materials 2002, Berlin Heidelberg: Springer-Verlag.

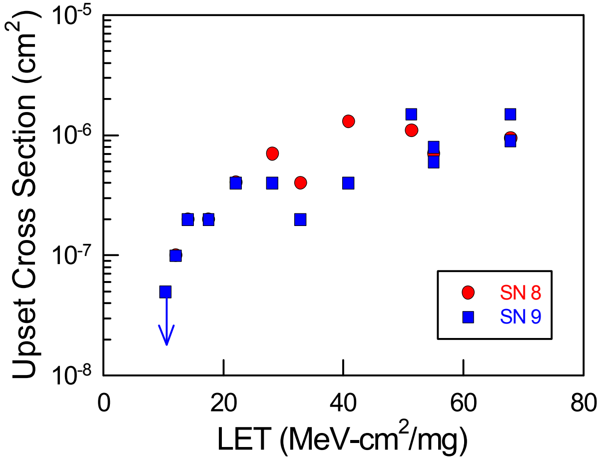
Single Event Effects

- **Soft errors (no permanent damage)**
  - Single Event Upset (SEU) – SRAMS, it can occur any time
    - Mitigation: error correction (time and space overhead), reloading memory (information lost)
  - Single Event Transient (SET) – digital logic circuits, ion has to hit at a certain time, false data latched in
    - Mitigation: Voting (redundant) circuits (time and space overhead)
- **Hard errors (permanent damage to device/circuit)**
  - Single Event Latchup (SEL)
  - Single Event Burn-out (SEB)
  - Single Event Gate Rupture (SEGR)
  - Single Event Snapback (SES)
  - SEB, SEGR, SES are catastrophic failures, SEL can lead to it, too
  - Generally under high field and high current conditions
    - Mitigation: Device/circuit has to be replaced, redesign circuit w/ current limits

How can a microbeam help failure analysis?

Generally broad beam tests are used to certify devices.

- **Set memory pattern**
- **Irradiate device**
- **Read memory and compare pattern**
- **Count errors**
- **Divide by fluence**

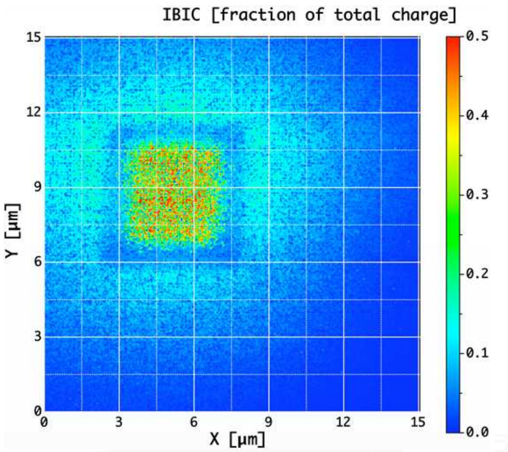


If higher that expected SEU cros er area) then

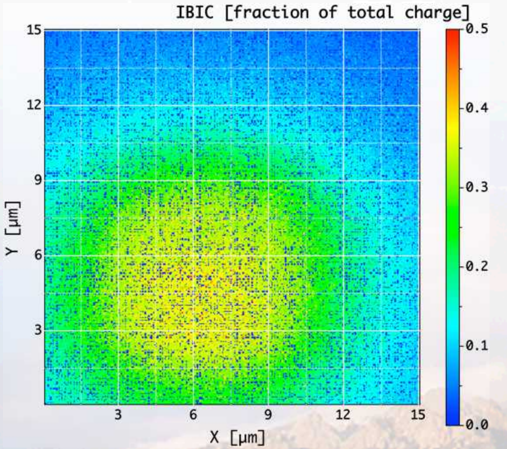
- **Microbeam SEE mapping can identify failing elements**
- **IBIC and TRIBIC can shed light on the failure mechanism**
- **IBIC and TRIBIC can confirm TCAD results or help models developed.**

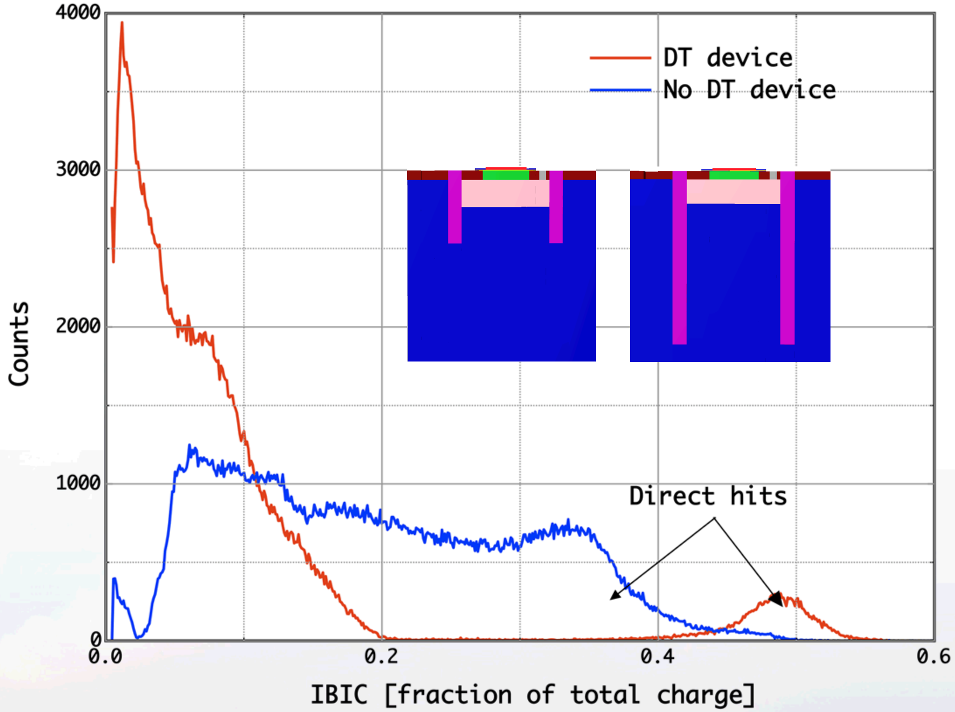
REM IBIC confirms SiGe HBT TCAD modeling

DT device



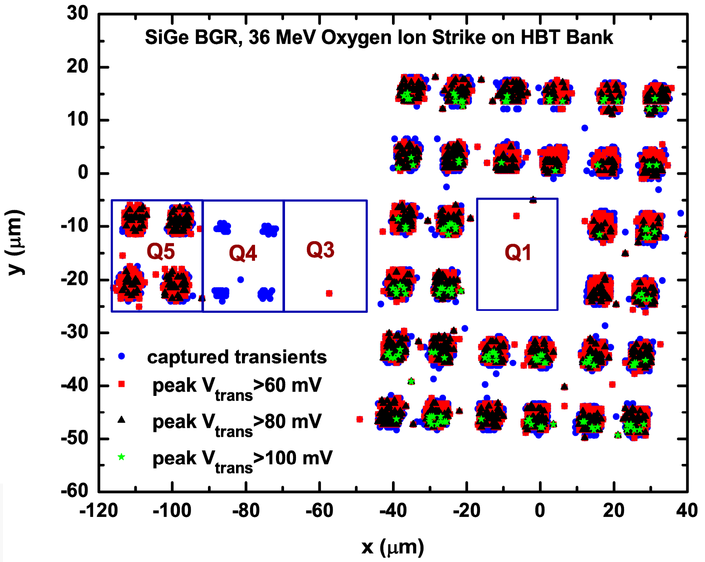
No DT device

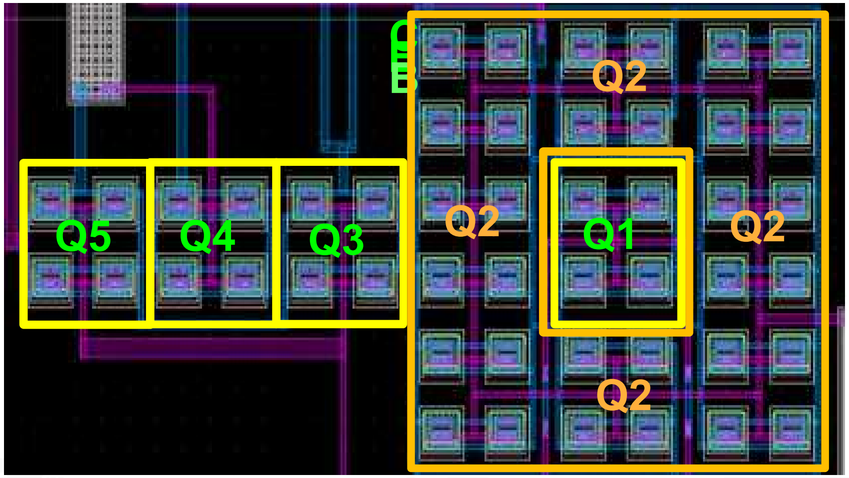


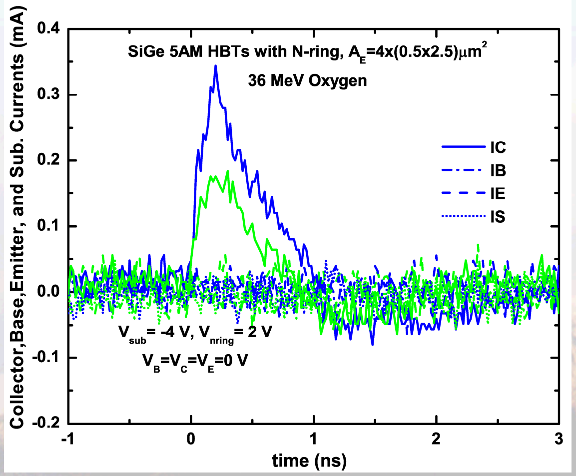


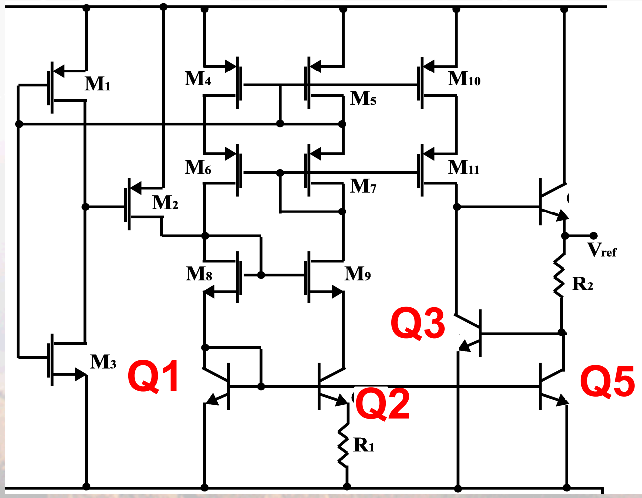
Deep trench isolation decreases the charge collection outside of the trench but increases it inside the trench. These experiments confirm TCAD modeling results.

SETs in SiGe BiCMOS BGRs



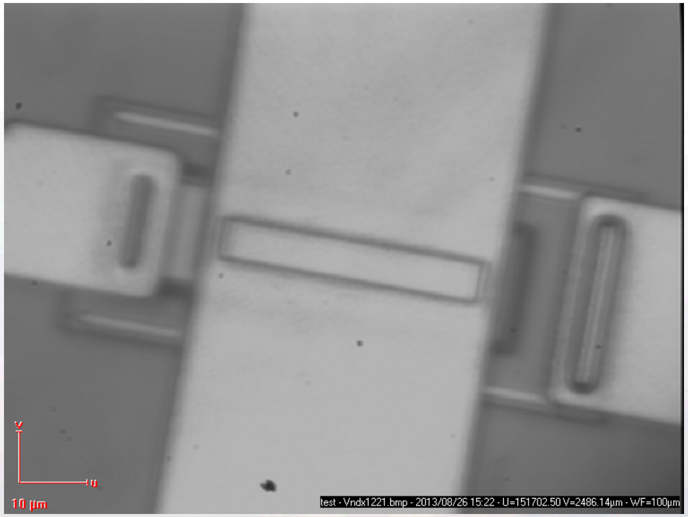


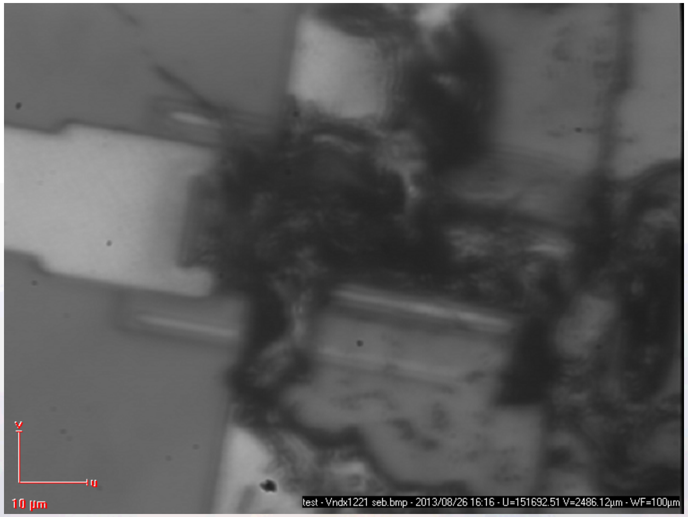




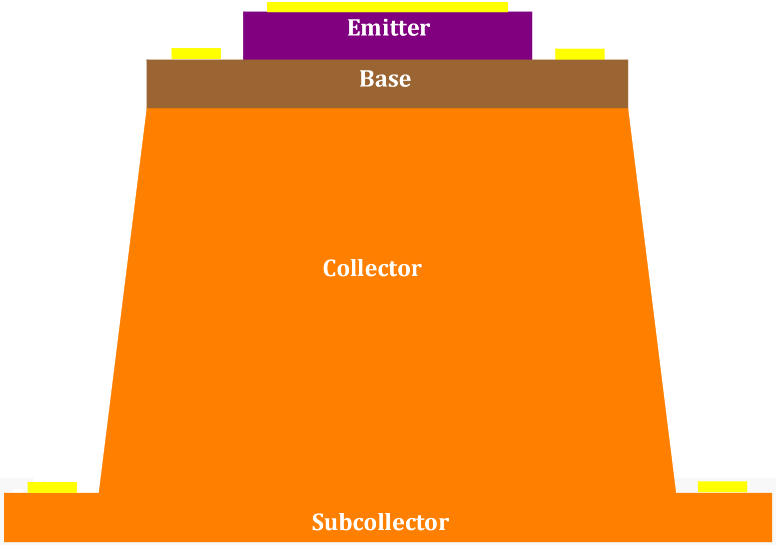
Single Event Burnout

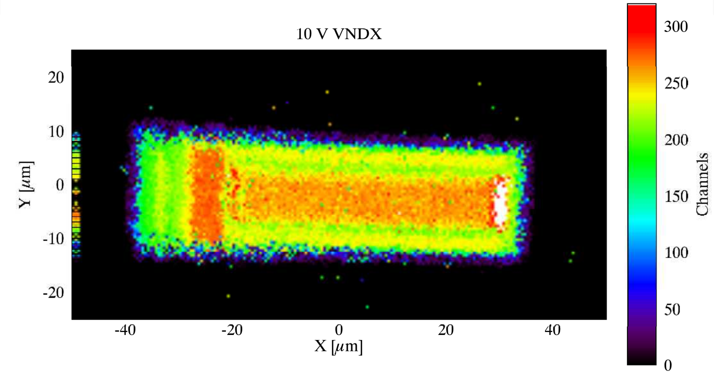
- Most catastrophic SEE failure
- Single ion hit ⇒ high current density ⇒ avalanche ⇒feedback ⇒ sustained high current/voltage stage ⇒ Joule heating ⇒ Burnout
- Usually occurs in high power MOSFETs, BJTs, and diodes (kV)
- We found that some III-V HBTs (not power devices) are sensitive to SEB and they have no LET threshold



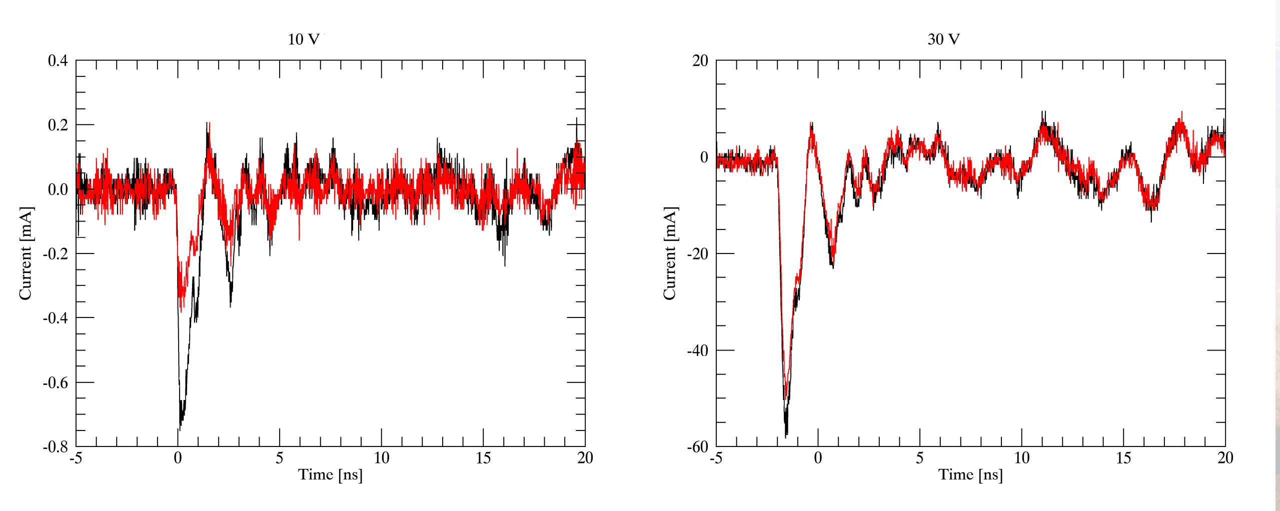


IBIC and TRIBIC on HBTs (28 MeV Si)

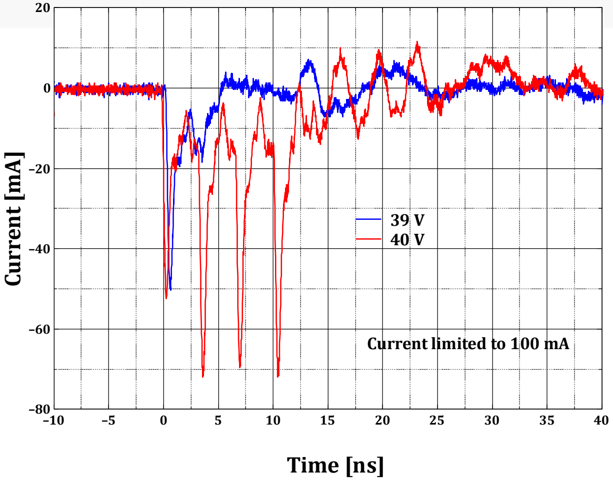


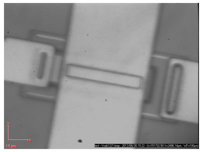


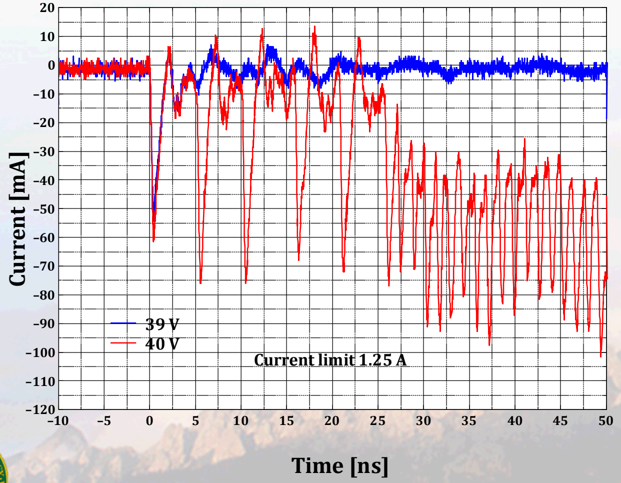
10 V normal induced current
30 V 100 fold increase in current
Avalanche!

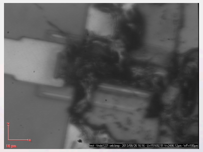


When does the avalanche starts?

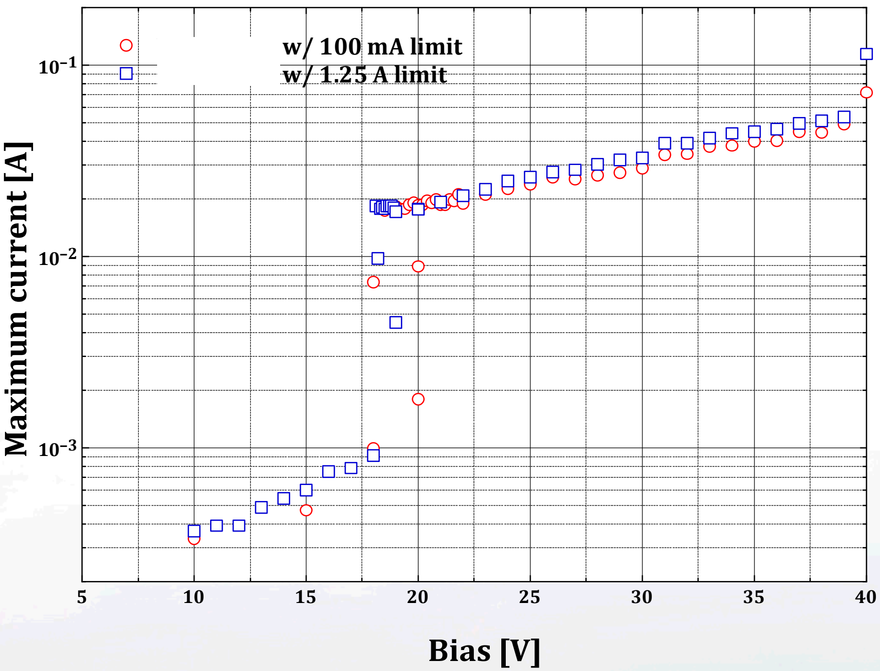








28 MeV Si 131008

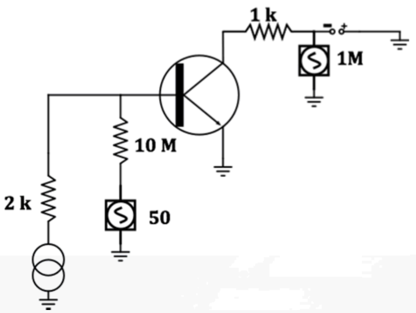


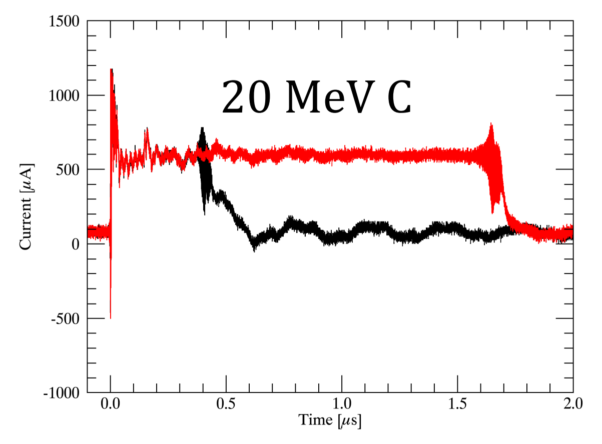
- Impact ionization starts avalanche
- Avalanche causes high current oscillations
- If current not limited burnout occurs

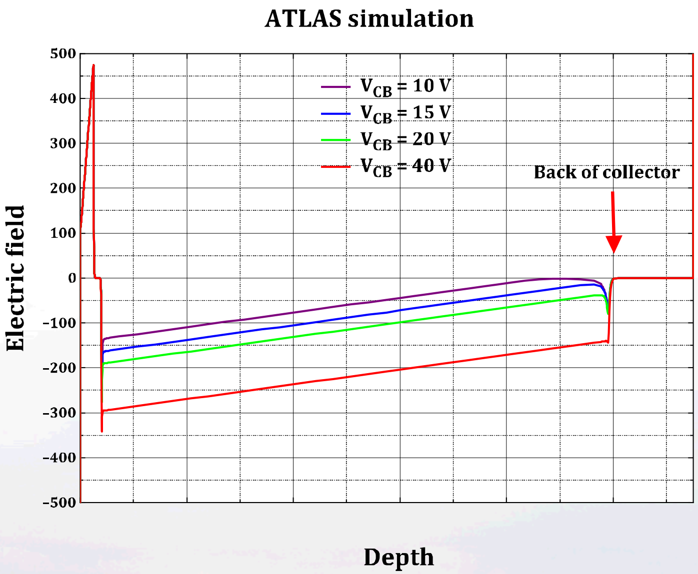
Can it be mitigated?

- **Right now only current limitation protects the device**
  - It still can lead to failure of the device (junction is open/short) but no visible damage

TCAD modeling to find better design





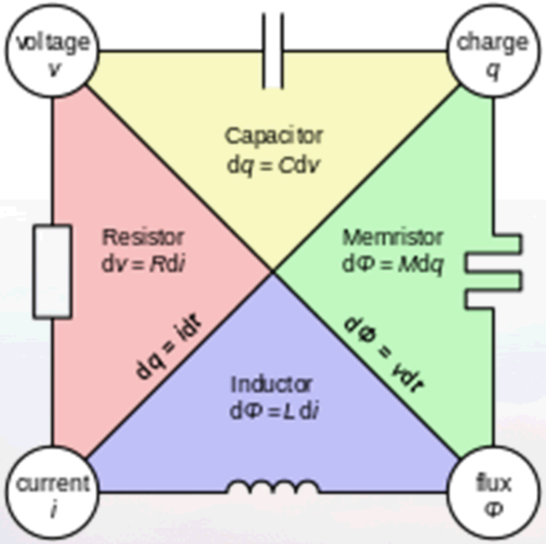


Avalanche seems to start when the collector is fully depleted.

How it happens

What is a memristor?

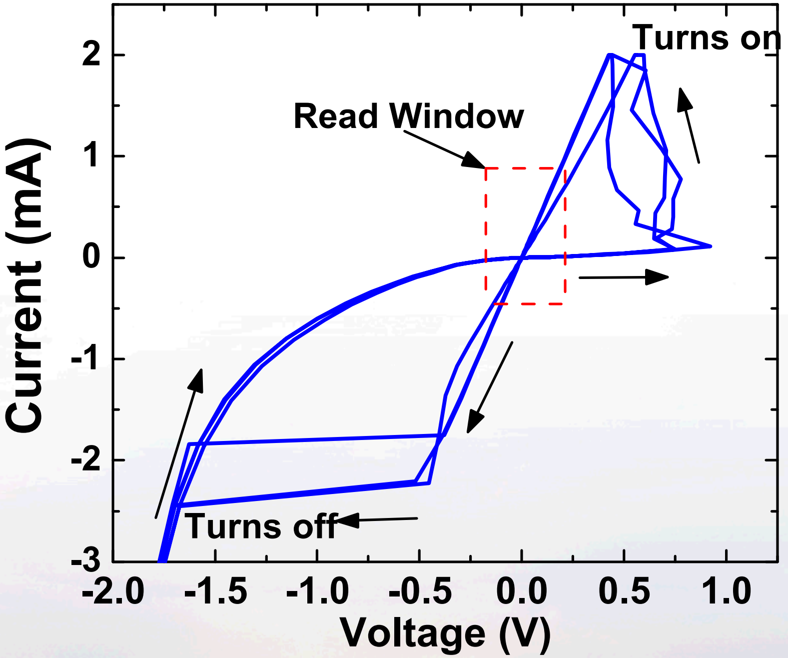
Leon Chua (Berkeley) 1971
Symmetry requires a fourth circuit variable, the memristor. No combination of RLC can duplicate the properties of a nonlinear memristor.



HP Labs (R.S. Williams) found it.

Strukov, D. B., et al. (2008). "The missing memristor found." Nature **453**(7191): 80-83.

Nonlinear characteristics offers memory-like properties



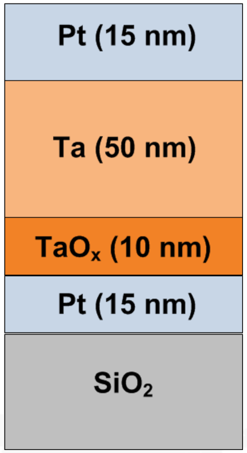
High applied voltage (several Volts) can change resistance, small voltage (mV) can read the resistance.

What would the memristor replace and why?

- **Current nonvolatile memory technologies (Flash) are limited by scaling**
- **Resistive RAM (ReRAM) has many favorable properties**
  - Scalability
  - Endurance (many writing/reading cycles)
  - Speed
  - Low power!
- **Question: Are there suitable for space applications? How do they respond to total dose, dose rate, single event effects, and displacement damage?**
- **They seem to be radiation hard against ionization (up to space radiation levels)**
- **What about displacement damage?**

How does a memristor work?

- **Today’s memristors are mostly TaO_x (older ones are TiO_x)**



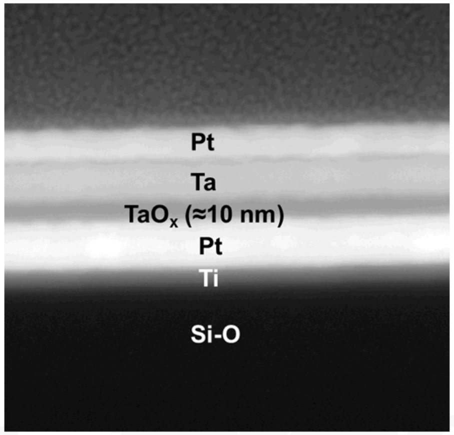
Pt (15 nm)

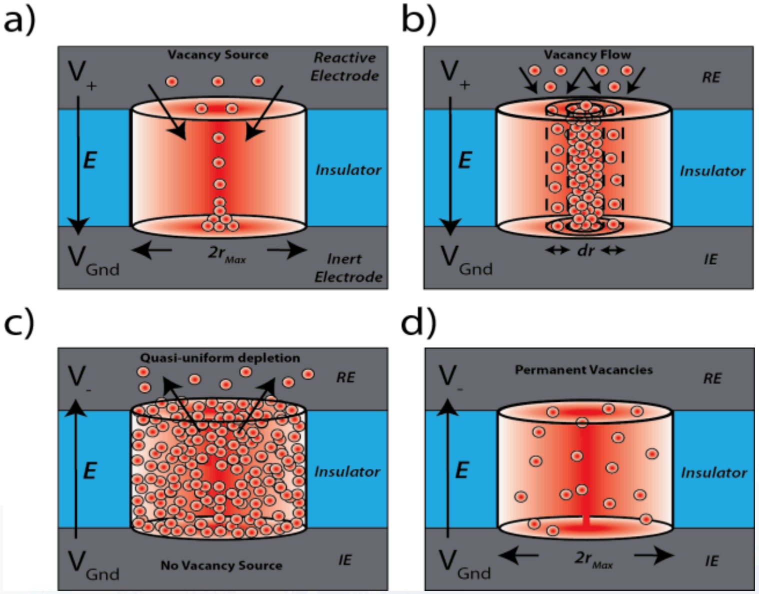
Ta (50 nm)

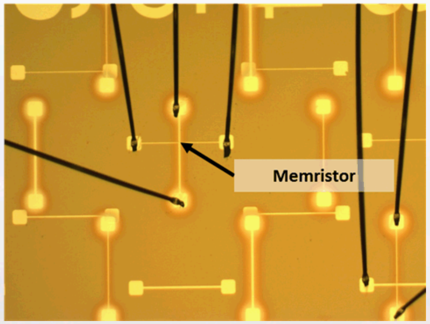
TaO_x (10 nm)

Pt (15 nm)

SiO_2





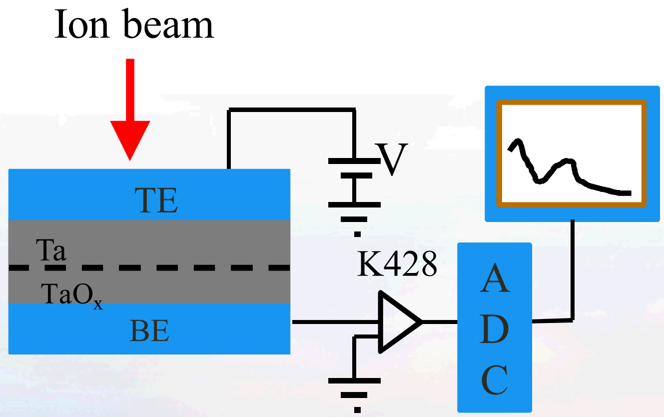


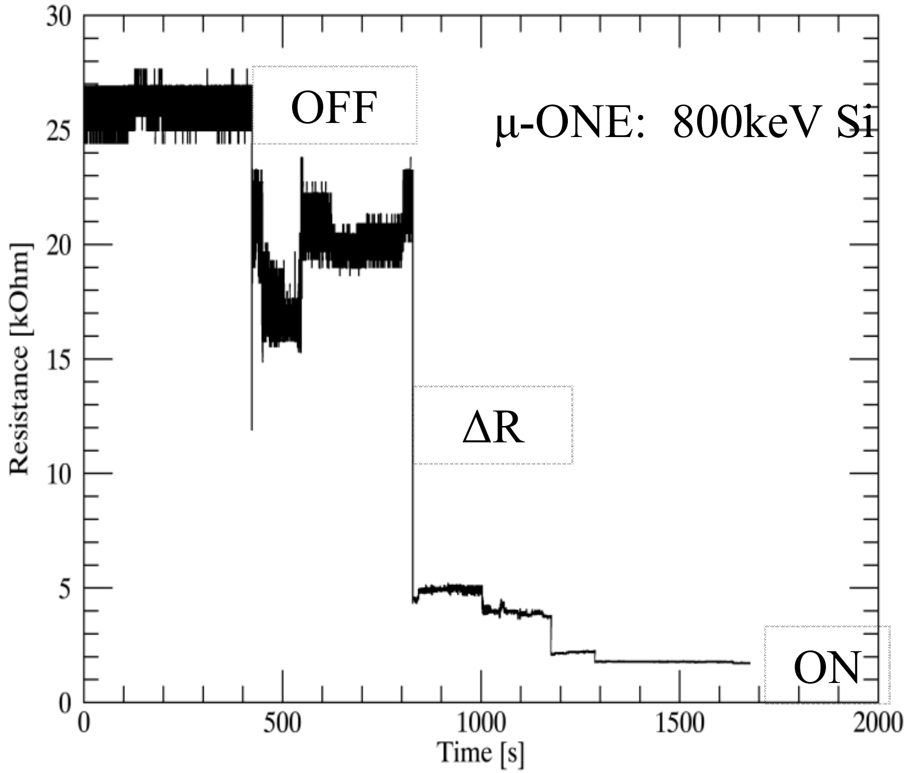
- Charged oxygen vacancies form a channel under high voltage (forming step)
- Voltage (through Joule heating) can deplete the channel or fill again (switching)

Mickel, P. R., Lohn, A. J., James, C. D. and Marinella, M. J. (2014), Isothermal Switching and Detailed Filament Evolution in Memristive Systems. Adv. Mater.. doi: 10.1002/adma.201306182

SEE by displacement damage?

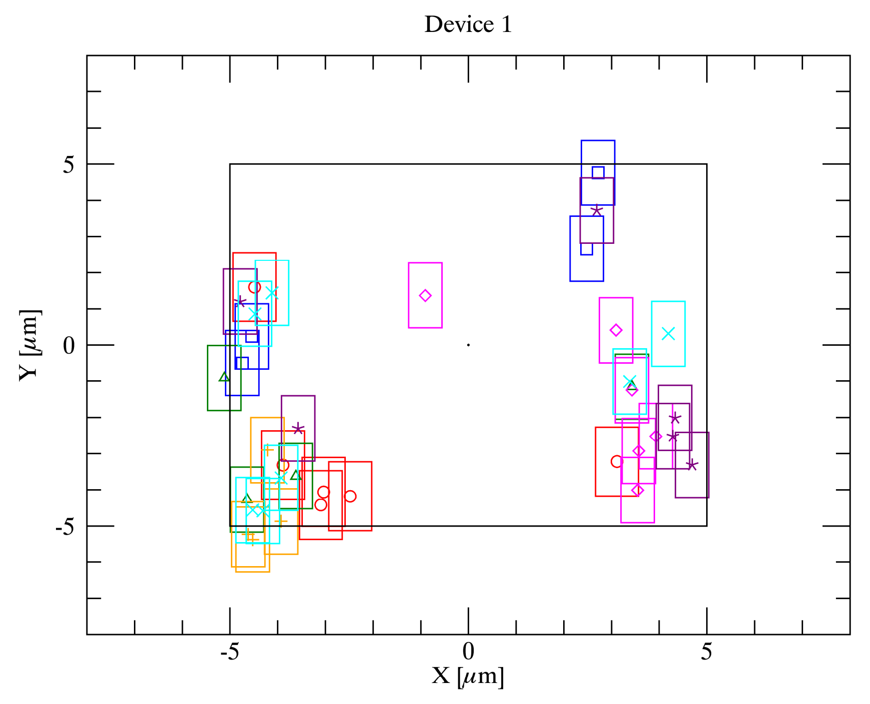
800 keV Low current (1000 ions/s) focused Si beam scanned over device and the resistance was monitored in-situ. Sudden resistance changes were correlated to ion beam position.

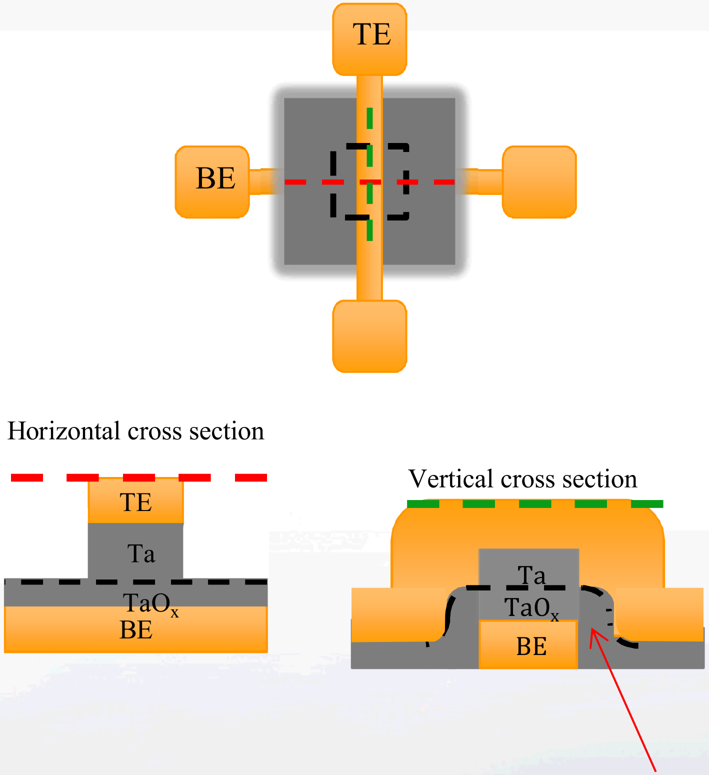




Resistance change (and eventually switching) occurs very fast. Conducting (already existing but in off state) channels are opening up due to individual ion hits. Device can be reset to OFF state several times, but it is slowly degrading.

Where are the sensitive areas?



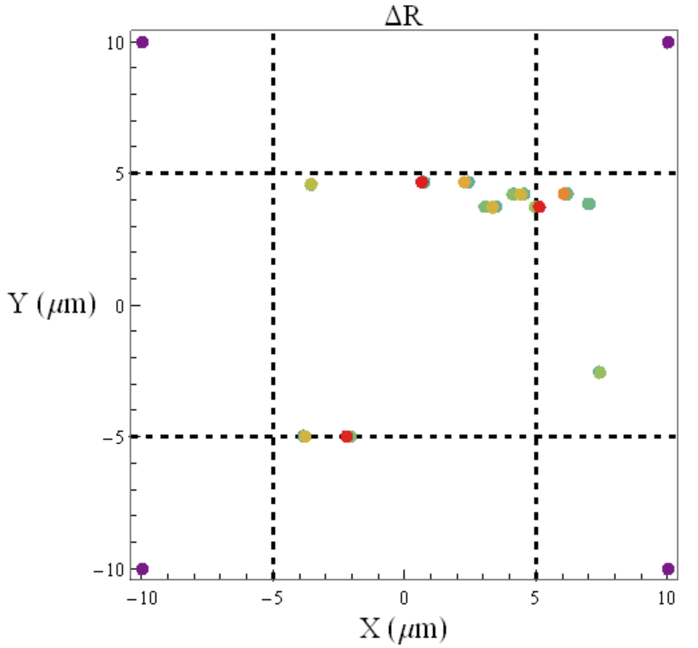


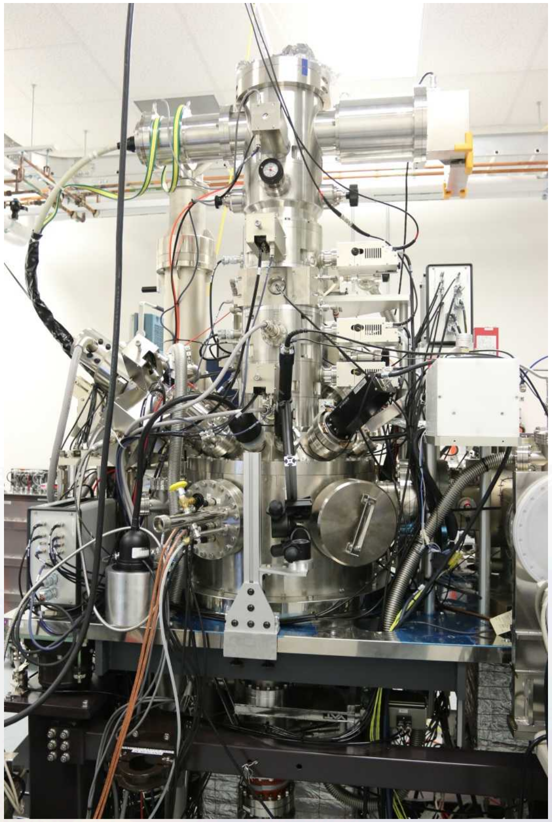
Sensitive areas (conductive filaments) are near the edges.

During forming the electric field is stronger near the edges.

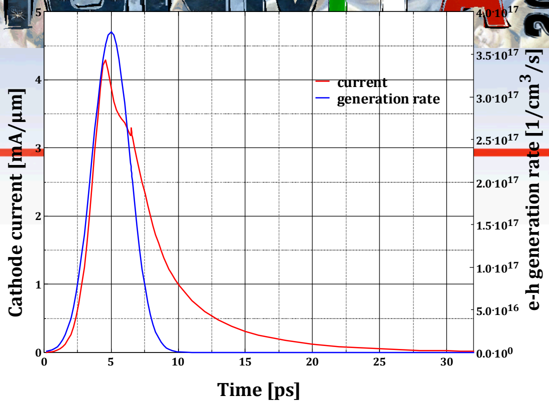
How to find the channels more precisely?

- **SNL NanoImplanter (nI)**
  - Variable Accelerating Potential: 10-100 kV
  - Fast Blanking and Chopping
    - Down to ~ 1 ion/pulse
  - Mass-Velocity Filter
  - Liquid Metal Alloy Ion Source
    - AuSiSb, 200 keV Si^{++} (<40 nm)

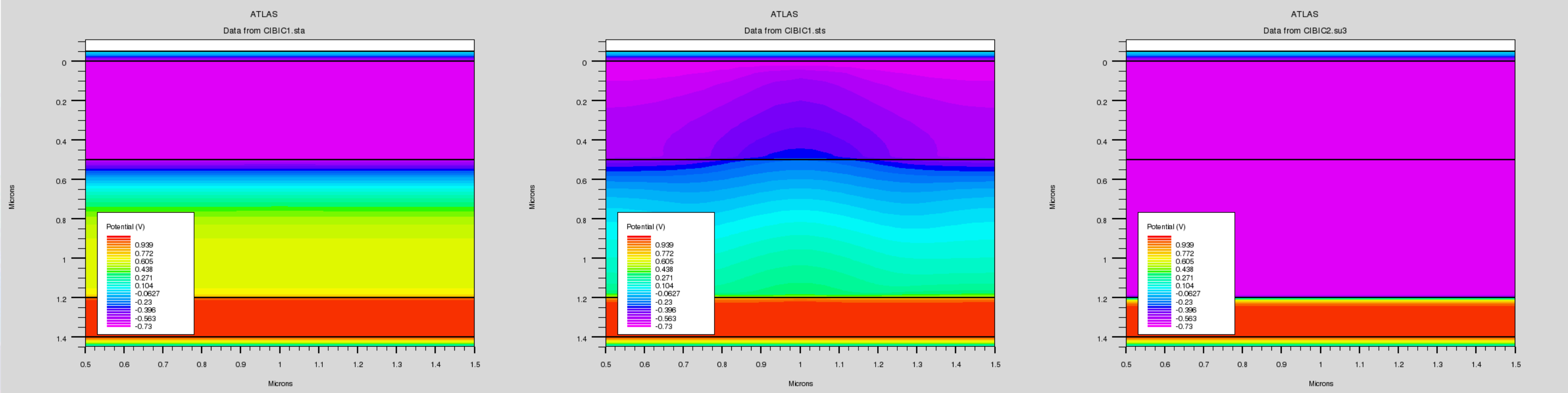




Modeling tools



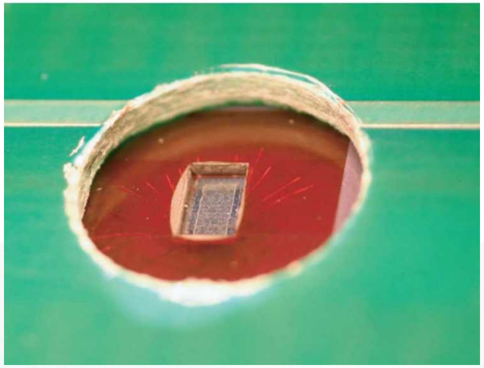
- **Space radiation environment modeling**
- **Radiation transport: GEANT4, SRIM, MARLOWE**
- **IBIC/TRIBIC modeling**
  - TCAD: ATLAS, Sentaurus, nanoTCAD (expensive, complicated, but includes lot of physics)
  - ITS (Jacoppo Forensis) 1D Monte-Carlo, simple quick calculation of IBIC
- **Circuit modeling: SPICE, Xyce**
- **Mixed mode calculations: circuit + 1 device = Single Event Effects**

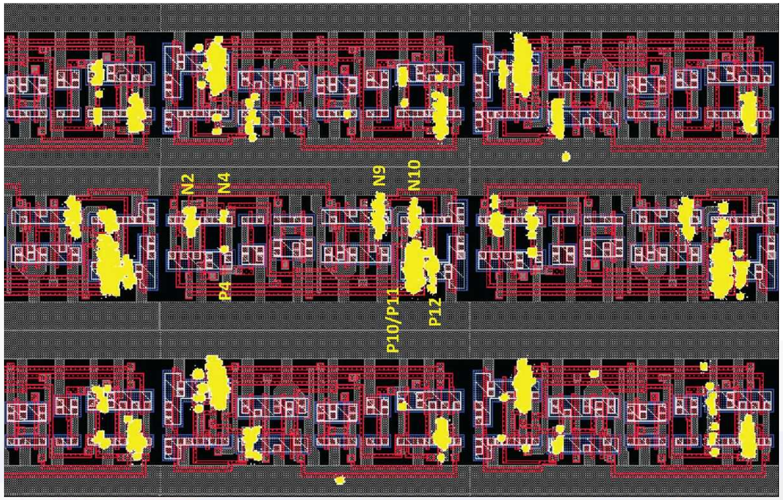


12 MeV C into AlGaAs/GaAs/AlGaAs photo voltaic

Limitations of heavy ion microbeams

- **Modern devices have many overlayers traditional microbeams cannot penetrate**
  - IPEM, IEEM - not very successful
  - Chip thinning from the back* – successful for SOI





- **Modern devices are very, very small, device size is smaller than beam spot**
  - New way to focus? Better lenses?

Shaneyfelt, M. R., et al. (2012). "SOI Substrate Removal for SEE Characterization: Techniques and Applications." Nuclear Science, IEEE Transactions on **PP**(99): 1-1.

Thank you for your attention!

Sandia National Laboratories