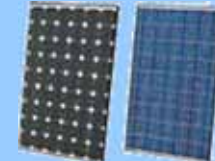
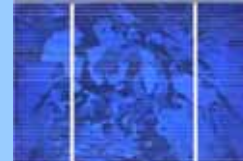
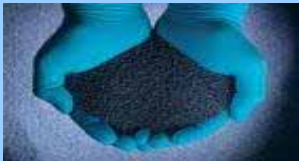
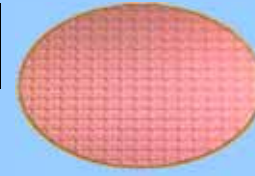
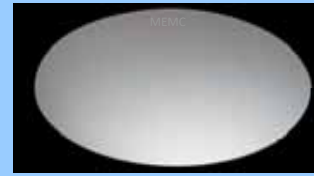


Exceptional service in the national interest



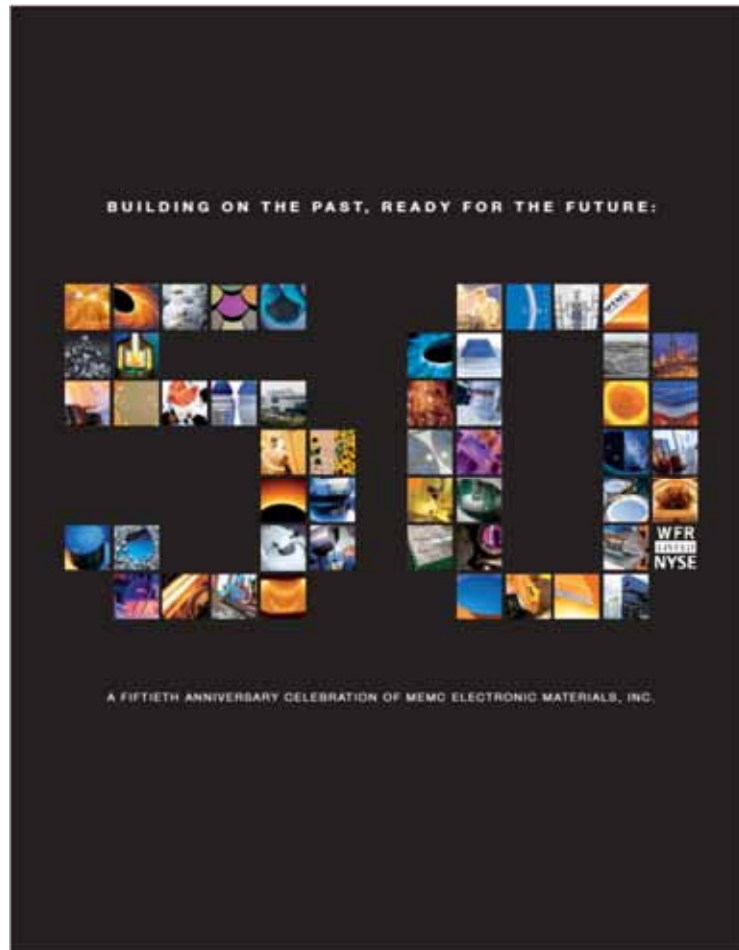
Manufacturing of Silicon Materials for Microelectronics and Solar PV

Babu Chalamala, Ph.D.



Sandia National Laboratories is a multi-mission laboratory managed and operated by National Technology and Engineering Solutions of Sandia, LLC, a wholly owned subsidiary of Honeywell International, Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525
SAND No:


Background Material

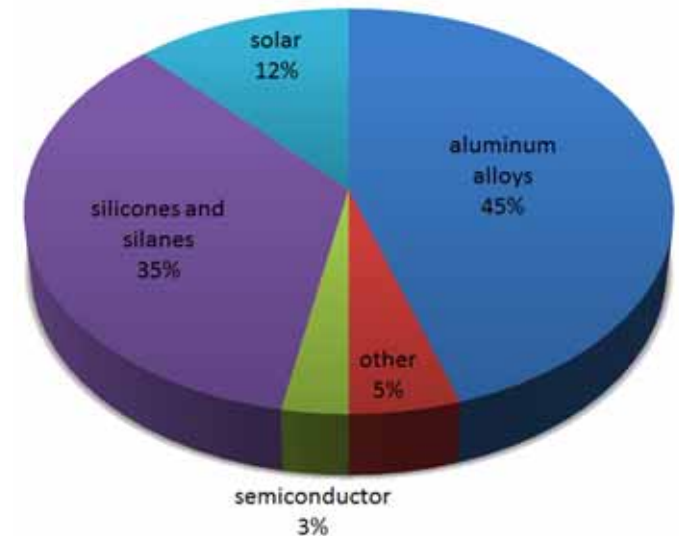


http://www.memc.com/assets/file/company/MEMC_book-optimized.pdf

<http://ieeexplore.ieee.org/xpl/tocresult.jsp?isnumber=6259910&punumber=5>

Silicon as an Industrial Material

Silicon Metal			
			
Composition	99% Silicon		
Main Market	Aluminum	Silicones	Semiconductors
Usage	Silicon source	Feedstock	Bulk Material

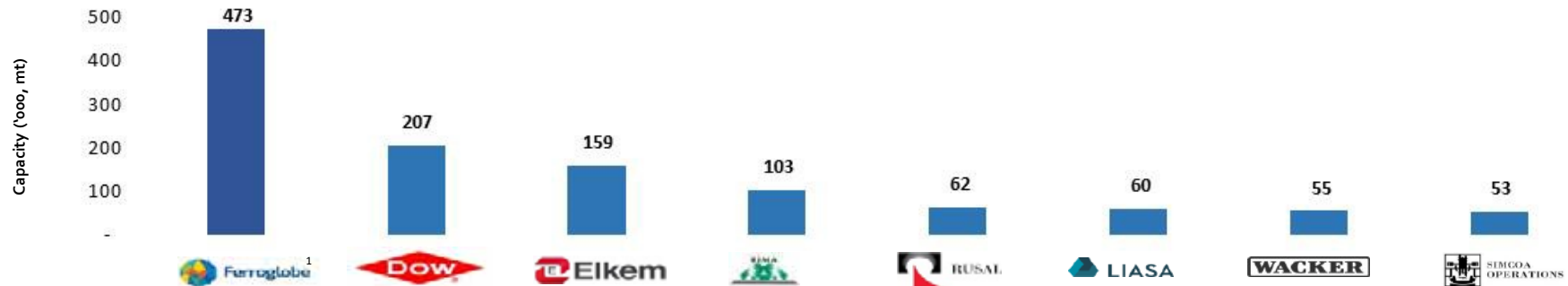
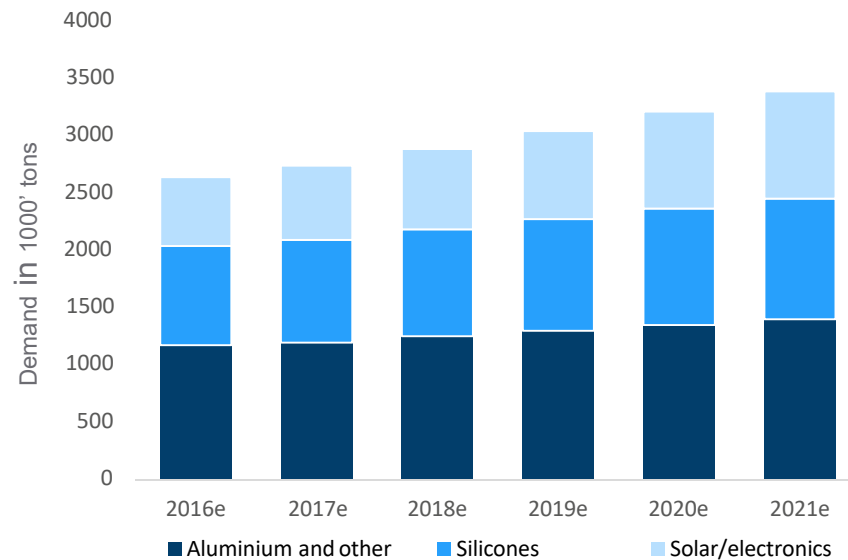


CRU Market Data, 2017

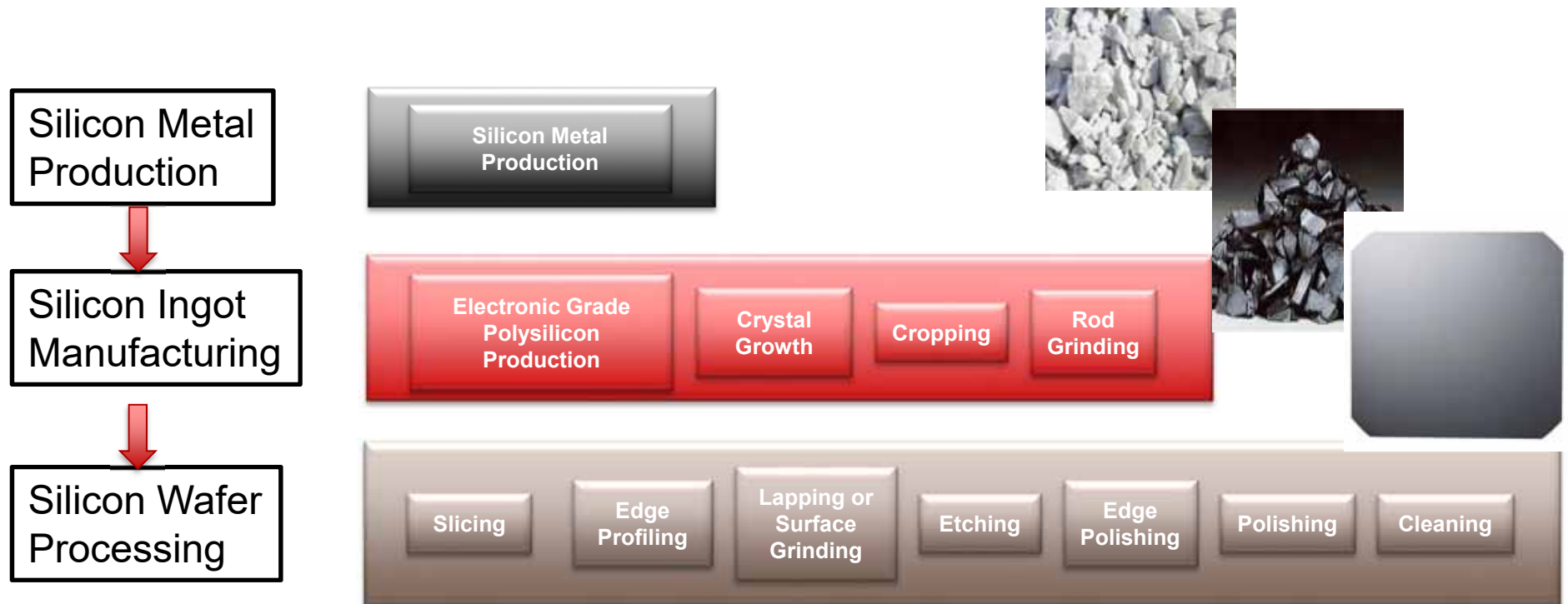
- Out of the 2.5 million of tons of silicon metal produced, about 300k tons goes into producing wafers for solar and microelectronics
- Metallurgical and chemical applications consume over 80% of Si produced

Silicon Materials Market

- With raising demand for Si in PV, both demand and production continues to grow.



From Quartz to Silicon Wafers

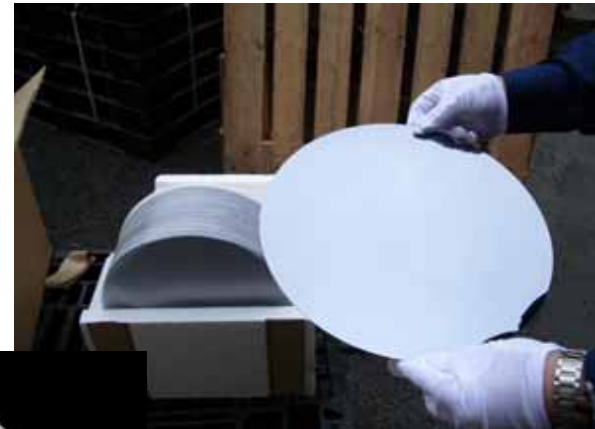
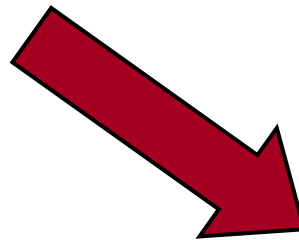


How Do We Make Silicon?



How do we go from quartz ...

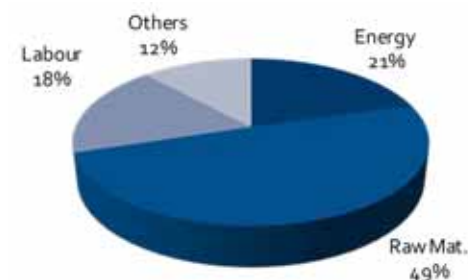
...to make silicon?



Silicon Metal Production



PRODUCT:	Metallurgical	Chemical	Polysilicon
MAIN MARKET:	Aluminum	Silicones	Solar
TYPICAL COMPOSITION:	99% Silicon		
MAIN CHEMICAL REACTION:	$\text{SiO}_2 \rightarrow \text{Si}$		
ORE:	High purity quartz		
CARBON SOURCE:	Low ash coal, charcoal, wood		
ENERGY REQUIRED (kWh/t)	12,000		

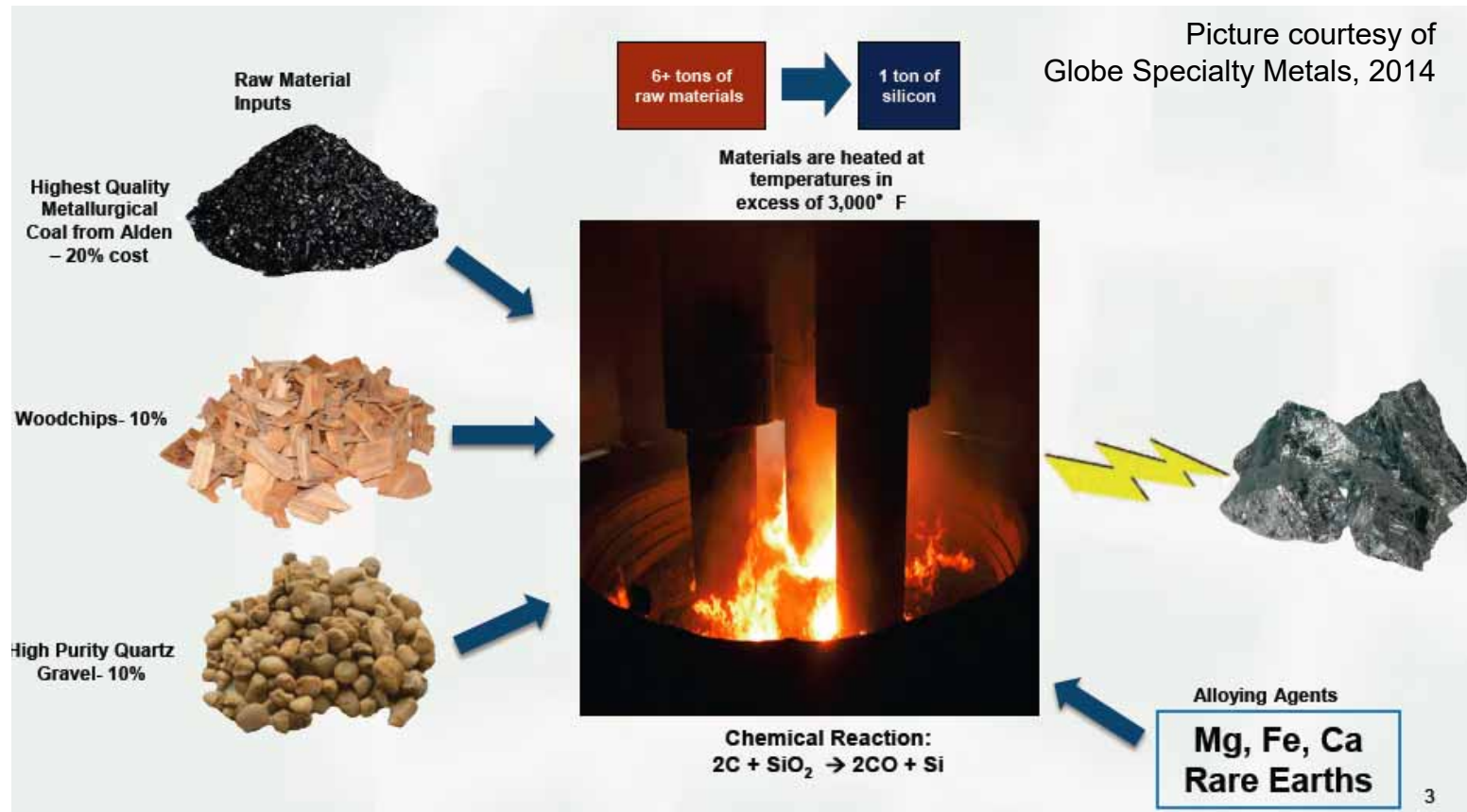


6 tons of Raw Material = 1 ton of SiMe

PRODUCTION COST BREAKDOWN

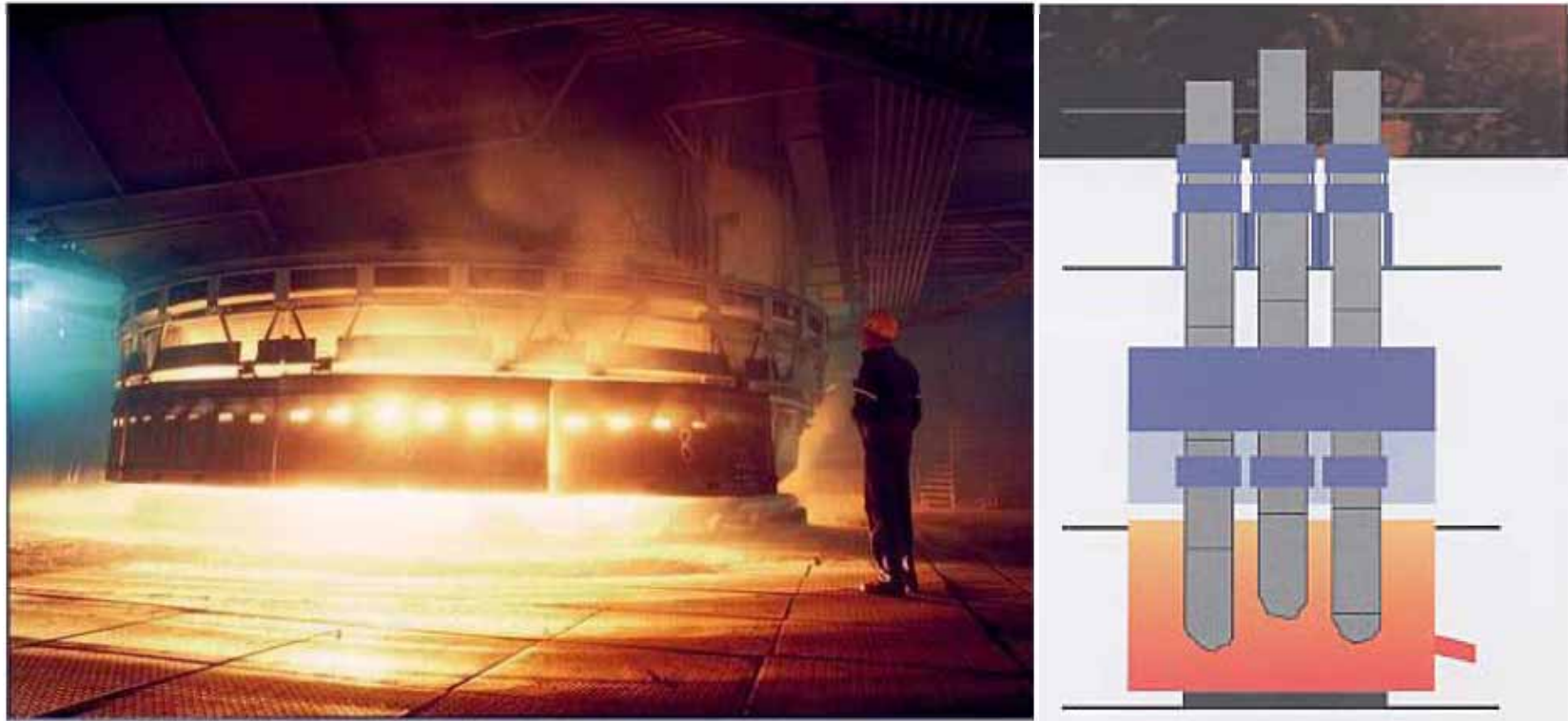
Source: Ferroglabe, CRU

How is Metallurgical Si Made?



Reduction of quartz in a submerged electric arc furnace. Highly energy intensive process. Large plants. A medium sized EAF has a crucible diameter of 7 m, graphite electrodes each 15 m tall, weighing 20 tons each.

How is Metallurgical Grade Silicon Made #2



A medium sized submerged arc furnace has a crucible diameter of about 7 metres. It is fed by three carbon electrode columns about 15 metres high and weighing about 20 tons each.

Source: http://www.carbonandgraphite.org/pdf/silicon_production.pdf

Si Smelting in a Submerged EAF

RAW MATERIALS FLOOR



TRANSFORMER FLOOR

ELECTRODES



TAPPING FLOOR



Graphics: Ferroglobe, 2017

Facility layout – Ferroglobe, Polokwane, South Africa



Graphics: Ferroglobe, 2017

For Si Metal Plants – Low Cost Electricity is Critical



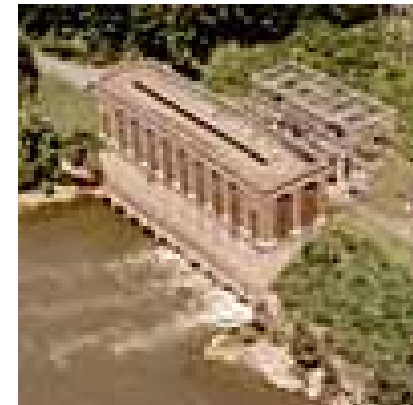
For every 1 ton of Si production
12 MWh of Electricity consumed



GSM Alloy Plant



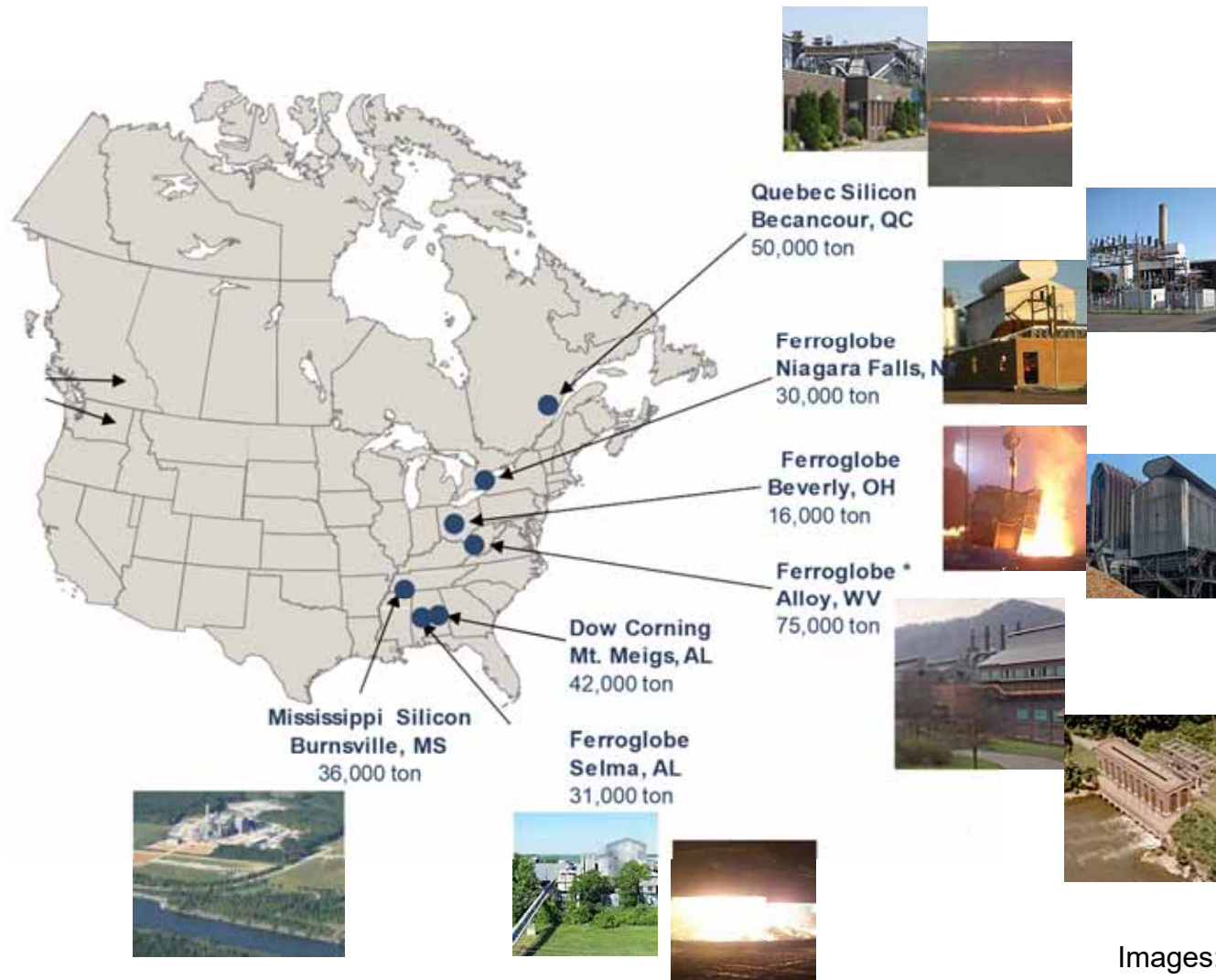
Electric Arc Furnace
in Operation



Hawk's Nest
Hydroelectric Plant

Source: Globe Specialty Metals

North American Si Metal Plants

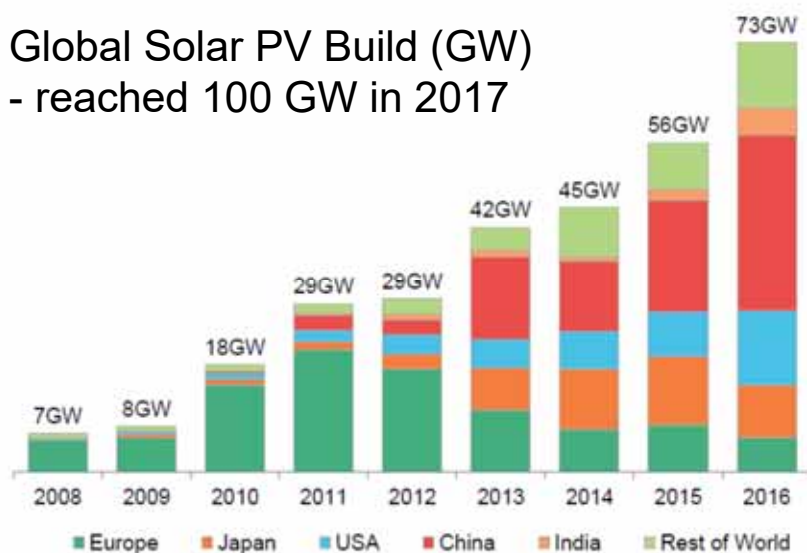


Images: Ferroglobe, DowCorning

GROWING MG Si METAL MARKET

- MG Si consumption was 2.2 Million Tons
- Demand growing at 6.0% from 2016 – 2020
- Growth largely driven by the growing demand for polysilicon for PV panels

Global Solar PV Build (GW)
- reached 100 GW in 2017



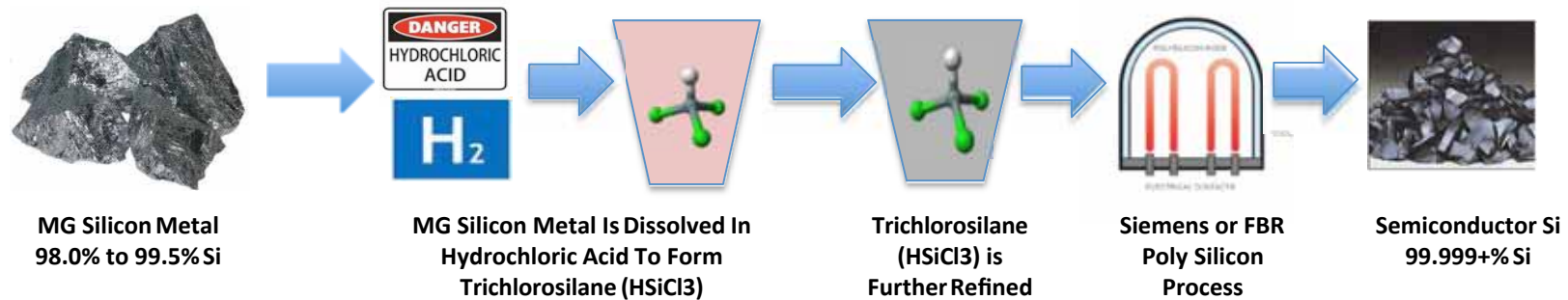
Source: Bloomberg New Energy Finance (2017)

MG Si Market Growth



Source: CRU 2015, Ferroglabe

Si metal to Semiconductor grade Polysilicon



Polysilicon



**70 MWh -
120 MWh**
to produce 1 ton
of polysilicon

Impurities in Silicon

Metallurgical grade

%Fe<0.5
%Ca<0.03
%Al<0.1
ppmP<limit

Chemical grade

%Fe<0.4
%Ca<0.03
Min<%Al<Max
ppmP<limit
Trace elements <limit

PolySilicon grade

%Fe<0.3
%Ca<0.03
Min<%Al<Max
ppmP<limit
ppmB<limit
Trace elements <limit

Solar grade

%Fe<0.001
%Ca<0.0001
%Al<0.0001
ppmP<1
ppmB<1
ppm others <10

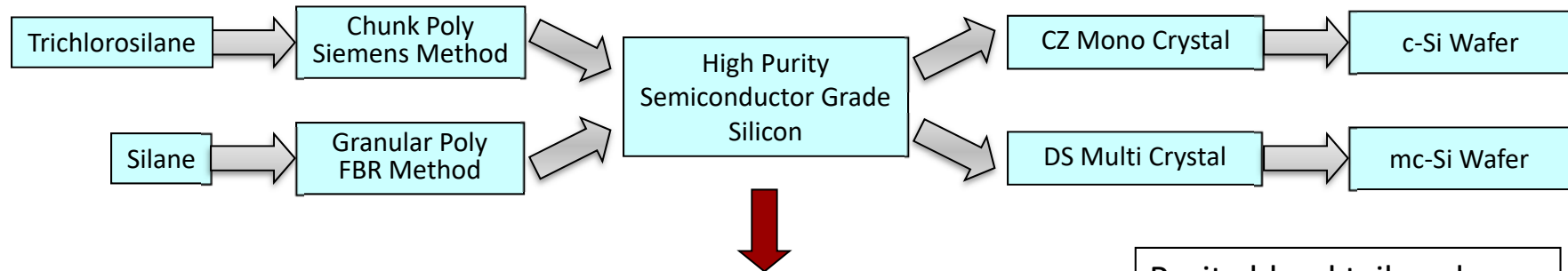
High Purity

%Fe<0.001
%Ca<0.0001
%Al<0.0001
ppmP : tailormade
ppmB : tailormade
ppm others : tailormade

Semiconductor Grade Si

Typical Impurity Level	
Boron	< 0.1 ppba
Phosphorous	< 0.1 ppba
Other Donors	< 0.03 ppba
Carbon	< 0.15 ppma
Transition Metals (Total Cu, Ni, Fe)	< 1 ppba

Silanes to Polysilicon to Wafers

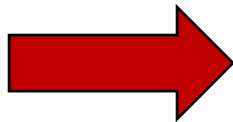


Typical Impurity Level	
Boron	< 0.1 ppba
Phosphorous	< 0.1 ppba
Other Donors	< 0.03 ppba
Carbon	< 0.15 ppma
Transition Metals (Total Cu, Ni, Fe)	< 1 ppba

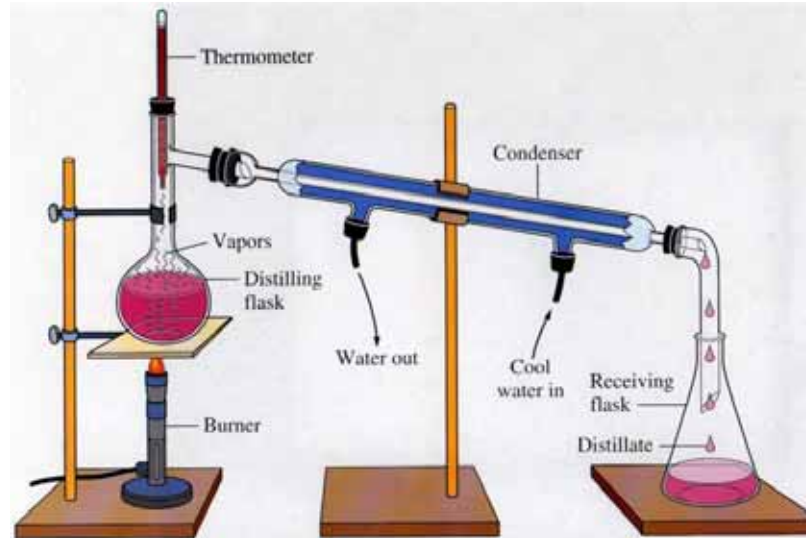
Purity blend tailored
to application

Purification of Metallurgical Grade Silicon

Laboratory scale
distillation



Impure TCS in



Pure TCS out



Industrial scale
distillation

Graphics: Courtesy of Graham Fisher
MEMC Electronic Materials

Purification of Metallurgical Grade Silicon



Metallurgical silicon costs about \$2 per kg

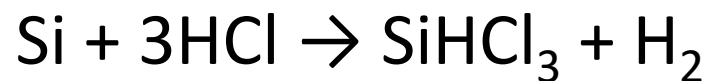
MG Si contains too many impurities for use in semiconductors or solar cells

In order to purify it we do this:

- 1) Convert it to a liquid compound containing silicon
- 2) Distillation of the liquid to purify it
- 3) Extract silicon from the high purity liquid

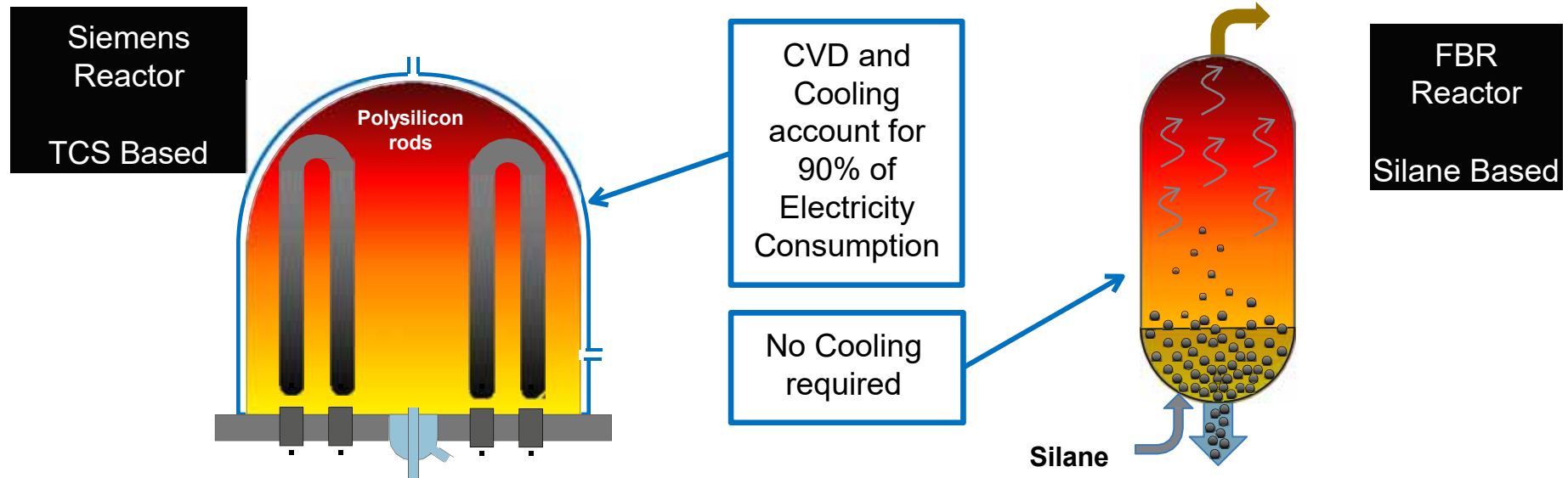
Step 1 is achieved through the following reaction

Silicon + Hydrochloric acid → Trichlorosilane + Hydrogen
Solid Liquid Liquid Gas



TriChloroSilane is often referred to as TCS

Polysilicon Production



Siemens Process

- Mature 40 year technology
- Batch process
- Requires post processing
- High cash cost

FBR Process

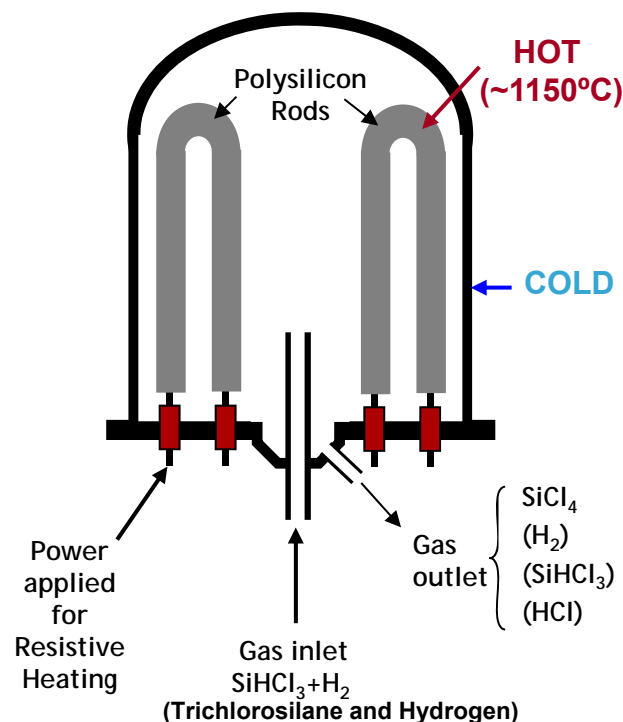
- Energy efficient
- Continuous production
- Lower cash cost

Siemens Process

- Convert metallurgical Silicon into Trichlorosilanes (TCS)



- Purify TCS in distillation columns
- Recover pure Si using Chemical Vapor Deposition (CVD)



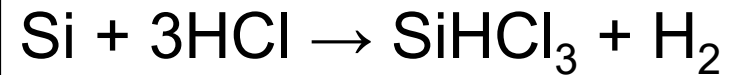
Cold wall reactor, high energy consumption. TCS conversion per pass is around 15%, recycling and lower productivity

Siemens Process

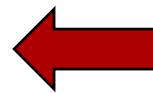
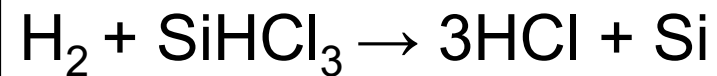


The Siemens process is commonly used to produce semiconductor grade silicon

We used this reaction to make TCS:

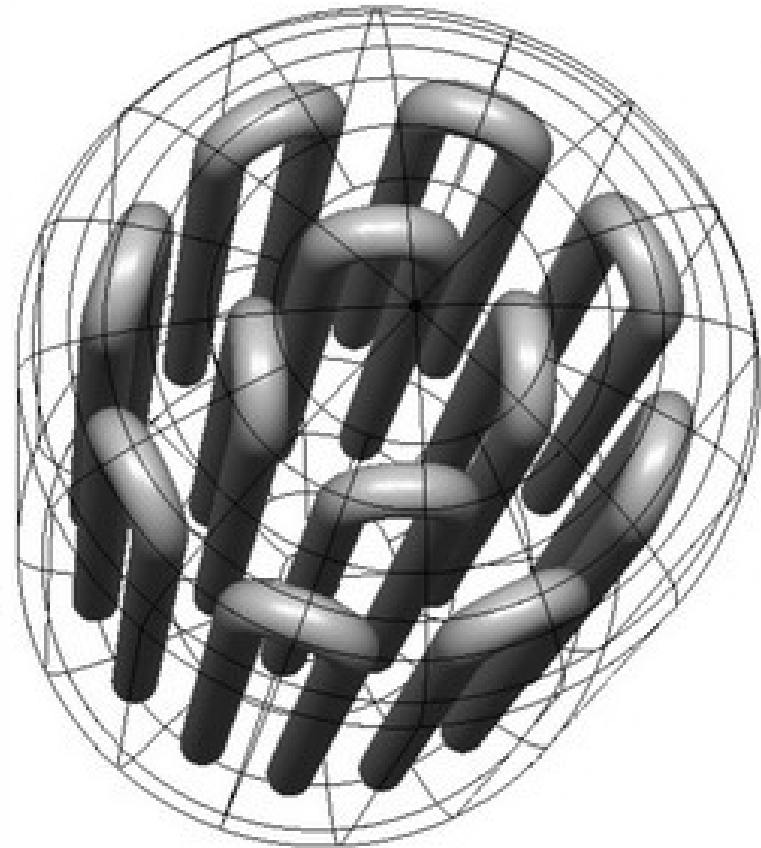
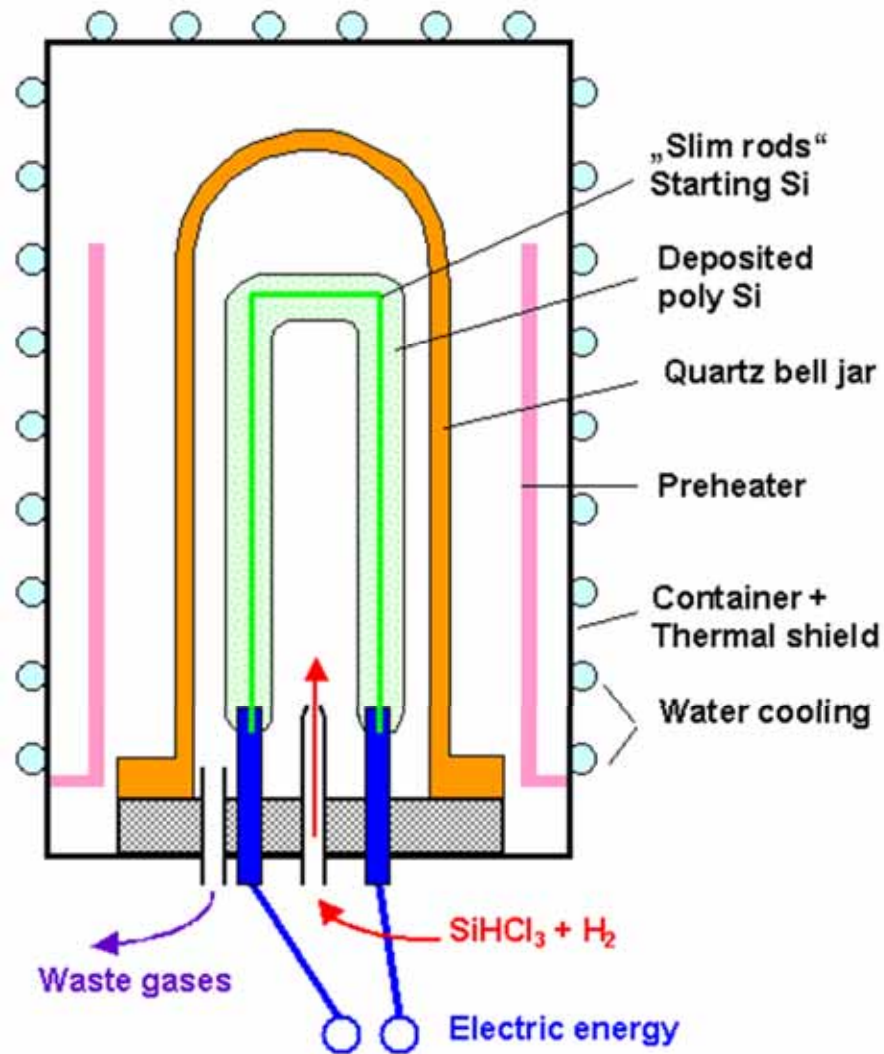


To go back to silicon we just run the same reaction backwards!



The reaction is run in a Siemens reactor that looks like this.

Inside the Siemens Reactor



Siemens Polysilicon



Siemen's reactor



Before polysilicon
growth – slim rods



As grown polysilicon
rods after a reactor run

Source: GR Fisher, Proc. IEEE, vol. 100, pp. 1454 – 1474, April 2012

**80% of the worlds polysilicon is produced using the
Siemen's process developed in the 1950's.**

Insides of Siemens Reactor



Before



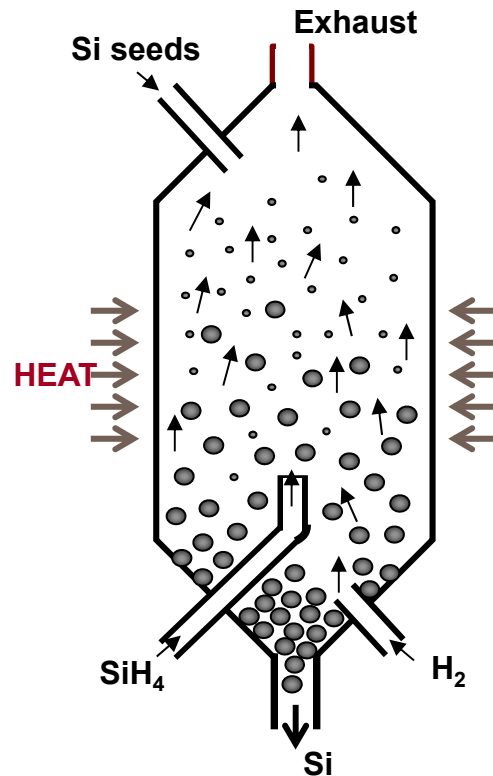
After

Si from Siemens Process – Chunk poly



Graphics: Graham Fisher
MEMC Electronic Materials

Fluidized Bed Reactor Production



Hot wall reactors
Higher throughput



Granular polysilicon has a higher packing density in the crucible and, because it flows, can be used to recharge hot crucibles lowering cost and improves throughput of crystal growth processes.

Poly-Si Production – Large Chemical Plants

**MEMC/SunEdison Polysilicon Plant
Merano, Italy (Siemens process)**



**MEMC/SunEdison Polysilicon Plant
Pasadena, TX (FBR process)**

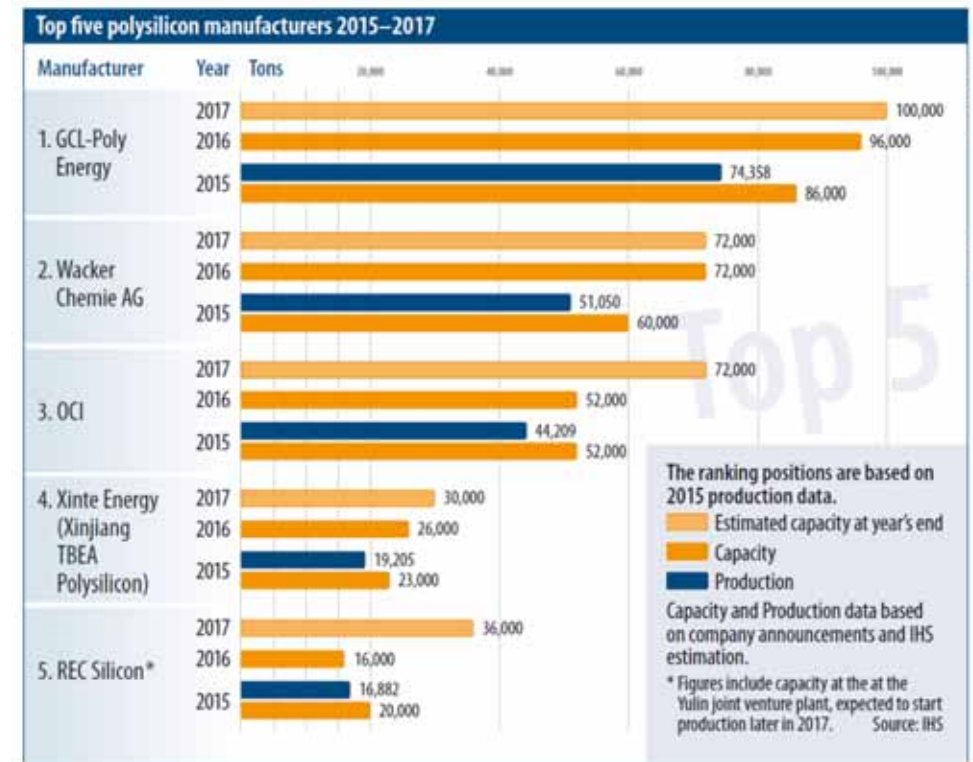
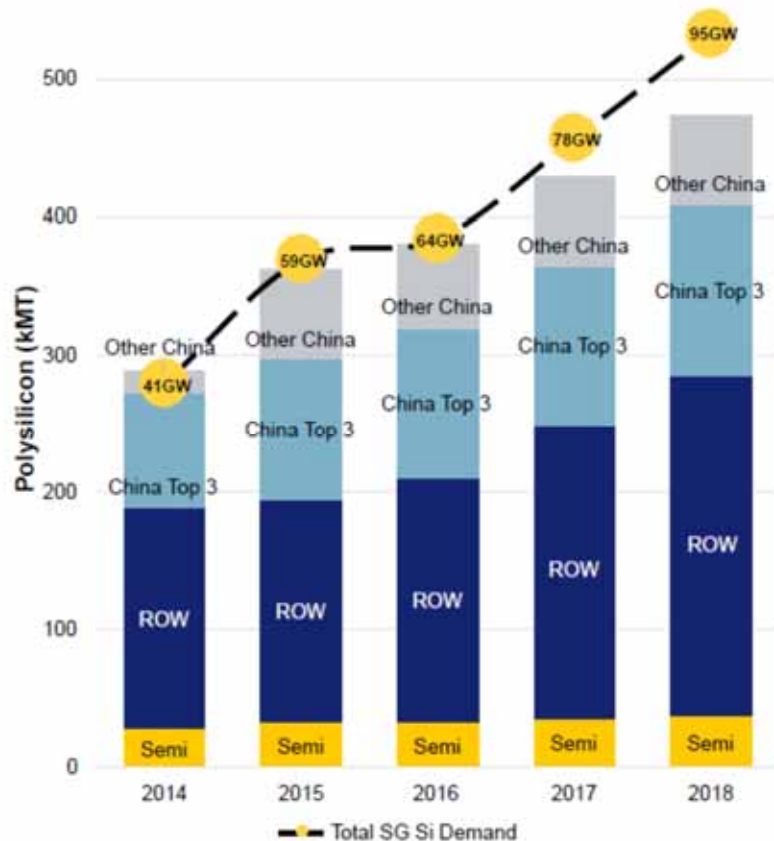


Large capital outlays
10000 ton capacity plant ~\$500M

**REC Silicon – Silane/Granular Poly Si Plant
Moses Lake, MT (FBR process)**



Growth in Polysilicon Production



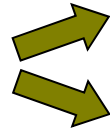
Over 90% of polysilicon is consumed by the PV Industry
 Size of the PV market in 2017: 75 GW; 2017: 100 GW, Si used <5g/W

Crystal Growth and Wafer Manufacturing

- Czochralski(CZ) growth remains the dominant process for monocrystalline crystal growth
- Significant advances in Continuous CZ process
- Directional solidification (DS) for multicrystalline wafers

Solar vs. Semiconductor Silicon

Polysilicon

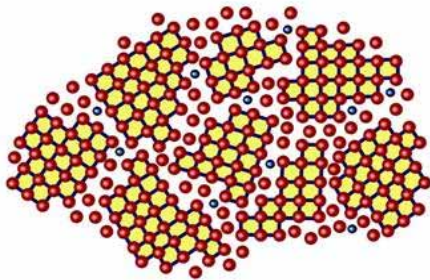


Semiconductor
Applications
Solar Applications

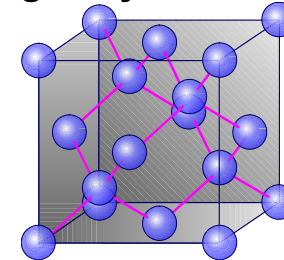
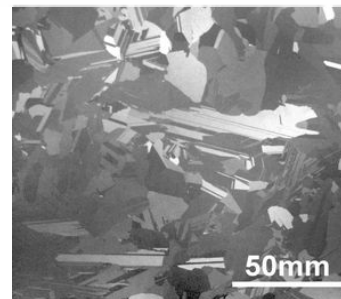
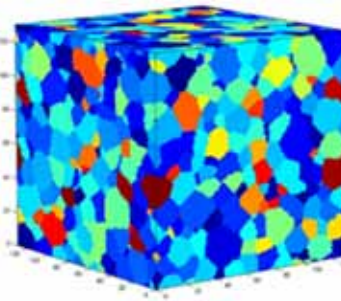


Monocrystalline silicon
Single crystal ~meters

Polysilicon
Grain size $\sim \mu\text{m} - \text{mm}$



Multicrystalline silicon
Grain size $\sim \text{mm} - \text{cm}$



Solar Wafers

<\$1
per unit

\$/W

Cost Metric

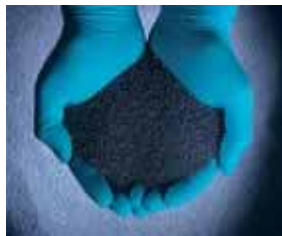
\$/in²

~\$100
per unit

Semi Wafers

Semiconductor vs. Solar

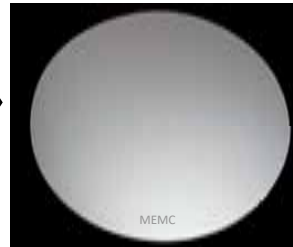
Semiconductor/Electronics Food Chain



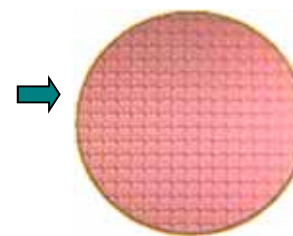
Polysilicon



Ingot



Wafers

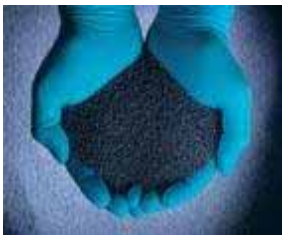


Semiconductors



Electronics

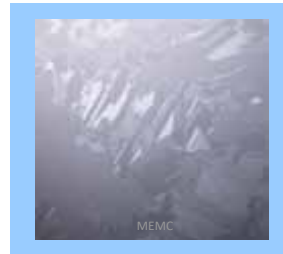
Solar Food Chain



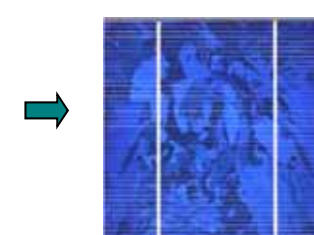
Polysilicon



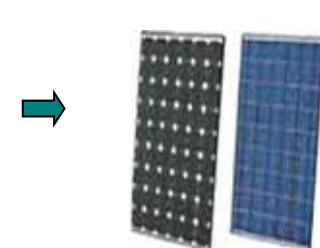
Ingot



Wafers

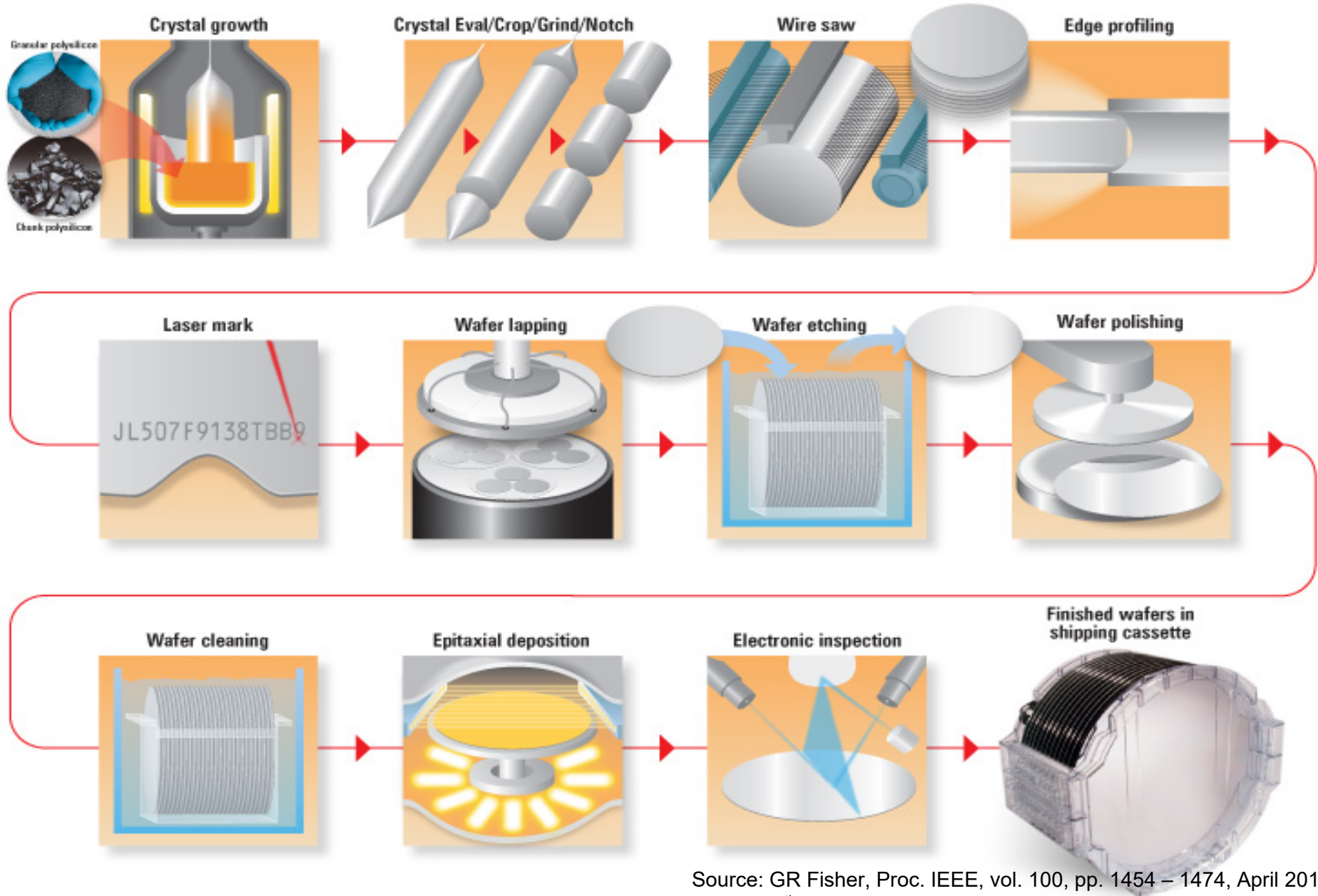


Cells



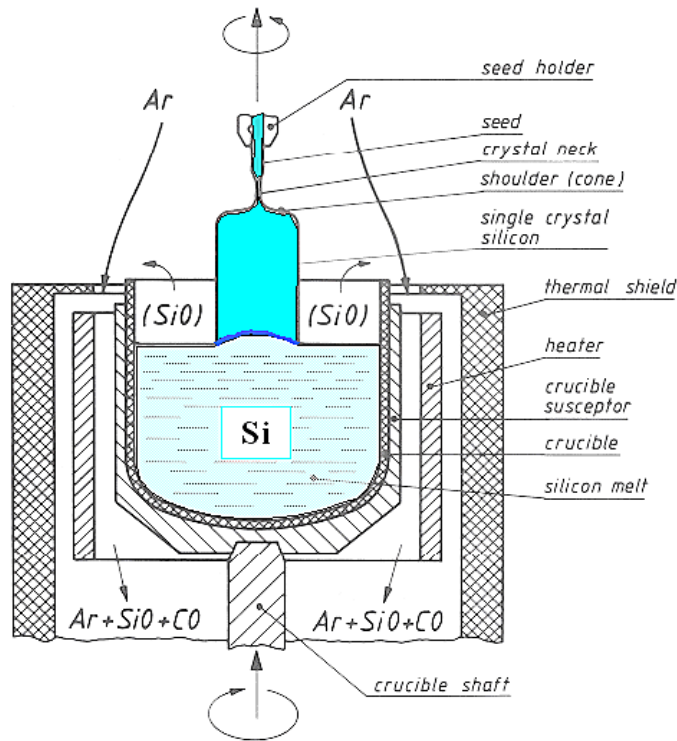
Solar Modules

Monocrystalline Si Wafer Manufacturing Process

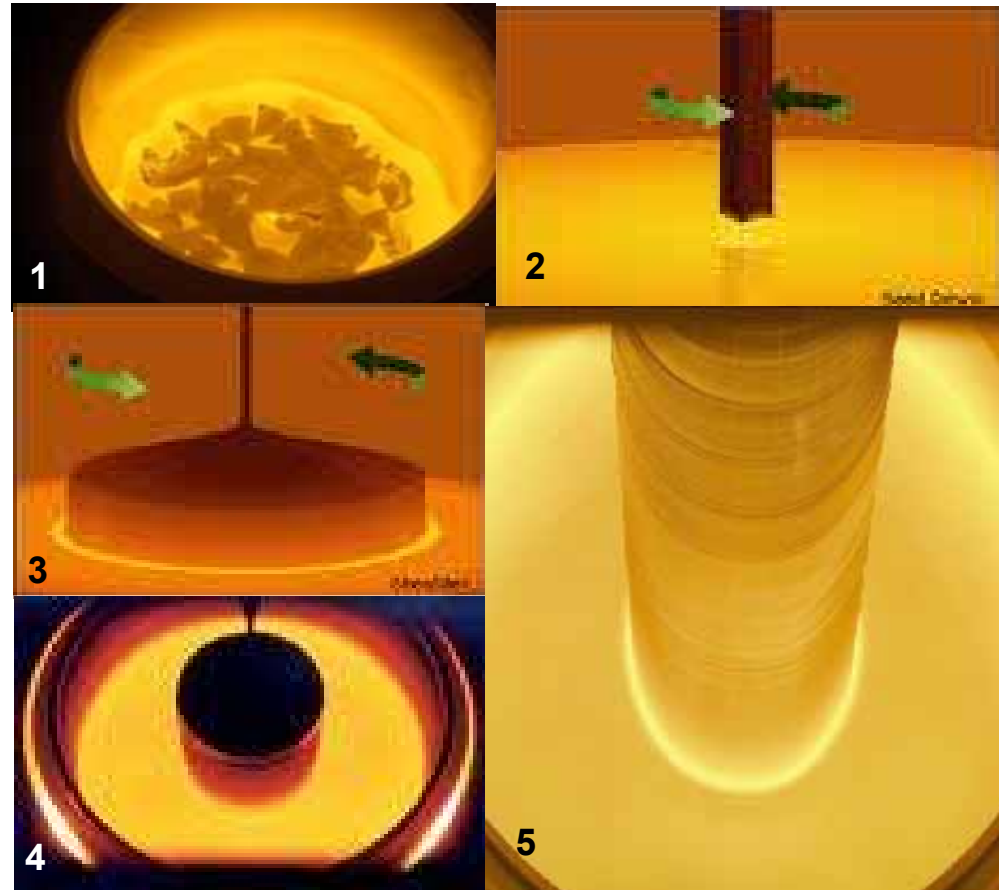


Source: GR Fisher, Proc. IEEE, vol. 100, pp. 1454 – 1474, April 2012
MEMC 50th Anniversary Volume, 2009

Crystalline Si Czochralski Crystal Growth



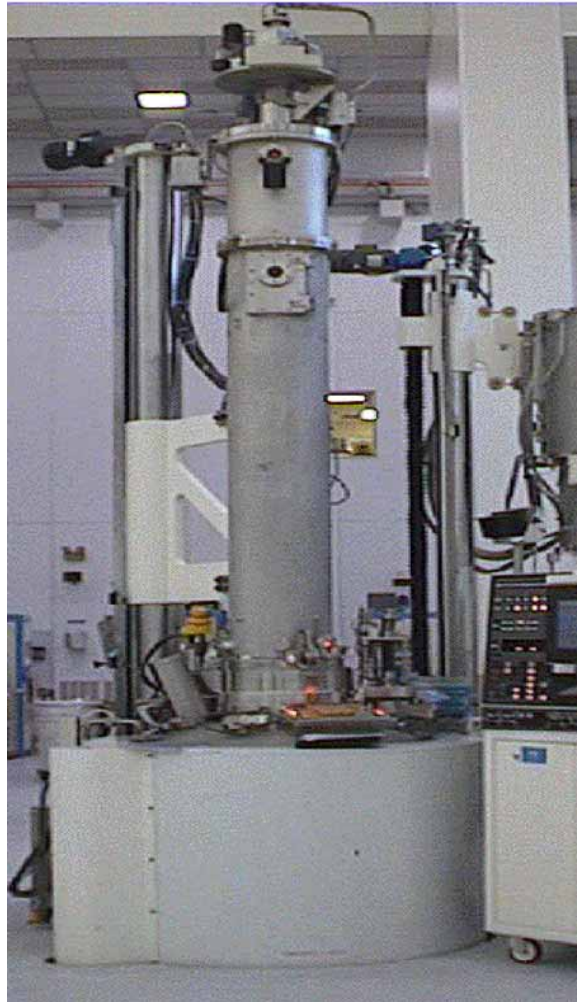
Crystal Puller



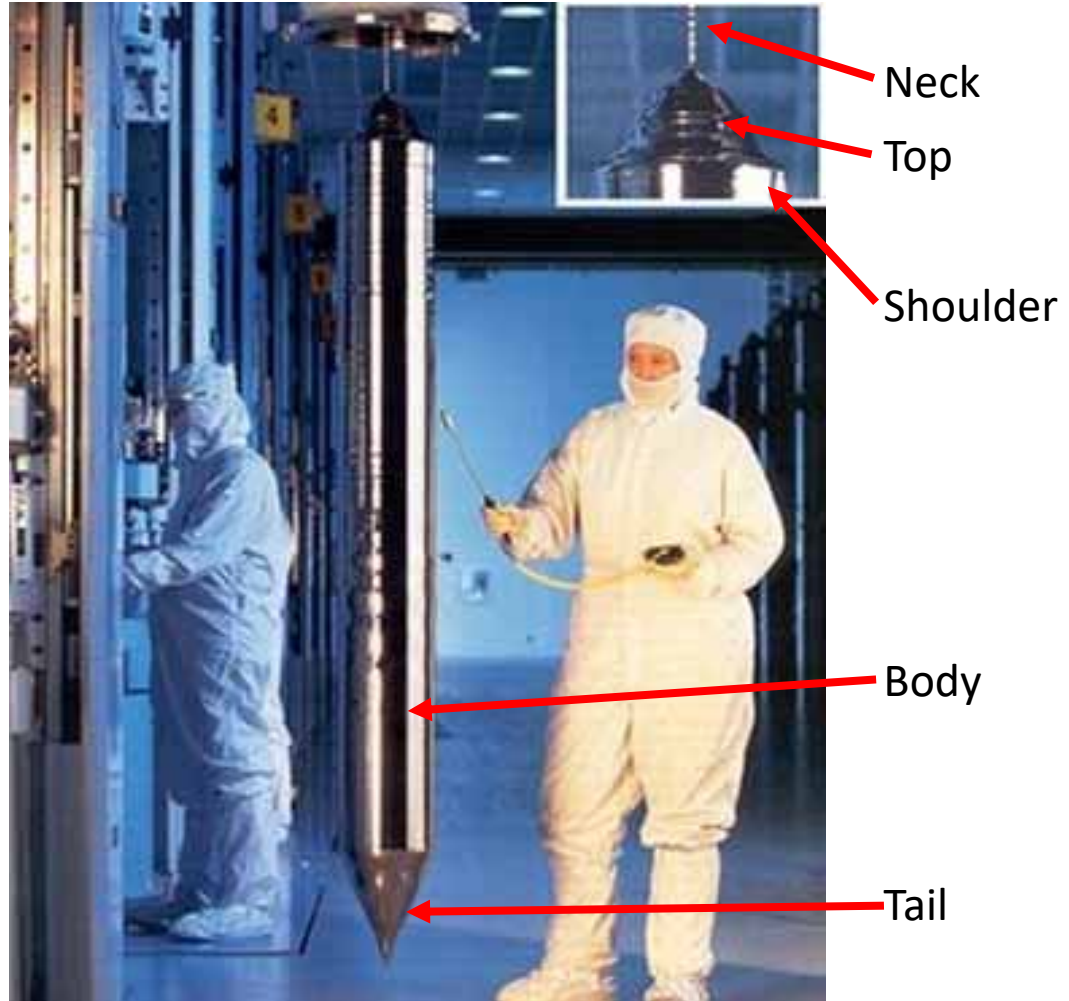
Various stages of Czochralski crystal growth,
1 Meltdown, 2 Seed Dip, 3 Top, 4 Shoulder, 5 Body

Source: GR Fisher, Proc. IEEE, vol. 100, pp. 1454 – 1474, April 2012

Czochralski Method for Silicon Crystal Growth

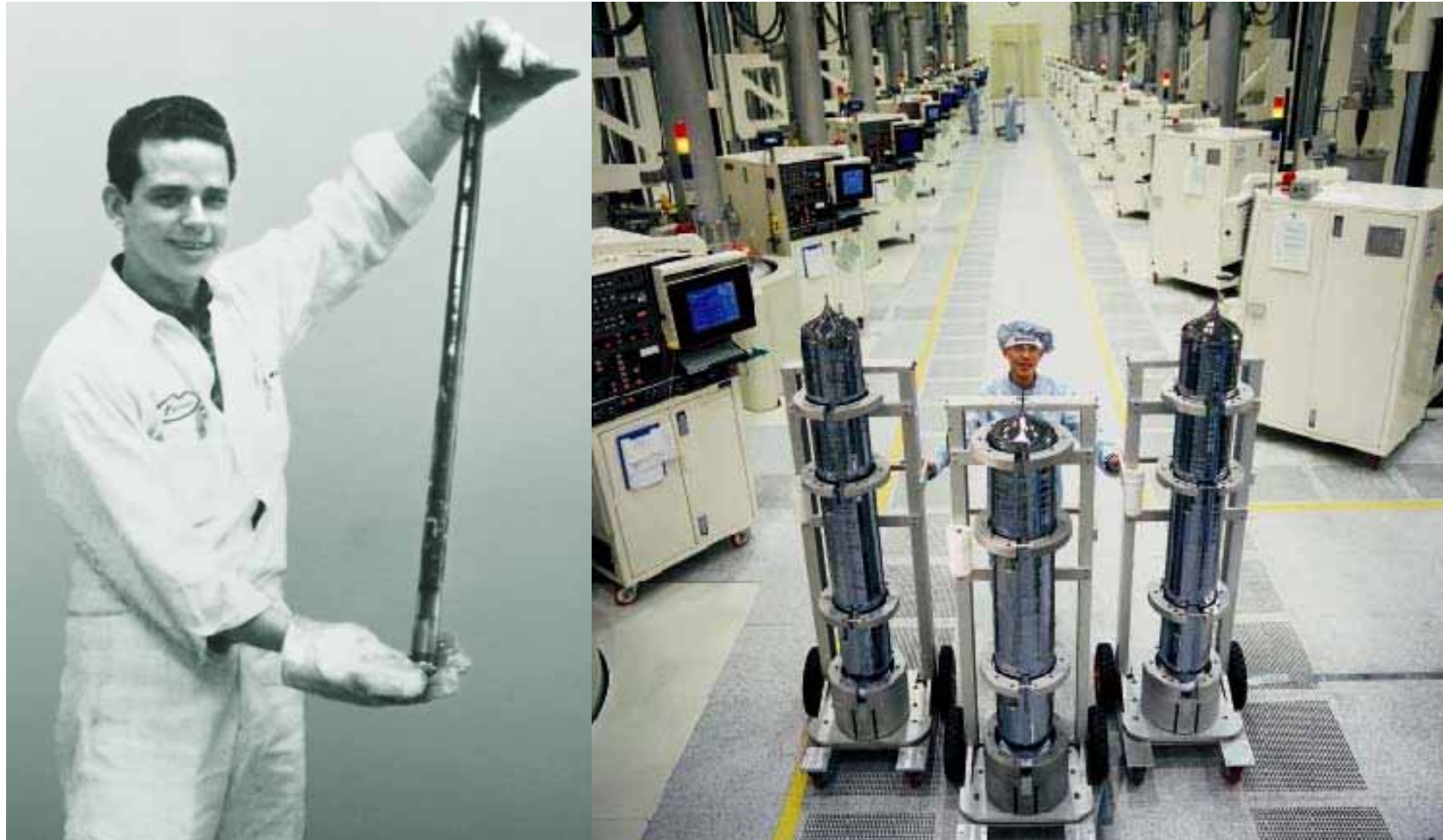


Crystal Puller



Product

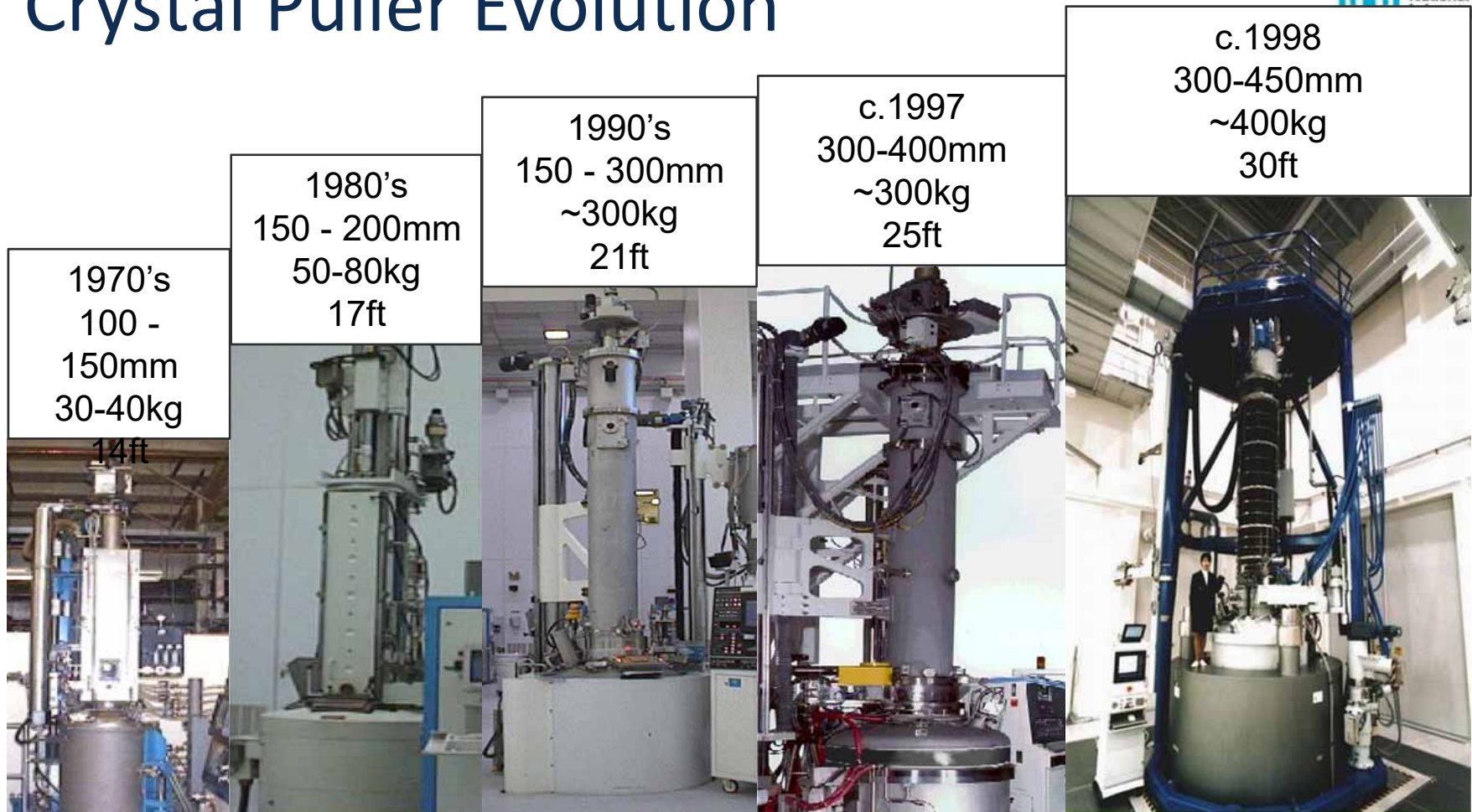
Typical Factory Floor



Early days of Czochralski(CZ) growth crystals were small and easy to handle. Current generation crystal are large, heavy and need specialized handling equipment.

Source: MEMC 50th Anniversary Volume, 2009

Crystal Puller Evolution



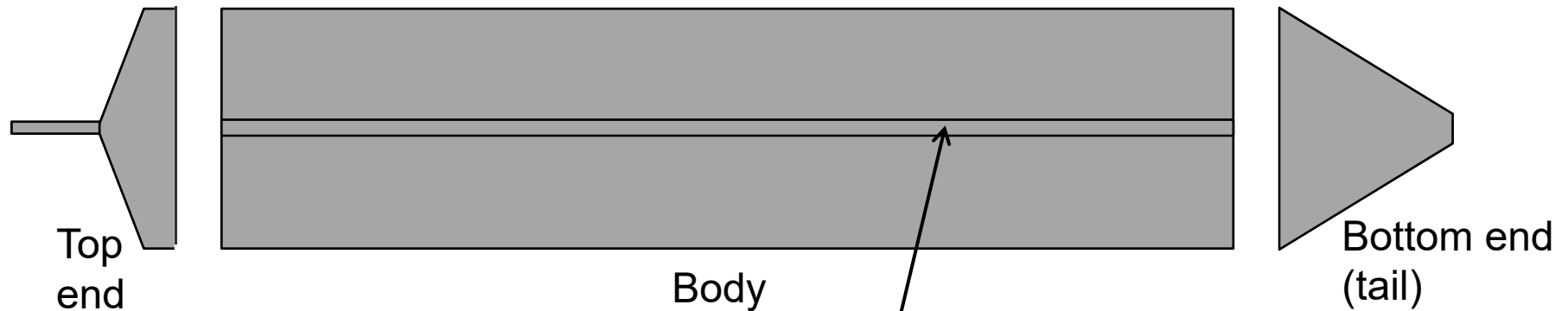
Examples of progress in Czochralski crystal pullers from 1970 through current diameter capability. Showing approximate period, crystal diameters, typical polysilicon charge weight and approximate height of the equipment above the working floor. Later models have services (water, argon, vacuum) below floor level. (Right hand photo shown is courtesy of Super Silicon Institute (SSI).)

Source: GR Fisher, Proc. IEEE, vol. 100, pp. 1454 – 1474, April 2012

Continuous Czochralski Crystal Growth

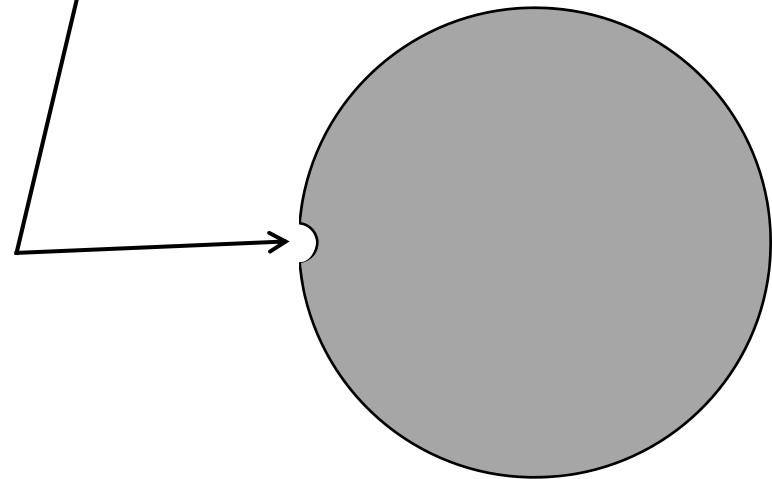


Wafer Slicing

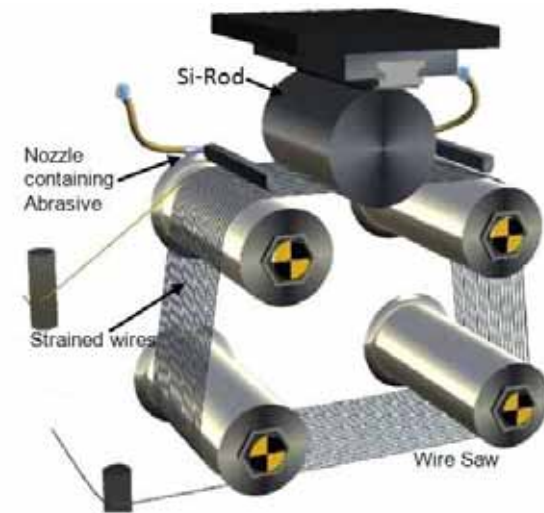


Before getting the ingot ready for slicing, top and tail ends are removed. Orientation of the crystal lattice determined by x-ray diffraction.

A notch is cut on outside aligned with the crystal lattice. Later when the wafers are cut from the ingot, each one has a notch which indicates the orientation of the crystal lattice.

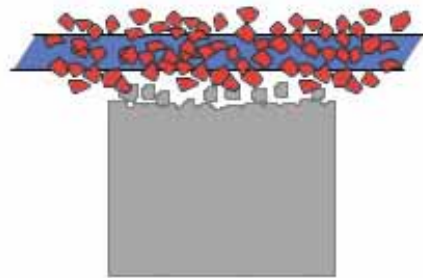


Wafer Slicing

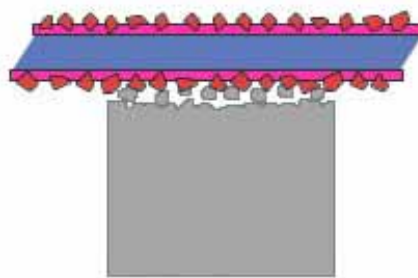


Solar wafers 180 - 220 μm thick, typical Semiconductor wafer $\sim 900\mu\text{m}$

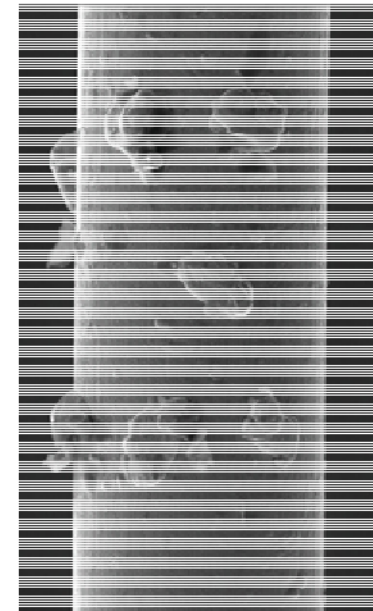
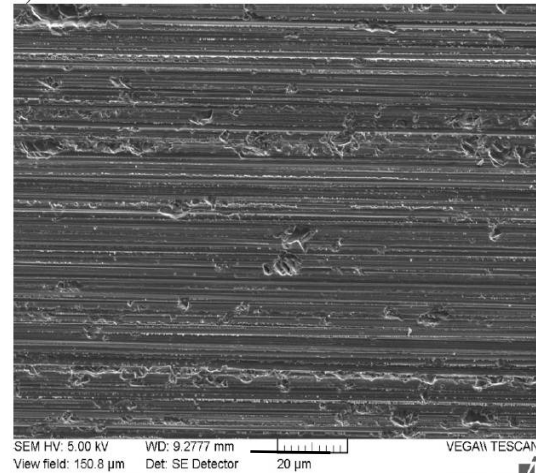
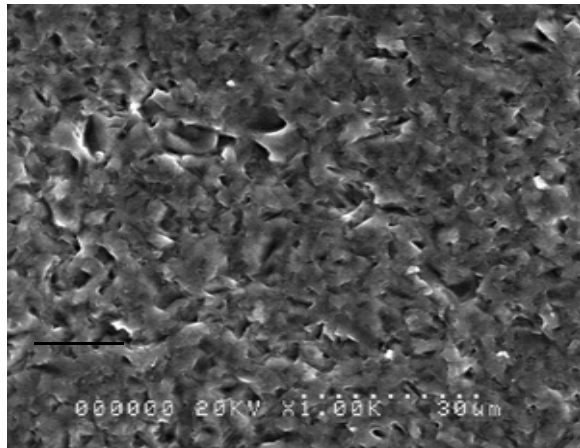
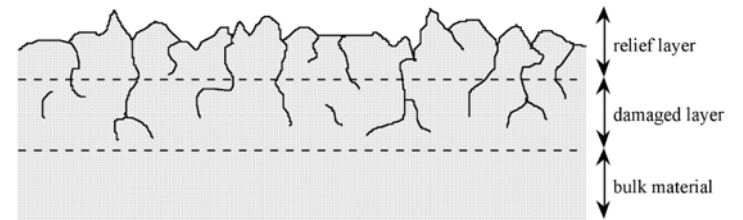
Wafer Slicing



Slurry-based method



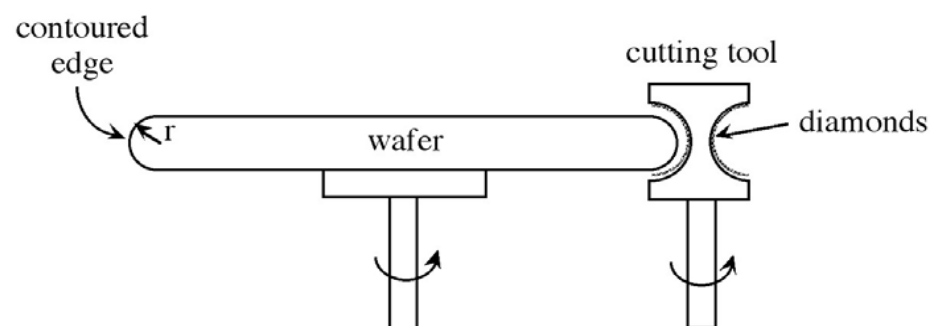
Fixed Abrasives method



Edge Profiling

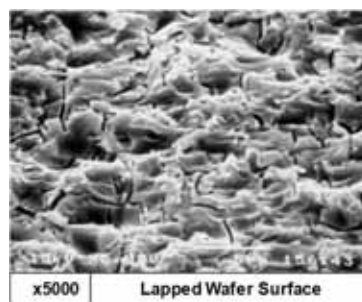
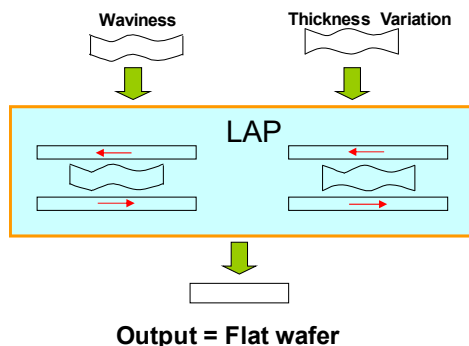
Purpose

- Produce a rounded wafer edge that is tougher and more resistant to chipping during handling
- Minimize edge surface roughness
- Minimize depth of damage on edge

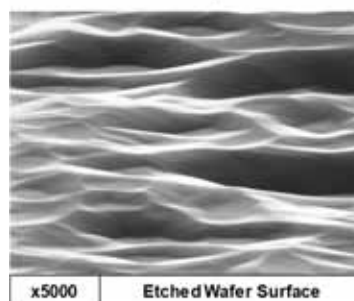


Lapping, Etching and Polishing

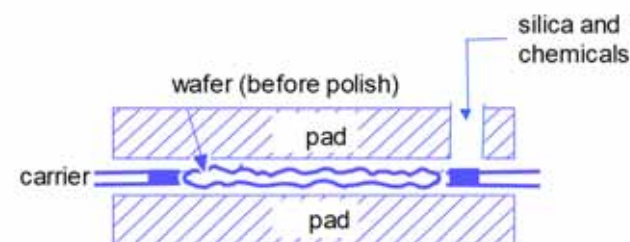
Lapping removes saw damage and produce a flat wafer. Etching and chemical mechanical polishing processes further improve the surface to almost atomically smooth.



Mechanical damage



Damage removed
Flat but not smooth



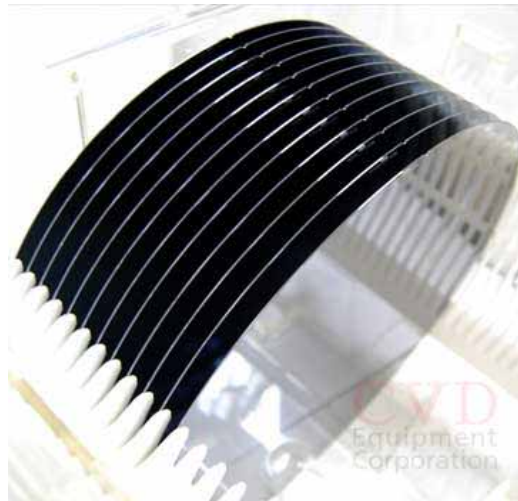
Finished Semiconductor Wafer

Flat to within 250nm

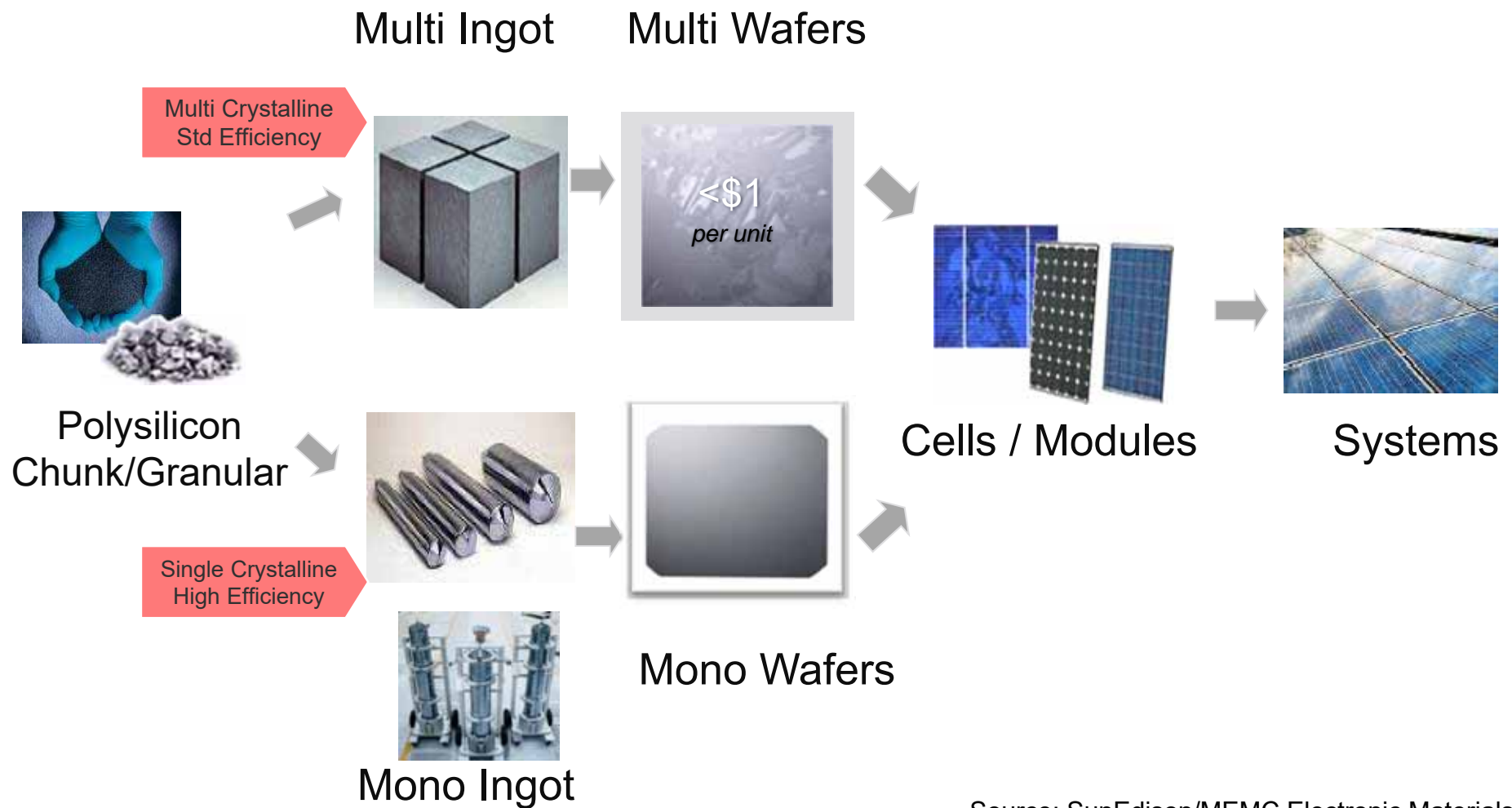
- equivalent to a football field flat to within 2 thousandth of an inch

Clean $<10^{10}$ unwanted impurity atoms/cm²

Purity $<10^{11}$ metal atoms/cm³



Silicon PV Food Chain

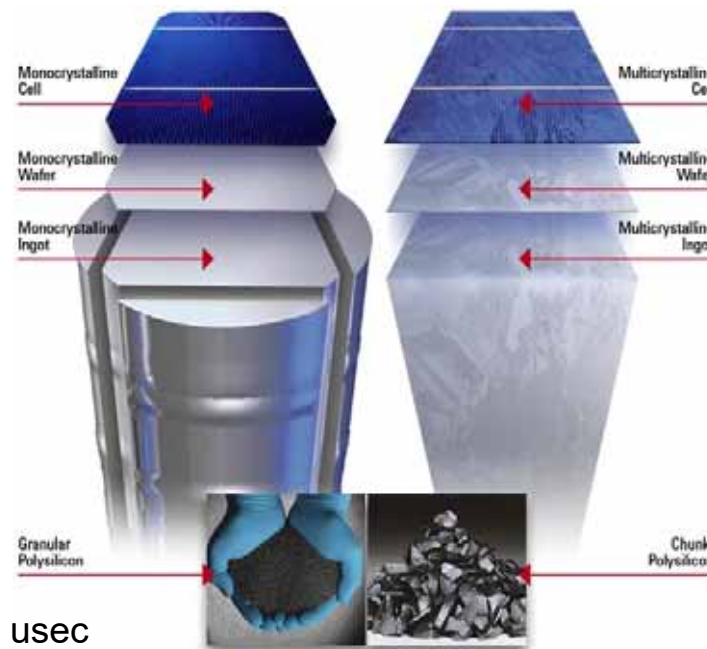


Source: SunEdison/MEMC Electronic Materials

Mono vs. Multi Silicon Wafers

Mono Characteristics

- P-type/N-type
- Resistivity $\sim 0.5\text{-}3\text{ohm-cm}$
- Nominal thickness $\sim \leq 200\mu\text{m}$
- Oxygen $< \sim 20\text{ppma}$
- Carbon $< \sim 1\text{ppma}$
- Dislocation-free
- Lifetime $> 10\text{usec}$ on block
- Passivated lifetime $> 100\text{-}1000\text{ usec}$
- Single orientation = lower reflectivity texturing

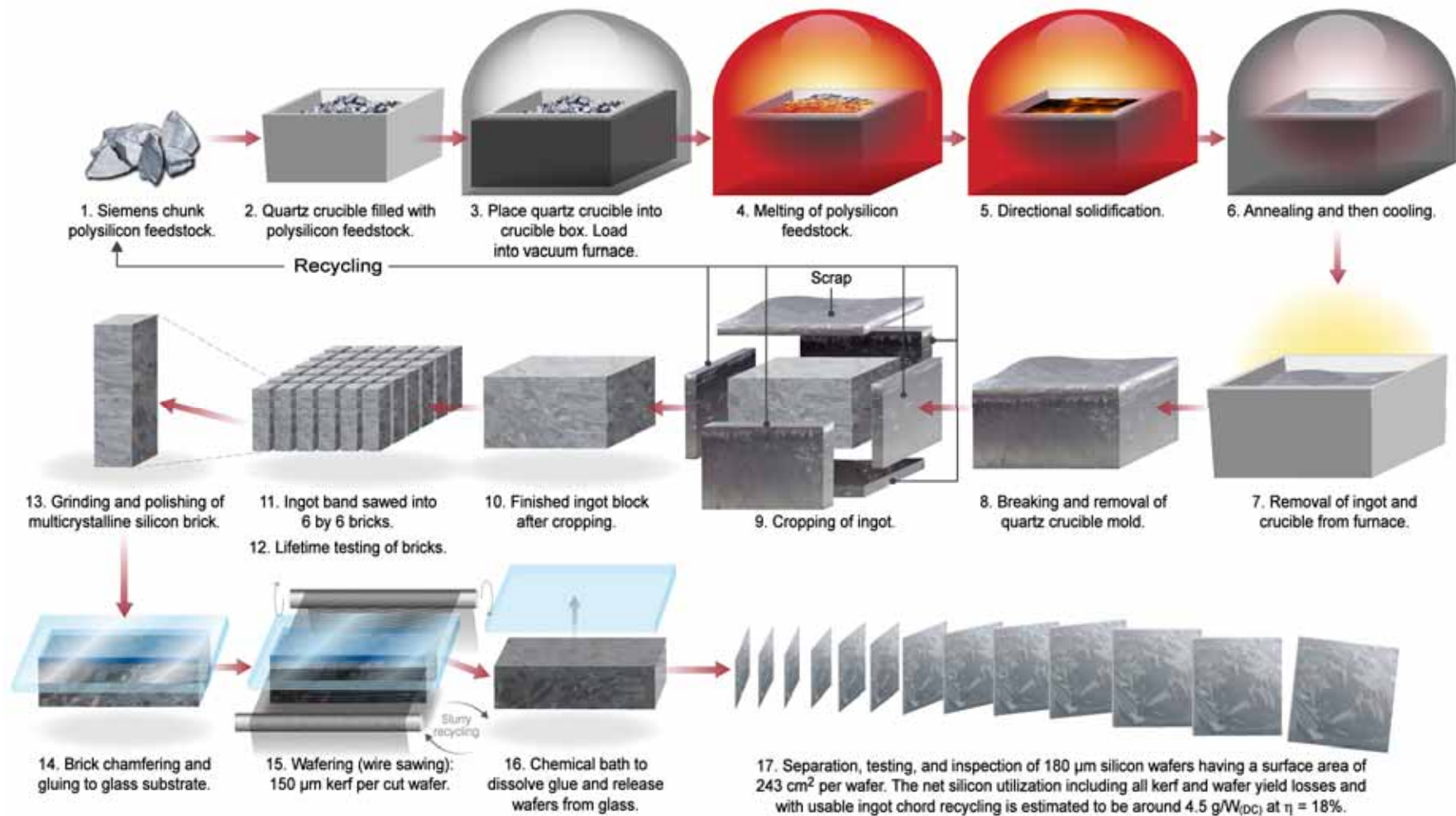


Multi Characteristics

- P-type
- Resistivity $\sim 0.5\text{-}3\text{ohm-cm}$
- Nominal thickness $\sim 200\mu\text{m}$
- Oxygen $< \sim 10\text{ppma}$
- Carbon $< \sim 10\text{ppma}$
- Dislocations $\sim E5/\text{cm}^3$
- Lifetime $> 2\text{usec}$ on block
- Passivated lifetime $> 10\text{usec}$
- Multi orientation = higher reflectivity texturing

Choice depends on application and cost requirements

Multicrystalline Si Wafer Manufacturing Process

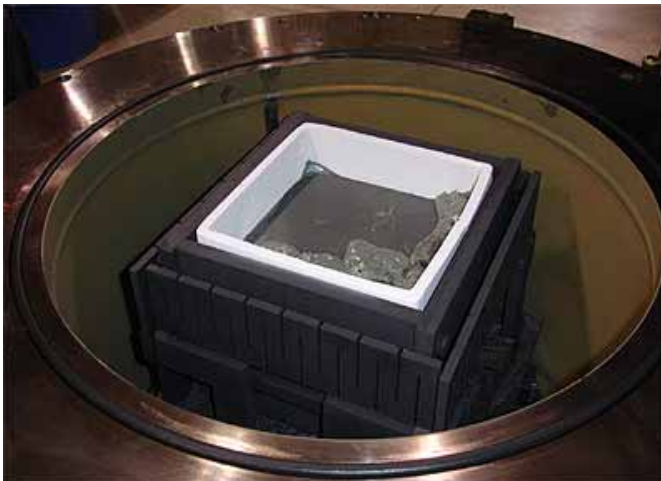


Graphic: courtesy of NREL, 2015

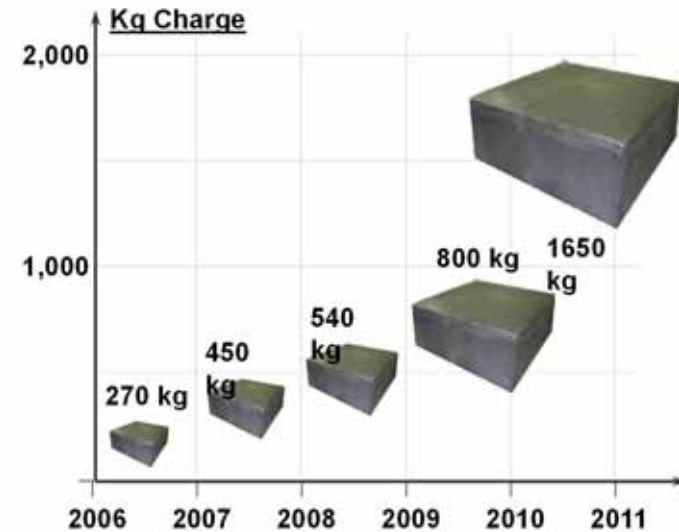
mc-Si Directional Solidification



Casting furnace



Open furnace after casting



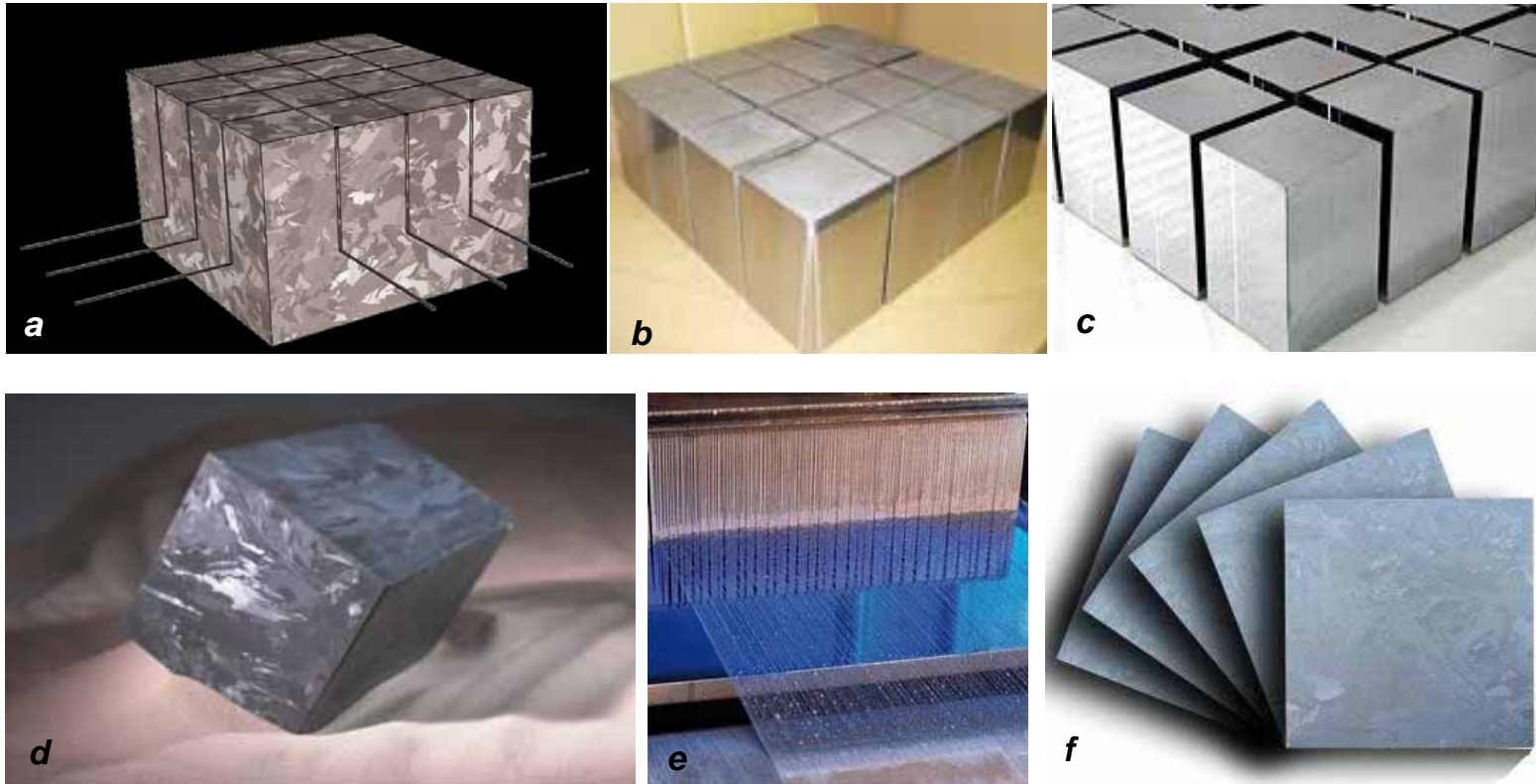
A . Deshpande, 2012 NREL Silicon Workshop
Images Courtesy of MEMC



Finished casting

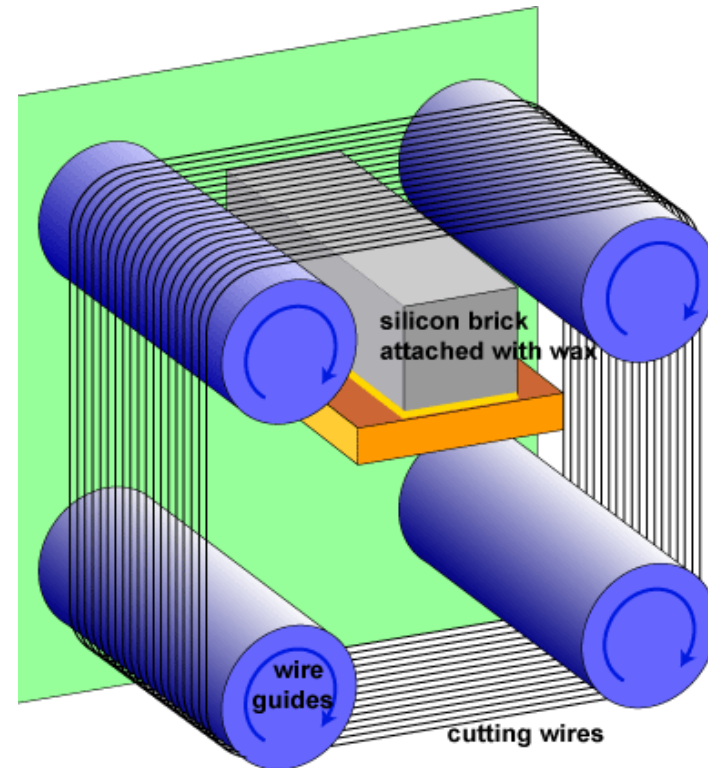
DSS allows for large cast

Fabrication of Solar Wafers



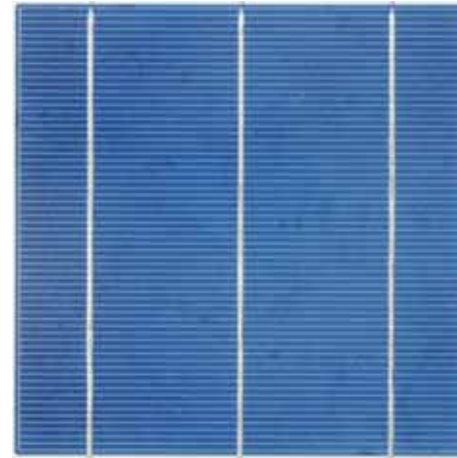
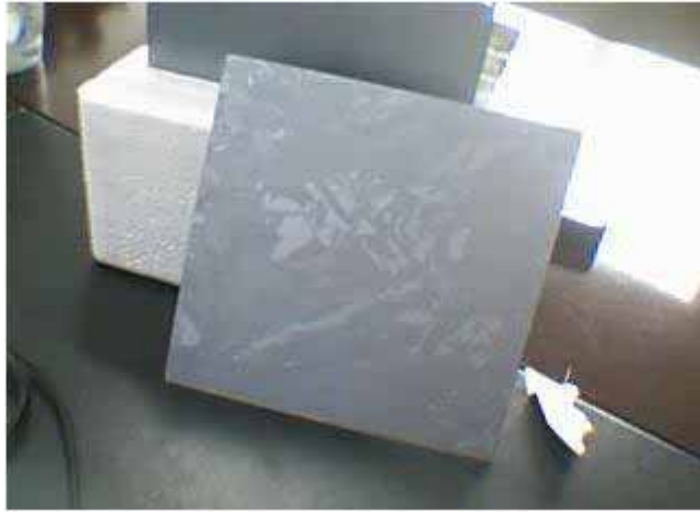
*(a & b) Sawn into bricks ; (c) Bricks are ground; (d) chamfered, then
(e) sawed into wafers, (f) polished wafers*

Wafer Slicing



Solar wafers 180 - 220 μm thick, typical Semiconductor wafer $\sim 900\mu\text{m}$

Finished Solar Wafer

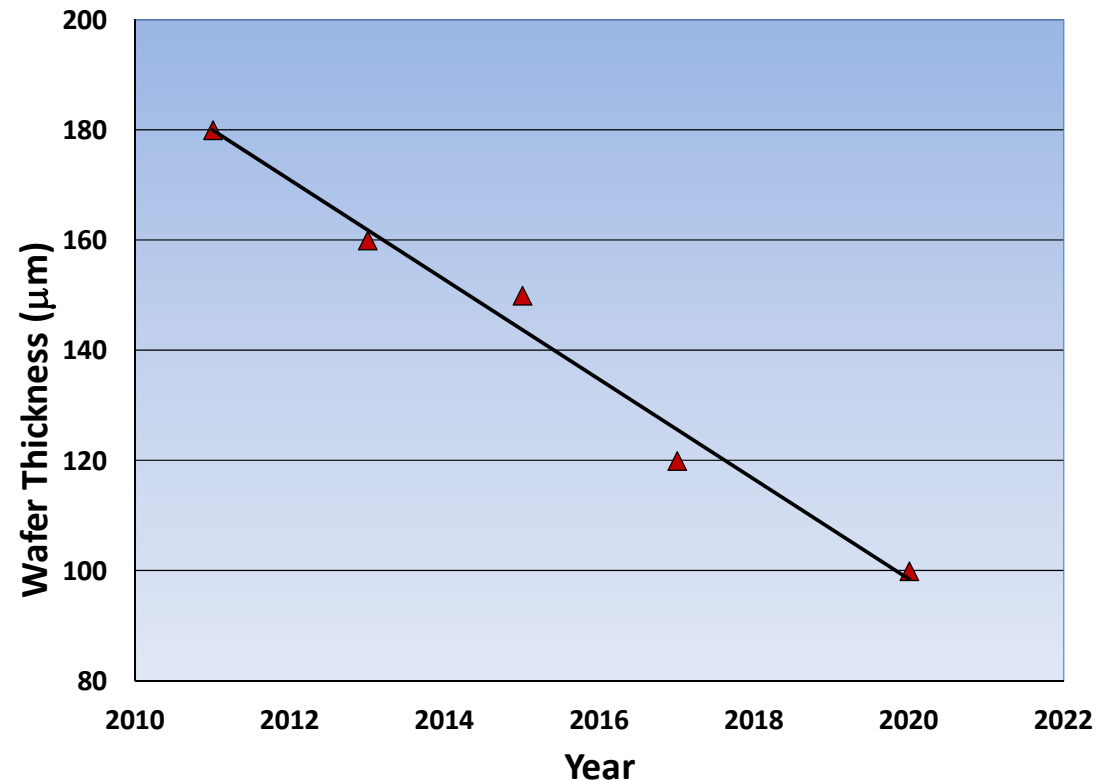


For solar applications cost is key

Processing downstream from slicing is limited to cleaning and an etch to remove some saw damage and add texture.

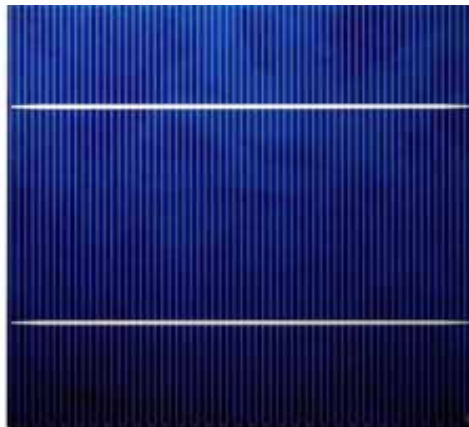
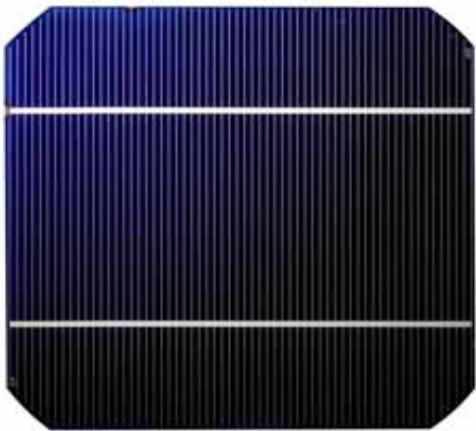


Trends in Wafer Technology



Projected trend in minimum wafer thickness processed in mass production of solar cells
(International Technology Roadmap for Photovoltaics, SEMI PVGroup/ITRPV, 2011).

Wafers to Cell and Modules



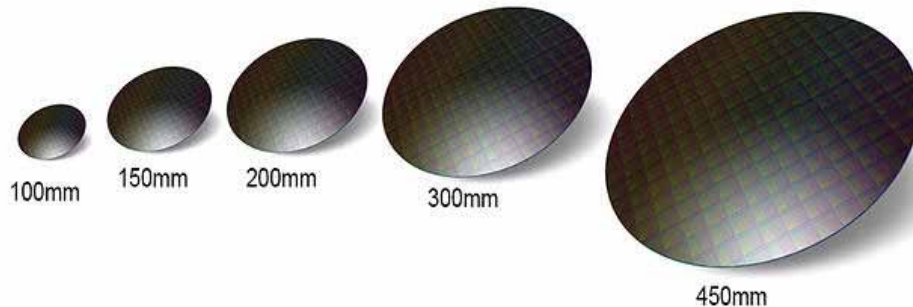
156 mm monocrystalline solar
wafer and cell.

156mm multi-crystalline
solar wafer and cell



Solar cell module
(from multi-crystalline wafers)

Scaling (size, volume, and performance)



Microelectronics

Si Substrates

20x scaling (30 yr)

50, 100, 150, 200, 300 mm

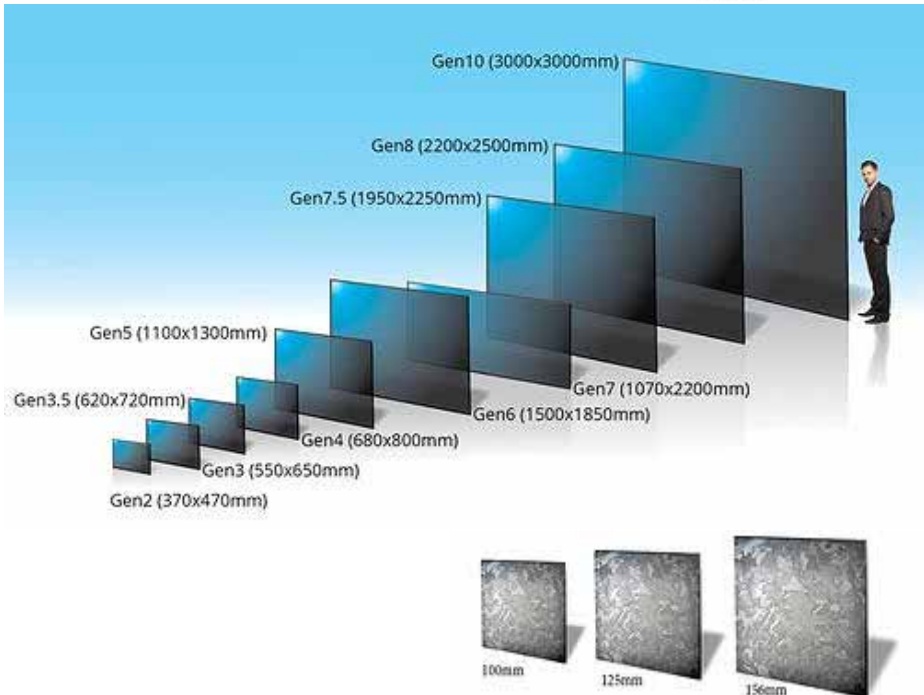
Flat Panel Displays

Glass Substrates

50x scaling (30 yr)

Gen1 (370x470mm)

Gen 8 (2200x2600 mm)



Solar Panels

Si Substrates

100 mm to 150 mm

2x scaling (20 yr)

Source: Brad Mattson, Sivapower

D. Mitzi, Solution Processing of Inorganic Materials, 2010

Summary

- Continuing advances in Si materials technology making
 - Microelectronics cheaper
 - Si PV reaching grid parity with fossil fuel electricity generation
- Manufacturing scale and growing demand for Si for PV further driving down the cost of polysilicon
- Further opportunities to improve materials utilization in Si PV

Acknowledgements



- Graham Fisher, Mike Seacrist, Bob Standley, and a number of colleagues at MEMC Electronic Materials/SunEdison Semiconductor for discussions and for presentation material.