SAND2014-157250

Single-Event Characterization of the 28 nm Xilinx Kintex-7 Field-Programmable Gate Array under Heavy-Ion Irradiation

David S. Lee
Sandia National Laboratories

Michael Wirthlin
Center for High Performance Reconfigurable Computing
Brigham Young University

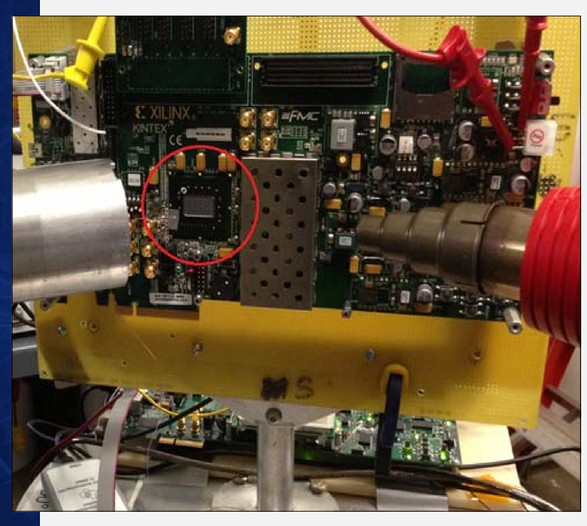
Gary Swift
Swift Engineering and Radiation Services, LLC

Anthony Le
Boeing

Abstract

This study examines the single-event response of the Xilinx 28 nm Kintex-7 FPGA irradiated with heavy ions. Results for single-event effects on configuration SRAM cells, user-accessible Flip-Flop cells, and BlockRAM™ memory are provided. This study also describes an unconventional single-event latch-up signature observed during testing.

Introduction



Test setup at Texas A&M Cyclotron. Illustrated is the Kintex-7 DUT (circled), beam output (left), and heat-gun utilized during SEL testing (right).

This study examines the single-event effects susceptibility of the Xilinx Kintex-7 Field-Programmable Gate Array. The Kintex-7 is the mid-range offering in the Xilinx Series-7 family of cutting edge FPGAs built on TSMC's 28 nm, high-κ metal gate process technology [1]. The purpose of this work is to determine the flight-worthiness and feasibility of utilizing these parts in space environments.

Device	Xilinx Kintex-7 XC7K325T
Package	FBG900C (flip-chip lidless, commercial)
Configuration	91,530,240 bits
Flip-Flops	407,600
BlockRAM™	16,404,480 bits
Slice Logic	50,950 (4 LUTs and 8 FFs per slice)
Other untested device features	10 clock management tiles, 1 PCI Express block, 16 Multi-Gigabit Transceiver blocks, 12-bit ADC, 840 DSP slices

Beam Parameters

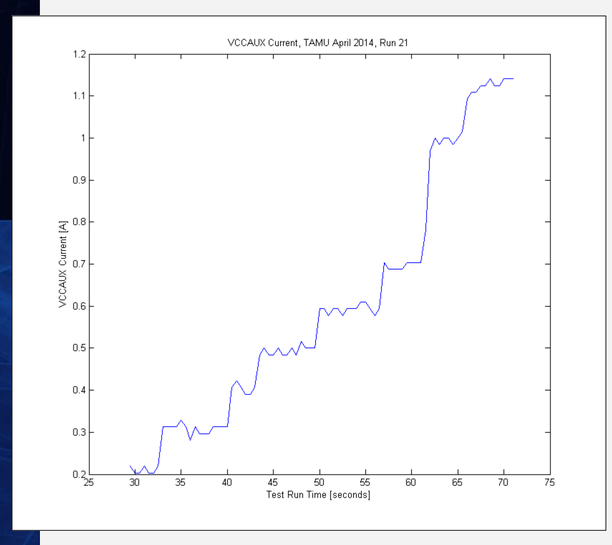
The device under test was irradiated with heavy ions at the Texas A&M University K500 Cyclotron and the Lawrence Berkeley National Laboratory 88-Inch Cyclotron. Testing utilized effective LETs from 1.5 to 126.1 MeV-cm2/mg.

Facility	TAMU	LBL	LBL	TAMU	LBL	TAMU	TAMU	TAMU	TAMU	LBL	LBL	TAMU	LBL	TAMU	LBL	TAMU	TAMU	TAMU
Effective LET	1.9	2.19	3.1	3.9*	4.38	6.3	6.9*	7.1*	8.8	9.7	13.8	24.2	30.9	32.9*	43.6	63.5	109.1	126.1
Initial LET	1.9	2.19	2.19	3.9	2.19	6.3	6.9	7.1	8.8	9.7	9.7	24.2	30.9	32.9	30.9	53.9	62.6	63.1
Angle	0	0	45	0	60	0	0	0	0	0	45	0	0	0	45	31.8	55	60

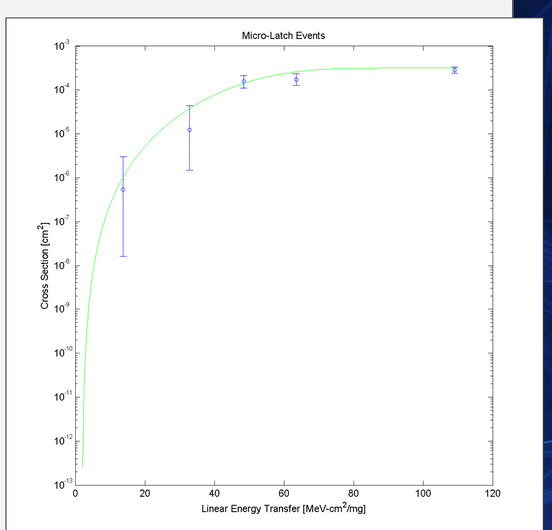
** = LET obtained through degrader*

Device SEL Results

- Numerous current-step anomalies attributed to single event latchup were observed on the VCCAUX supply (1.8 V) when testing at high LET, high temperature, and maximum biases.
- Current would increase in steps of 125 mA (σ_t=40 mA).
- Current events would not clear through configuration scrubbing nor through assertion of the device's reset (PROG) pin.
- Current events cleared through power cycle or by reducing voltage to 1.2 V then returning to 1.8 V (demonstrating the holding voltage signature of parasitic bipolar latch structures [2] and indicates this is not from upset-induced contention or single-event functionality mode changes).
- No observable damage or loss of functionality, but have not yet fully exercised all circuits tied to VCCAUX.
- Event cross-section worsens at higher temperature and high biases.
- Lower LET threshold for this event appears to be around 15 MeV-mg/cm^2.
- All other Kintex-7 voltage rails appear to be latchup-free.



Current step events identified during SEL testing. Typical VCCAUX current draw is 210±16 mA. This run shows seven (possibly eight) current step events.



Weibull curve for the current step event.

Event Rates

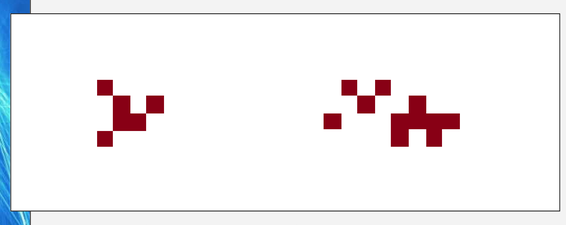
The event rates from CREME96 are listed below, assuming a GEO orbit, solar minimum conditions, and 100 mils of aluminum shielding:

	Configuration Memory	**User Flip-Flops**	**Flip-Flop Slice Resets**	**BlockRAM**	**Current-step SEL Events**
Per Bit	1.52E-8 / day	1.33E-8 / day	3.2E-8 / slice / day	2.81E-7 / day	N/A
Per Device	1.12 / day	5.42E-3 / day	1.63E-3 / day	4.62 / day	9.2E-5 / day

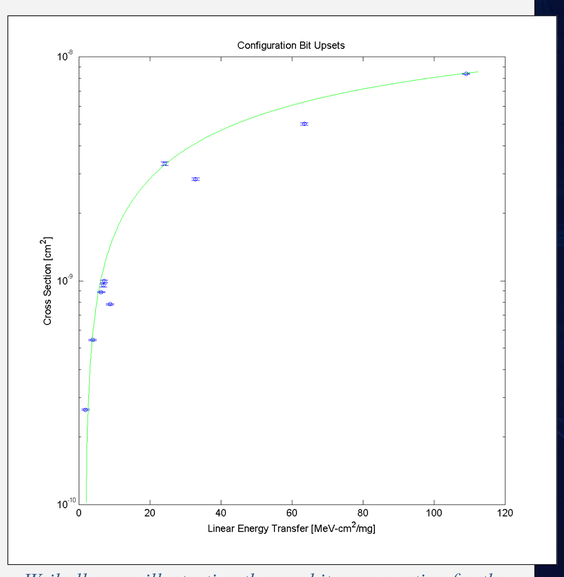
SEU Results

I. Configuration Memory Bits

- Static configuration memory test performed by configuring, irradiating, and then reading back the device.
- Comparisons are masked to only include bits pertinent to device operation and to exclude dynamic content (such as user flip-flop data).
- Multiple-bit SEU clusters in configuration words and adjacent logical addresses seem to indicate some physical interleaving of bits. An analysis of these multiple-bit events and their implication to inferring physical device layout is discussed in [3].



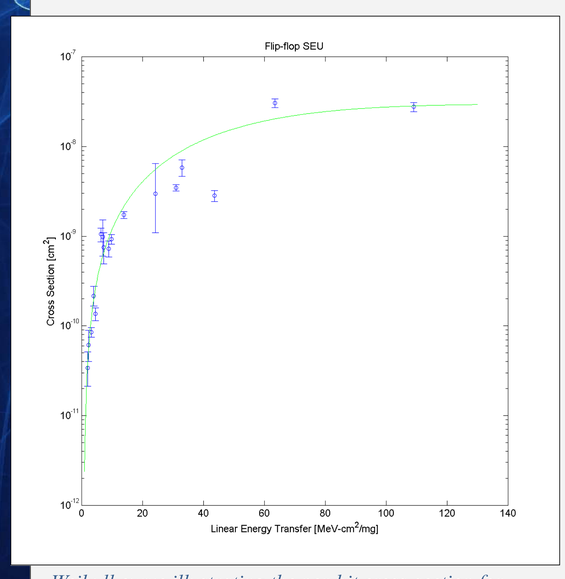
A pictorial representation of multiple-bit upset shapes. Configuration words are ordered into columns. Horizontally adjacent bits are in logically adjacent words.



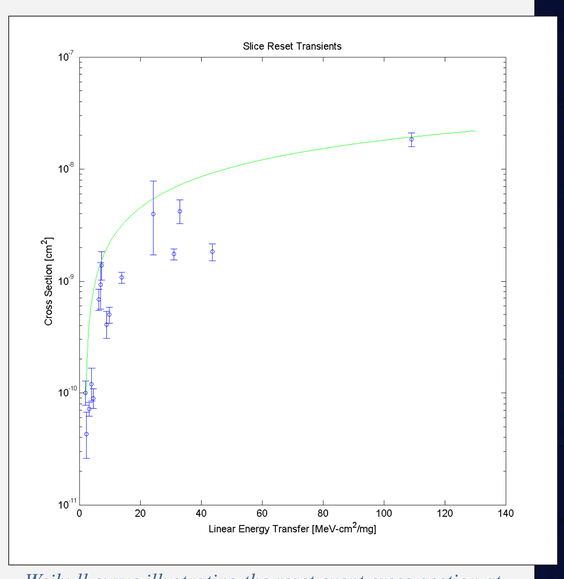
Weibull curve illustrating the per-bit cross-section for the configuration memory bits.

II. Flip-Flops

- Flip-flops tested through a test design containing several long flip-flop chains. Half of the chains were initialized to 1 and half were initialized to 0. Flip-flops were not clocked during irradiation.
- Resets were configured to either reset or preset the flip-flop to ensure that reset transients would always flip the value of the flip-flop opposite of its initialized value.
- Results indicated two error signatures: (1) a flip of a single flip-flop data value due to SEU or possibly by reset transient only affecting a single flip-flop; and (2) SET-induced reset that would travel down a physical FPGA column affecting anywhere from 1 to 42 slices (most often 1 or 2).
- Single value flips from SEU or single-cell resets were not biased to either 0- or 1-initialized flip-flops.
- Observed slice reset transients are especially important to note for designers, as this phenomenon could be particularly defeating to design mitigation strategies (most notably TMR).



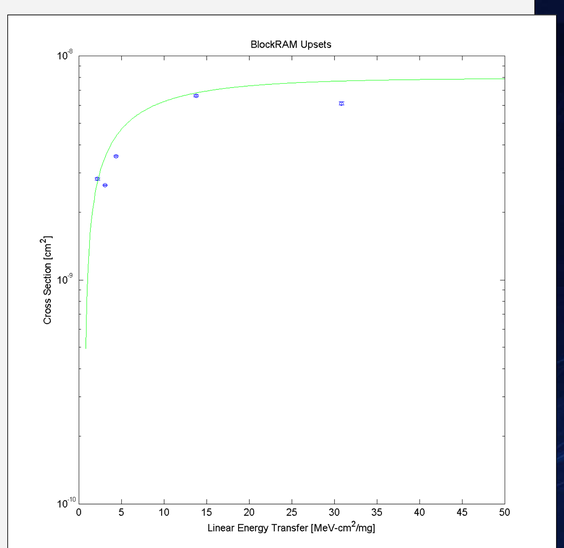
Weibull curve illustrating the per-bit cross-section for individual flip-flop upsets.



Weibull curve illustrating the reset event cross-section at the slice level.

III. BlockRAM™

- BlockRAM was tested by instantiating all of the available BlockRAM into test designs loaded into the Kintex-7, with some cells initialized to 1 and the others initialized to 0.
- BlockRAM was not exercised in the design or clocked during irradiation.
- Initial analysis indicates a bias in upsets weighted towards cells holding 1 values. Cells storing 1s were 5-6x more likely to upset than cells storing 0s. However, additional data is necessary for validation of this claim.



Weibull curve illustrating the overall average per-bit cross-section for individual BlockRAM bit upsets.

References

[1]7-Series FPGAs Overview (v1.14) [Online]. Available: http://www.xilinx.com/support/documentation/data_sheets/ds180_7Series_Overview.pdf, last accessed February 2, 2014.

[2] Hu, G. J.; Bruce, R. H., "A CMOS Structure with high latchup holding voltage," *IEEE Electron Device Letters,* vol.5, no.6, pp.211-214, Jun 1984.

[3] Wirthlin, M.; Lee, D.; Swift, G.; Quinn, H., "A Method and Case Study on Identifying Physically Adjacent Multi-Cell Up sets Using 28nm Interleaved and SECDED-Protected Arrays," submitted to *IEEE Transactions on Nuclear Science*, July 2014.

This work was supported by the Laboratory Directed Research and Development program at Sandia National Laboratories, a multi-program laboratory managed and operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Corporation, for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000 and by the I/UCRC Program of the National Science Foundation under Grant No. 0801876. Unclassified, unlimited release.