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A HV silicon vertical JFET: TCAD simulations

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Abstract

In the future ATLAS Inner Tracker detector (ITk), several silicon strip modules will be biased by a single High-Voltage (HV) line, so that a switch between each strip sensor and the HV line is required to disconnect faulty sensors. Such a switch must satisfy strict requirements, such as being radiation hard, being able to sustain high voltages in the OFF state and being able to operate in a high magnetic field. At Brookhaven National Laboratory we conceived a new kind of solid-state switch that can potentially meet all the specs: it is a HV silicon vertical JFET. Before designing and fabricating the JFET, we did a study using numerical TCAD simulations that demonstrate the feasibility of fabricating the device in a standard planar technology. We report such simulations, highlighting in particular a few key parameters to which the JFET performances are most sensitive.

Keywords: TCAD simulations, JFET, power devices, high voltage

1. Introduction

The ATLAS detector at the Large Hadron Collider (LHC) will undergo multiple upgrades to improve detector performance to prepare for the LHC's transition to the High Luminosity LHC (HL-LHC). One of the main upgrades is the replacement of the current tracker with an all-silicon inner tracker (ITk) [1]. The outer part of the ITk consists of silicon strip detectors mounted on carbon composite structures that provide mechanical support, cooling, and electrical services to groups of sensors. Due to lack of space, groups of sensors will need to share the same High Voltage (HV) bias line. Consequently, the failure of a single sensor due to its developing a short or going into breakdown will result in the loss of operation of the other sensors sharing the same HV bias. It is desirable to have a remote-controlled switch on each sensor's HV line that could be opened to isolate a failed sensor from the common HV bus and allow continued operation of the working sensors on that bus.

An R&D program called HV Mux was initiated by Brookhaven National Laboratory (BNL) to find a high voltage switch that could operate above the 500V sensor bias, operate in a 2T magnetic field, and survive radiation doses of 50 Mrad and fluences of $1.2 \cdot 10^{15} n_{eq}/cm^2$ [2]. The switch is the key component of an HV Mux circuit made of additional discrete components driven by a custom ASIC, all of which are mounted on a kapton circuit board epoxied to each silicon sensor. Commercial transistors fabricated in wide bandgap materials such as silicon carbide and gallium nitride have been investigated. Additionally, BNL has collaborated on a

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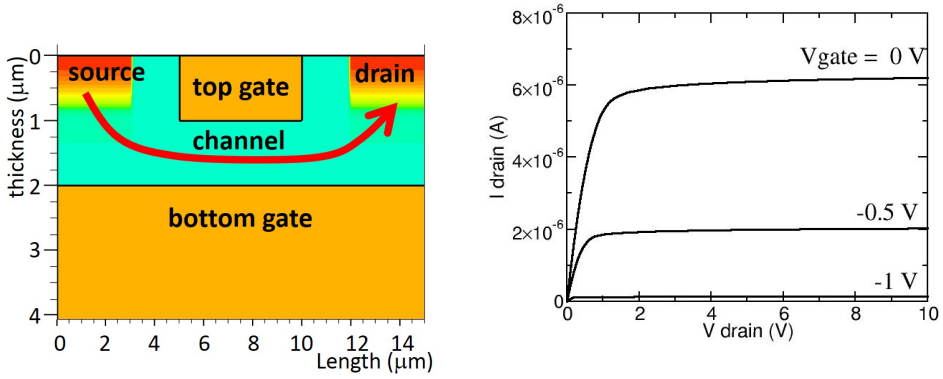

Figure 1: Geometry of the simulated standard JFET (the red arrow shows the path of the electrons of the source-to-drain current), and its output characteristics (referring to a $1-\mu m$ wide structure).

custom silicon vertical JFET using 3D trench technology [3]. Prototypes have been fabricated by CNM (Barcelona, Spain) [4].

Here we report on the design of a custom vertical JFET for HV Mux that is fabricated using only planar silicon technology and therefore promises to be simpler and cheaper to fabricate than the 3D Trench JFET. The emphasis in this paper is on the TCAD simulations which guided the JFET design. In Section 2, the geometry of the device is presented and compared with the standard JFET by using an oversimplified structure for both JFETs. In Section 3, the effect of various parameters is described, and finally in Section 4 the feasibility in the planar process is described.

2. STANDARD JFET VS VERTICAL JFET

The standard silicon JFET is an elementary solid-state device, whose theoretical treatment can be found in any textbook on silicon devices (for example [5], chapter 6). For the sake of comparison with the HV vertical JFET that we are going to discuss, we simulated an oversimplified structure. Fig.1 shows the two-dimensional geometry of the standard JFET. The top and bottom gates, which in this particular simulation are shorted together (JFET in triode configuration), are uniformly doped with an acceptor concentration of $10^{18} cm^{-3}$ (in the following, we consider n-type JFETs only). The channel is n-doped with a donor concentration of $10^{16} cm^{-3}$; it makes then step junctions with the two gates. The channel length is 5μm, which is the length of the overlapping of the two gates, while the channel thickness is 1μm. The source and the drain sit close to the channel ends. The output characteristics of such a device, i.e. the drain currents as a function of the drain voltage, for different values of the gate voltage, are shown in Fig. 1.

Fig. 2 shows the two-dimensional geometry of the proposed HV vertical JFET. At the surface of the device, as in the case of the regular JFET, there are the source and the top gate. Again, as in the case of the regular JFET, the channel runs over all the length of the surface. The drain contact, instead, sits on the opposite side of the wafer. The distance between the surface and the drain is set by the wafer thickness, or by the thickness of the epitaxial layer. The bottom gate features an interruption in its implant to allow the source-to-drain current to flow through it,

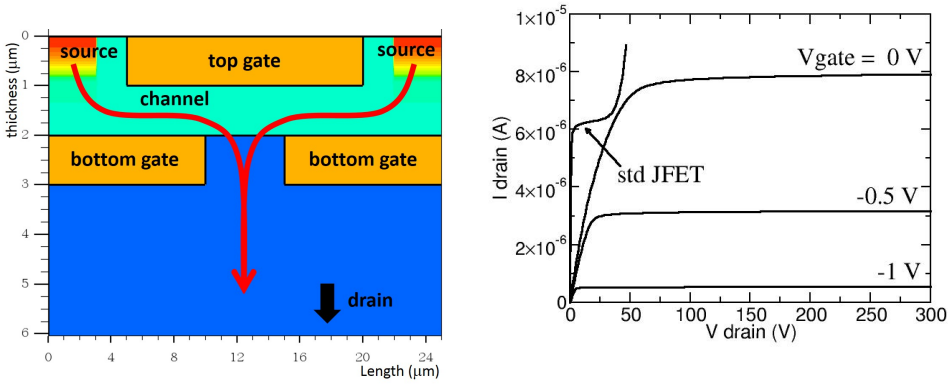

Figure 2: Left, geometry of the simulated 2D HV-JFET (the red arrow shows the path of the electrons of the source-to-drain current). From $Y = 2\mu m$ downward, the current flows in a medium- or high-resistivity epitaxial layer. Right, output characteristics (referring to a $1-\mu m$ wide structure). Also shown for comparison, the standard JFET current for $V_{gate} = 0$, as in Fig. 1, which shows a breakdown at 40V.

between these two terminals. The top gate overlaps with the bottom gate by the channel length, in this case $5\mu m$ to ease the comparison with the standard JFET of Fig. 1. The top gate covers also the gap in the bottom gate.

To increase the channel width (and thus the source-to-drain current and the transconductance), standard JFETs usually adopt an interdigitated geometry, where wide parallel source and drain electrodes alternate themselves in a linear array (with the top gate separating them). In the vertical JFET, top gate electrodes alternate only with source electrodes, the drain being the uniform electrode on the back. In the structure of Fig. 2, which will be in the following our reference geometry for the HV-JFET, to ease the comparison with the JFET of Fig. 1, the channel parameters are the same, i.e. the donor doping concentration N_C is $10^{16} cm^{-3}$, the thickness X_C is 1μm and the length 5μm. The acceptor doping concentration of both gates (again short-circuited during the simulations) is $10^{18} cm^{-3}$. The device of Fig. 2 is symmetric with respect to a vertical axis passing through mid top gate and, since in TCAD simulations Neumann's boundary conditions apply, only half of the geometry needs to be simulated. Fig. 2 shows the simulated output characteristics of this half device. As can be seen, the magnitude of drain currents in saturation is comparable to the standard JFET, given the same V_{gate}. Before irradiation the total sensor current will be typically less than $1\mu A$ with a full depletion voltage specified to be less than 300V. The curves show that this device, which is however just an oversimplification, is perfectly able to handle the pre-irradiation requirements on the voltage and on the current. We comment about the post-irradiation requirements at the end of this section.

The turn-off voltage, defined as the gate voltage which fully depletes the channel close to the source end, is given analytically by the equation ([6], page 250):

$$V_{turn-off} = -V_{bi} + \frac{q}{8\varepsilon_{Si}} N_C X_C^2$$

where V_{bi} is the built-in voltage of the gate/channel junction. $V_{turn-off}$ in the HV JFET is the same as in the regular JFET (about 2V), since the dimensions and the doping of the channel and the gates are the same for both simulated devices.

The parameter, as extracted from these curves, that is very different between the two types of devices is the drain voltage required for the onset of saturation, $V_{D,sat}$. In fact, due to the small dimension of the gap, the bottom gate is very effective in shielding the drain voltage: a much larger drain voltage must be applied so that the channel gets the sufficient bias at its end to deplete the channel itself. However, this structure can sustain very large drain voltages, because the full $V_{gate} - V_{drain}$ voltage difference falls in the high or medium resistivity substrate, as happens in the case of a 1-dimensional PIN diode. For comparison, the regular JFET breaks down at about 40V, due to the proximity of the gate and drain terminals. The breakdown voltage of the bottom gate/drain junction is strongly dependent on the doping concentration and thickness of the epitaxial layer, as happens in a regular PIN diode [7]. Also, a guard ring termination structure must be carefully designed, externally to the bottom gate, to prevent the development of high electric fields at the Si/SiO_2 interface. This termination must sustain at least the foreseen operating voltage between the gate and the drain (this topic is outside of the scope of the present paper).

Another difference is the amount of the gate leakage current. As the depletion region extends into the substrate, a leakage current will be generated in this volume. This current flows between the drain and the gate and, for geometrical reasons, is much higher than in the standard JFET.

In Fig. 3 a, the electrostatic potential in the bulk, a few microns from the Si/SiO_2 interface, is plotted in the case of $V_{gate} = -0.5V$ and $V_{drain} = 100V$. The potential distribution within the channel is very similar to the one expected in the regular JFET in saturation for the same V_{gate}; in fact the currents are almost the same. Despite the high voltage applied to the drain, the bottom gate prevents the high voltage from penetrating the gap and limits the maximum voltage in this region to only about 6V. The electron current that flows in the channel is shown in Fig. 3 b. It flows from source to drain without encountering any potential barrier along its path and along the maximum gradient of the electrostatic potential.

In Fig. 4, for the same bias point of Fig. 3, the equipotential lines in the bulk are shown. In these simulations, the bulk is an n-type epitaxial layer $50\mu m$ thick (doping concentration of $10^{14}cm^{-3}$, so the depletion voltage is 200V). The simulation has been done below the depletion voltage with $V_{drain} = 100V$. Nevertheless, the substrate is slightly depleted by the current flow, which creates a voltage drop in the resistive substrate. Note how the current spreads laterally.

This new device potentially satisfies the conditions required (or preferred) for HV Mux:

- a voltage larger than 500V can be sustained by the bottom gate/drain junction, once the substrate doping concentration and thickness are optimized. High-resistivity thick substrates are preferred ([7], chapter 2);
- as a thin semiconductor device, it can be operated in magnetic fields;
- it is normally ON;
- the turn-off voltage can be adjusted to be $|V_{gs}| \lesssim 3V$;

While JFETs are known to be resistant to a large extent to ionization damage [8], tolerance to displacement damage can be an issue. The radiation damage increases

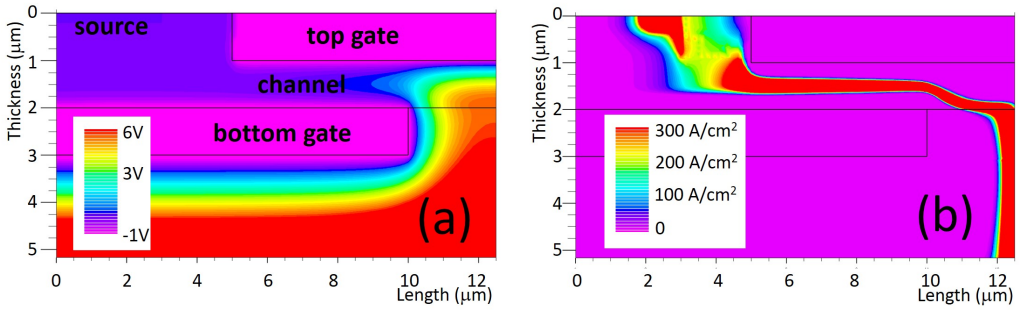

Figure 3: (a) Equipotential lines for an applied bias of $V_{drain} = 100V$, source at zero, gate at -0.5V, red color is +6V, blue is 0V. (b), electron current density. The plots are zooms of the first 5 μm from the Si/SiO_2 interface.

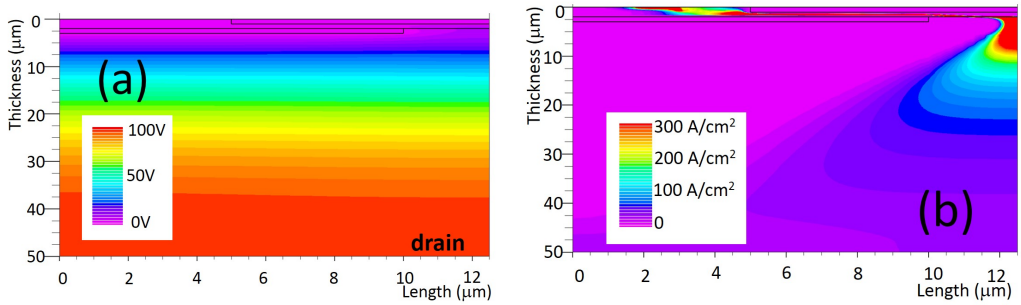

Figure 4: (a) Equipotential lines in the bulk of the vertical JFET for an applied bias of $V_{drain} = 100V$, source at zero, gate at -0.5V. (b), electron current density.

the effective ohmic resistance of the undepleted substrate in the ON state, with the net result that, for the same V_{ds} and V_{gs}, a lower current flows. To mitigate this issue, larger devices, made by very wide sources, should be chosen by design. Also, low resistivity thin substrates would be preferable, but would lead to lower breakdown voltages as opposed to the 500V requirement above. On the other hand, larger devices lead to higher gate currents after irradiation in the OFF state. In fact, if before irradiation the gate leakage current is negligible, during irradiation the gate current scales up with the fluence and the depleted volume below the bottom gate.

To check if this device can sustain the maximum expected fluence of $1.2{\cdot}10^{15} n_{eq}/cm^2$, TCAD simulations have been run inserting the radiation-generated traps according to the "Perugia model" [9]. We used again the structure of Figure 2, which refers to a device $1\mu m$ wide (the width is the dimension into the paper). From the results, a source-to-drain current of $10nA$ has been obtained at $V_{gate} = 0V$ (i.e. ON state), a 10^3 decrease with respect to the pre-irradiation simulations. Since after irradiation, the total sensor current is expected to be 1 mA, a device width of $1mA/(10nA/\mu m) = 10cm$ is therefore needed. Considering that the device in Figure 2 is $25\mu m$ long, 40 of them can be parallelized in an interdigitated configuration to fit in a length of $1mm$. In a $1 \cdot 1mm^2$ area, thus, a $40 \cdot 10^3 \mu m = 4cm$ wide device can fit and, accordingly, a $10 - cm$ wide vertical JFET can be as small as $2.5mm^2$.

The post-fluence gate leakage current will be $7.5\mu A$, considering a depleted volume of $50\mu m \cdot 2.5mm^2$ and a damage constant of $5 \cdot 10^{-17} A/cm$ [9], as confirmed by the same TCAD numerical simulations. These numbers are within the specifications.

3. EFFECT OF GAP DIMENSION AND CHANNEL DOPING

One important feature in the design of the HV-JFET is the dimension of the gap in the bottom gate, covered by the top gate, through which the source-to-drain current flows. We simulated the output characteristics of a few structures that differ from the reference geometry in Fig. 2 just by the gap length (10 or 15 μm instead of 5 μm). We verified that the saturation current for a given gate voltage is the same. This indicates that the potential distribution inside the channel, which governs that amount of current flowing through the channel, is unaffected by the gap dimension. Therefore, the turn-off voltage remains the same. The saturation voltage $V_{D,sat}$, however, depends on the gap dimension as shown in Fig. 5. Larger gaps result in lower $V_{D,sat}$ since the drain voltage is less effectively shielded by the bottom gate and thus more strongly influences the channel potential. Making the gap longer introduces an unwanted effect: there is an increase in the peak electric field at the top gate/channel junction at mid-gap, which can potentially lead to breakdowns. Here, higher electric fields develop because the channel sees a large voltage under the gap. As can be seen in Figure 6, the larger the gap, the greater is the electric field. However, the magnitude of the electric field in this region is almost impossible to calculate analytically and must be numerically simulated.

Increasing the channel doping results in higher turn-off voltages and higher electric fields at the top gate/channel junction (a shown in Figure 6), which limits the maximum operating drain voltage that avoids breakdown. However, it is interesting to notice how the output characteristics modify under an increase of the doping concentration of the channel, while keeping all the other parameters fixed as in Fig. 2 (so, the gap length is again $5\mu m$). In the case of a doping of $3 \cdot 10^{16} cm^{-3}$, as in Fig. 7, for $V_{gate} = 0$, the device reaches the saturation regime for drain voltages much larger than 1kV, since the channel does not reach the necessary voltage to pinch off the channel. For higher gate voltages, the drain current can reach saturation, although at very high voltages. For example, at $V_{gate} = -1V$, $V_{D,sat} = 1000$V. The output characteristics of a few vertical JFET structures have been simulated, which differ only for the doping of the channel, while keeping the gap dimension at $5\mu m$, as in Fig. 2. The $V_{D,sat}$ extracted from these curves is reported in Fig. 7: as can be seen, it is a strong function of the channel doping. In the HV-Mux application, when in the ON state, the device does not need to operate in saturation, provided the current capacity is high enough in the linear region. However, the V_{DS} must be minimized to reduce the power dissipation within the HV-JFET.

4. SITUATION IN A REAL DEVICE

The device structure of the reference geometry is clearly an oversimplification of a real device. Its aim was to help in determining the device performances and the main parameters that govern the behavior of the device. During an actual fabrication, an approximation of this geometry can be obtained if we follow a process flow as sketched in Fig. 8, left column, which is like the one described in [10]. Here, over the thickness of the substrate (which can be an epitaxial layer), a bottom gate implant is first performed (Fig. 8 a) and then a second thin epitaxial layer is grown (Fig. 8 b). This epitaxial layer, if properly doped, can act as the channel of the JFET; however in this case it will extend also externally to the bottom gate and potentially cause problems in the guard ring termination. A possible alternative is to grow an epitaxial

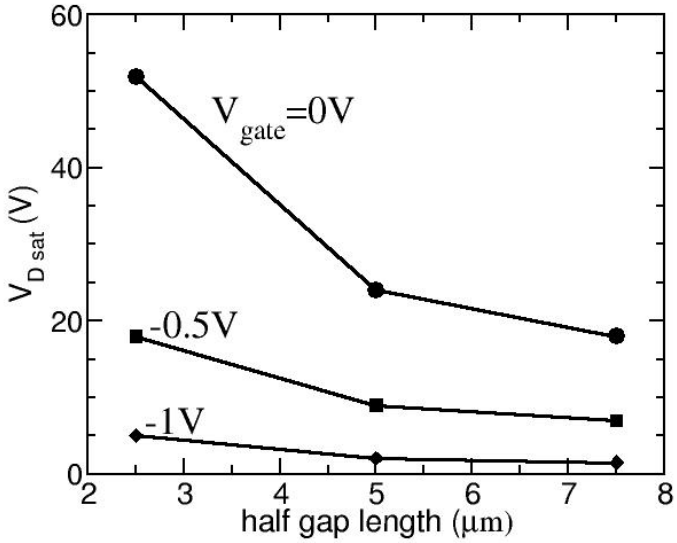

Figure 5: $V_{D,sat}$ as a function of the (half) aperture in the bottom gate, for different gate voltages.

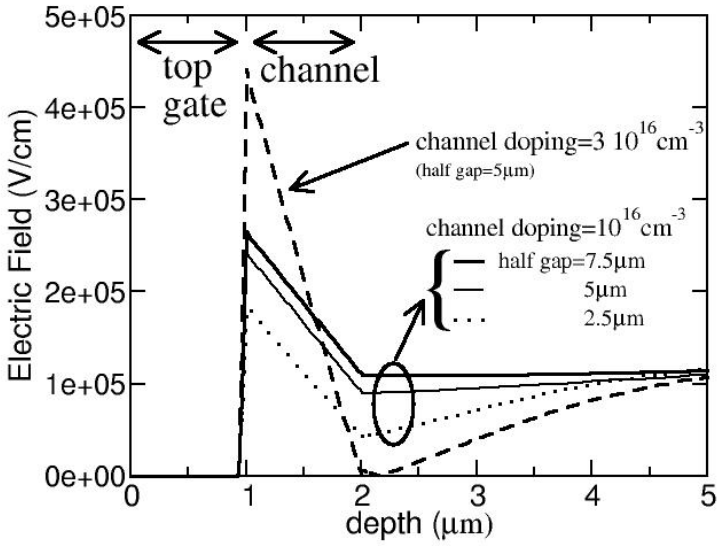

Figure 6: Vertical cutlines of the electric field at mid gap in the OFF state, for structures differing for the gap length or the channel doping. In all cases, $V_{drain} = 500V$, while $V_{gate} = -2V$ for the channel doping of $10^{16}cm^{-3}$, and $V_{gate} = -6V$ for the channel doping of $3 \cdot 10^{16}cm^{-3}$.

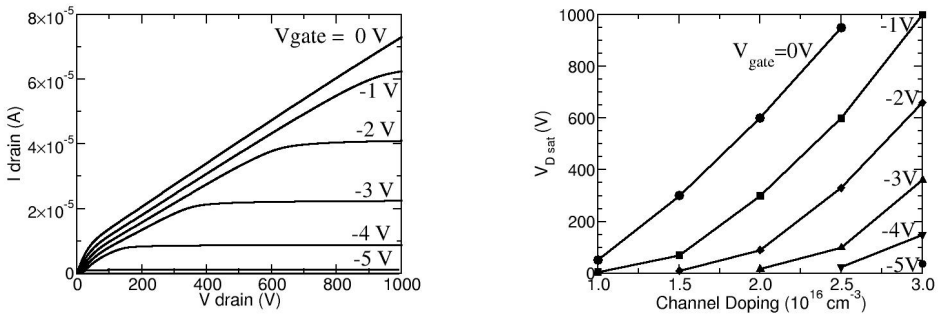

Figure 7: Left: output characteristic of a HV JFET with channel concentration of $3 \cdot 10^{16} cm^{-3}$, instead of $1 \cdot 10^{16} cm^{-3}$, as in the structure of Fig. 2. Right: $V_{D,sat}$ as a function of the channel doping concentration, for different values of the gate voltages.

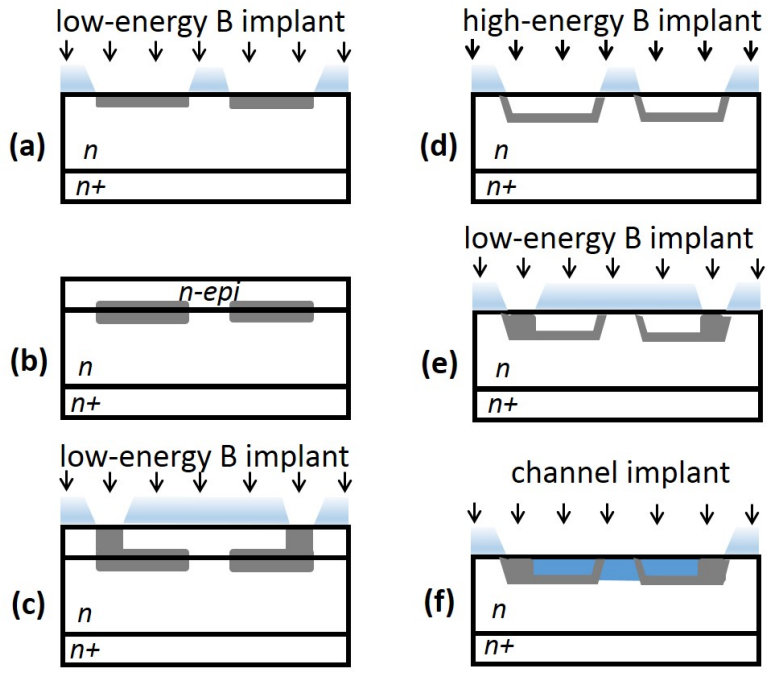

Figure 8: On the left, process flow using an additional epitaxial layer growth which can avoid the horn effect: (a) a low energy boron implantation (in the case of an n-type JFET) is performed, the pattern being defined using a standard photoresist, (b) an additional epitaxial layer is grown on the top, and the implant is diffused, (c) another boron implant connects the deep boron implant to the surface, for metal connection. The other implants (source, channel and top gate) are within this well. Right, process flow using only ion-implantations: (d) high-energy boron implant, suffering from horn effect, (e) the same implant as in c) may be needed, (f) the channel implant must be high enough for it not to be compensated by the bottom gate implant.

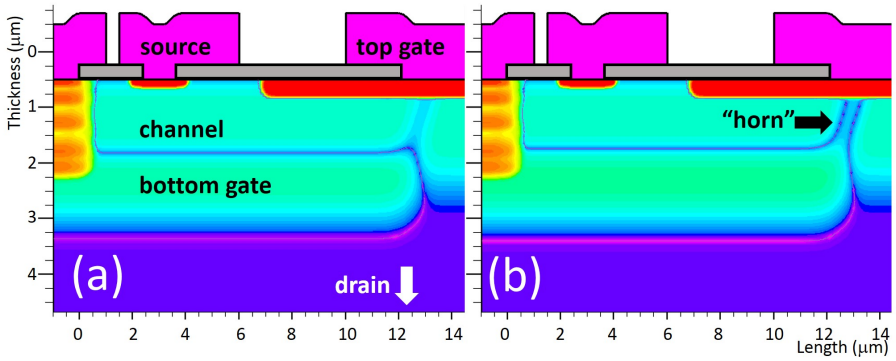

Figure 9: Simulations of possible structures fabricated in a single-epitaxial layer planar process. A "horn" appears, when the bottom gate implant, which goes through the oxide/resist stack at the edge of the gap, compensates for the channel doping. In (a) bottom gate dose is $1.2 \cdot 10^{12} cm^{-2}$, in (b) bottom gate dose is $1.4 \cdot 10^{12} cm^{-2}$.

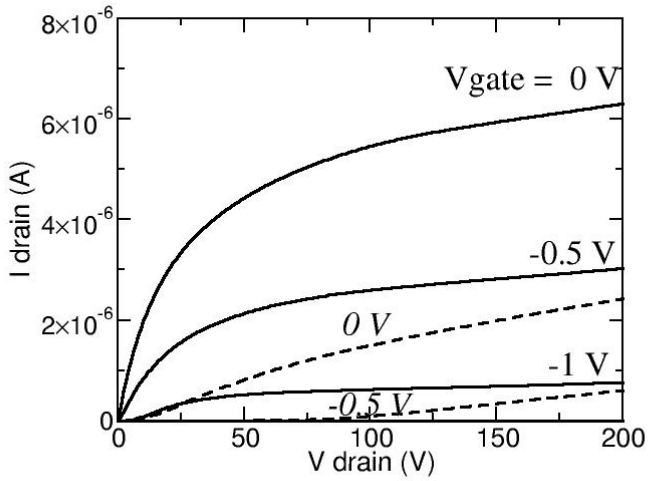

Figure 10: Output characteristic of the HV JFETs of Figure 8: solid (respectively dashed) lines refer to the structure in Fig. 9 a (respectively b).

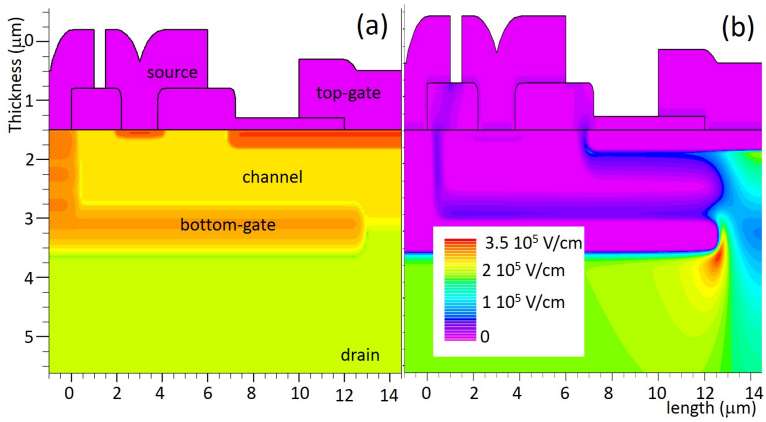

Figure 11: for the geometry shown in (a), (b) shows the electric field at breakdown, in this case at $V_D = 850V$.

layer as doped as the substrate and to implant on it the channel. On this additional thin epitaxial layer, the other implants, such as the top gate and the source, can be then implanted and diffused. It may be necessary to implant also a boron layer to ohmically connect the bottom gate at the surface (Fig. 8 c). If we are limited by process capability to use just a single epilayer planar process, this ideal situation is not achievable. In this case, the starting point will be the epitaxial layer (or the high-resistivity wafer) in which the bottom gate is implanted first (Fig. 8 d), by means of a high energy ion beam. Since in the region of the gap there are a thick oxide and a photoresist to prevent the bottom gate high-energy implant to go through, we suffer from a "horn effect" at the edge of this region, where some of the bottom gate implant gradually passes through the stack and finally reaches the silicon/oxide interface. The term "horn" has been introduced in [10], where a description of this effect is detailed. The acceptors introduced by this implant (boron) can compensate for the donors of the channel implant (phosphorus) and block (or limit) the source-to-drain current (Fig. 8 f). As a consequence, the implanted dose of the bottom gate must not be too high with respect to the implanted dose of the channel. For example, in Fig. 9, the problem is depicted. Here the channel is as in Fig. 2 ($1\mu m$ thick and $10^{16}cm^{-3}$ doped, simulating a net implanted dose of $10^{12}cm^{-2}$). Fig. 9 a shows the case when the bottom gate has been implanted with a boron dose of $1.2 \cdot 10^{12}cm^{-2}$, and a horn is visible, connecting the edge of the bottom gate to the surface. Still it is not enough to compensate the n-type channel. Fig. 9 b shows the case in which a dose of $1.4 \cdot 10^{12}cm^{-2}$ is implanted, which is slightly larger than the case in Fig. 9 a: in this situation the horn compensates for the channel doping, resulting in a parasitic junction between channel and bottom gate.

The effect of the presence of the horn on the I-Vs of the output characteristics is striking (Fig. 10). A horn which is unable to compensate for the channel doping does not affect the current, which is the same as in Fig. 3 (in fact the horn is in a region where the currents already experience a drift toward the drain). On the other hand, a horn which compensates for the channel doping severely decreases the amount of current and lowers the turn-off voltage as well. The horn effect, thus, must be avoided in an actual fabrication. Since the doping of the horn is not controllable, it is advisable to process in parallel a few wafers differing for the channel dose to have at least one functional wafer among them.

The channel doping is constrained by the requirements to have reasonably low turn-off voltages, and to avoid high electric fields below the top gate. This constrains the doping of the bottom gate (as to avoid the horn effect), which can be so low as to result in a non-negligible depletion of the bottom gate implant, as large drain voltages are applied to the JFET. This is especially severe when the resistivity of the epitaxial layer is not high. For example, an epitaxial thickness of 50 μm with a donor doping of $10^{14}cm^{-3}$ (as the one used in the simulations) has an integrated dose of $5 \cdot 10^{11}cm^{-2}$, about half of the bottom gate dose. This fact can also limit the maximum voltage that can be applied to the drain. These considerations show that the parameter space that can be chosen for a fabrication is limited but, as demonstrated by the TCAD simulations reported in Fig.9, it is still wide enough to assure a functional production.

We expect differences between the breakdown voltage in a simple PIN diode and in HV vertical JFET. In a regular PIN diode, the highest electric fields develop at the junction of the p shallow implant with the substrate, where the curvature

of the shallow implant is smaller. In the vertical JFET, there are two additional critical regions: the gap end, where the curvature of the bottom gate implant may be small, and in the middle of the gap, at the channel/top gate junction. So, lower breakdown voltages as compared to the PIN diode are expected in the vertical JFET. As an example, in Fig. 11b the electric field at the breakdown is shown for the sample geometry of Fig. 11a. For this particular geometry, TCAD simulations give $V_{drain,BD} = 850V$. In this case, the highest fields develop at the gap border, while at the mid-gap the electric field increases with the gap length.

5. CONCLUSIONS

We have presented TCAD simulations of a new silicon device, a vertical silicon High-Voltage JFET, initially conceived as a switch for silicon strip sensors. With respect to a standard JFET device, it can have the same turn-off voltage, the same ON currents, but can sustain much higher drain voltages. Many parameters must be optimized according to the specific application, such as gap length, channel doping, substrate thickness and doping. Moreover, if a fabrication must be done using a single-epitaxial layer planar process, many parameters are intercorrelated, and additional care is needed in optimizing within that parameter space. In fact, at BNL we did fabricate working prototypes of both n-type and p-type HV vertical JFETs using the planar process only: the adopted fabrication technology as well as the measurement results will be detailed in a future paper.

6. Acknowledgements

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