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Planar MultiLayer Fabrication of Josephson Junctions (Nb/TaN/Nb & Nb/NbSi/Nb)

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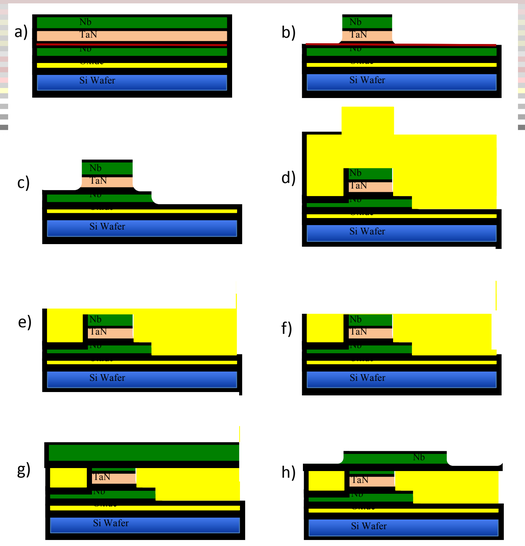
Motivation

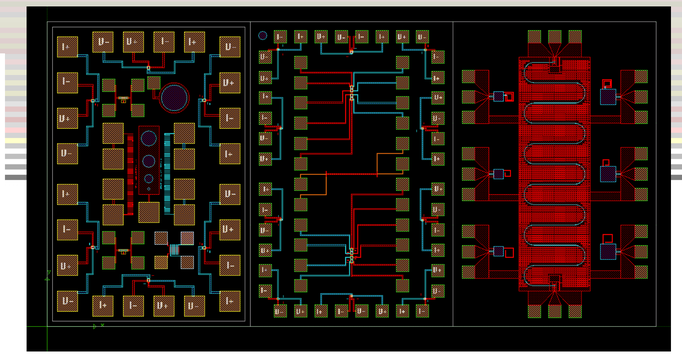
- This work establishes technology for a multilayer, planar process for self shunted Josephson junction technology with production considerations to move from a μfab to a 200 mm, 200 nm node in a CMOS production fab.
  - CMP (chemical mechanical polish) and plasma etch chemistry were matched to CMOS tools.
- Demonstrated here, we show a 150 mm wafer level process where junction technology can be switched in-situ.
- By having a high temperature 250 C IMD (inter-metal dielectric) deposition, a direct route for different junction technologies at different layers is achievable.

Fabrication Approach

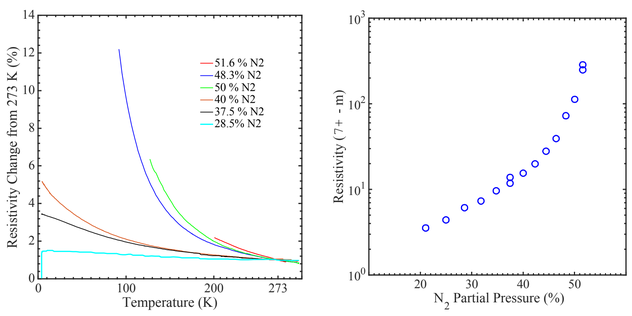
- Utilize a Nb deposition which has demonstrated to have terminal oxidation of ~ 5 nm after 2 years in atmosphere. TaN stoichiometry is controlled to establish different junction IcRn's.
- Deposition of M1 and junction layer is performed continuously in the same tool to protect junction layers (Nb 2000A/ Al 50A/ Nb 500A/ TaN 100-200A / Nb 2500A). This process is repeated to create M2 and higher. The TaN layer is skipped for all Nb vias.



Fab Sequence



Recticle Layout



Sputtered TaN Stoichiometry

Fabrication Details

Nb, TaN, NbSi, Al deposition done in a Denton Discovery 550 at room temperature

- Nb: 225 W DC, Ar 22.5 sccm, 4.8mT pressure – 8.4 K Tc (MPMS)
- TaN : 250 W DC, Ar 15 sccm, N_2 5-15 sccm – < 8 sccm demonstrated Tc

Plasma etch performed in Plasma Therm VersaLine ICP RIE (13.56 MHz)

- Junction etch: SF_6/C_4F_8/Ar 50/90/5 sccm, ICP/Bias 900/14 W, 15.8 mT
- Metal Layer etch: Cl_2/BCl_3 30/12 sccm, ICP/Bias 1000/20 W, 1.5 mT
- Ar Mill: Ar 25 sccm, Bias 400W, 10 mT

CMP: IPEC 472 soft membrane carrier modified – using a colloidal silica slurry & ammonium hydroxide based clean

References

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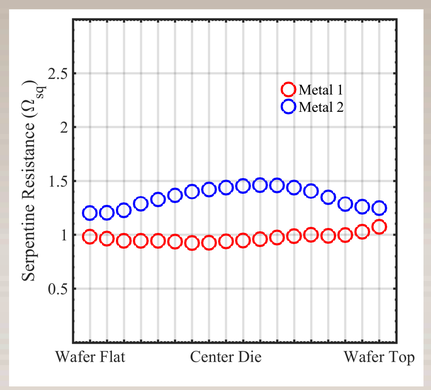
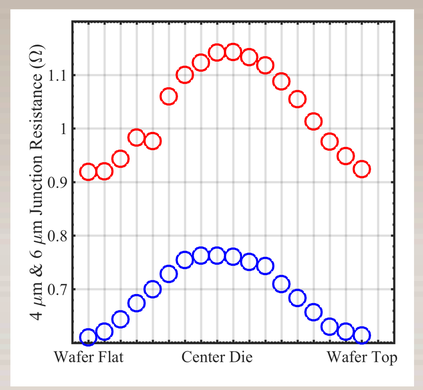
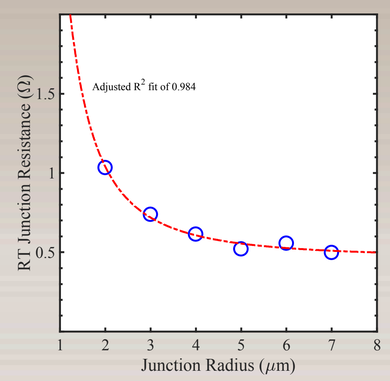
Nb/TaN/Nb Electrical Measurements

I. Room Temperature & Cryogenic Measurements

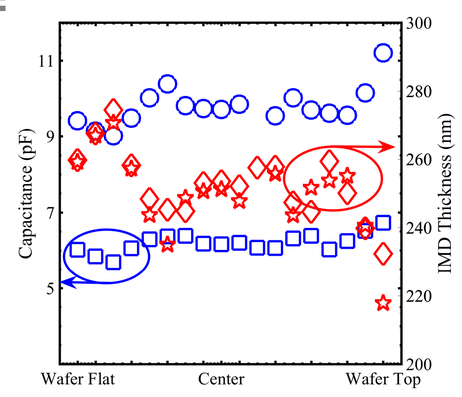
- Electrical I-V measurements over 18 die across the center of the wafer of M1, M2 and the 4 and 6 μm junctions yield insight to deposition uniformity (both in thickness and in stoichiometry). C-V measurements of the IMD suggest CMP uniformity and dielectric quality.

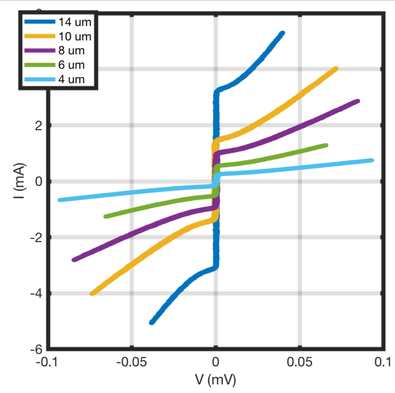






- M1 suggests a deposition uniformity (non reactive sputtering) of 6.5%.
- The 4/6 μm RT junction uniformity is ~ 19.5%. With M1 suggesting 6.5% uniformity, the likely culprit is the reactive sputtering of TaN.
- RT junction resistance measurements suggest a good fit to R~1/radius².
- Capacitance measurements suggests that after the CMP and Ar mill, the IMD thickness was about 250 nm with 13% thickness uniformity.

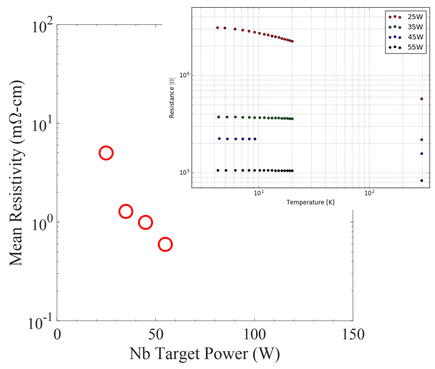


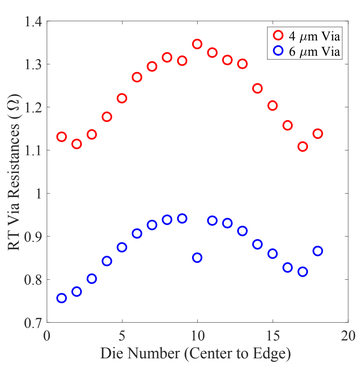


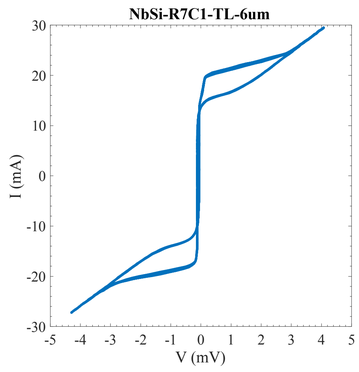
Demonstration of Nb/NbSi/Nb Electrical Measurements

I. Room Temperature & Cryogenic Measurements

- Using a Nb & Si co-sputtering, the Nb target power was varied to control NbSi stoichiometry.
- This wafer's fabrication then utilized the same fabrication sequence as above to create the TaN junctions.







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