

Design & Control Methodology for Improved Operation of a HV Bipolar Hybrid Switched Capacitor Converter

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We will address...

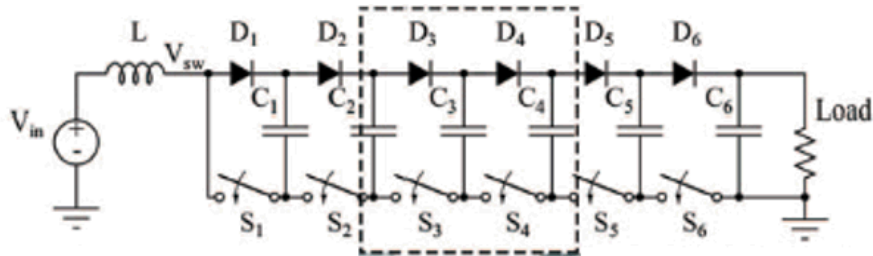
- Motivation and previous work
- Proposed HSCC topology
- Analytical and hardware results
- Future work

What Has Been Done and Why?

A Wide Application Space is Possible

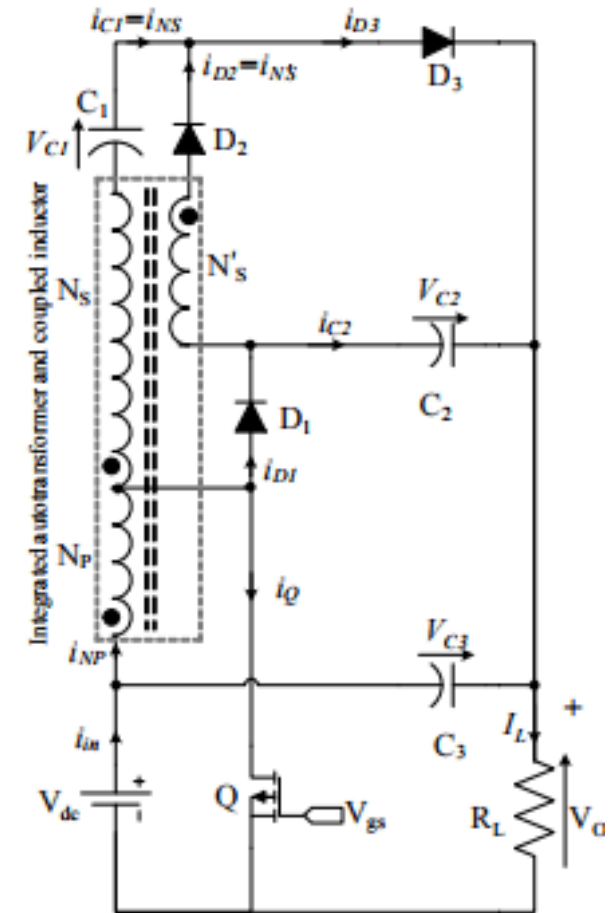
- MVDC grid connection for renewable resources
 - Solar PV
 - Wind
- Military
 - Naval electric ship
 - Pulsed power systems
- Other high gain DC systems

Let's Consider Prior Approaches to Achieve Higher Gain



Six-stage voltage multiplier with 6 active switches [1]

- Various capacitor-diode voltage multiplier circuits have been built demonstrating high gain
- Converters were limited to several hundred volts or low switching frequency



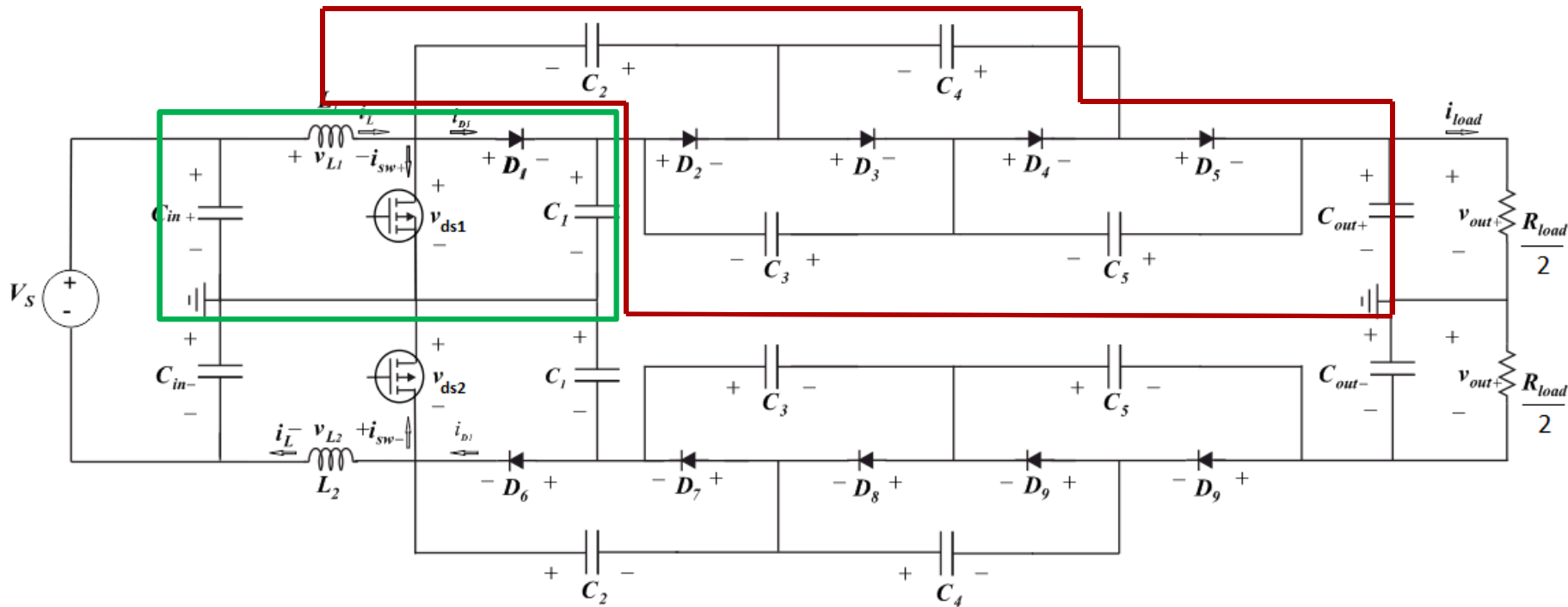
Voltage multiplier with autotransformer and coupled inductor[2]

[1] W. Chen, A. Q. Huang, C. Li, G. Wang and W. Gu, "Analysis and Comparison of Medium Voltage High Power DC/DC Converters for Offshore Wind Energy Systems," in *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 2014-2023, April 2013.

[2] Y. P. Siwakoti, F. Blaabjerg and P. C. Loh, "Ultra-step-up DC-DC converter with integrated autotransformer and coupled inductor," 2016 *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, 2016, pp. 1872-1877.

Proposed Hybrid Switched Capacitor Circuit

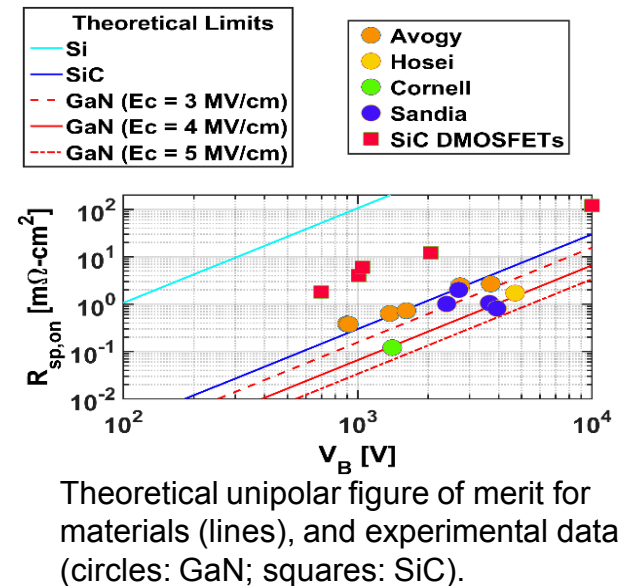
The Hybrid Circuit Utilizes Charge Pump for Additional Gain



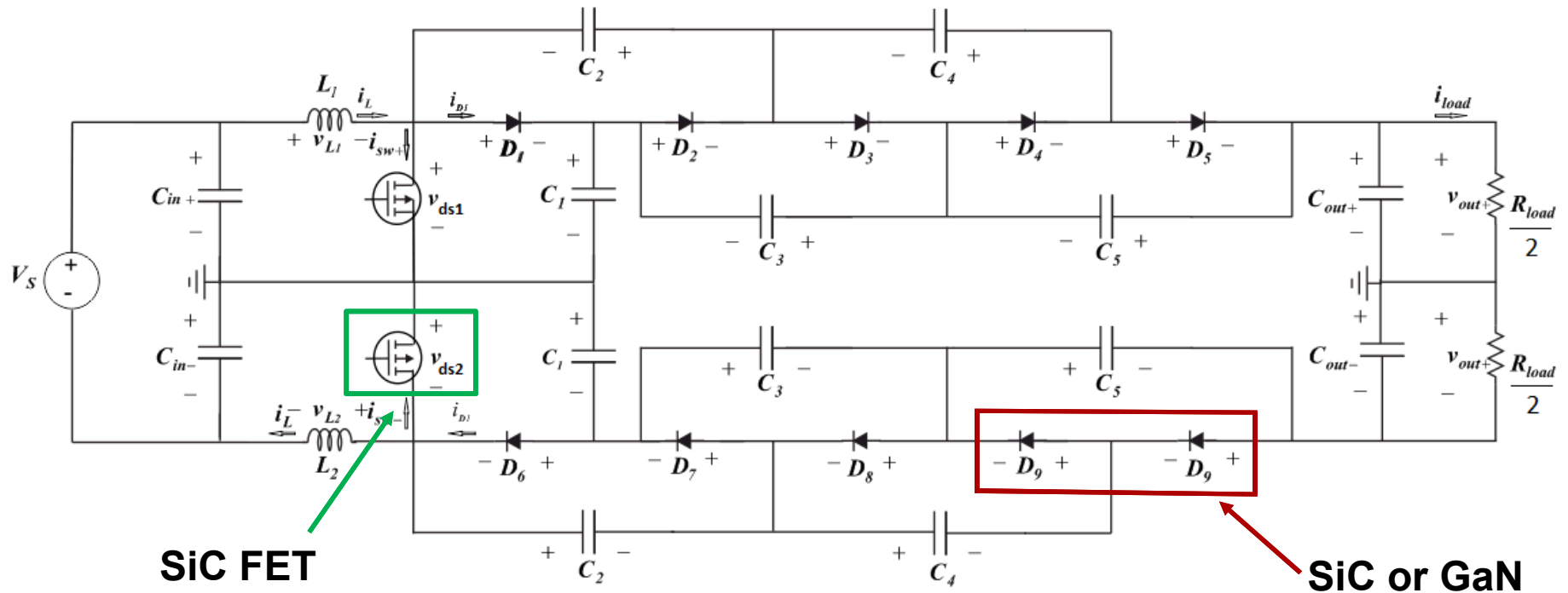
- The hybrid switched capacitor circuit (HSCC) is a traditional boost on the input side using the inductor to store and transfer energy
- The “top” capacitor rail connects to the switch node allowing charge transfer between elements while the “bottom” rail maintains and balances voltages
- The output voltage is divided between N stages allowing for high voltage gains

Wide-Bandgap Devices Realize Improved Converter Performance

- Leveraging the higher voltage, higher temperature and increased switching frequency of wide bandgap (WBG) devices greatly improves power density
- SiC has much higher figure-of-merit than Si
- SiC devices (FETs and diodes) have matured considerably
- GaN has a higher figure-of-merit and may further improve converter design
- While GaN diodes have been realized in the 1-4 kV regime, commercial GaN FETs have not been developed to sufficiently support high voltages necessary for MVDC/HVDC conversion
- So ... we propose a converter that may be used with SiC FETs and GaN diodes



SiC and GaN devices can Further Improve Power Density

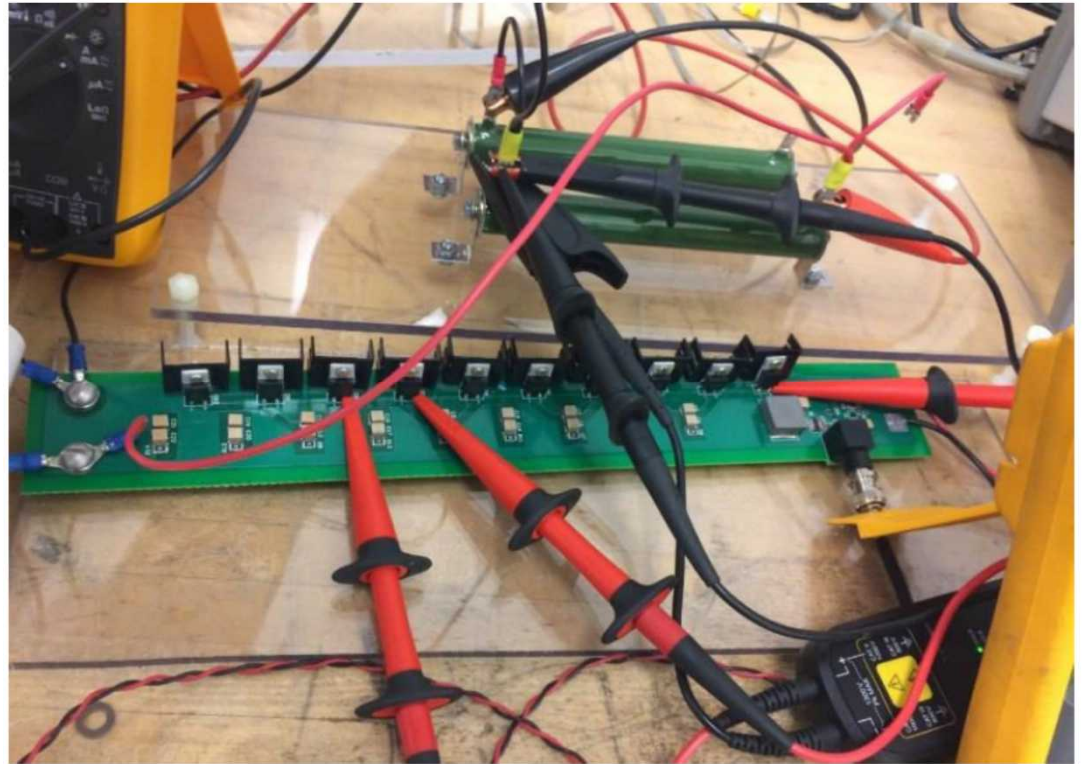


- SiC FET with SiC or GaN diodes simplify circuit design
- Bipolar design halves voltage stress per component for a given output voltage
- Current is shared between multiple paths, reducing parallel component count

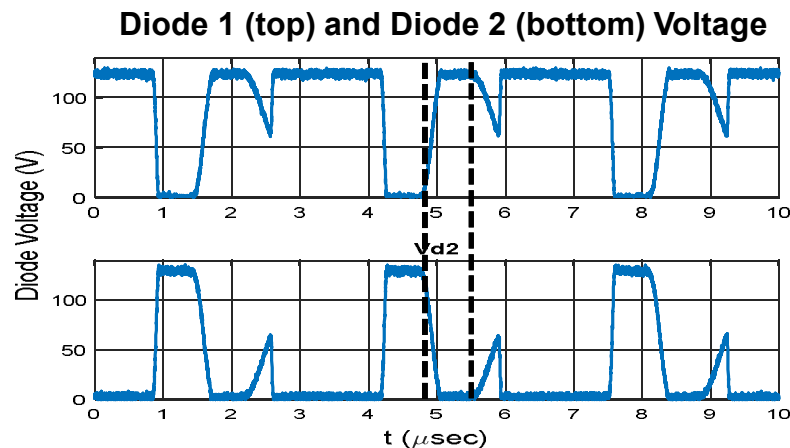
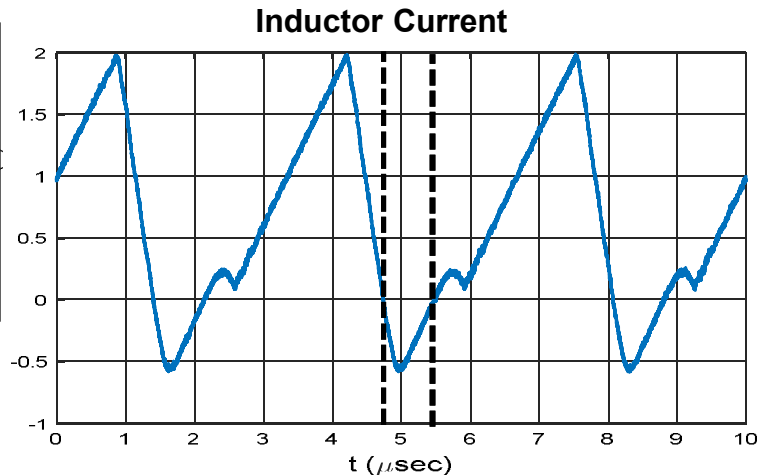
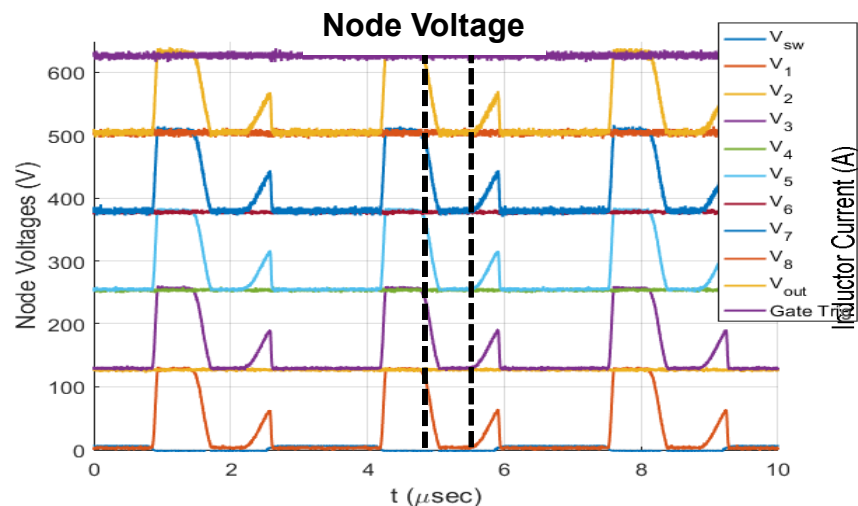
Hardware and Analytical Results

A Reduced Scale Prototype Verified Simulation Results

- 4-stage low voltage HSCC was built to validate simulation results
- All node voltages and currents were measured
- Various loading was applied

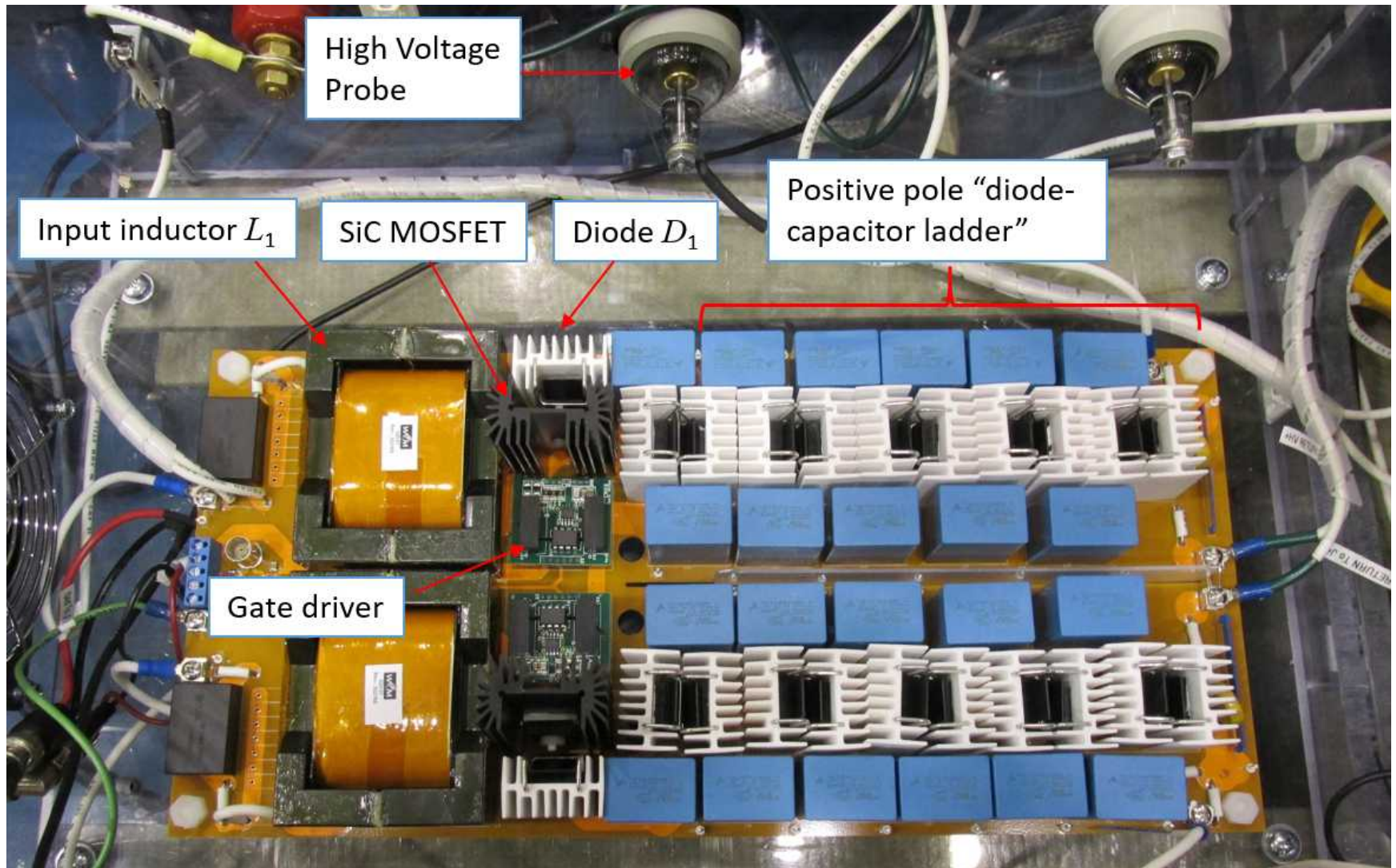


Earlier Prototype Gives Insight to Circuit Operation

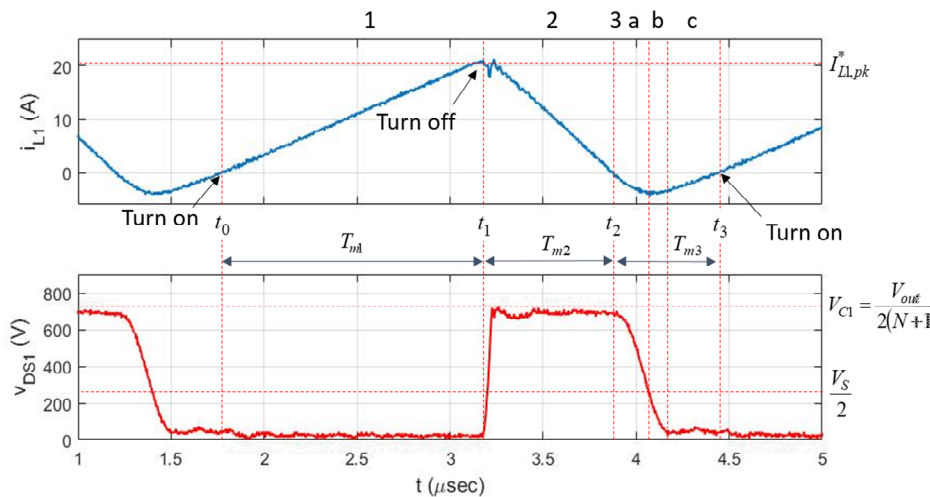
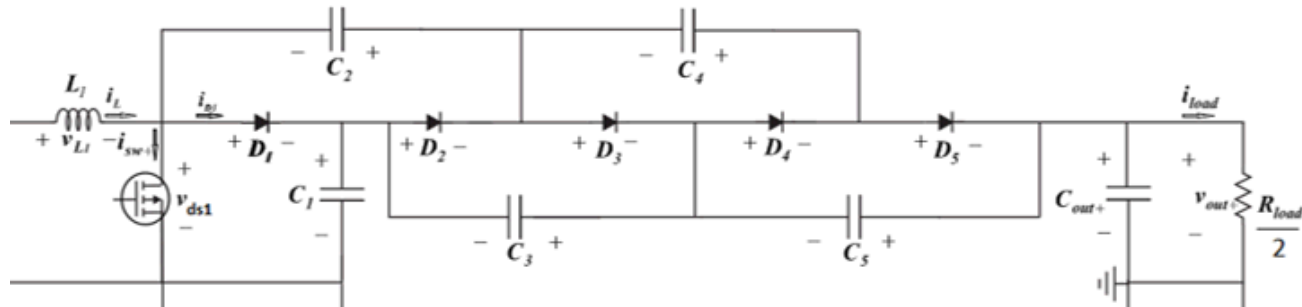


- Inductor current goes negative due to direct connection with upper rail capacitors.
- While inductor current is negative, diode biasing is reversed as if switch was turning 'on'.

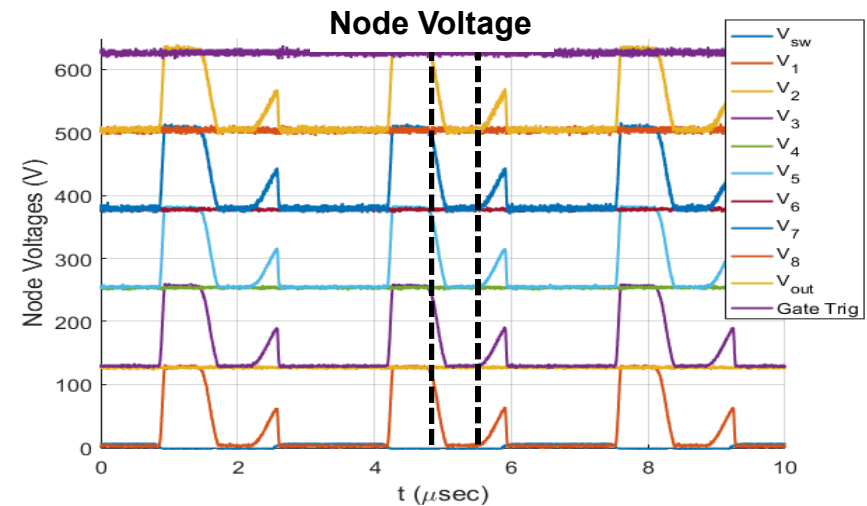
Bipolar HSCC was Assembled and Tested



Inductor Current and Drain Voltage Allow Soft-Switching

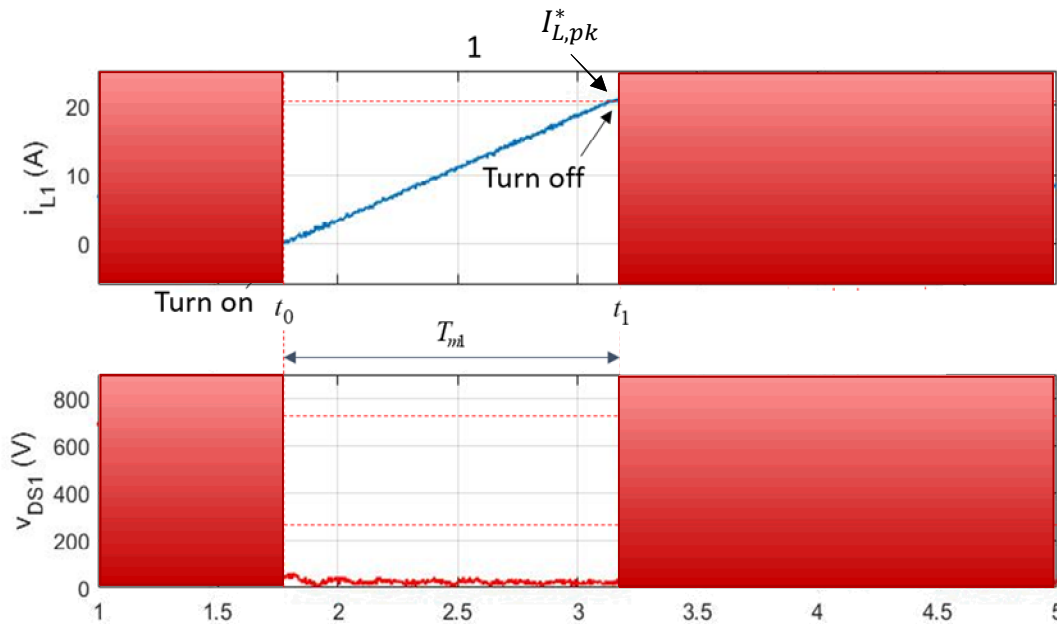


Positive polarity - I_{L1} (top), V_{DS} (bottom)

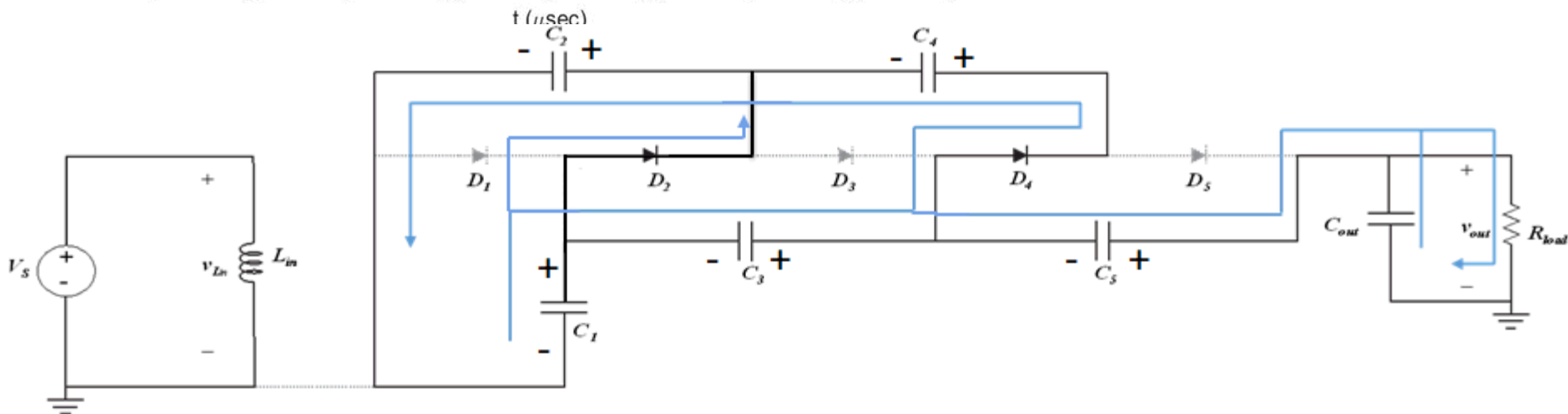


Node voltages of $N=4$ stage HSCC [3]

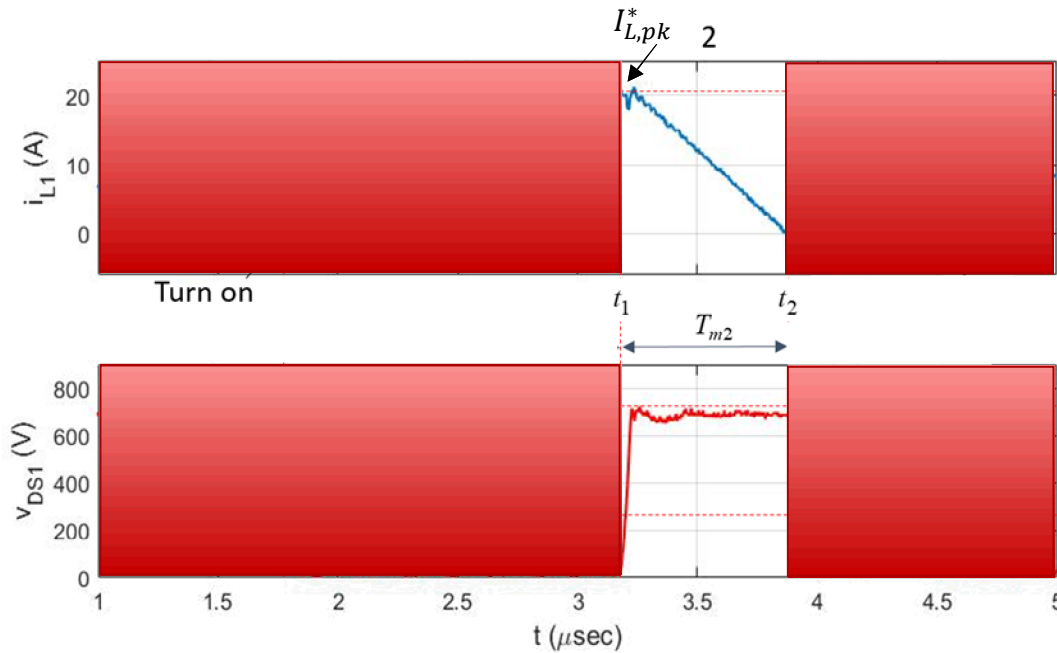
Mode 1 – Switch ‘on’/Inductor Charging



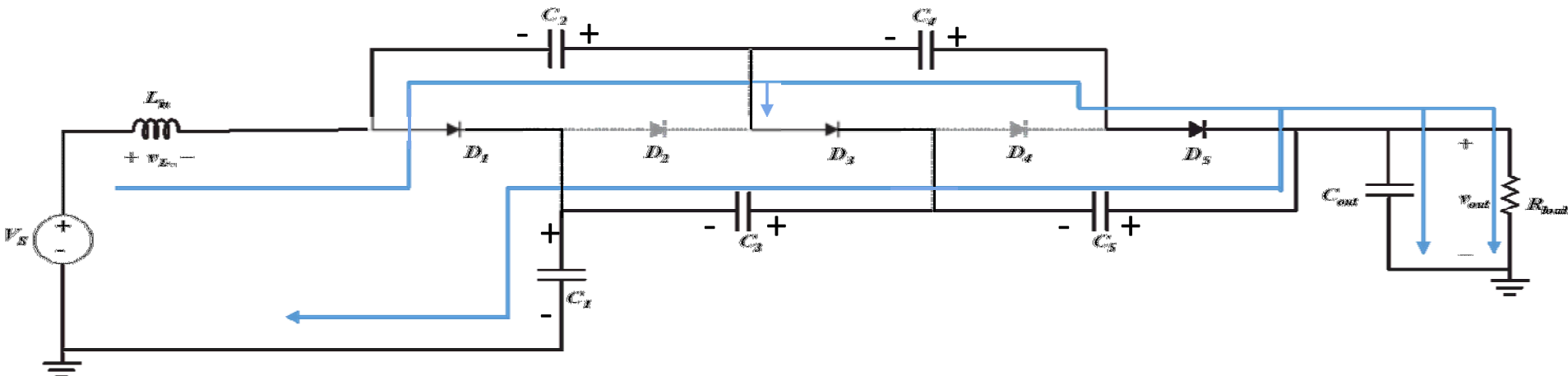
- The switch is turned ‘on’ at t_0
- Inductor current increases as linear ramp
- $V_{DS1} = 0$



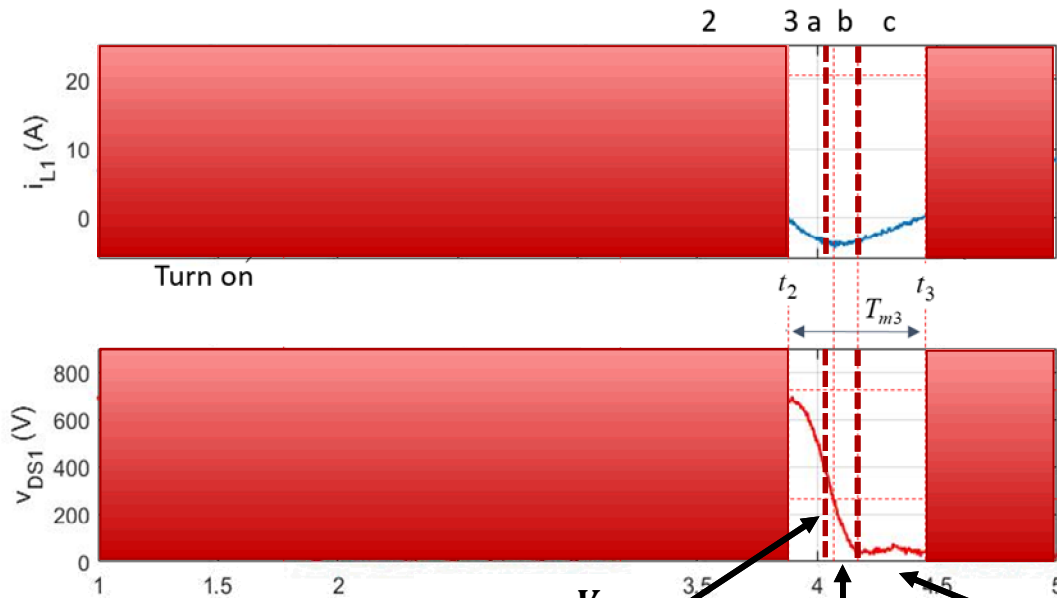
Mode 1 – Switch 'off'/Inductor Discharging



- The switch is turned 'off' at t_1
- $I_{L1} > 0$
- $V_{DS1} = \frac{V_{out}}{2(N+1)}$

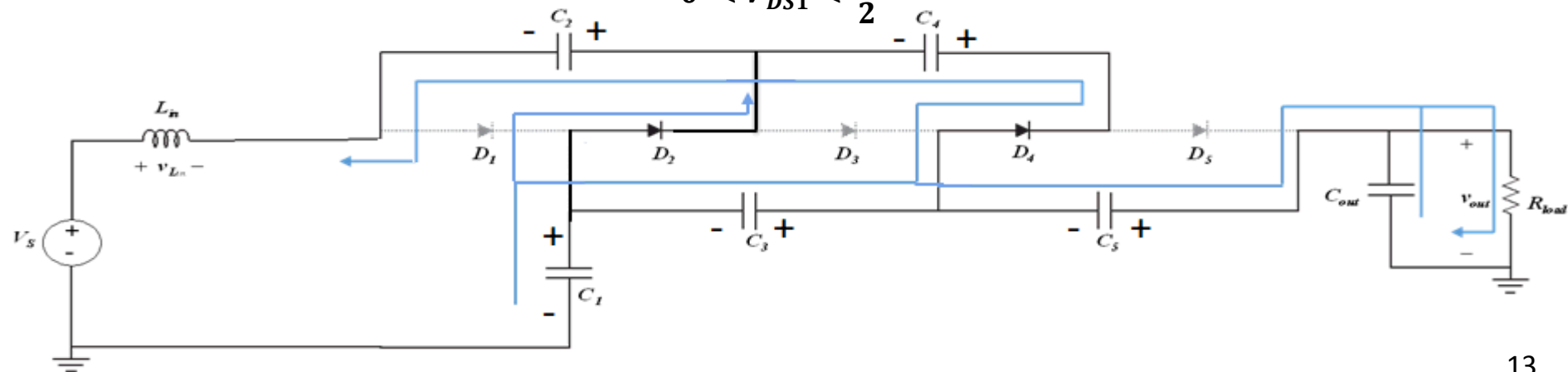


Mode 3a-3c – Switch 'off'/Inductor Current is Negative



- $I_{L1} < 0$
- Mode 3a – $V_{DS1} > \frac{V_s}{2}$
- Mode 3b – $0 < V_{DS1} < \frac{V_s}{2}$
- Mode 3c – $V_{DS1} = 0$

$V_{DS1} > \frac{V_s}{2}$
 $0 < V_{DS1} < \frac{V_s}{2}$
 $V_{DS1} = 0$



Analysis Provided Parameters for Circuit Performance

Equation	Mode 1	Mode 2	Mode 3
T_{mx}	$\frac{2L_1}{V_s} I_{L1,pk}$	$\frac{2I_{L1}(N+1)}{V_{out} - V_s\beta} I_{L1,pk}$	$\frac{1.375\tau_{cp}}{V_s(N+1)} V_{out}$
Q_x	$\frac{I_{L1}}{V_s} I_{L1,pk}^2$	$\frac{I_{L1}(N+1)}{V_{out} - V_s(N+1)}$	$\frac{\tau_{cp}^2}{I_{L1}} (0.6301 \frac{V_{out}}{(N+1)} - 0.4727 \frac{V_{out}^2}{V_s(N+1)^2})$

$$\tau_{CP} = \sum_{n=1}^{N+1} C \left(r_C + \frac{r_D}{2n+1} \right)$$

$$\beta = N + 1$$

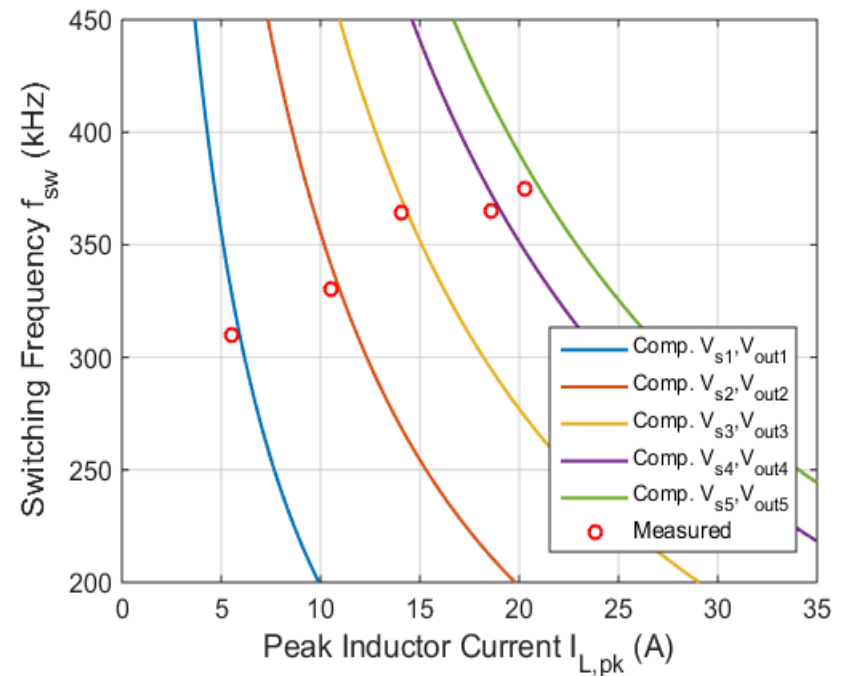
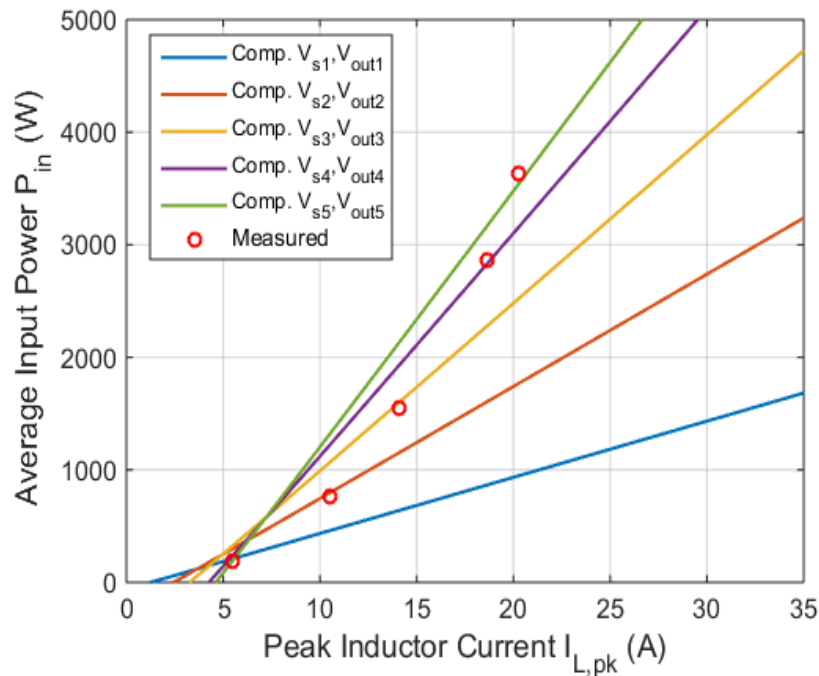
$$T_{sw} = \left(\frac{2L_1}{V_s} + \frac{2L\beta}{V_{out} - V_s\beta} \right) I_{L1,pk} + \frac{1.375\tau_{cp}}{V_s\beta} V_{out}$$

$$P_{in} = V_s \frac{(Q_1 + Q_2 + Q_3)}{T_{sw}}$$

$$f_{sw} = \frac{1}{\left(\frac{2L_1}{V_s} + \frac{2L\beta}{V_{out} - V_s\beta} \right) I_{L1,pk} + \frac{1.375\tau_{cp}}{V_s\beta} V_{out}}$$

Analytical and Hardware Results Are Close Match

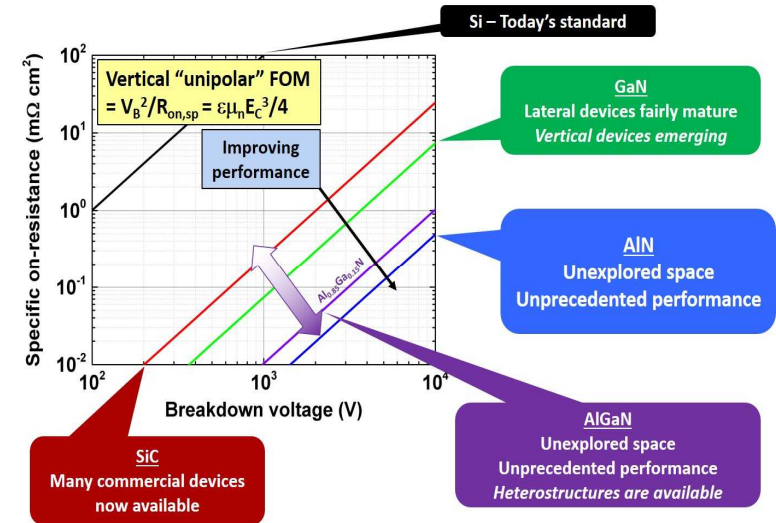
Exp.	V_s (V)	$I_{L,pk}$ (A)	V_{out} (V)	P_{in} (W)	Eff (%)	Gain	f_{sw} (kHz)	$I_{L,min}$ (A)
1	100	5.52	2142	190.4	97.88	21.44	310	-1.44
2	200	10.5	4247	766.2	97.56	21.26	330	-2.56
3	300	14.1	5911	1543.8	97.64	19.72	364	-3.12
4	400	18.6	7788	2855.6	97.63	19.47	365	-3.60
5	460	20.3	8630	3632.6	96.93	18.77	375	-3.92



Future Work

Next Steps will Further Improve Power Density and Efficiency

- Implementation of vertical GaN diodes is expected to further decrease power losses
- Power density can be improved by parameter optimization
 - Inductor sizing
 - Capacitor sizing
- Analysis will be adopted to a control approach to implement zero voltage/current switching



[4] Various Semiconductor FOM

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 - Lee Rashkin – Sandia National Labs
 - Jane Lehr – University of New Mexico

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