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Technology Roadmap and Systems Engineering Model for sCO2 Power Cycle Development

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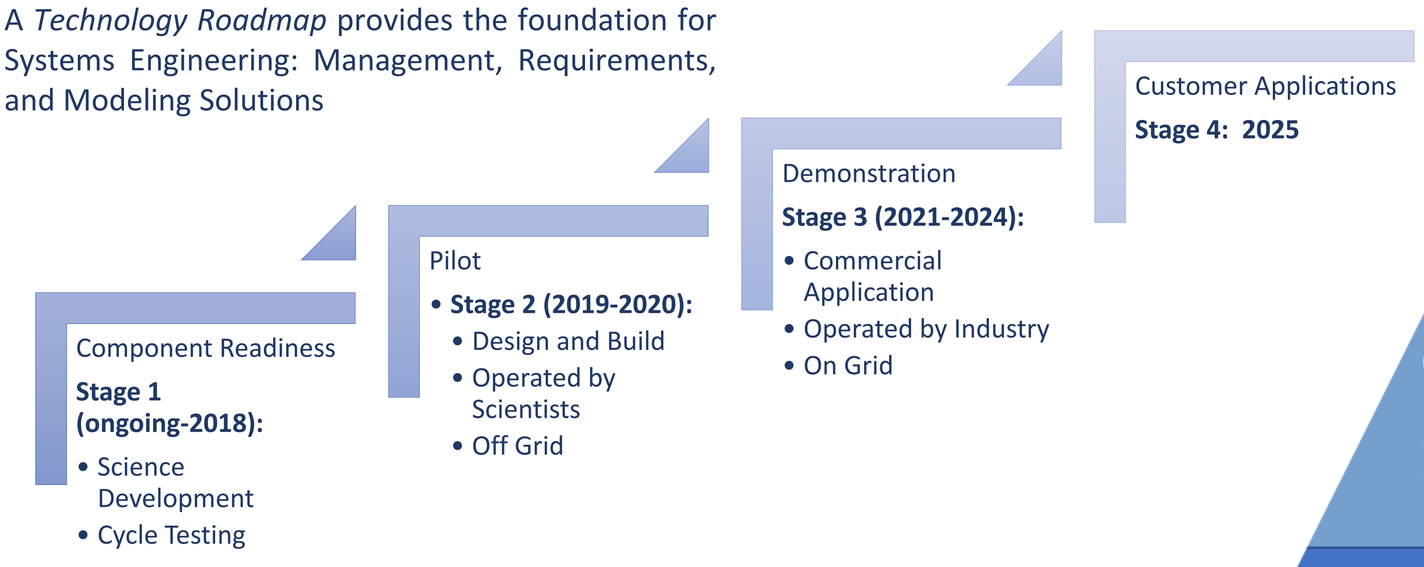
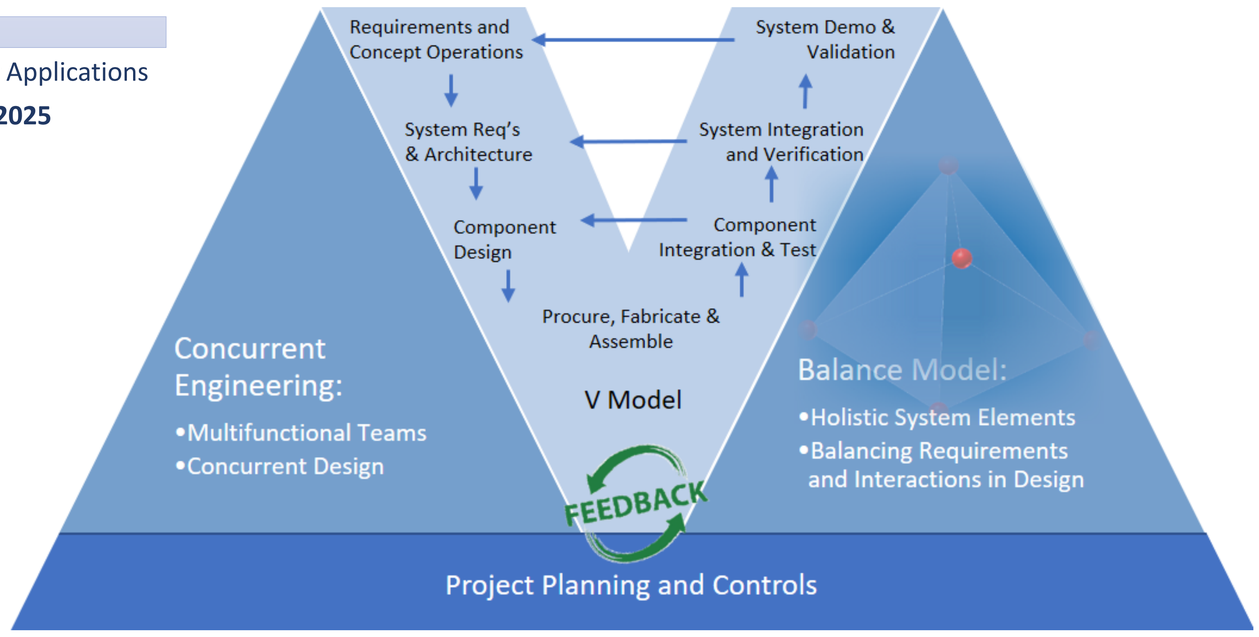
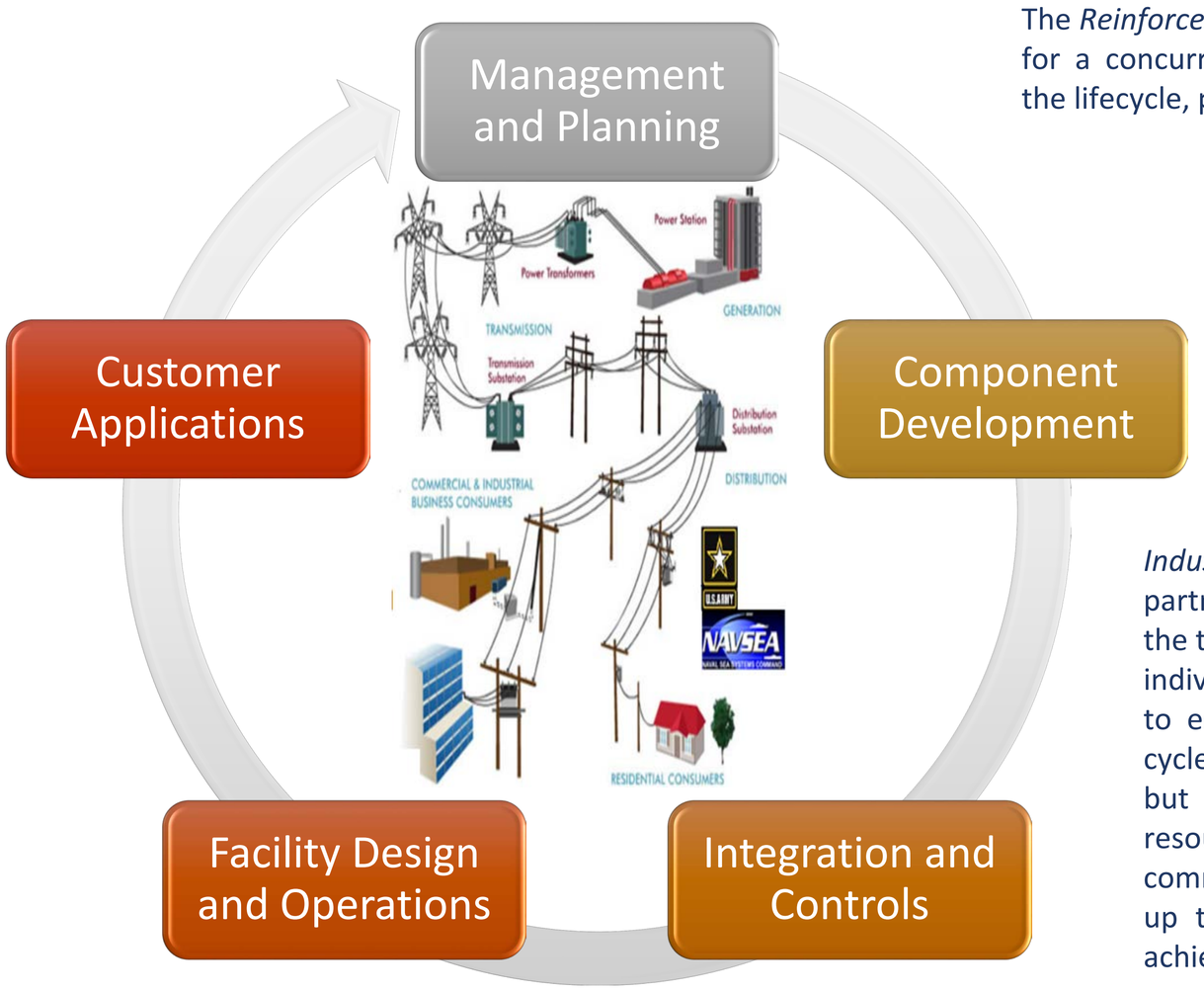
A *Technology Roadmap* provides the foundation for Systems Engineering: Management, Requirements, and Modeling Solutions





Systems and Requirements Modeling guided by end-use applications raise potential for modularity and reconfiguration.

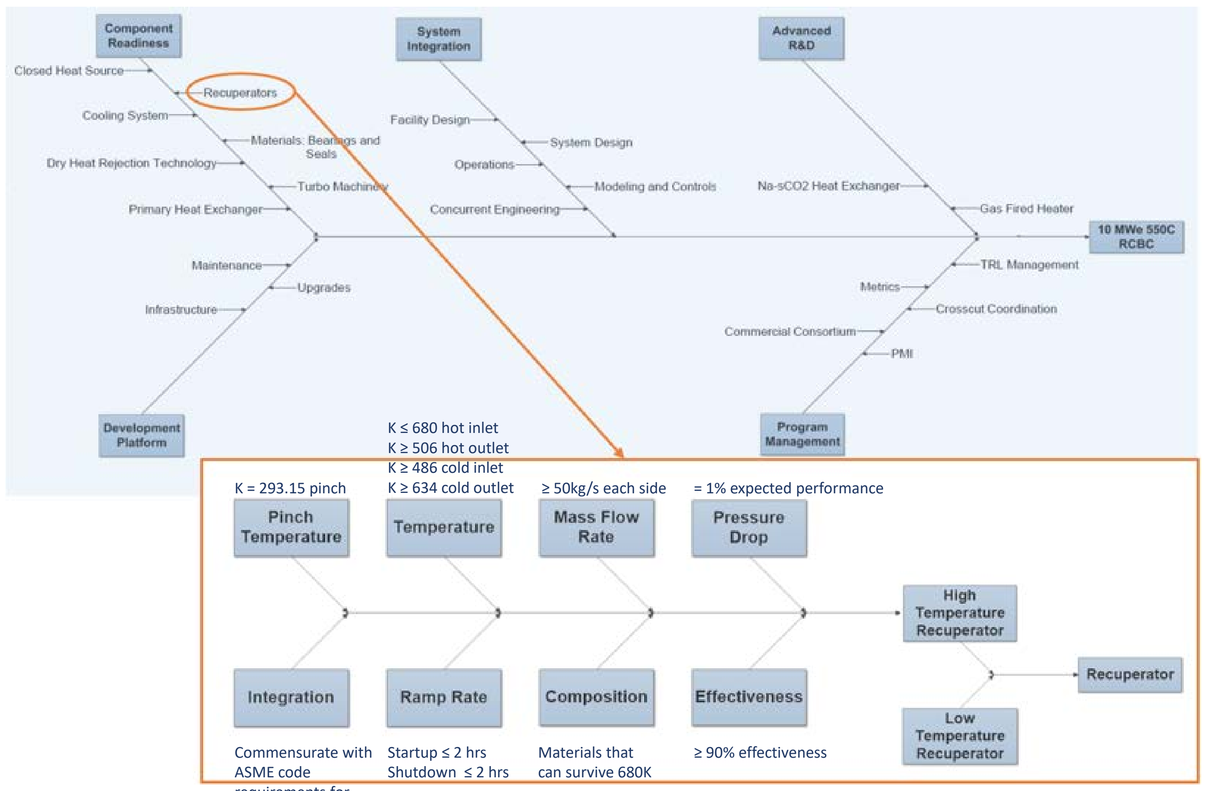
Application	Motivation	Size [MWe]	Temp. [C]	Pres. [MPa]
Advanced Reactor Designs (Includes Sodium and High Temp Reactors (gas, molten salts)	Efficiency Size Water reduction	10 – 300	350 – 800 +	20 – 35
Small Modular Reactors	Compact size Dry cooling			
Gas Turbine Bottoming		10	Low Temp	
Shipboard Propulsion	Efficiency Size	10 – 100	500 - 1000	35
Shipboard House Power	Efficiency Size	< 1 – 10	230 - 650	15 – 35
Waste Heat Recovery	Efficiency Size Simple cycles	1 – 10	< 230 - 650	15 - 35
Concentrated Solar Power	Efficiency 50% Size Dry cooling	3	700	35
Geothermal	Efficiency	1 – 50	100 - 300	15
Natural Gas fuel cycle, targeting distributed energy	Dry cooling	1-25	750	42
Fossil Fuel (indirect heating)	Efficiency Water reduction	300 – 600	550 - 900	15 – 35
Fossil Fuel (direct heating)	Efficiency Water reduction facilitates CO2 capture	300 – 600	1100 - 1500	35



The *Reinforced V Model for Systems Engineering* calls for a concurrent, holistic system design guided by the lifecycle, provider, and consumer demands.

Component Technology Readiness Levels (TRL) Management aims to retire risks of system components individually, to increase the probability of a successful demonstration and viability at commercial levels.

Industry Collaboration is possible when partners share a common target to develop the technology along the path towards their individual goals. Partnerships do not need to encompass the full extent of the R&D cycle until the final application is achieved, but rather allow flexibility to optimize resources and capacity towards a faster common goal, while simultaneously freeing up time and resources on both sides to achieve individual goals.



The *System TRL* can only be as high as the lowest component TRL and its interactions.