Understanding Middle-point Inductance's Effect on Switching Transients for Multi-chip SiC Package Design with P-cell/N-cell Concept

Fei Yang[1], Zhiqiang (Jack) Wang[2], Zheyu Zhang[1], Steven Campbell[2], Fred Wang[1,2], Madhu Chinthavali[2]

[1]Center for Ultra-wide-area Resilient Electric Energy Transmission Networks (CURENT)
The University of Tennessee
Knoxville, TN 37996-2250, USA
fyang17@vols.utk.edu

[2]Power Electronics and Electric Machine Group
Oak Ridge National Laboratory
Knoxville, TN 37932, USA

***Abstract*—Middle-point inductance L_{middle} can be introduced in power module designs with P-cell/N-cell concept. In this paper, the effect of middle-point inductance on switching transients is analyzed first using frequency domain analysis. Then a dedicated multiple-chip power module is fabricated with the capability of varying L_{middle}. Extensive switching tests are conducted to evaluate the device's switching performance at different values of L_{middle}. Experiment result shows that the active MOSFET's turn-on loss will decrease at higher values of L_{middle} while its turn-off loss will increase. Detailed analysis of this loss variation is presented. In addition to switching loss variation, it is also observed that different voltage stresses are imposed on the active switch and anti-parallel diode. Specifically, in the case of lower MOSFET's turn-off, the maximum voltage of lower MOSFET increases as L_{middle} goes up; however, the peak voltage of anti-parallel diode decreases significantly. The analysis and experiment results will provide design guidelines for multiple-chip power module package design with P-cell/N-cell concept.**

***Keywords*—middle-point parasitic inductance; multiple-chip in parallel; SiC power module; split converter**

I. INTRODUCTION

Silicon Carbide (SiC) power devices are acknowledged in high power converters for their fast switching speed and low on-resistance [1]–[4]. To fully exploit the fast-switching capability of SiC devices in a power module, package designs with P-cell/N-cell concept have been utilized because of the low power loop inductance and reduced voltage spikes [5]–[15]. In existing SiC modules with P-cell/N-cell concept, the current rating is low and less than three MOSFETs are paralleled. To design a high current SiC power module with multiple chips, a proper scaling method is needed.

Two different scaling methods can be used. The first method is split scaling where all the N-cells and P-cells are scaled independently at the initial stage. Then their middle points are connected as shown in Fig. 1. Identical scaling, on the other hand, connects the middle point of an N-cell with the middle point of a P-cell first forming a basic unit. Then the basic units are scaled as shown in Fig. 2. In both cases, the output or middle point of each cell needs to be connected. This is realized through direct-bonded-copper (DBC) level copper trace connection or external connections. Correspondingly, a new parasitic, middle-point inductance L_{middle}, will be introduced.

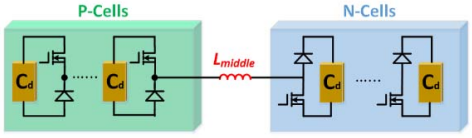


Fig. 1. Package Design with split scaling.

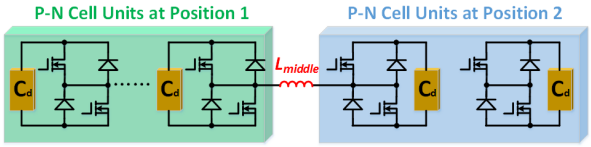


Fig. 2. Package Design with identical scaling.

Previous publications [16], [17] have discussed the role of middle-point inductance in split converters. Both pointed out that the turn-on loss can be reduced in the split converter design. In reference [17], the benefits of reduced dv/dt at output terminal and attenuated cross-talk effect are also observed.

However, the value of L_{middle} in those split converters are large: usually in the range of tens of uH. For multi-chip power module with P-cell/N-cell split scaling design, L_{middle} is within several hundred of nH. With a small value of L_{middle}, the middle point inductance will participate more actively in the switching transients. Meanwhile, none of these studies exploits the effect of L_{middle} on the device's voltage spikes during the switching transients. Since the voltage spike is an important factor determining the number of paralleled devices and switching

speed, it is meaningful to have a better understanding of the effect of L_{middle} on device's switching transients systematically.

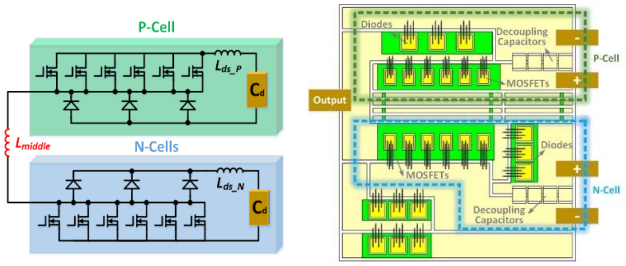
In this paper, the middle-point inductance's effect is analyzed in the frequency domain. Then a dedicated SiC multiple-chip split-scaled power module is designed with the capability of varying the values of middle-point inductance. Extensive switching tests are carried out at different conditions to study middle-point inductance's effect. Specifically, the switching loss and voltage spike variations of the devices due to the change of L_{middle} will be summarized and analyzed.

II. Multiple-frequency Ringing Phenomenon in a SiC Multiple-chip Module with Split Scaling

The study of the middle-point inductance's effect arises from an experimental observation of multiple-frequency ringing in the switching waveforms of a multiple-chip SiC power module based on P-cell/N-cell split scaling. In this section, this phenomenon will be described together with the introduction of the split-scaled SiC module package design.

A. SiC Multi-chip Package Design with Split Scaling

A phase-leg configuration is packaged, and its circuit diagram is illustrated in Fig. 3 (a). For each switch, six 1200 V SiC trench MOSFETs from Rohm are paralleled, and three 1200 V SiC Schottky diodes are used as the anti-parallel diodes.



(a) Circuit diagram (b) Physical layout

Fig. 3. Layout design of the power module.

The real physical layout is shown in Fig. 3 (b). It can be seen that P-cell/N-cell design methodology is adopted in the split scaling. Namely, all the devices on each P-cell are paralleled and located close together. The remaining devices belonging to N-cell are placed in a similar way. Decoupling capacitors can be directly embedded inside the module as well to mitigate the external parasitic inductance's effect. In the prototype, the decoupling capacitors are not packaged inside the module simply for the convenience of measuring the device's drain current with an external co-axial shunt resistor. The middle points of the P-cell and N-cell are connected through DBC-level copper traces.

Through the vertical pins shown in Fig. 4, kelvin gate-to-source connections are realized to minimize common-source inductance's effect. Similarly, dedicated kelvin drain-to-source sensing pins are designed to accurately measure the real voltage across the devices during switching transients. All the gate signals and voltage sensing signals are connected to the gate drive board, which is mounted right on top of the power module.

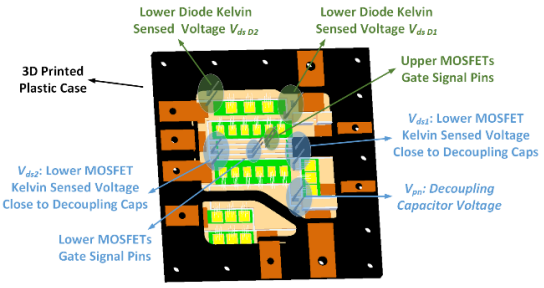


Fig. 4. Location of kelvin gate signal pins and voltage sensing pins.

3D printed high-temperature plastic case is designed to press the DBC substrate in close contact with the baseplate with ten screws at different locations. Thermal grease is used in between the bottom of the DBC and the top of the baseplate. Mounting holes are designed in the case as well to provide mechanical support for the gate drive board above. Laminated dc-link bus bar can be directly connected to the module from the right, and the middle point output pins are on the left side. The fabricated module is shown in Fig. 5.

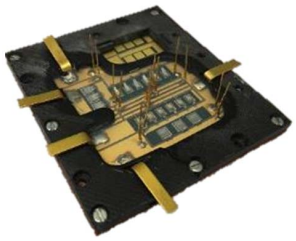


Fig. 5. Fabricated phase-leg module with split scaling.

B. Multiple-frequency Ringing Phenomenon

To evaluate the switching performance of the multiple-chip power module with split-scaling, a double-pulse-test (DPT) bench is built. To start with, the gate drive board is mounted on top of the power module first as indicated in Fig. 6. Standard BNC connectors are positioned on the gate drive board for kelvin V_{ds} measurement. Two pairs of twisted wires are located on the right for connections with the double-pulse-test board. The complete switching test setup is shown in Fig. 7. The circuit is configured such that the lower MOSFETs are the active switching devices. The drain current of lower MOSFETs is measured through an on-board 15 mΩ coaxial shunt. As discussed previously, the real device voltage is accessible

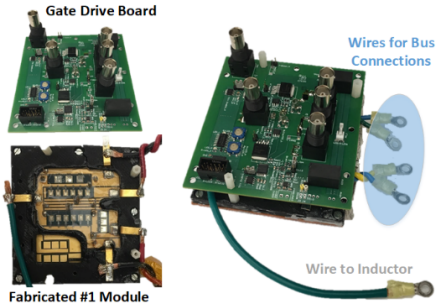


Fig. 6. Real power module with gate drive board.

through the kelvin connection. On-board ceramic and film capacitors are put close to the power terminals of the module. Short circuit protection circuit is inserted in between the dc-link capacitors and the film capacitors.

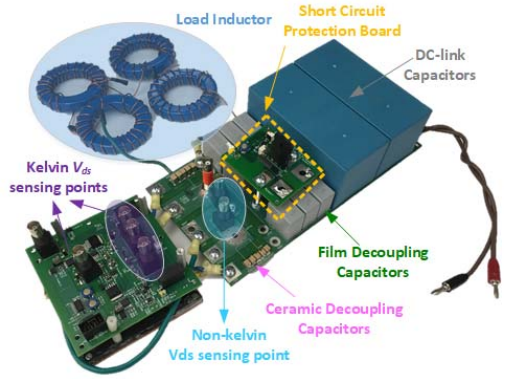


Fig. 7. DPT setup for the split-scaled power module.

At first, only the N-cells are connected to the dc-link for switching performance evaluation. The experimental turn-off switching waveforms of kelvin drain-to-source voltage, drain current, and the gate voltage are shown in Fig. 8. The load current is 100 A, dc-link voltage is 600 V, and the external turn-off gate resistor's value is 5 Ω. During the ringing period, only one resonant frequency is observed.

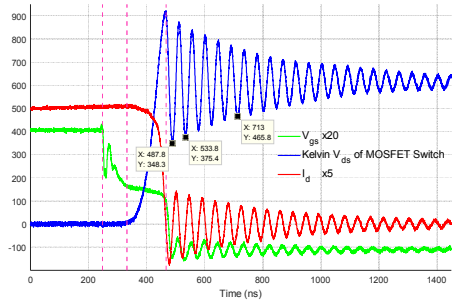


Fig. 8. Turn-off waveforms of lower MOSFETs with N-cell connected.

Assuming the on-board decoupling capacitor's voltage is constant, the high-frequency equivalent circuit during the ringing period can be derived as illustrated in Fig.9. It can be seen that the single resonant frequency is determined by the junction capacitance of the paralleled MOSFETs and the lumped power loop inductance [18].

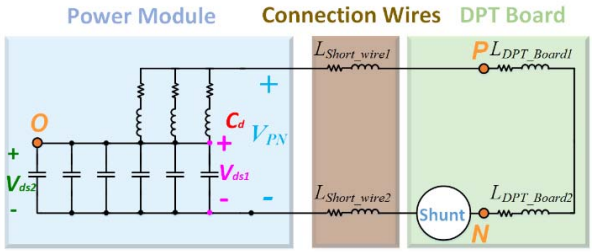


Fig. 9. High-frequency equivalent circuit of N-cell DPT during turn-off ringing period.

The value of the lower MOSFETs' junction capacitor is nearly flat above 500 V, and 644.9 pF is obtained at 600 V for the lower MOSFETs. The ringing frequency of V_{ds} is around 22 MHz, and the power loop inductance L_{ds} is calculated to be:

$$L_{ds\_N} = \frac{1}{4 \cdot \pi^2 \cdot f_0^2 \cdot C_{ds}} = 81.15 \text{ nH} \quad (1)$$

In the next step, both P-cells and N-cells are connected to the power stage board for switching test evaluation. The experiment conditions are the same as the N-cell double-pulse-test. The turn-off waveforms of the lower MOSFETs' kelvin V_{ds}, drain current and gate voltage are shown in Fig. 10. The kelvin voltage waveform of the lower anti-parallel diode is also illustrated in the orange line. As can be seen, for both voltage waveforms of lower MOSFET and lower anti-parallel diode, two resonant frequencies are observed. The higher one f_1 is around 24.27 MHz and the lower one f_2 is around 2.00 MHz. This multiple-frequency ringing is also observed in the drain current.

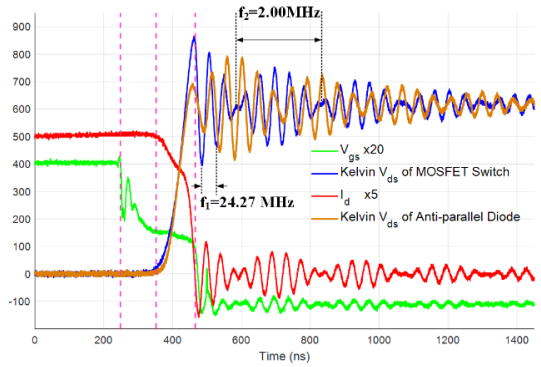


Fig. 10. Turn-off waveforms with P-cells, N-cells connected at 100 A.

III. Analysis in Frequency Domain

To find out the cause of this phenomenon, the frequency domain analysis is used. Previously, this method has been proven effective in analyzing the ringing frequency of a single N-cell with one TO-packaged MOSFET and one diode [19]. For this multi-chip split-scaled phase-leg module, the frequency domain analysis can also be applied.

Fig. 11 shows the high-frequency equivalent circuit during the ringing period. On the load inductor side, its equivalent parallel capacitor is considered. Both the lower MOSFETs and lower anti-parallel diodes are modeled as capacitors with single values. The upper MOSFETs and anti-parallel diodes are modeled as resistors at high frequency since the body diode of the MOSFET and the anti-parallel diodes would together conduct the load current during the ringing period. The decoupling capacitor is also considered in the circuit diagram. The dc-link capacitor is shorted at high frequency. Compared to the phase-leg configuration with a single device, the middle-point inductance is introduced in this multi-chip package.

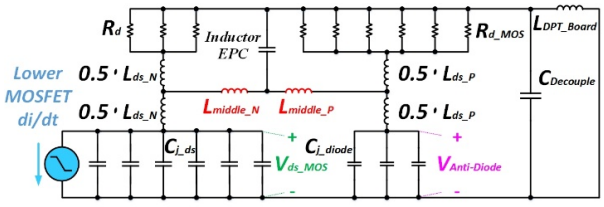


Fig. 11. Equivalent circuit in lower MOSFET turn-off ringing period.

The excitation for this impedance network is the lower MOSFETs' channel di/dt. It will generate responses at various frequencies. Correspondingly, these excitations will cause voltage ringing of various frequencies on both lower MOSFETs and lower anti-parallel diodes. The ringing frequencies are dominated by the network's impedance. Therefore, the impedance of V_{ds_MOS} over $i_{channel}$ is studied over a wide range of frequencies.

To extract the ringing frequencies correctly, accurate values of all the circuit parameters are needed. Previously, the power loop inductance of the N-cell L_{ds_N} is extracted to be 81.15 nH based on the switching test of N-cells exclusively. Similarly, the lumped power loop inductance value of the P-cell is required. A double-pulse-test with P-cell solely is implemented to obtain this value. After the upper MOSFET is turned on, the power loop parasitic inductance of P-cell will resonate with the junction capacitor of the lower anti-parallel diodes. A ringing frequency of 21.63 MHz is obtained, and the power loop inductance of the P-cell is extracted to be:

$$L_{ds\_P} = \frac{1}{4\cdot\pi^2\cdot f_0^2\cdot C_{ds}} = 81.60 \text{ nH} \quad (2)$$

The equivalent parallel capacitance value of the load inductor is measured from impedance analyzer, and 3.5 pF is obtained. The middle-point inductance is formed by the DBC-level copper trace, and the value of the middle-point parasitic inductance is extracted in Ansys Q3D based on its geometry. Fig. 12 illustrates the location of sink and source for extraction of L_{middle}. At high frequency, the extracted value of L_{middle} is 5.47 nH. The parasitic inductance in between the on-board decoupling capacitor and dc-link capacitor is also simulated to be 20.15 nH.

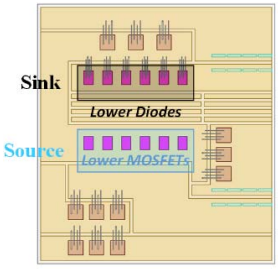


Fig. 12. Geometry setting to extract L_{middle}.

With all the circuit parameters ready, the impedance network is built in LTspice. To mimic the channel di/dt, an ac current excitation is in parallel with the junction capacitor of the lower MOSFET. The impedances of $Z_{Mos} = V_{ds\_MOS}/i_{channel}$ is obtained as shown in Fig. 13.

As can be seen, two resonant frequencies are observed, which are close to each other. One is at $f_L = 21.85\ MHz$, and the other one is $f_H = 29.96\ MHz$. If an equal value of amplitude is assumed, the resulting signals will have zero-crossing points (with an offset of dc-link voltage) at two frequencies of f_{Z_D} and f_{Z_C}:

$$\frac{f_{Z\_D}}{2} = f_D = \frac{f_H - f_L}{2} = \frac{29.96-21.85}{2} = 4.06\ MHz \quad (3)$$

$$\frac{f_{Z\_C}}{2} = f_C = \frac{f_H + f_L}{2} = \frac{29.96+21.85}{2} = 25.91\ MHz \quad (4)$$

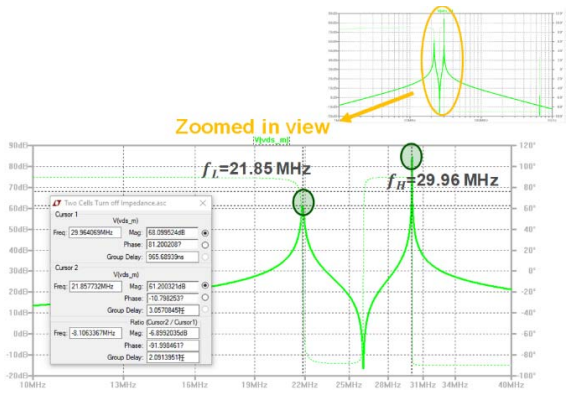


Fig. 13. Impedance of V_{ds_MOS} over $i_{channel}$ for the module under test.

f_C and f_D are the resulting multiple ringing frequencies in time domain. These values are approximate to the observed two ringing frequencies ($f_1 \approx 25\ MHz$, and $f_2 \approx 2\ MHz$) separately in experiment as shown in Fig. 10. It can be inferred that the middle-point inductance L_{middle} is the cause of the multiple-frequency ringing.

Fig. 14 shows another simulation of Z_{Mos} at different values of L_{middle}. As L_{middle} increases, f_H is decreasing but f_L is almost unchanged. According to equation (3) and (4), f_D will always decrease. Equivalently, the lower ringing frequency in experiment f_2 is expected to decrease as well. When L_{middle} is above a certain value, a single frequency is obtained.

Considering the case of large L_{middle}, the current in L_{middle} will remain its previous value during the switching transients. Accordingly, L_{middle} can be treated as an open circuit at high frequency. Then a single frequency will be obtained for N-cell, which is solely determined by the power loop parasitic inductance and the junction capacitance of the MOSFETs.

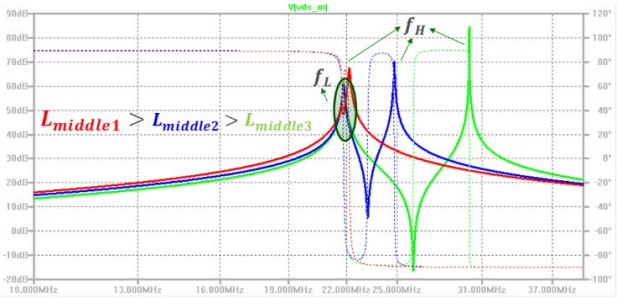


Fig. 14. The impedance of V_{ds_MOS} over $i_{channel}$ with different L_{middle}.

IV. Experiment Evaluation of Middle-Point Inductance's Effect

Based on previous analysis, different values of L_{middle} will have different impacts on the switching transients. It is meaningful to investigate its effect on the switching transients in a multiple-chip split-scaled package design, especially for fast-switching devices where the influence of parasitic parameters is more significant.

A. Module Modification

To conduct the study, a dedicated module is built with the capability of varying the values of middle-point inductance. Fig. 15 demonstrates the specific DBC substrate for fabrication. The

copper trace connecting the two middle points are cut out. Afterward, two output terminal pins are soldered to the middle point of each cell respectively. The middle-point inductor will be connected outside for easier variation of the value of L_{middle}. Specifically, L_{middle} can be changed by varying the length of the wires. The remaining layout and components are the same as discussed previously. The final assembled module is shown in Fig. 16 with the gate drive board installed.

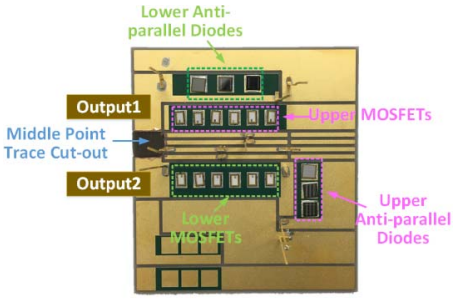


Fig. 15. Dedicated DBC substrate for evaluating L_{middle}'s effect on switching transients.

Fig. 16. Fabricated module with gate drive board for evaluating the effect of L_{middle} during switching transient.

B. Experiment Study of Middle-point Inductance's Effect

Fig. 17 (a) to (c) exhibit the experimental turn-off waveforms of lower MOSFETs' gate voltage, kelvin-sensed V_{ds}, drain current and lower anti-parallel diodes' voltage at different values of L_{middle} with $R_{g,off} = 7.5\,\Omega$. It can be observed that the lower ringing frequency of f_2 does change with the value of middle-point inductance: f_2 drops from 1.79 MHz to 1.26 MHz as L_{middle} increases from 50 nH to 160 nH. At $L_{middle} = 1600\,nH$, a single resonant frequency of 20.45 MHz is observed which indicates a decouple of P-cell with the N-cell. Both the switching loss and voltage spikes will change at different values of L_{middle}.

In the following sections, the switching performance of the split-scaled module will be evaluated at different values middle-point inductance (10 nH, 50 nH, 160 nH, 650 nH and 1600 nH). The gate resistor values are varied at 5 Ω, 7.5 Ω and 10 Ω. All the double-pulse-test is carried out at room temperature.

1) Middle-point inductance's effect on turn-on loss

At first, the turn-on switching losses of the lower MOSFETs are compared. Fig. 18 illustrates the experimental result at different load currents, gate resistors and L_{middle}. It is observed that the turn-on switching loss will decrease as the value of L_{middle} goes up over a wide range of load current.

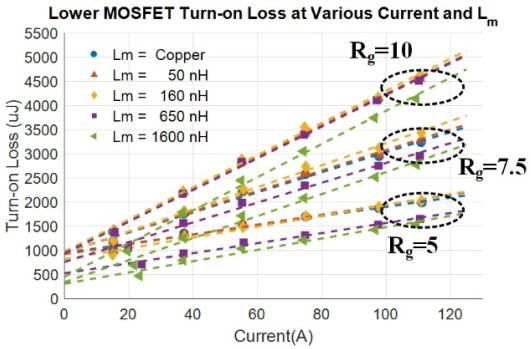
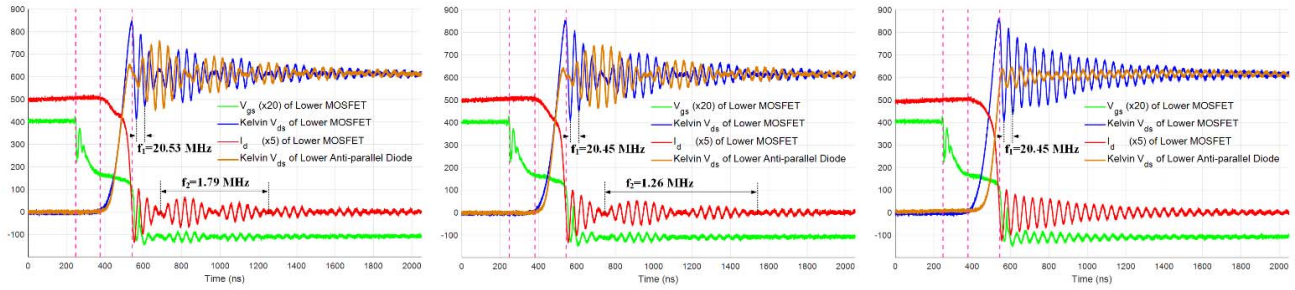


Fig. 18. Turn-on loss results at different L_{middle}.

Several factors contribute to the reduced turn-on loss at increased value of L_{middle}. First, V_{ds} falls more quickly when L_{middle} is larger. This can be explained by the fact that the effective output capacitance to be charged or discharged will be smaller because of the decoupling effect at higher values of L_{middle}. Correspondingly, with the same gate drive circuit, V_{ds} will drop more quickly leading to reduced power loss. This is verified from the experimental result. Fig. 19 illustrates the turn-on waveforms of the lower devices at $L_{middle} = 50\,nH$ and $L_{middle} = 1.6\,uH$ with all other conditions the same. It can be observed the MOSFET's drain-to-source voltage falls more quickly in the case with a larger value of middle-point inductance.

Another reason is that the peak drain current of lower MOSFET will be smaller at a higher value of L_{middle}. When L_{middle} is small, the measured drain current composes of the charge current of upper anti-parallel diode, the charge current of upper MOSFET and the discharge current of lower anti-parallel diode as indicated in Fig. 20. All these currents will lead to excessive overlap losses in the lower MOSFET since the V_{ds} of active switching device has not reached zero.

However, when the value of L_{middle} is large, the drain-to-source voltage of the lower anti-parallel diode is not falling together with V_{ds} of lower MOSFET as indicated in Fig. 19. Consequently, the discharge current of lower anti-parallel diode



(a) $L_{middle} = 50\,nH$ (b) $L_{middle} = 160\,nH$ (c) $L_{middle} = 1600\,nH$

Fig. 17. Experimental lower MOSFET turn-off switching waveforms at different values of L_{middle} with $R_{g,off} = 7.5\,\Omega$.

and the charge current of upper MOSFET will not introduce extra overlap losses on lower MOSFET. Thus, the overlap loss will be smaller with a large value of L_{middle}.

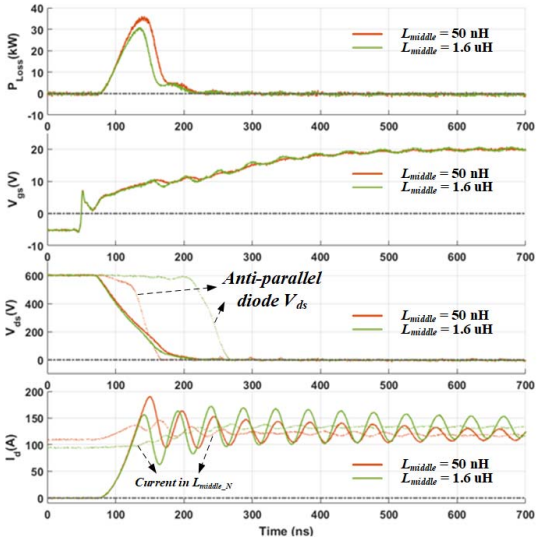


Fig. 19. Turn-on waveforms at $R_{g,on} = 5\ \Omega, I_{load} = 110\ A$ with $L_{middle} = 50\ nH$ and $L_{middle} = 1.6\ uH$ respectively.

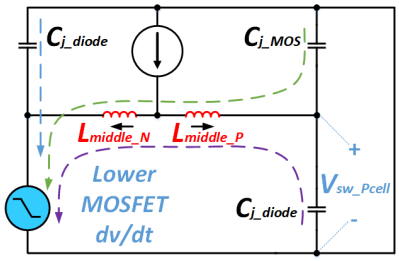


Fig. 20. Composition of measured drain current during turn-on.

In other words, large L_{middle} effectively decouples the P-cell with N-cell, and prevents the overlap losses due to the other phase-leg. This decoupled effect at large value of L_{middle} can also be observed in Fig. 18 from the fact that turn-on switching loss at 0 A is decreasing as L_{middle} goes up. The zero A turn-on loss include three parts: the C_{oss} charge of upper anti-parallel diode, the C_{oss} charge of upper MOSFETs and the C_{oss} discharge of lower anti-parallel diode. In the extreme case when the value of L_{middle} is zero, all these C_{oss} charge and discharge energy of the switches except lower MOSFETs will be measured. Therefore, the measured turn-on loss at 0 A will be at its maximum value when L_{middle} is small. However, when L_{middle} is very large, it can be regarded as an open circuit during the switching transients. Therefore, only the charge of upper anti-parallel diode's C_{oss} will be measured. Consequently, the 0 A turn-on loss will merge at different points in experiment as indicated in Fig. 18.

2) Middle-point inductance's effect on turn-on loss

The turn-off loss result at different values of L_{middle} is summarized as shown in Fig. 21. As can be seen, the turn-off loss is always increasing as L_{middle} increases. Two reasons contribute to the increased turn-off loss. First, because of the reduced equivalent output capacitance at larger value of L_{middle}, the drain-to-source voltage is increasing more quickly. Consequently, more overlap loss is obtained at a given drain current. This is verified through the comparison of the experimental turn-off waveforms at $L_{middle} = 50\ nH$ and $L_{middle} = 1.6\ uH$ shown in Fig. 22.

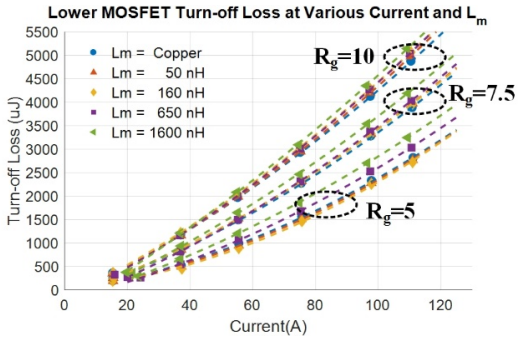


Fig. 21. Turn-off loss results at different L_{middle}.

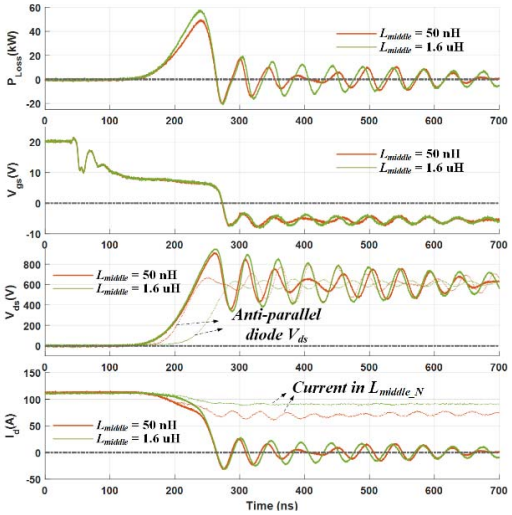


Fig. 22. Turn-off waveforms at $R_{g,on} = 5\ \Omega, I_{load} = 110\ A$ with $L_{middle} = 50\ nH$ and $L_{middle} = 1.6\ uH$ respectively.

Second, at higher values of L_{middle}, more current remains to flow through the lower MOSFET in the dv/dt period. The measured drain current of the lower MOSFET constitutes of three parts: the discharge current of upper anti-parallel diode, the discharge current of the upper MOSFET, and the charge current of the lower anti-parallel diode as shown in Fig. 23. At large L_{middle}, the other switching cell is decoupled. Correspondingly, more current remains in the lower MOSFET at a given load current. Combining the higher V_{ds} and higher drain current, the overlap loss will be larger at a higher value of L_{middle}.

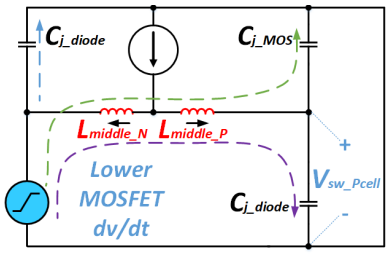
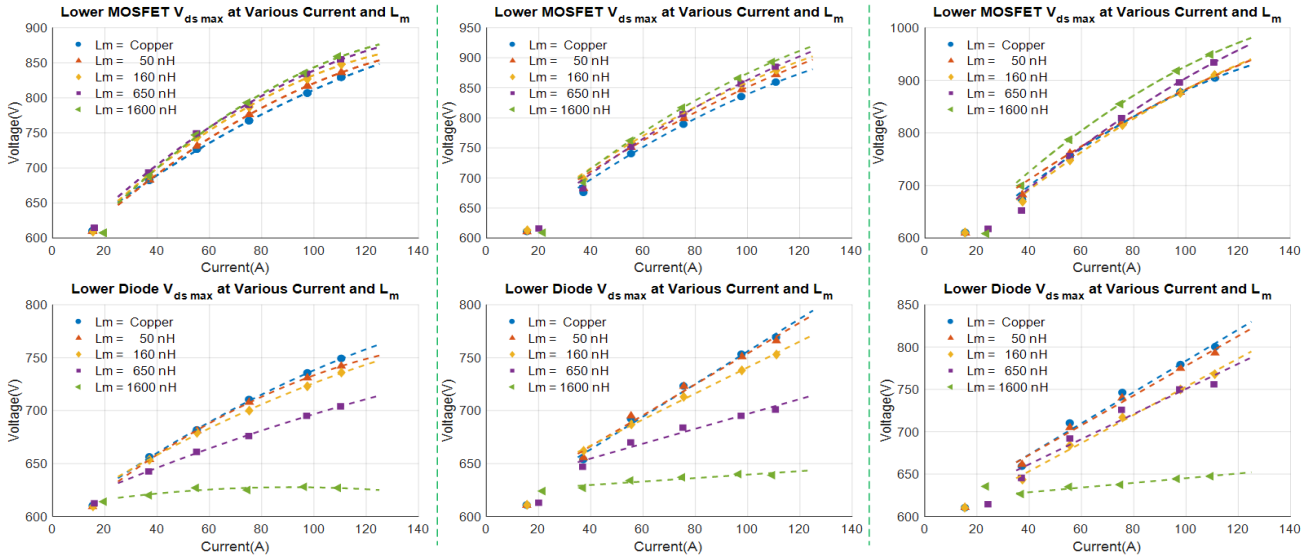


Fig. 23. The composition of measured drain current during turn-off.



(a) $R_g = 10\ \Omega$ (b) $R_g = 7.5\ \Omega$ (c) $R_g = 5\ \Omega$

Fig. 24. Maximum voltage at different L_{middle} during lower MOSFET turn-off.

3) Effect of L_{middle} on voltage spikes during lower MOSFET's turn-off

As discussed previously, the lower MOSFETs and lower anti-parallel diodes will experience extra voltage stress during the switching transients of lower MOSFETs' turn-off.

The voltage spikes of the lower devices during lower MOSFET's turn-off are summarized in Fig. 24 at different values of gate resistors, load current and L_{middle}. Both voltages will increase with the load current. However, as L_{middle} increases, the maximum voltage of the MOSFET keeps increasing while the maximum voltage of the anti-parallel diode has dropped significantly. At $R_{g,ext}$=10 Ω and $I_{load} = 110\ A$, the lower MOSFET's voltage overshoot increases by 17% when L_{middle} is increased from 10 nH to 1.6 uH. Meanwhile, around 80% reduction of voltage overshoot is observed for the lower anti-parallel diode. In fact, the lower anti-parallel diode's voltage overshoot is small and almost flat over the load current in the case of $L_{middle} = 1.6\ uH$.

4) Effect of L_{middle} on voltage spikes during upper MOSFET's turn-on

During the upper MOSFET's turn-on transients, the lower MOSFET and lower anti-parallel diode will also experience voltage spikes. To evaluate the voltage spikes variation at different L_{middle}, another group of tests is implemented and the result at $R_{g,off} = 10\ \Omega$ is demonstrated in Fig. 25.

Like the case of lower MOSFET's turn-off, the voltage spikes of the lower MOSFET and lower anti-parallel diode are also different because of the effect of L_{middle}. However, an opposite trend of voltage spike variation is observed for the case of upper MOSFET's turn-on. To be specific, as L_{middle} increases, the lower MOSFET's voltage will decrease while the anti-parallel diode's voltage will build up. Considering the turn-on condition at $R_{g,ext} = 10\ \Omega$ and $I_{load} = 110\ A$, the induced voltage overshoot on lower MOSFET is reduced by 56% as L_{middle} changes from 10 nH to 1.6 uH. On the other hand, the lower anti-parallel diode's overshoot is increased by 40%.

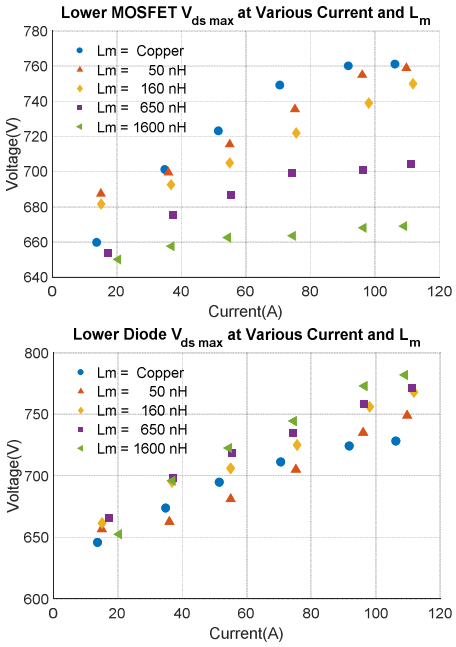


Fig. 25. Maximum voltage at different L_{middle} with $R_{g,off} = 10\ \Omega$ during upper MOSFET turn-on.

V. Conclusion and Future Work

In this paper, the phenomenon of multiple-frequency ringing in a multiple-chip split-scaled SiC power module is explained from a frequency domain analysis. It is found that a new parasitic parameter, middle-point inductance L_{middle}, can affect the switching transients actively. To verify this analysis, a dedicated module is built with the capability of varying L_{middle}.

Extensive switching tests are implemented at different load conditions, and it is found that the turn-on loss will decrease as L_{middle} increases. Meanwhile, the turn-off loss will increase. Detailed loss reduction or increase due to the variation of middle-point inductance is analyzed in this paper.

Furthermore, the experiment results indicate that L_{middle} will stress the active switch and anti-parallel diode differently in terms of voltage spikes. Specifically, considering lower MOSFET's turn-off, the voltage overshoot on the lower MOSFETs will increase by 17% in experiment as L_{middle} goes up. However, the overvoltage on the lower anti-parallel diode will decrease, and more than 80% reduction are observed. For upper MOSFET's turn-on case, an opposite trend is obtained: the peak voltage on lower MOSFET will decrease as L_{middle} increases while the diode's maximum voltage will build up. Therefore, in designing package layout with multiple-chip, the value of middle-point inductance should be controlled to make sure all the devices are operating within the device's maximum voltage rating at different operating conditions.

In terms of future work, the middle-point inductance's effect on voltage spikes at a lower value of power loop inductance will be investigated. Afterwards, a general multi-chip design guideline will be presented.

ACKNOWLEDGMENT

This research was sponsored by the Electric Drive Technologies Program, DOE Vehicle Technologies Office, under contract DE-AC05-00OR22725 with UT-Battelle, LLC. This work made use of the Engineering Research Center Shared Facilities supported by the Engineering Research Center Program of the National Science Foundation and the Department of Energy under NSF Award Number EEC-1041877 and the CURENT Industry Partnership Program.

REFERENCES

[1] Y. Cui *et al.*, "High efficiency data center power supply using wide band gap power devices," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2014, pp. 3437–3442.

[2] F. Wang and Z. Zhang, "Overview of silicon carbide technology: Device, converter, system, and application," *CPSS Trans. Power Electron. Appl.*, vol. 1, no. 1, pp. 13–32, 2016.

[3] X. Ding *et al.*, "Analytical and Experimental Evaluation of SiC-inverter Nonlinearities for Traction Drives Used in Eletric Vehicles," *IEEE Trans. Veh. Technol.*, vol. PP, no. 99, p. 1, 2017.

[4] Y. Cui *et al.*, "Characterization and modeling of silicon carbide power devices and paralleling operation," in *IEEE International Symposium on Industrial Electronics*, 2012, pp. 228–233.

[5] Y. Xu, I. Husain, H. West, W. Yu, and D. Hopkins, "Development of an ultra-high density Power Chip on Bus (PCoB) module," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1–7.

[6] S. Li, L. M. Tolbert, F. (. Wang, and F. Z. Peng, "Stray Inductance Reduction of Commutation Loop in the P-cell and N-cell-Based IGBT Phase Leg Module," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3616–3624, 2014.

[7] X. Zhao *et al.*, "Flexible epoxy-resin substrate based 1.2 kV SiC half bridge module with ultra-low parasitics and high functionality," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 4011–4018.

[8] M. Frisch and T. Ernö, "Power module with additional low inductive current path," in *International Conference on Integrated Power Electronics Systems*, 2010, pp. 1–6.

[9] L. D. Stevanovic, R. A. Beaupre, E. C. Delgado, and A. V Gowda, "Low inductance power module with blade connector," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2010, pp. 1603–1609.

[10] Z. Chen, Y. Yao, D. Boroyevich, K. D. T. Ngo, P. Mattavelli, and K. Rajashekara, "A 1200-V, 60-A SiC MOSFET Multichip Phase-Leg Module for High-Temperature, High-Frequency Applications," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2307–2320, 2014.

[11] P. Beckedahl, S. Buetow, A. Maul, M. Roeblitz, and M. Spang, "400 A, 1200 V SiC power module with 1nH commutation inductance," in *International Conference on Integrated Power Electronics Systems (CIPS)*, 2016, pp. 1–6.

[12] K. Takao and S. Kyogoku, "Ultra low inductance power module for fast switching SiC power devices," in *IEEE International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, 2015, pp. 313–316.

[13] A. K. Solomon, A. Castellazzi, N. Delmonte, and P. Cova, "Highly integrated low-inductive power switches using double-etched substrates with through-hole viases," in *IEEE International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, 2015, pp. 329–332.

[14] F. Yang, Z. Liang, Z. J. Wang, and F. Wang, "Design of a low parasitic inductance SiC power module with double-sided cooling," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 3057–3062.

[15] S. Seal and A. H. Mantooth, "High Performance Silicon Carbide Power Packaging—Past Trends, Present Practices, and Future Directions," *Energies* , vol. 10, no. 3. 2017.

[16] H. Li, S. Munk-Nielsen, S. Bęczkowski, and X. Wang, "SiC MOSFETs based split output half bridge inverter: Current commutation mechanism and efficiency analysis," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014, pp. 1581–1588.

[17] Q. Yan *et al.*, "Performance Evaluation of Split Output Converters With SiC MOSFETs and SiC Schottky Diodes," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 406–422, 2017.

[18] F. Yang, Z. Liang, Z. Wang, and F. Wang, "Parasitic inductance extraction and verification for 3D Planar Bond All Module," in *International Symposium on 3D Power Electronics Integration and Manufacturing (3D-PEIM)*, 2016, pp. 1–11.

[19] Z. Chen, D. Boroyevich, P. Mattavelli, and K. Ngo, "A frequency-domain study on the effect of DC-link decoupling capacitors," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2013, pp. 1886–1893.