Development of a Low-inductance SiC Trench MOSFET Power Module for High-Frequency Application

Zhiqiang (Jack) Wang[1], Fei Yang[2], Steven Campbell[1], Madhu Chinthavali[1]

[1]Power Electronics and Electric Machinery Group
Oak Ridge National Laboratory
Knoxville, TN 37932, USA
wangz@ornl.gov

[2]Center for Ultra-wide-area Resilient Electric Energy Transmission Networks (CURENT)
The University of Tennessee
Knoxville, TN 37996-2250, USA

***Abstract*—This paper deals with the development of a low-inductance multiple-chip power module with state-of-art 1200 V SiC Trench MOSFETs for high-frequency application. Specifically, a phase-leg power module package with integrated decoupling capacitance is fabricated based on P-cell/N-cell concept, and the packaging design is discussed in detail. Dedicated double pulse test is built, and a gate driver with cross-talk suppression function is designed to support the fast switching speed operation of SiC Trench MOSFETs. The parasitic inductance and current density distribution of the power module are simulated and extracted for the purpose of voltage spike limiting. The temperature dependent static and switching characteristics of the developed module are evaluated as well, and the key differences from traditional SiC double-diffused MOS (DMOS) are identified and discussed. Based on the turn-off switching characterization results, a lumped equivalent power-loop parasitic inductance of ~ 6 nH is achieved for the designed power module.**

Keywords—SiC Trench MOSFET; multiple-chip power module; low parasitic inductance

I. INTRODUCTION

SiC power devices have been characterized extensively in both discrete packages and power modules [1]–[9], and their benefits are being acknowledged. While state-of-art SiC power devices generally use Vertical-DMOS structure, Trench-MOS structure can further reduce the on-resistance and junction capacitance, leading to higher current density and faster switching speed. To thoroughly exploit the unique capability of SiC Trench MOSFET, power module packaging with low parasitic inductance needs to be developed.

Previously, various low parasitic inductance modules have been designed for SiC DMOS [10]–[14]. Due to the noncommercial availability of bare die SiC Trench MOSFET, there are few papers dealing with its packaging design. In [15], four 900V SiC Trench MOSFETs from Rohm are paralleled to form a switch position for a phase leg module. Fast switching is achieved together with an on-resistance of 1.5 mΩ per switch position. Meanwhile, the package layout is designed to ensure symmetric loop inductance for paralleled devices. In another recent literature [16], a 1200V/100A SiC Trench phase leg module is fabricated with Infineon Trench MOSFET. Low specific on-resistance is achieved compared to traditionally DMOS. Nonetheless, the detailed packaging design and comprehensive evaluation of multi-chip SiC Trench MOSFET power module are still lacking.

In this paper, a low inductance SiC Trench module with embedded decoupling capacitance is designed and fabricated based on the P-cell/N-cell concept [17]. First, the detailed layout design is introduced. Then, the temperature dependent static and switching characteristics of the fabricated module under different gate resistances and load current levels are evaluated and discussed. Based on the turn-off switching performance evaluation, the power loop parasitic inductances are calculated and compared with simulation results to verify the effectiveness of the designed package.

II. DESIGN OF MULTIPLE-CHIP POWER MODULE

1200 V SiC Trench MOSFETs and 1200 V SiC Schottky diodes from Rohm are used in this phase leg power module. The current ratings of each MOSFET and each diode are around 50A at 25°C case temperature.

P-cell/N-cell design concept is adopted for the power module layout for minimized power-loop inductance. Fig. 1 shows the circuit schematic of the module. To be specific, all the devices on each P-cell are paralleled and located close together, and the rest devices belonging to N-cell are placed in a similar way. Then, the current commutation loops for both P-cell and N-cell are optimized in terms of reducing the value of power loop inductance. The middle points of the P-cell and N-

cell are connected through direct-bonded-copper (DBC). In this design, six MOSFETs and three diodes constitute one P (N)-cell. L_{ds_P} and L_{ds_N} represent the power loop inductance of the P-cell and N-cell respectively. The power loop inductances of each cell are optimized in the package layout in order to utilize the benefits of fast-switching capability of SiC Trench MOSFET. Fig. 2 illustrates the real physical layout of the package. Decoupling capacitors are directly embedded inside the module to mitigate the overall switching loop inductance.

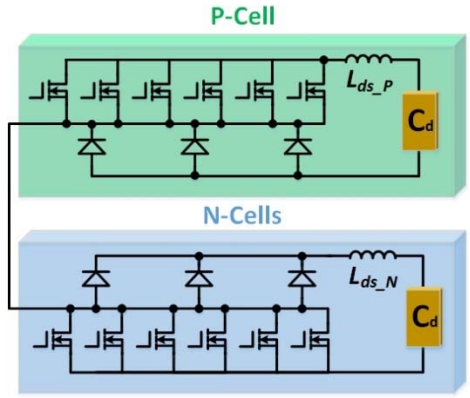


Fig. 1. Circuit diagram of the power modules.

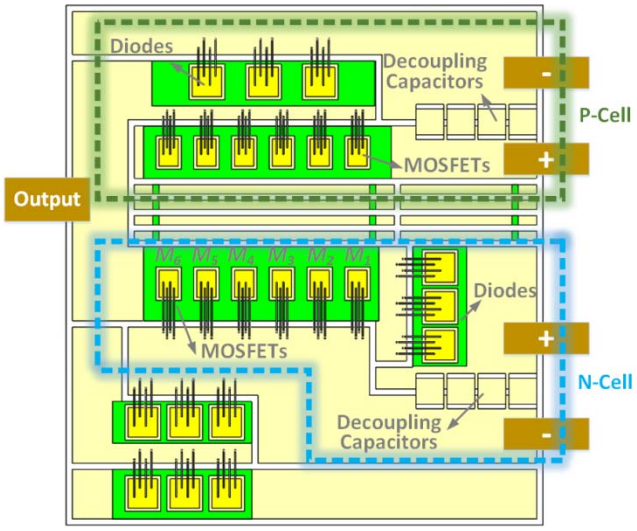


Fig. 2. Physical package layout of the phase leg module.

Using the extraction method in [22], the power loop parasitic inductance and current distribution of the designed layout are obtained through simulation using the ANSYS Q3D Extractor. The current distribution within both switching loop areas is also simulated, as shown in Fig. 3. Current is evenly distributed among the bare dies within both switching loop areas.

One limitation of this design is that the values of power loop inductance for each paralleled device are not the same. As a result, those paralleled devices will have different voltage spikes during the switching transients. Take N-cell layout for example, six MOSFETs (M_1 to M_6) are paralleled as the lower active switch. M_1 is located closer to the decoupling capacitors while M_6 is further away as shown in Fig. 2. The power loop inductance values of M_1 to M_6 are simulated as summarized in Table I.

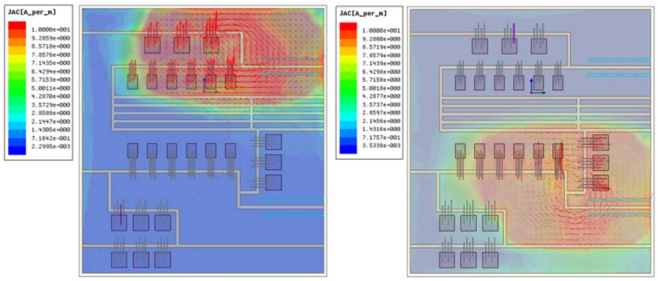


Fig. 3. Current distribution of P-cell (left) and N-cell (right).

TABLE I. COMPARISON OF POWER LOOP INDUCANCE FOR DIFFERENT DEVICES IN PARALLEL.

Device	Turn-off Inductance during di/dt
M_1	4.58 nH
M_2	4.87 nH
M_3	5.09 nH
M_4	5.78 nH
M_5	6.32 nH
M_6	6.71 nH

As can be seen, M_6 has the largest power loop inductance, and its voltage spike during turn-off will also be higher than other devices under the same conditions. To verify this analysis, dedicated Kelvin drain-to-source sensing pins are designed to measure the real voltages across the device accurately during switching transients. More details will be elaborated further in the experiment verification section. Fig. 4 shows the physical location of those sensing pins along with the location of gate signal pins.

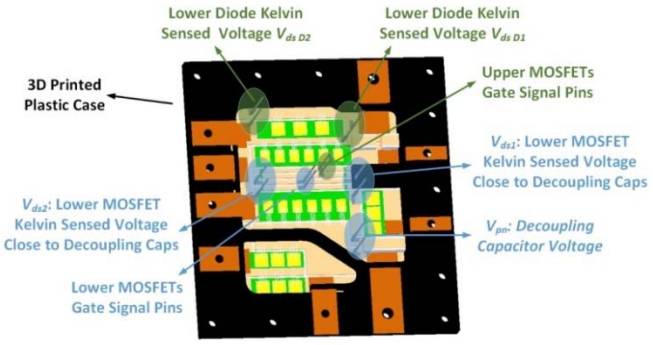


Fig. 4. Location of Kelvin gate signal pins and voltage sensing pins.

3D printed house is designed to press the DBC substrate in close contact with the baseplate. Thermal grease is used in between the bottom of the DBC and the top of the baseplate. All the gate signal pins and voltage sensing pins are connected to the gate drive board, which is mounted right on top of the module. The fabrication procedures include several key steps: 1) die-attach, and pin-attach (gate, source, and voltage sensing pins); 2) die interconnection using 5-mil wire bonds; 3) power terminal attach and house attach; 4) encapsulation to protect the die and wirebonds from mechanical and chemical damage. The fabricated power module is shown in Fig. 5.

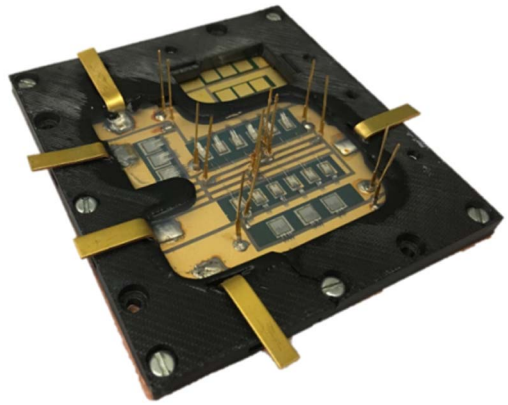


Fig. 5. Fabricated phase leg module.

III. STATIC CHARACTERIZATION

The static performance of the 1200 V SiC Trench MOSFETs are characterized with Keysight B1505a curve tracer. The power module is sitting on top of a hot plate, and its temperature dependent characteristics are evaluated. Fig. 6 shows the test set up for static characterization.

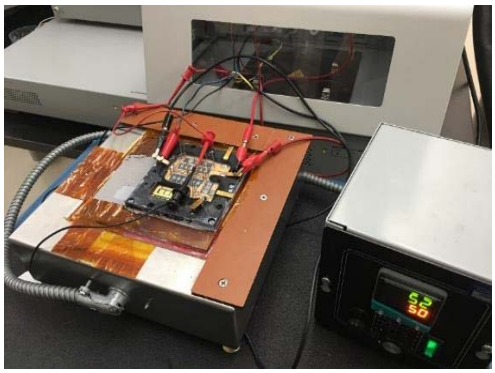


Fig. 6. The test set up for static characterization of the 1200 V SiC Trench MOSFET module.

The output characteristic of low-side MOSFETs is measured, as shown in Fig. 7. The on-resistance increases as temperature increases at high gate voltage such as 20V, while the opposite trend is observed at lower gate voltages. This trend, similar to SiC DMOS, can be explained by the fact that the channel resistance $R_{on,channel}$ decreases at elevated temperature while the drift region resistance $R_{on,drift}$ increases as temperature rises. When the gate voltage V_{gs}=20 V, the on-resistance $R_{ds,on}$ is mainly dominated by the drift region resistance. Therefore, a positive temperature coefficient of on-resistance is observed. On the contrary, the channel resistance is more significant role at $V_{gs} = 10\ V$ or lower. Consequently, the on-resistance behaves an opposite temperature coefficient. The temperature dependent on-resistance at 20V gate voltage is summarized in Fig. 8. At room temperature, the on-resistance value is 7.46 $m\Omega$. The positive temperature coefficient of on-resistance is beneficial for current balancing of multi-chip modules. The transfer characteristic is shown in Fig. 9, which presents the coherent feature of output characteristic. As junction temperature increases, the threshold voltage is decreasing, while the transconductance is slightly increased at elevated temperatures.

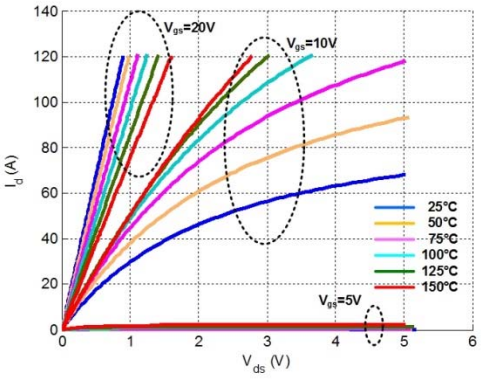


Fig. 7. Output characteristics of SiC Trench MOSFETs.

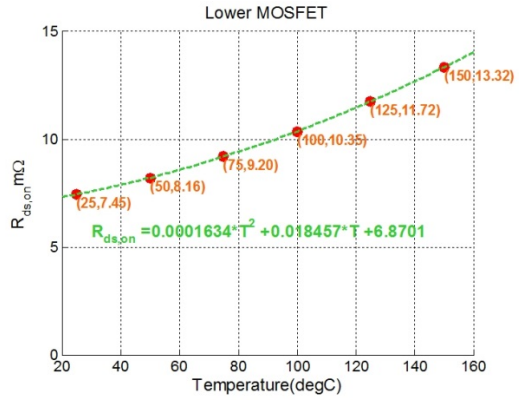


Fig. 8. Temperature dependent on-state resistance.

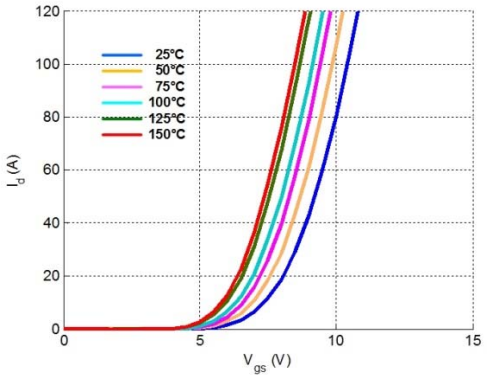


Fig. 9. Low-side MOSFETs transfer characteristics

Meanwhile, the body diode of the Trench MOSFETs are evaluated at various junction temperatures with $V_{gs} = 0\ V$. Fig. 10 shows the characteristics of low-side MOSFETs. Below 50 A, the forward voltage drop and equivalent on-resistance of its body diode present a negative temperature coefficient, which indicates the body diodes may not be suitable for paralleling in terms of current sharing.

At room temperature, the low-side MOSFETs' body diode is also characterized at different gate voltages as shown in Fig. 11. The forward characteristic with $V_{gs} = 0\ V$ is shown in the blue line while the forward curve with $V_{gs} = -5\ V$ is drawn in red. Obviously, the curve shifts to the right as the gate voltage decreases, as summarized in Table II. If anti-parallel diodes are not used, the load current would flow through the body diodes

during dead time. Consequently, more conduction loss would be induced in the body diode if a negative gate voltage is applied. In the case where anti-parallel diodes are used, a negative gate voltage helps to prevent body diode conduction.

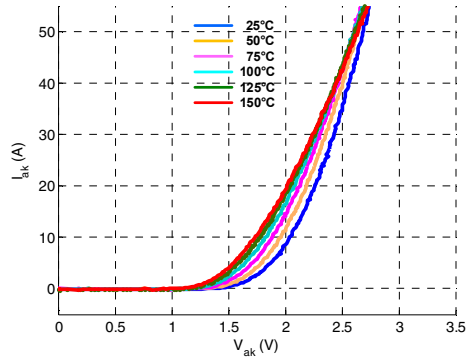


Fig. 10. Temperature-dependent forward characteristics of body diodes.

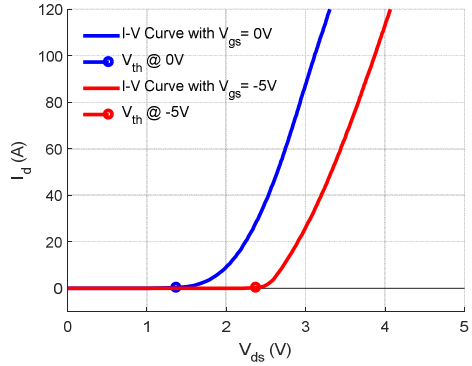


Fig. 11. Forward characteristic of body diodes with different gate voltages.

TABLE II. PARAMETER SHIFT OF BODY DIODE AT DIFFERENT GATE VOLTAGES.

V_{gs}	V_{th}	R_{diode}
0 V	1.37 V	10.0 mΩ
-5 V	2.37 V	11.4 mΩ

The anti-parallel SiC Schottky diodes are also characterized. The output characteristic of the low-side paralleled diodes at different junction temperatures is shown in Fig. 12. As expected, as T_j increases the threshold voltage decreases while the resistance increases. With a current level higher than 30 A, a positive temperature coefficient is observed, and the anti-parallel diodes are suitable for parallel operation at high current.

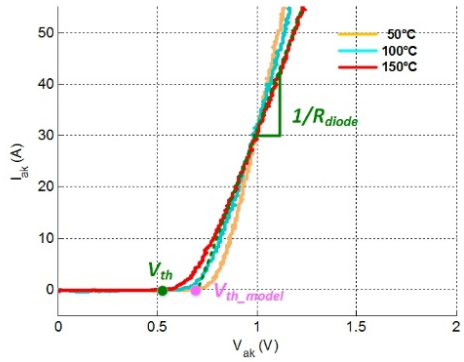


Fig. 12. Low-side anti-parallel diode I-V characteristics at different T_j.

The voltage blocking capability and nonlinear junction capacitance of the devices are characterized as well before conducting switching performance evaluation. Fig. 13 illustrates the voltage blocking capability of the Trench devices under different junction temperatures. With a DC blocking voltage of 900 V, a leakage current of less than 20 nA is observed. For accurate capacitance measurement, a special fixture is designed to accommodate the power module to the factory fixture to compensate the error caused by connection wires. Specifically, a rectangle piece of phenolic board is cut. Then three holes are drilled with male banana connectors screwed inside. One side of the banana connectors are mated with the curve tracer unit, and the other side is soldered to separate magnet wires representing gate, drain source. Afterward, the magnetic wires are bent to fit the power module terminals and the wires' positions are fixed with tape. Open and short calibrations are implemented to compensate the impedance introduced by the wires. Fig. 14 shows these two compensation connections. The power module is lastly connected to the fixture for testing as shown in Fig. 15.

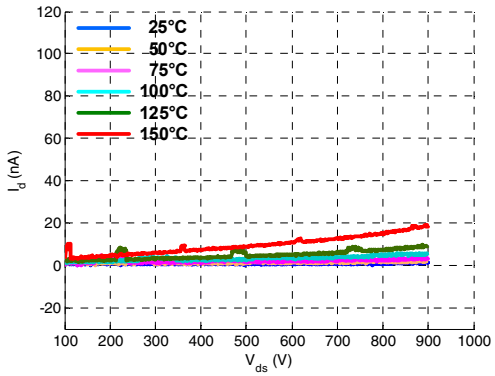
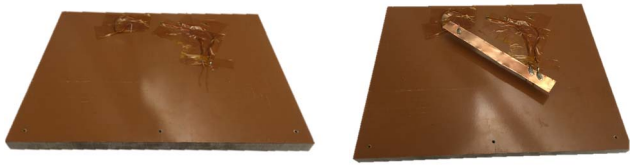


Fig. 13. Characterization of low-side MOSFET's blocking capability.



(a) Open compensation (b) Short compensation

Fig. 14. Compensation of the connection wires for C-V measurement.

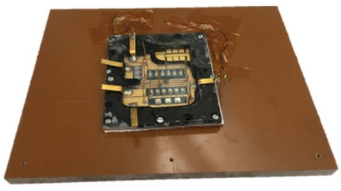


Fig. 15. Power module in connection with a fixture for C-V test.

The nonlinear junction capacitance versus drain-to-source voltage of the SiC Trench MOSFETs is shown in Fig. 16. Both high-side and low-side MOSFETs have identical capacitance values. At a dc voltage of 600 V, the energy-equivalent capacitor value is calculated to be 807.62 pF. Similarly, the 1200V SiC Schottky diode is tested using the same method. The testing result is shown in Fig. 17 for both high-side and low-side anti-parallel diodes. 761.92 pF is obtained for the energy-equivalent capacitor value at 600 V.

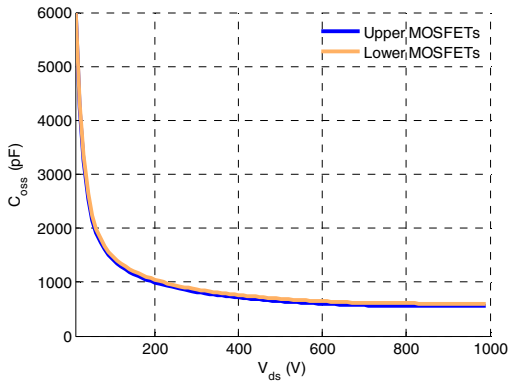


Fig. 16. MOSFETs' nonlinear junction capacitance versus voltage.

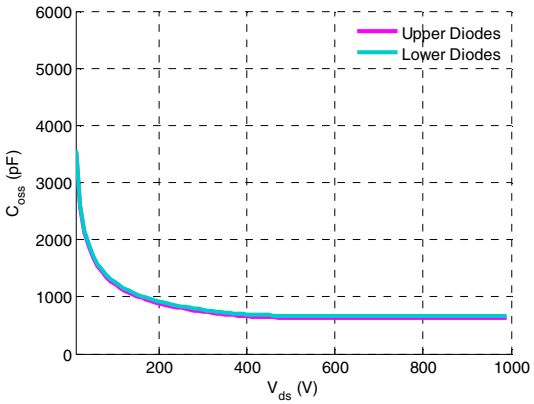


Fig. 17. Schottky diodes' nonlinear junction capacitance versus voltage.

IV. Switching Characterization

A gate driver with cross-talk suppression function and a double pulse test power stage are designed to support the fast switching speed and high frequency operation of the developed power module, and the overall test setup is shown in Fig. 18.

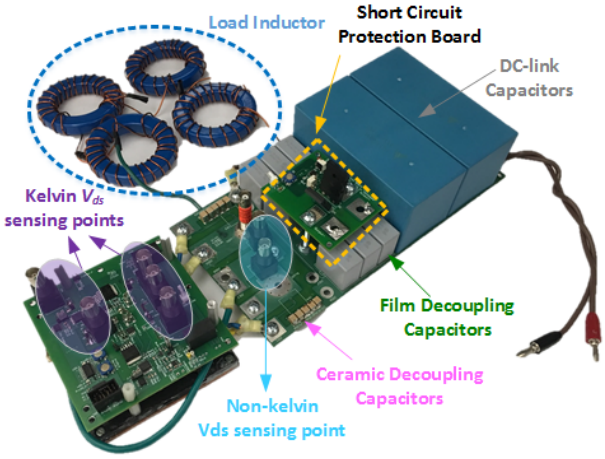
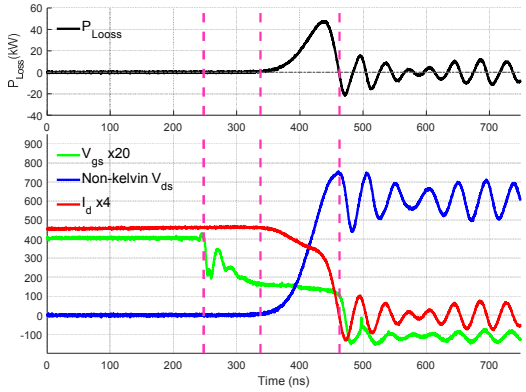


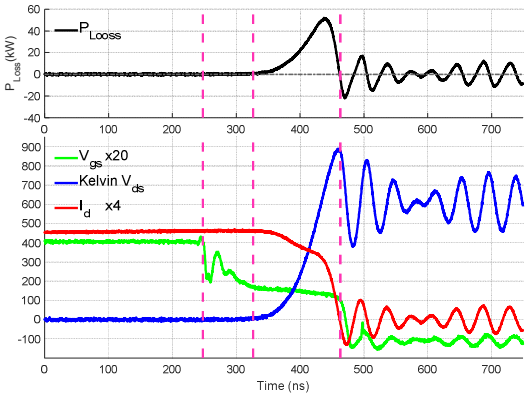
Fig. 18. Double pulse test setup.

A. Comparison of Kelvin and Non-Kelvin Voltage Sensing

As discussed previously, the real device voltage is accessible through the Kelvin connection pins within the module. A switching comparison is conducted for the module using Kelvin and non-Kelvin connection. The turn-off and turn-on switching waveforms are shown in Fig. 19 and Fig. 20 respectively for Kelvin and non-Kelvin cases, with a load current of 120 A and dc-link voltage of 600 V. The external gate resistance is selected to be 5 Ω.



(a) Non-kelvin V_{ds}



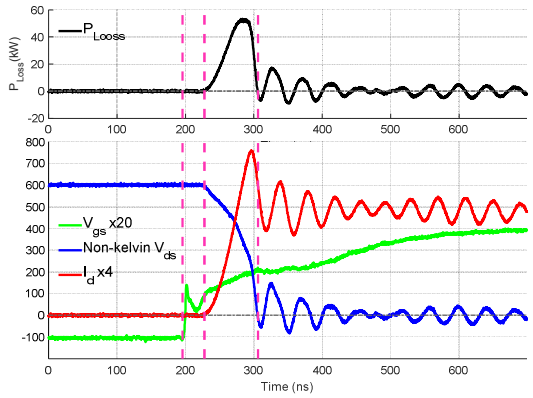
(b) Kelvin V_{ds}

Fig. 19. Experimental turn-off switching waveforms at 600 V, 120 A and $R_{g,ext} = 5\ \Omega$.

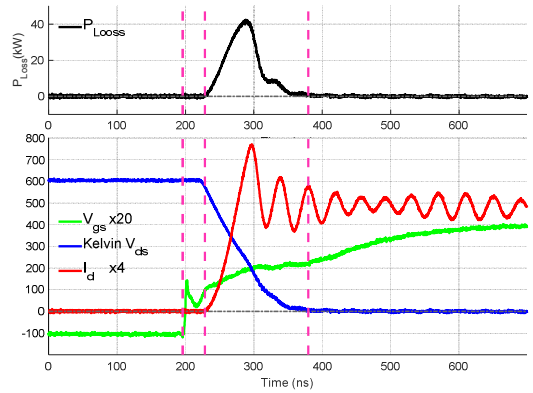
During turn-off transient, the inductive load current shifts from the low-side MOSFETs to the high-side anti-parallel diodes. The drain current of low-side MOSFETs has a negative slew rate. Therefore, the Kelvin voltage V_{ds_kelvin} is higher than $V_{ds\_non\_kelvin}$ during turn-off due to the extra parasitic inductance between Kelvin and non-Kelvin sensing points. This is verified experimentally in Fig. 19: the Kelvin V_{ds} is ~900 V while non-Kelvin V_{ds} is ~750 V. As a result, the turn-off switching loss would be larger if it is calculated from Kelvin V_{ds}.

On the other hand, the Kelvin sensed voltage is lower during turn-on as the slew rate of drain current changes to a positive value. Fig. 20 shows the comparison of voltage waveforms during turn-on. As can be seen, the profile of V_{ds} is changed when the voltage is measured from the Kelvin sensing pins, and the drain-source voltage drops faster during the initial stage compared to $V_{ds\_non\_kelvin}$, contributing to a lower switching loss.

At $R_{g,ext} = 10\ \Omega$, the switching losses are compared for calculations from different voltage sensing points as shown in Fig. 21. It can be seen that although the turn-on and turn-off loss values are different, the total switching energy loss is almost the same within the tested current range.



(a) Non-kelvin V_{ds}



(b) Kelvin V_{ds}

Fig. 20. Experimental turn-on switching waveforms at 600 V, 120 A and $R_{g,ext} = 5\ \Omega$.

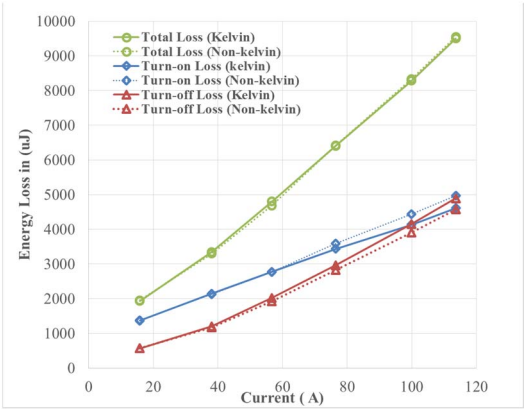


Fig. 21. Switching loss comparison of Kelvin and non-Kelvin voltages with $R_{g,ext} = 10\ \Omega$.

B. Temperature Dependent Turn-on Loss Evaluation

The temperature dependent switching performance of the power module is evaluated under junction temperatures from 25ºC 125 ºC with different gate resistances, and the Kelvin voltage is used for switching loss characterization of the module.

Fig. 22 shows the turn-on switching waveforms of low-side MOSFETs at various junction temperatures with $R_{g,ext} = 5\ \Omega$. As temperature increases, the gate threshold voltage V_{th} decreases and transconductance g_m increases. Therefore, during the current rising stage, the drain current rises more quickly at higher temperatures owing to a faster slew rate of transconductance, as indicated in the equation below:

$$t_{ir} = R_g C_{iss} ln(\frac{V_{cc}-V_{th}}{V_{cc}-V_{miller}}) = R_g C_{iss} ln[\frac{V_{cc}-V_{th}}{V_{cc}-(V_{th}+\frac{I_L}{g_m})}] \quad (1)$$

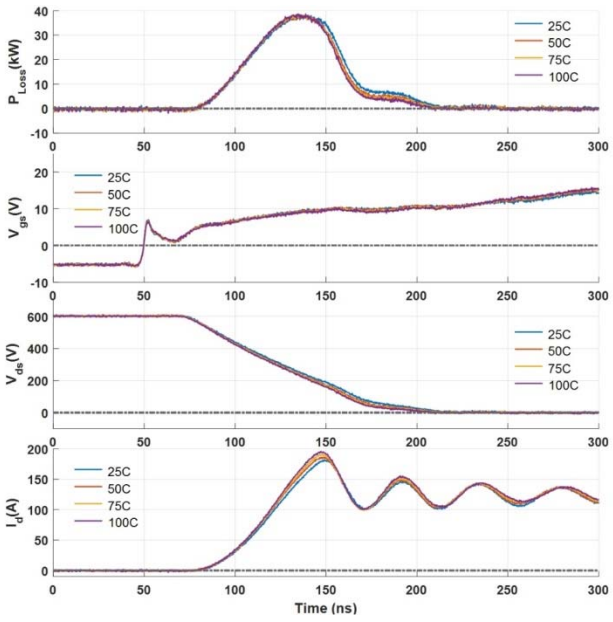


Fig. 22. Turn-on waveforms at different junction temperatures with $R_{g,ext} = 5\ \Omega$.

Considering the increased switching speed and the power loop inductance, the voltage drop across the device will also drop more quickly. Therefore, the switching loss during current rise time will be smaller as temperature increases.

During voltage falling stage, the gate miller plateau voltage V_{miller} can be expressed by (2), where I_L is the load current. At higher T_j, the plateau voltage will be lower. As a result, the gate current increases and the voltage fall time t_{vr} will decrease as indicated in (3), where R_g is the total gate resistance, V_{cc} is the positive gate voltage and Q_{gd} is the total charge needed to discharge C_{gd} from high voltage to on-state voltage. Therefore, the turn-on loss during voltage falling stage will decrease at higher junction temperatures.

$$V_{miller} = V_{th} + \frac{I_L}{g_m} \quad (2)$$

$$t_{vf} = \frac{R_g Q_{gd}}{V_{CC}-V_{miller}} \quad (3)$$

Combining the turn-on loss variation during current rising stage and voltage falling stage, the total turn-on switching loss will decrease as temperature increases. Fig. 23 shows the experimental turn-on switching loss results at different combinations of operating conditions. At higher junction temperature, the turn-on switching loss is lower, validating the previous theoretical analysis. Meanwhile, the turn-on loss is reduced with lower gate resistance as expected.

C. Temperature Dependent Turn-off Loss Evaluation

The turn-off waveforms under the same operating conditions as turn-on transients are shown in Fig. 24. The turn-

off loss is mainly generated in the voltage rising and current falling stages.

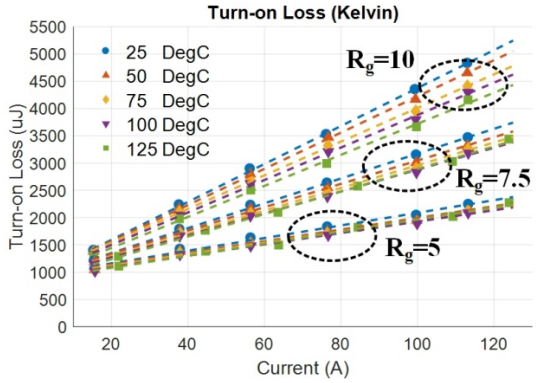


Fig. 23. Turn-on loss data at different T_j, $R_{g,ext}$ and load current.

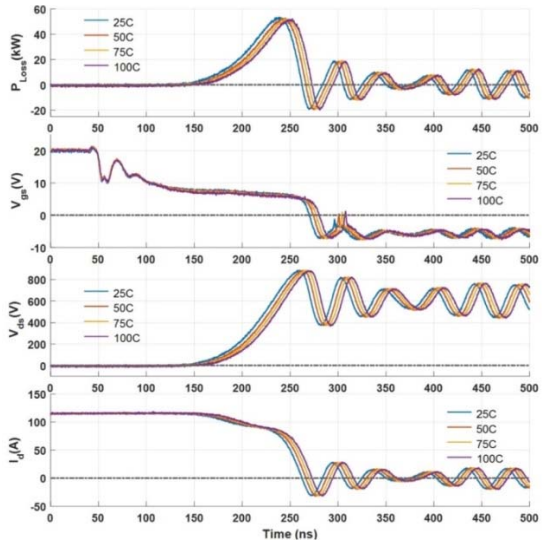


Fig. 24. Turn-off waveforms at different junction temperatures with $R_{g,ext} = 5\ \Omega$.

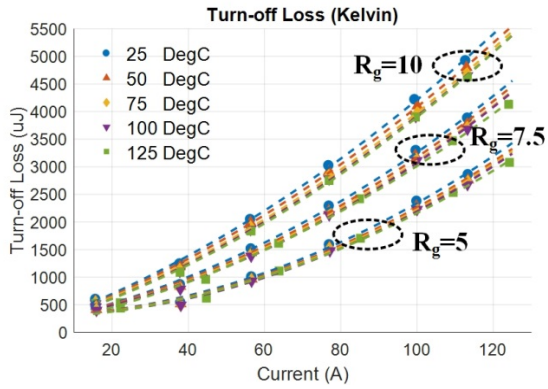


Fig. 25. Turn-off loss data at different T_j, $R_{g,ext}$ and load current.

During the voltage rising stage, the gate voltage is almost constant and stays at V_{miller}. The miller plateau voltage is mainly determined by load current I_L as indicated in (2). As discussed previously, under the same load condition V_{miller} will be lower as T_j increases. Therefore, the gate discharge current will decrease, and the voltage rise time t_{vr} will increase as indicated in (4), where V_{ee} represents the negative gate drive voltage. Consequently, the switching loss during the voltage rising stage $E_{off,VR}$ will increase at elevated temperatures.

$$t_{vr} = \frac{R_g Q_{gd}}{V_{miller} - V_{ee}} \tag{4}$$

During the current falling stage, the gate voltage is changing from V_{miller} to threshold the voltage V_{th} with a time constant $R_g \cdot C_{gs}$ considering a first order system in the gate loop. Both V_{miller} and V_{th} will decrease at higher T_j. However, the net result of $|V_{miller} - V_{th}|$ will decrease since the transconductance g_m is slightly increased as T_j builds up. Correspondingly, the current falling time will be lower as indicated in the following equation:

$$t_{if} = R_g C_{iss} ln(\frac{V_{miller}}{V_{th} - V_{ee}}) = R_g C_{iss} ln[\frac{(V_{th} + \frac{I_L}{g_m})}{V_{th} - V_{ee}}] \tag{5}$$

Moreover, as can be seen from the transfer characteristics in Fig. 9, the current slew rate will be a little bit faster as T_j builds up especially during the quadratic region. Thus, the channel current slew rate will increase at higher junction temperatures. Combining the reduced current falling time and the higher channel current slew rate, the resulting overlap loss during turn-off current fall time $E_{off,CF}$ will be lower.

The total turn-off loss consists of $E_{off,VR}$ and $E_{off,CF}$. $E_{off,VR}$ is increasing while $E_{off,CF}$ is decreasing as T_j elevates. Therefore, the total turn-off loss can be either positive or negative temperature coefficient. Fig. 25 shows the experimental turn-off loss data under different conditions. For the tested device, the turn-off loss is decreasing as junction temperature increases.

D. Experimental Parasitic Inductance Extraction

The parasitic inductance of the module is also extracted and compared with simulation results. To obtain the value of parasitic inductance, only the N-cell is connected to the double pulse board, and circuit diagram is drawn in Fig. 26. In the figure, V_{PN} represents the bus voltage across the terminal of the power module. V_{ds1} represents the Kelvin voltage of devices closest to the decoupling capacitors while V_{ds2} is the voltage of the device most far away from decoupling capacitors.

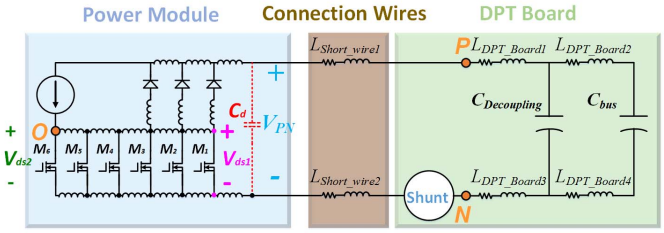


Fig. 26. Circuit diagram of the N-cell double pulse test set up.

The same parasitic inductance extraction method has been discussed in [18]. The voltage across V_{PN} is compared with the real voltage across the devices, and the parasitic inductance values are derived based on the voltage difference and drain current slew rate measured from coaxial shunt. To ensure the channel *di/dt* is dominating during the turn-off process, a large external gate resistor (10 Ω) is selected, and the device is turned off at a large load current of 138 A. Fig. 27 illustrates

the turn-off waveforms of terminal voltage V_{PN}, Kelvin sensed voltage V_{ds1} and load current I_{ds}. The power loop parasitic inductance obtained from V_{ds1} is calculated to be:

$$L_{ds1} = 19.09\ \text{V}/(3.18\ \text{A/ns}) = 5.15\ \text{nH}. \quad (6)$$

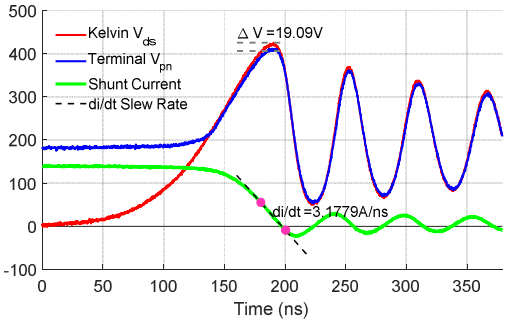


Fig. 27. Turn off waveforms for extraction of L_{ds} from V_{ds1}.

Compared to the simulation values summarized in Table I, this value is in between the parasitic inductance value of M_1 and that of M_6; but it is closer to the value of M_1. This is reasonable because all the MOSFETs are conducting the current, and the extracted value cannot represent the parasitic inductance value considering a single device. Therefore, the extracted value is between the parasitic inductance value of M_1 (4.58 nH) and that of M_6 (6.71 nH). Moreover, since the sensing pins are located physically closer to M_1, the extracted value is closer to the parasitic value of M_1. Similarly, the power loop parasitic inductance is also extracted from V_{ds2} as shown in Fig. 28. The voltage spike is a little bit larger in the case of V_{ds2}, and the extracted value is:

$$L_{ds2} = 20.97\ \text{V}/(3.19\ \text{A/ns}) = 6.62\ \text{nH} \quad (7)$$

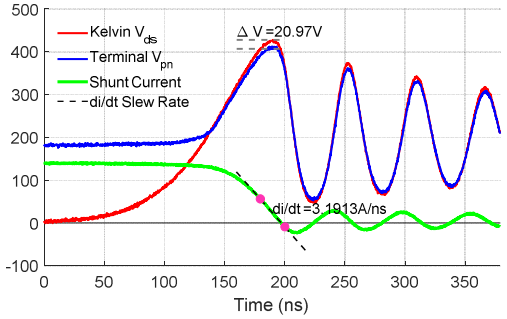


Fig. 28. Turn off waveforms for extraction of L_{ds} from V_{ds2}.

V. Conclusion and Future Work

This paper presents the design and development of a low-inductance multi-chip power module based on state-of-art 1200V SiC Trench MOSFETs. A comprehensive temperature dependent static and switching characterization are performed, and the switching loss variation is analyzed in detail. It is found that the specific SiC Trench MOSFET presents different switching loss trench compared to traditional SiC DMOS, i.e. both the turn-on and turn-off losses decrease as the junction temperature increases. Dedicated Kelvin voltage connection is implemented for parasitic inductance extractions. The experimental results match with the simulation results, and ~6 nH power-loop inductance is achieved by using P-cell/N-cell concept with embedded decoupling capacitance.

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