Loss Analysis and Mapping of a SiC MOSFET Based Segmented Two-Level Three-Phase Inverter for EV Traction Systems

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***Abstract*—Emerging wide-bandgap based power semiconductor devices are gaining popularity in power electronic systems for automotive applications with the aim of increased power density, reduced weight and increased efficiency. In this work, loss analysis and mapping of a segmented two-level inverter based on SiC MOSFETs are presented in order to identify the challenges in design of power electronics and electric machines for EV applications. The paper starts with description of the EV traction system that is chosen as the study case, followed by segmented inverter topology, power device selection and sizing. The theoretical switching, conduction and dead-time conduction loss analysis for the SiC MOSFETs in the segmented two-level inverter topology are presented under any given operating condition. The analysis is followed by loss mapping of the motor, inverter and overall EV traction system. The loss maps of the inverter and the motor show that each component has different thermal loading trends under given torque-speed characteristics. Therefore, various operating conditions have to be considered for the design of traction system components to ensure reliability and high performance, which are critical requirements for EV systems.**

***Index terms*—** Wide bandgap (WBG) power devices, electric vehicles (EV), SiC MOSFET, segmented inverter, traction systems.

I. Introduction

Wide-bandgap (WBG) based power semiconductor devices, specifically silicon carbide (SiC) MOSFETs and gallium nitride (GaN) HEMTs have gained attention from automotive industry due to well known superior properties in comparison to conventional silicon (Si) based MOSFETs and IGBTs. Si based MOSFETs provide high switching speeds due to unipolar conduction mechanism, but suffer from high conduction losses due to increased on-state resistance at high blocking voltage class (above 600 V) due to absence of minority carriers [1], [2]. Because of unfeasible conduction performance of standard Si MOSFETs at high blocking voltage class (above 600 V), Si IGBTs gained popularity with excellent conduction performance with bipolar conduction mechanism, and with the penalty of reduced switching speed due to minority carrier existence in device channel. The superior performance of SiC MOSFETs and GaN HEMTs at 600 V blocking class, and SiC MOSFETs at 1200 V blocking class have been discussed thoroughly in literature [3], [4].

SiC MOSFETs have gained attention from electric vehicle (EV) system developers due to maturity of the technology in comparison GaN based devices and various papers have been published that show the benefits of using WBG devices for traction applications and wireless charging [5], [6]. It is shown that WBG devices can provide higher performance in comparison to Si devices under wide temperature and switching frequency range, which leads reduction in cooling and filtering requirements. The system weight and volume reduction in EV applications provide significant benefits in terms of range extension and researchers have been focusing on introducing new power electronic topologies, power devices, motor topologies and system architectures in order to advance the EV vehicle adoption. As the WBG devices and EV systems have not matured yet, the benefits of these devices with novel topologies for EV systems must be investigated.

In this study, a commercial EV traction system has been used to study the loss analysis and mapping of SiC MOSFET based segmented two-level three-phase inverter. The analysis can be used to identify the loss distribution in traction systems to optimize coupled or decoupled cooling system designs based on thermal loading from each system component. In Section II, the details of the commercial EV traction system have been presented. In Section III, the segmented inverter system description and analytical derivation of the conduction and switching losses for SiC MOSFET without external anti-parallel diode have been presented. In Section IV, the loss map of the permanent magnet (PM) traction motor, conduction and switching loss map of the inverter based on torque-speed

characteristics are discussed.

II. Case Study: 2016 BMW i3

Traditional traction systems for electric vehicles are based on two-level three-phase inverters with PM motors as the load. The simplified representation of this system configuration is presented in Fig. 1. The inverter utilizes the winding inductance in the three phase machine as an output filter, and six Si IGBTs with anti-parallel Si diodes are used to form the two-level three-phase inverter topology. The high voltage DC link in the schematic represents the DC distribution in the vehicle and can be directly connected to the battery system or to a step-up DC/DC converter depending on the battery voltage and system architecture. DC link capacitor C_{DC} provides ripple current for the inverter. The volume of the capacitor can be significant in traction systems due to large ripple current requirement of the inverter and high voltage DC link ripple current minimization effort to maximize the battery life.

Oak Ridge National Laboratory have evaluated various commercial electric and hybrid electric vehicles in order to confirm power electronics and electric motor technology status and identify barriers and gaps to prioritize/identify R&D opportunities. Over the years, 11 different vehicles have been evaluated and the evaluation results can be found in [7] and [8]. Among the evaluated systems, 2016 BMW i3 has the highest peak power density [kW/L] and specific power density [kW/kg] for the motor and the inverter, and therefore for the overall traction system. Due to this reason, it is selected as the suitable candidate to evaluate benefits of SiC MOSFETs in EV systems. The traction system parameters are presented in Table I. The peak power rating of the system is 125 kW, with 250 Nm maximum torque capability. Switching frequency is selected as 5 kHz and commercial two-level three-phase Si IGBT and Si diode based power module from Infineon is used for the inverter, which is presented in Fig. 2a. Four IGBTs and diodes are used in parallel for each switch in order to reach 550 A DC current rating at 75 ^{o}C module case temperature. The motor and the inverter are cooled with a series connected liquid cooling system. The system ratings specified in Table I are used as the design parameters of the SiC MOSFET based inverter design and loss analysis in the following sections. The

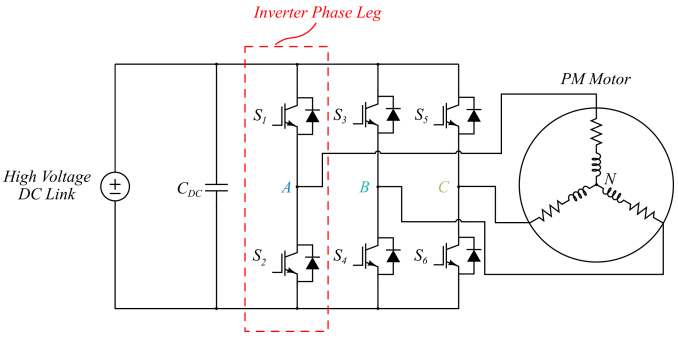
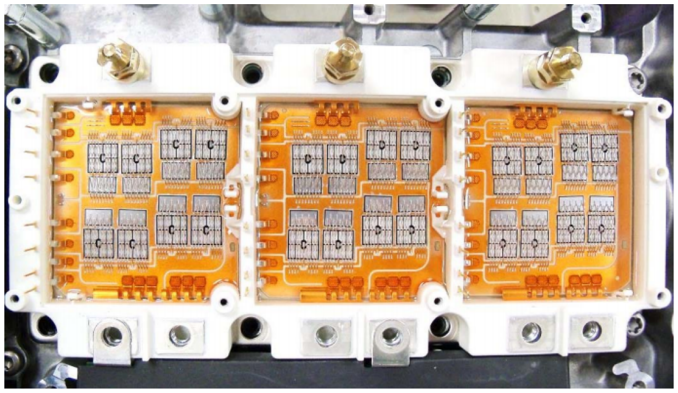


Fig. 1: Standard two-level three-phase inverter with PM traction motor in EV systems.

TABLE I: BMW i3 Traction System Parameters

Peak Power $P_{OUT_{pk}}$	125 kW
DC Link Voltage V_{DC}	360 V
Maximum Torque T_{max}	250 Nm
Inverter Topology	Two-level three-phase
Switching Frequency f_{sw}	5 kHz
Power Module	Infineon FS800R07A2E3
DC Link Capacitor C_{DC}	475 μF, 450 V
IGBT Collector Emitter Voltage V_{CE}	650 V
IGBT Collector Current I_C	550 A @ T_C=75 ^{o}C
Diode Forward Current I_F	550 A @ T_C=75 ^{o}C
Motor and Inverter Cooling	% 50 water, % 50 ethylene glycol liquid cooling



(a)

(b)

Fig. 2: (a) Two-level three-phase Si IGBT and Si Diode based power module [7], (b) permanent magnet motor used in BMW i3 traction system [8].

performance of the motor is characterized experimentally and the characterization results are used in this study to evaluate loss variation of the SiC based system under different torque-speed operating points.

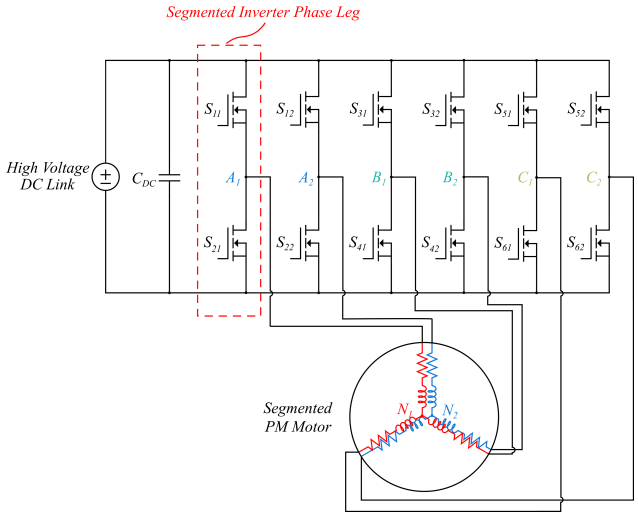


Fig. 3: Segmented two-level three-phase inverter with PM traction motor in EV systems.

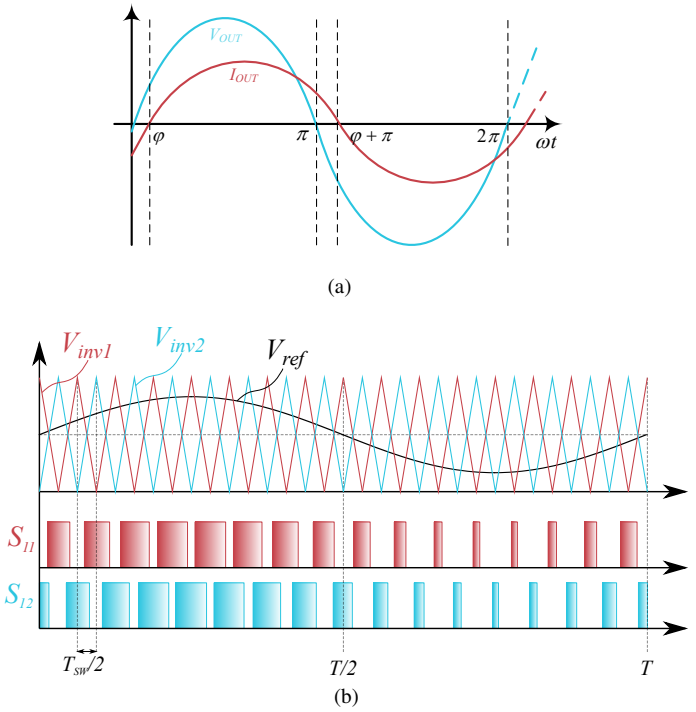


Fig. 4: a) Approximated output voltage and current waveforms for loss analysis and b) PWM signals for single phase in the segmented two-level configuration.

III. Segmented Two-Level Inverter and Loss Analysis

The standard two-level three-phase inverter presented in Fig. 1 requires a bulky capacitor to absorb the large ripple current caused by the pulse width modulated operation. In order to reduce the filtering requirements at the DC bus, a segmented topology is presented by Su et al. in [9], which can reduce the DC link bus capacitor up to 60 % without increasing total semiconductor area. The schematic of the proposed segmented system with SiC MOSFETs and the appropriate PWM signals for a single phase leg two-level configuration are presented in Figs. 3 and 4b respectively. The segmented phase legs X_1 and X_2, where X can be replaced with phase names A, B or C in Fig. 3, are modulated with sinusoidal PWM signals. The same reference signal V_{ref}, and $T_{sw}/2$ phase shifted carrier signals $V_{inv1,2}$ are used for segmented legs in each phase. With this configuration, the fundamental voltage waveforms generated by each segmented leg are identical and therefore, the total phase current is identical to non-segmented configuration. The DC link ripple current is reduced by splitting phase current into two branches and interleaving with 180 degrees phase shift.

A. Semiconductor Loss Analysis

The semiconductor power loss analysis in terms of conduction and switching losses is conducted to evaluate the performance of segmented two-level three-phase inverter. The segmented two-level three-phase inverter considered for this analysis is presented in Fig. 3. In this configuration, for reverse conduction, external anti-parallel diodes are not used, and synchronous rectification capability of SiC MOSFETs with intrinsic body diode conduction during dead-time is utilized. In [10], it is shown that it is practical to eliminate external body diode in voltage source inverters without compromising efficiency. However, dead-time should be minimized and dead-time losses have to be considered in loss analysis due to increased conduction losses across the intrinsic body diode of the SiC MOSFET.

The conduction and switching losses are calculated based on sinusoidal approximated output voltage and current waveforms, excluding switching ripple current and harmonics. The approximated output voltage and current waveforms for this analysis are illustrated in Fig. 4a. An arbitrary phase shift ϕ between output voltage and current is shown to derive conduction loss equations for any power factor condition. The output current of the inverter leg shown in Fig. 4a can be expressed as:

$$i(t) = \widehat{I}_{OUT} \cdot sin(\omega t - \phi) \tag{1}$$

where $\widehat{I}_{OUT}$ is the output current amplitude. According to Fig. 4b, the conduction time of each device can be expressed by duty cycle D. For phase A, the duty cycle of S_{11} or S_{12} during positive half of the output voltage is:

$$D_+(t) = \frac{1 + M \cdot sin(\omega t)}{2} \tag{2}$$

where M is the modulation index varying between 0 and 1. Modulation index is defined by the ratio of peak of phase output voltage and DC link voltage:

$$M = \frac{\widehat{V}_{OUT}}{\frac{V_{DC}}{2}} \tag{3}$$

Therefore the duty cycle for the lower switch D_- can be

calculated as follow:

$$D_{-}(t) = \frac{1 - M \cdot sin(\omega t)}{2} \tag{4}$$

After the definition of fundamental output voltage and current waveforms, duty cycle and phase shift; conduction and switching losses for each switch can be derived.

1) Conduction Loss: For SiC MOSFETs in the segmented phase leg shown in Fig. 3, the on-state voltage drop across the switch and therefore conduction loss at positive half without considering dead time effects can be calculated as follow:

$$v_{on}(t) = R_{DS} \cdot \frac{i(t)}{2} \tag{5}$$

$$P_{cond_+} = \frac{1}{2\pi} \int_0^{\pi} \frac{i(t)}{2} \cdot v_{on}(t) \cdot D_{+}(t) \cdot \mathrm{d}(\omega t) \tag{6}$$

$$\begin{aligned} P_{cond_+} =& \frac{1}{2\pi} \int_0^{\pi} \frac{\widehat{I}_{OUT}^2}{4} \cdot sin^2(wt - \phi) \\ & \cdot R_{DS} \cdot \frac{1 + M \cdot sin(wt)}{2} \cdot \mathrm{d}(\omega t) \end{aligned} \tag{7}$$

$$\begin{aligned} P_{cond_+} =& \frac{\widehat{I}_{OUT}^2 \cdot R_{DS}}{16\pi} \left[\frac{1}{4} sin(2\phi - 2wt) - \frac{\phi}{2} + \frac{wt}{2} \right]_0^{\pi} \\ & + \frac{\widehat{I}_{OUT}^2 \cdot R_{DS} \cdot M}{4 \cdot 4\pi \cdot 12} \Big[cos(2\phi - 3wt) \\ & - 3cos(2\phi - wt) - 6cos(wt) \Big]_0^{\pi} \end{aligned} \tag{8}$$

$$P_{cond_+} = \frac{\widehat{I}_{OUT}^2 \cdot R_{DS}}{16\pi} \left[\frac{\pi}{2} + M \cdot \left(\frac{cos(2\phi)}{3} + 1 \right) \right] \tag{9}$$

where R_{DS} is on-state resistance of the switch at given temperature. Similarly the conduction loss at negative state can be calculated:

$$P_{cond_-} = \frac{1}{2\pi} \int_0^{\pi} \frac{i(t)}{2} \cdot v_{on}(t) \cdot D_{-}(t) \cdot \mathrm{d}(\omega t) \tag{10}$$

$$\begin{aligned} P_{cond_-} =& \frac{1}{2\pi} \int_0^{\pi} \frac{\widehat{I}_{OUT}^2}{4} \cdot sin^2(wt - \phi) \\ & \cdot R_{DS} \cdot \frac{1 - M \cdot sin(wt)}{2} \cdot \mathrm{d}(\omega t) \end{aligned} \tag{11}$$

$$\begin{aligned} P_{cond_-} =& \frac{\widehat{I}_{OUT}^2 \cdot R_{DS}}{16\pi} \left[\frac{1}{4} sin(2\phi - 2wt) - \frac{\phi}{2} + \frac{wt}{2} \right]_0^{\pi} \\ & - \frac{\widehat{I}_{OUT}^2 \cdot R_{DS} \cdot M}{4 \cdot 4\pi \cdot 12} \Big[cos(2\phi - 3wt) \\ & - 3cos(2\phi - wt) - 6cos(wt) \Big]_0^{\pi} \end{aligned} \tag{12}$$

$$P_{cond_-} = \frac{\widehat{I}_{OUT}^2 \cdot R_{DS}}{16\pi} \left[\frac{\pi}{2} - M \cdot \left(\frac{cos(2\phi)}{3} + 1 \right) \right] \tag{13}$$

The total conduction loss for the half of the period can then be calculated as

$$P_{cond_t} = P_{cond_+} + P_{cond_-} = \frac{\widehat{I}_{OUT}^2 \cdot R_{DS}}{16} = \frac{I_{RMS}^2 \cdot R_{DS}}{8} \tag{14}$$

where I_{RMS} is the RMS value of the phase current. However, in reality, dead time between complementary switches have to be applied in order to avoid shoot through and the intrinsic body diode of the SiC MOSFET will conduct during this interval. As the on-state performance of the body diode is worse than the channel of the device, and the dead-time interval can be significant in comparison total switching period in high switching frequency applications; the ideal conduction loss Eqs. 9, 13 and 14 have to be modified. The on-state voltage drop across body diode of the SiC MOSFET v_{dt}, during dead-time can be expressed with the following equation:

$$v_{dt}(t) = -V_f + \frac{\widehat{I}_{OUT}}{2} \cdot R_{SD} \cdot sin(\omega t - \phi) \tag{15}$$

where V_f is on-state threshold voltage of the body diode and R_{SD} is the on-state resistance of the body diode. Based on Eq. 15, the dead-time conduction loss for 0 to ϕ region in Fig. 4a is:

$$P_{dt_1} = \frac{1}{2\pi} \int_0^{\phi} v_{dt}(t) \cdot \frac{i(t)}{2} \cdot t_{dt} \cdot 2 \cdot f_{sw} \cdot \mathrm{d}(\omega t) \tag{16}$$

$$\begin{aligned} P_{dt_1} =& \frac{t_{dt} \cdot f_{sw}}{\pi} \left[V_f \cdot \frac{\widehat{I}_{OUT}}{2} - V_f \cdot \frac{\widehat{I}_{OUT}}{2} \cdot cos(-\phi) \right. \\ & \left. + \frac{\widehat{I}_{OUT}^2}{4} \cdot R_{SD} \left(\frac{\phi}{2} - \frac{1}{4} sin(2\phi) \right) \right] \end{aligned} \tag{17}$$

Similarly, the dead-time conduction loss for ϕ to π region in Fig. 4a is:

$$P_{dt_2} = \frac{1}{2\pi} \int_{\phi}^{\pi} v_{dt}(t) \cdot \frac{i(t)}{2} \cdot t_{dt} \cdot 2 \cdot f_{sw} \cdot \mathrm{d}(\omega t) \tag{18}$$

$$\begin{aligned} P_{dt_2} =& \frac{t_{dt} \cdot f_{sw}}{\pi} \left[V_f \cdot \frac{\widehat{I}_{OUT}}{2} \left(cos(\pi - \phi) - 1 \right) \right. \\ & \left. + \frac{\widehat{I}_{OUT}^2}{4} \cdot R_{SD} \left(\frac{\pi - \phi}{2} + \frac{1}{4} sin(2\phi) \right) \right] \end{aligned} \tag{19}$$

Dead time t_{dt} also means reduction of conduction time as the applied gate pulse time is reduced by dead-time duration. The reduction of power loss in a switch due to dead-time can be calculated as follow:

$$\begin{aligned} P_{dt_{red}} = & \frac{1}{\pi} \int_0^{\pi} R_{DS} \cdot \frac{\widehat{I}_{OUT}^2}{4} \cdot sin^2(\omega t - \phi) \\ & \cdot t_{dt} \cdot f_{sw} \cdot \mathrm{d}(\omega t) \end{aligned} \tag{20}$$

$$P_{dt_{red}} = \frac{t_{dt} \cdot f_{sw} \cdot R_{DS} \cdot \widehat{I}_{OUT}^2}{8} \tag{21}$$

Considering symmetrical operation between positive and negative halves of the output waveform in Fig. 4a and conduction loss Eqs. 9, 13, 17, 19 and 21, the conduction loss of the switch S_{11} or S_{21} in the segmented two-level inverter can be expressed as:

$$P_{cond_{S_{11,21}}} = P_{cond_+} + P_{cond_-} + P_{dt_1} + P_{dt_2} - P_{dt_{red}} \tag{22}$$

2) Switching Loss: At any power factor condition, the total switching loss across a single switch S_{11} or S_{21} can be expressed as:

$$P_{switch_{S_{11,21}}} = P_{ON} + P_{OFF} + P_{RR_D} \tag{23}$$

where P_{ON} and P_{OFF} are the turn-on and turn-off switching power losses of the SiC MOSFET respectively and P_{RR_D} is the reverse recovery loss across the body diode of the MOSFET. In the datasheet of commercial SiC MOSFETs, the turn-on loss data usually includes the reverse recovery loss dissipated across the device under test. Therefore, three switching loss components specified in Eq. 23 are sufficient to calculate the switching losses in a two level phase leg. Based on the SiC MOSFET device datasheet or characterization results, the P_{ON}, P_{OFF} and P_{RR_D} can be calculated as:

$$P_{ON} = \frac{1}{2\pi}\int_0^{\pi} \frac{\widehat{I}_{OUT}}{2}\cdot sin(wt)\cdot V_{DC} \cdot f_{sw}\cdot \frac{E_{ON_{test}}}{V_{DS_{test}} I_{DS_{test}}} \mathrm{d}(wt) \tag{24}$$

$$P_{ON} = \frac{f_{sw}}{\pi}\cdot \frac{\widehat{I}_{OUT}}{2}\cdot V_{DC}\cdot \frac{E_{ON_{test}}}{V_{DS_{test}} I_{DS_{test}}} \tag{25}$$

$$P_{OFF} = \frac{1}{2\pi}\int_0^{\pi} \frac{\widehat{I}_{OUT}}{2}\cdot sin(wt)\cdot V_{DC} \cdot f_{sw}\cdot \frac{E_{OFF_{test}}}{V_{DS_{test}} I_{DS_{test}}} \mathrm{d}(wt) \tag{26}$$

$$P_{OFF} = \frac{f_{sw}}{\pi}\cdot \frac{\widehat{I}_{OUT}}{2}\cdot V_{DC}\cdot \frac{E_{OFF_{test}}}{V_{DS_{test}} I_{DS_{test}}} \tag{27}$$

$$P_{RR_D} = \frac{1}{2\pi}\int_0^{\pi} \frac{1}{6}\cdot t_b \cdot I_{RRM}\cdot V_{DC}\cdot f_{sw}\cdot \mathrm{d}(wt) \tag{28}$$

$$P_{RR_D} = \frac{f_{sw}}{12}\cdot t_b \cdot I_{RRM}\cdot V_{DC} \tag{29}$$

where test conditions such as switching loss energies $E_{ON,OFF_{test}}$ are normalized with respect to inverter operating conditions. I_{RRM} is the peak reverse recovery of the SiC MOSFET diode and t_b is the time for diode current to decay from I_{RRM} to zero. In Eqs 24-27, it is assumed that the switching losses P_{ON} and P_{OFF} change linearly with respect to change of I_{DS} and V_{DC}. However, depending on the device technology and rating, the P_{ON} and P_{OFF} might have nonlinear relationship with V_{DC} and I_{DS}. In that case, equations based on curve fitting of the switching loss data in datasheet can be used to improve accuracy of switching loss calculations.Finally, by using the equations in the previous sections, the total semiconductor loss in a segmented phase leg can be expressed as:

$$P_{Loss_t} = 2\cdot\left(P_{cond_{S_{11,21}}} + P_{switch_{S_{11,21}}}\right) \tag{30}$$

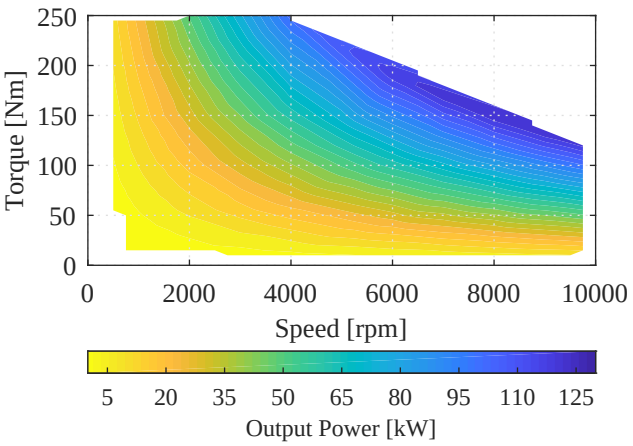


Fig. 5: Experimental mechanical power map of the PM traction motor.

IV. Device Selection and Loss Mapping

A. SiC MOSFET Die Selection and Sizing

The system parameters in Table I are used to determine current and voltage rating of the switches in the designed inverter. With given DC link voltage 360 V, SiC MOSFETs from two different manufacturers with 650 V and 900 V drain-source blocking ratings are considered. Potential SiC MOSFET bare dies with key parameters are presented in Table II. The number of parallel dies for each die has been selected to reach approximately 6 mΩ on-state resistance for each switch in a segmented leg at 125 ^{o}C case temperature. The dead-time and the switching frequency for the analysis are selected as 1 μs and 30 kHz respectively.

The experimental data from the characterization of the PM motor such as phase current I_{OUT}, motor torque T_m, motor speed ω_m and mechanical output power P_m are used as the input parameters for the loss analysis. The output power map of the characterized PM traction motor shown in Fig. 2b is presented in Fig. 5. To determine the maximum semiconductor power loss in the segmented inverter with the bare die options presented in Table II, maximum torque region in Fig. 5 is selected as the operating area although it is not close to maximum power region of the motor. In a PM machine, T_m can be considered proportional to I_{OUT}, and the switching and conduction losses in the devices are strongly linked to I_{OUT}, as it can be seen from the loss analysis in Section III. Therefore maximum loading region of the inverter will be the low speed, high torque operating region. The conduction and switching losses with three different dies at 30 kHz switching frequency are presented in Figs. 6 and 7 respectively. From Fig. 6, it can be seen that dies A and B provide the lower conduction loss in comparison to die C. However, from Fig. 7, it is clear that the increase in conduction loss with die C can be compensated by lower switching loss in comparison to dies A and B. At given operating conditions, the margin gained by lower switching loss with die C is not enough to compensate the increased conduction losses and the total semiconductor loss for three

TABLE II: SiC MOSFET Die Parameters

	Die A	Die B	Die C
V_{DS}	650 V	650 V	900 V
R_{DS} @ T_C=25 ^oC	22 mΩ	30 mΩ	10 mΩ
R_{DS} @ T_C=125 ^oC	29 mΩ	40 mΩ	12 mΩ
I_{DS} @ T_C=125 ^oC	65 A	49 A	140 A
E_{ON} @ T_C=25 ^oC	252 μJ @ I_{DS}= 36 A	168 μJ @ I_{DS}= 27 A	1.35 mJ @ I_{DS}= 100 A
E_{OFF} @ T_C=25 ^oC	201 μJ @ I_{DS}= 36 A	112 μJ @ I_{DS}= 27 A	0.83 mJ @ I_{DS}= 100 A
Number of parallel dies for $R_{DS_{11,21}} \approx$ 6 mΩ @ T_C=125 ^oC	5	7	2

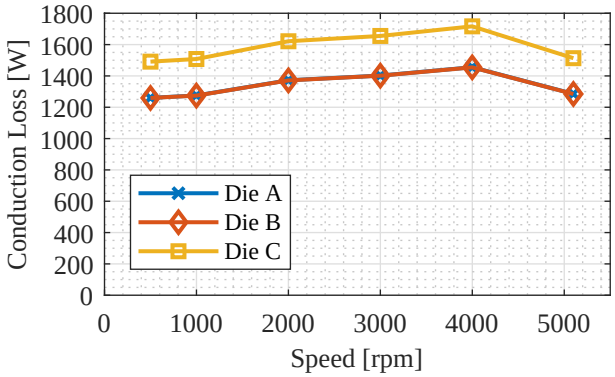


Fig. 6: Conduction loss of the segmented inverter at 30 kHz switching frequency.

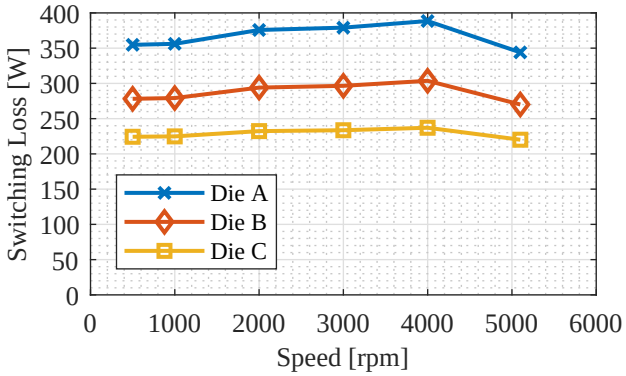


Fig. 7: Switching loss of the segmented inverter at 30 kHz switching frequency.

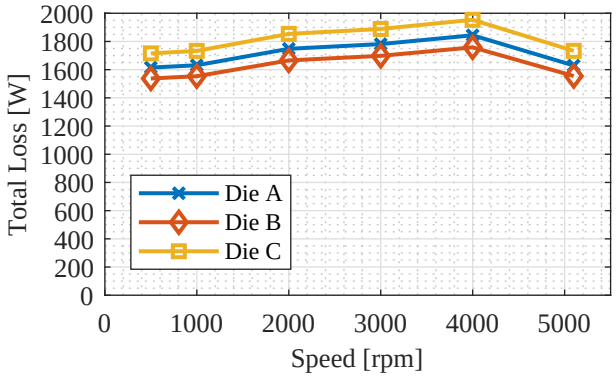


Fig. 8: Total semiconductor loss of the segmented inverter at 30 kHz switching frequency.

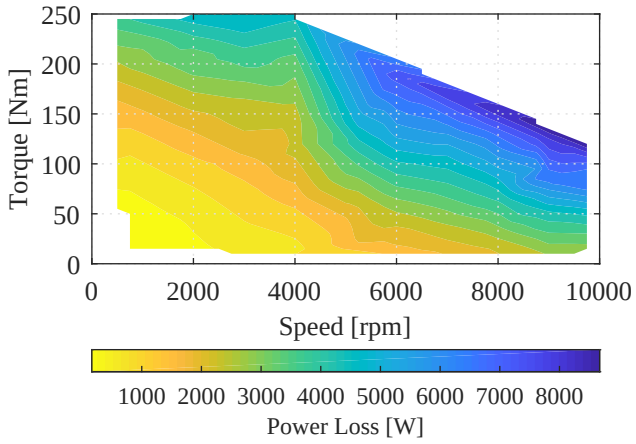


Fig. 9: Experimental loss map of the traction motor.

options are presented in Fig. 8. Die B die provides the lowest semiconductor losses, however the number of parallel dies per switch is higher than die A and die C options. Taking into consideration number of parallel dies per switch, total semiconductor losses, and distribution of power losses in the module to avoid thermal hot spots; die A is selected as the optimum die for this study. In the next section, loss mapping of the inverter, motor and combined system will be presented based on this selection.

B. Loss Mapping of the Designed System

According to the experimental characterization of the PM motor and the analytical loss derivation of the segmented two-level inverter with selected SiC MOSFET die in the previous section, the loss maps of the motor, inverter and overall traction system have been generated in order to characterize the power loss and therefore the thermal loading of the individual components, and the overall system under all possible steady state operating conditions.

Firstly, the loss map of the PM motor based on experimental

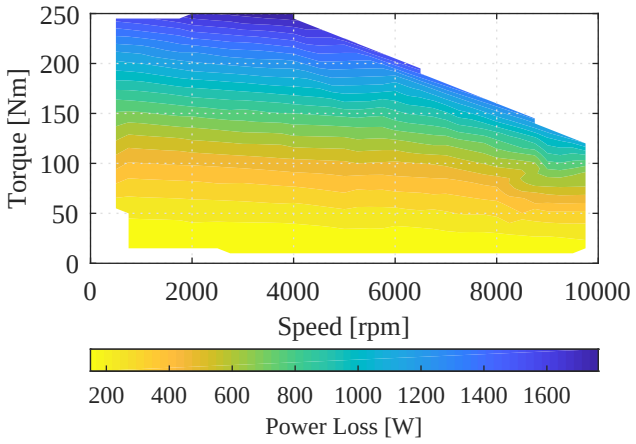


Fig. 10: Semiconductor loss map of the segmented inverter.

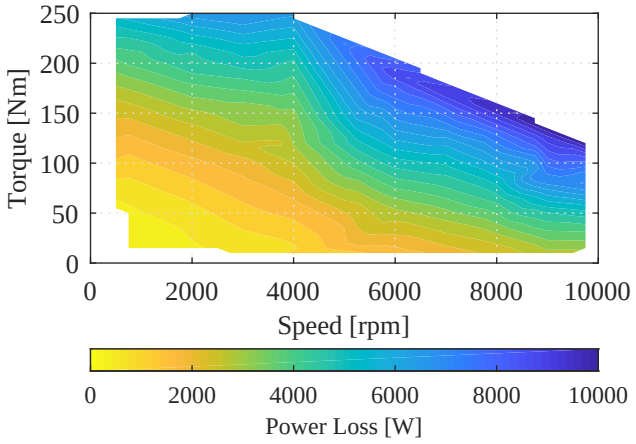


Fig. 11: Loss map of the overall system.

characterization is evaluated. The coolant temperature of the motor was set to 65 ^{o}C with 10 L/min flow rate during the characterization and motor loss is measured by recording the difference between electrical power input and mechanical power output in the dynamo meter setup. [7]. The experimental loss map of the PM motor at different torque and speed conditions is presented in Fig. 9. The maximum power loss occurs at high speed, low torque conditions where the motor is operated close to its rated power 125 kW. The loss across the motor varies between 1000 to 8500 kW. On the other hand, the semiconductor loss map of the segmented inverter, which includes condition and switching losses, with 30 kHz switching frequency can be seen in Fig. 10. The direct relation between the output torque of the motor and the inverter loss is quite clear. Within the given operating range, the inverter loss varies from 200 W and up to 1700 W, mainly dependent on the torque demand of the motor. By using the results presented in Figs. 9 and 10, overall system loss map has been generated and presented in Fig. 11. It can be seen that overall system loss is dominated by the motor loss due to high performance of SiC MOSFETs and overall loss trend is very similar to motor loss trend. In automotive traction system, usually the inverter and the motor are cooled with the same coolant with a series type of thermal network and the overall system loss determines the stress on the thermal network. However, the loss map of individual components show that the loss trend varies between components and this variation has to be taken into account during the thermal design of the system in order to avoid localized hot spots and ensure high reliability.

V. Conclusion

In this work, the loss analysis and mapping of a traction system for EV vehicles is discussed. The analytical loss derivation of a segmented two-level inverter based on SiC MOSFET without anti-parallel diode is presented and used to select optimum SiC MOSFET die configuration for the selected application. The theoretical analysis is then used to assess the loss trend of the segmented two-level inverter. Based on torque-speed characteristics and loss mapping of individual components, the overall system performance is presented. It is shown that each component has different thermal loading trends under given torque-speed characteristics. Therefore, various operating conditions have to be considered for the design of traction system components to ensure reliability and high performance, which are critical requirements for EV systems.

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