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FinFET technologies for Digital Systems with Radiation Requirements: TID, SEE, Basic Mechanisms, and Lessons Learns

Michael P. King

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Motivation

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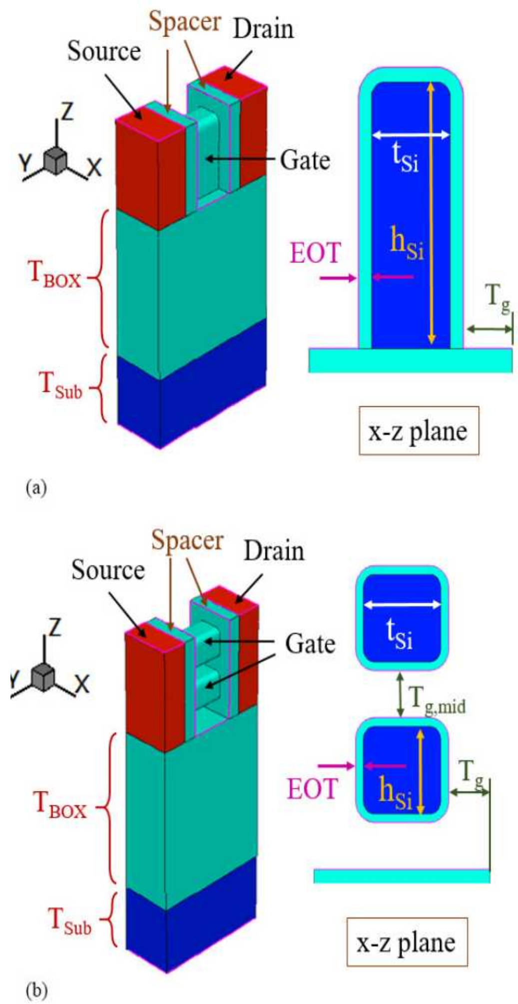
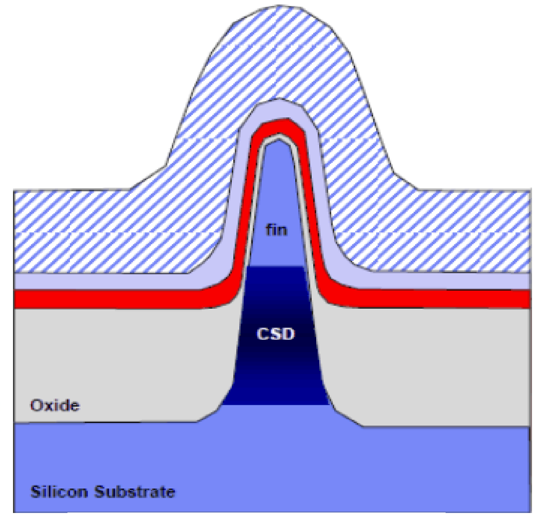
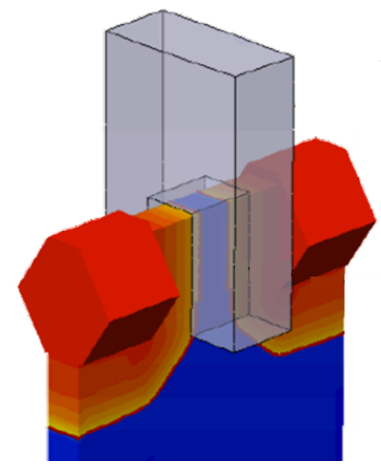
- Most commercial fabs have migrated to FinFETs below 20-nm gate length feature sizes
- FinFETs exhibit improved electrostatic control of the channel and improved reliability compared to equivalent scaled planar CMOS
- Some work on the TID response of FinFETs has been presented at IRPS, NSREC, and RADECs







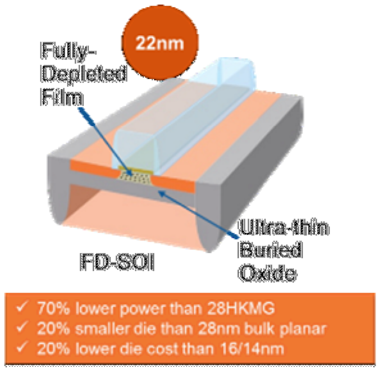
T. Hook, FDSOI Conference, Taiwan, 2013

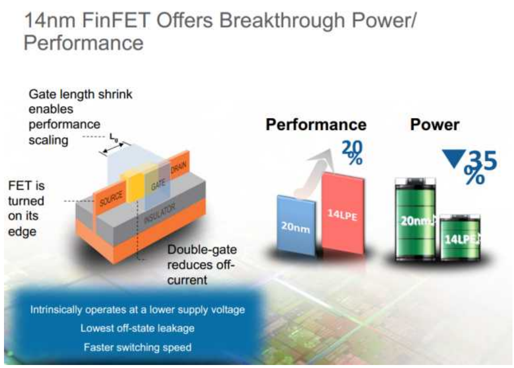
Outline

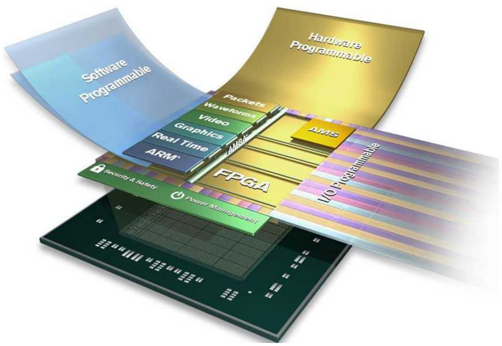
- Technology overview
- A very basic review of radiation effects in CMOS devices
- TID in 14/16-nm FinFET devices
- Single-event upset in 14/16-nm FinFETs: data and some mechanisms
- Observation of single-event latchup in a 14/16-nm FPGA?
- Conclusions

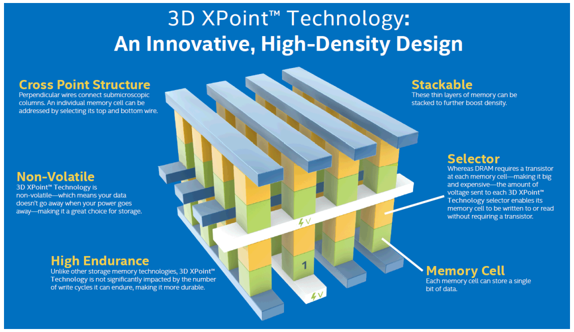
Current Technology Engagements

- GlobalFoundries
  - 14-nm FinFETs
  - 22-nm FDSOI
- NVM
  - Optane / 3D CrossPoint
- IBM
  - 32-nm PDSOI
  - 22-nm PDSOI
- TSMC
  - 16-nm FPGAs (Xilinx)



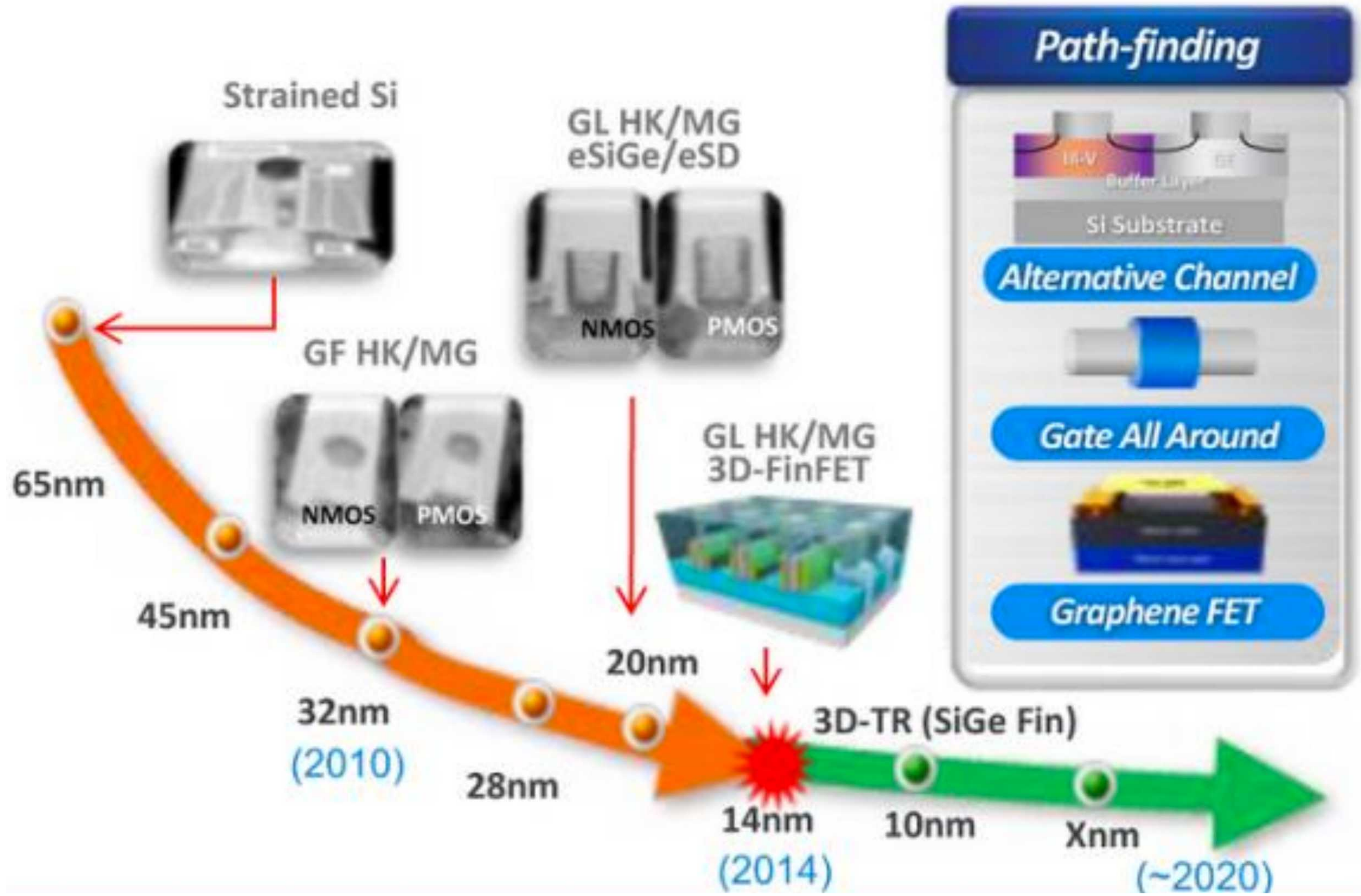




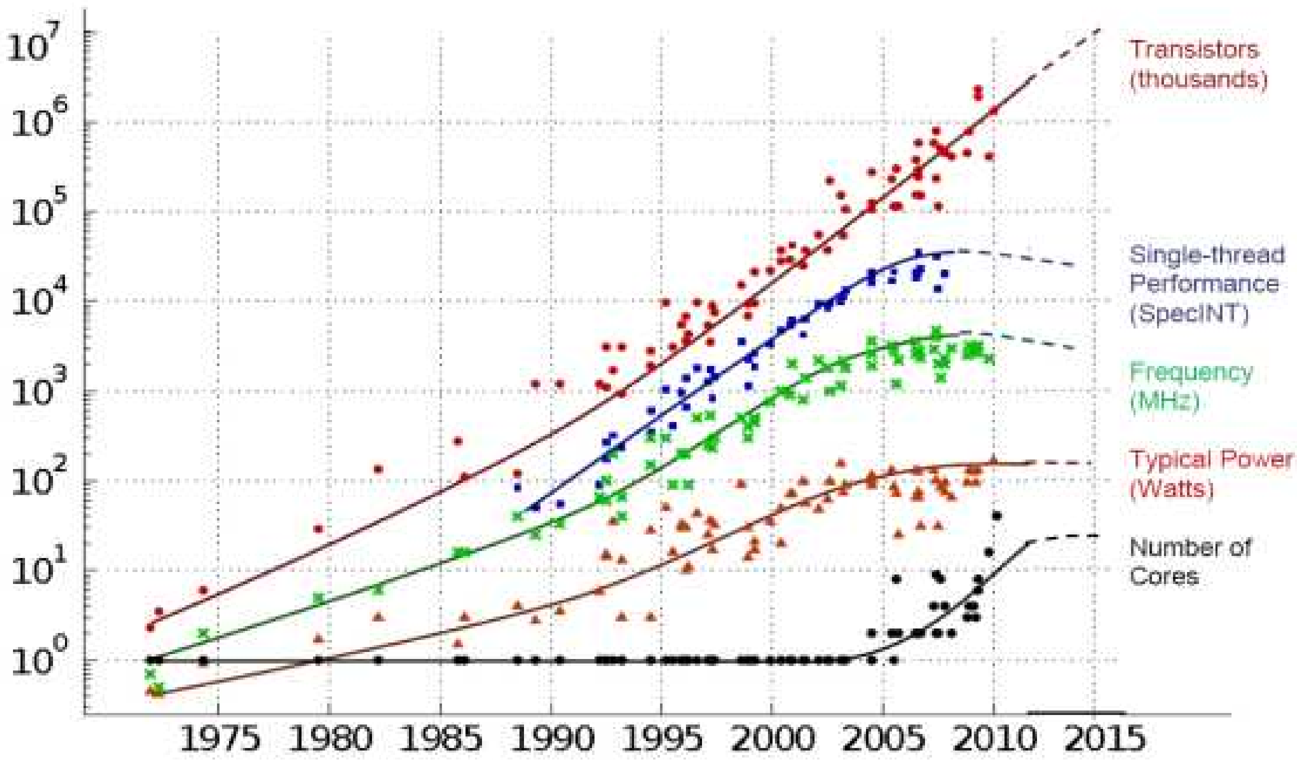


TECHNOLOGY PROGRESSION

Path to FinFET Technology



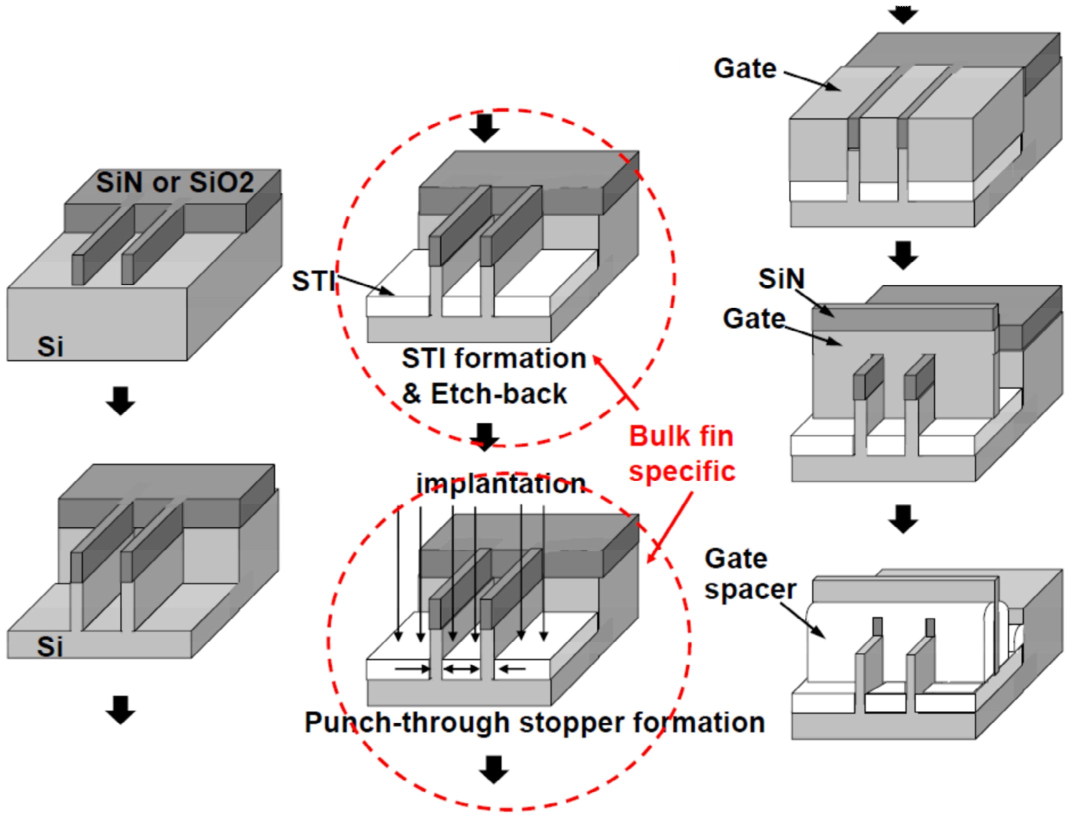
Technology Scaling Trends



1995	1997	1999	2001	2004	2006	2008	2010	2012	2014
350 nm	250 nm	180 nm	130 nm	90 nm	65 nm	45 nm	32 nm	22 nm	14 nm

Bulk FinFET Processing Technology

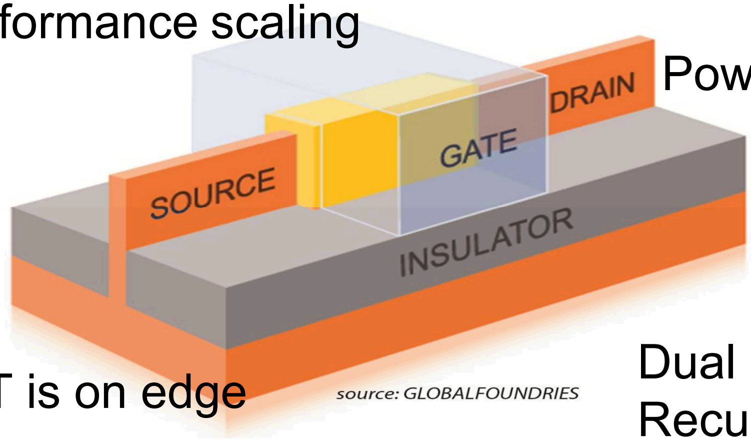
- Increasing processing complexity
- More challenging lithography
  - Quad patterning
  - Soon EUV
- Line edge roughness
- Isolation steps
  - STI
  - CSD/SSRW



A. Yagishita (Toshiba), SOI Short Course (2009)

Advantages / Challenges

Gate length shrink
Performance scaling

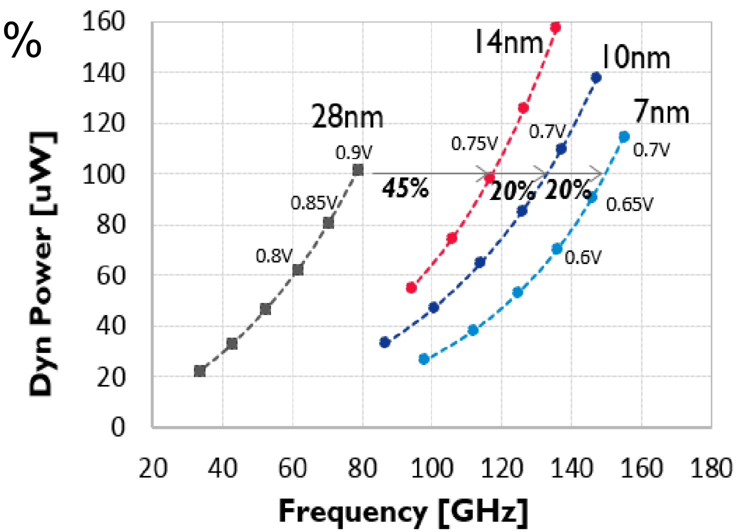


FET is on edge

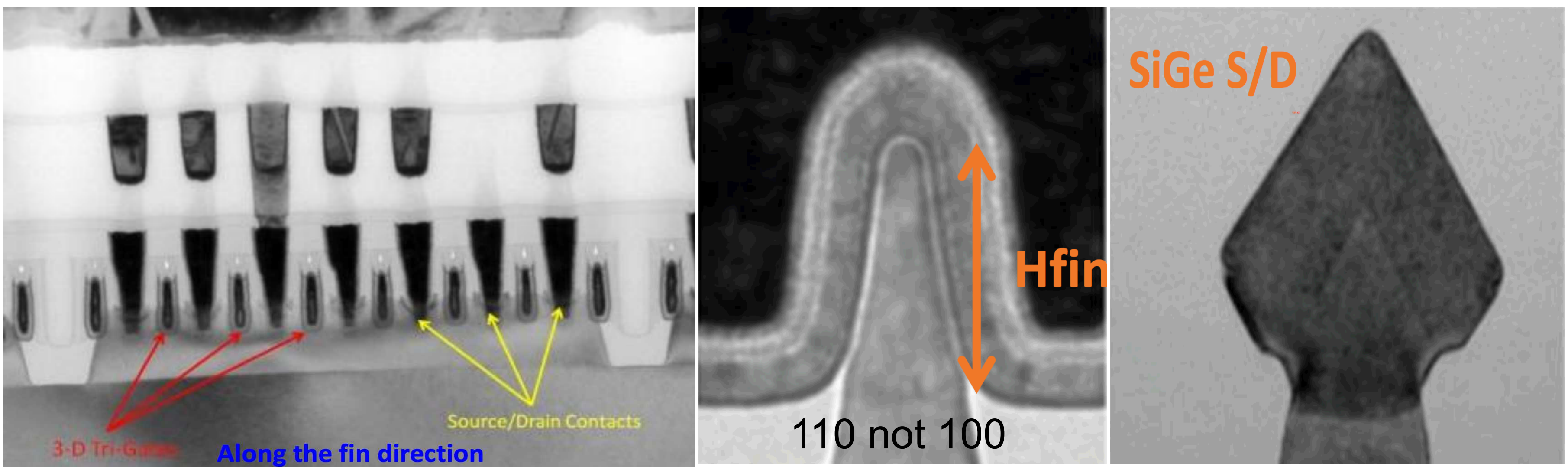
Performance ↑ 20 %

Power ↓ 35%

Dual gate
Recuces I_{off}

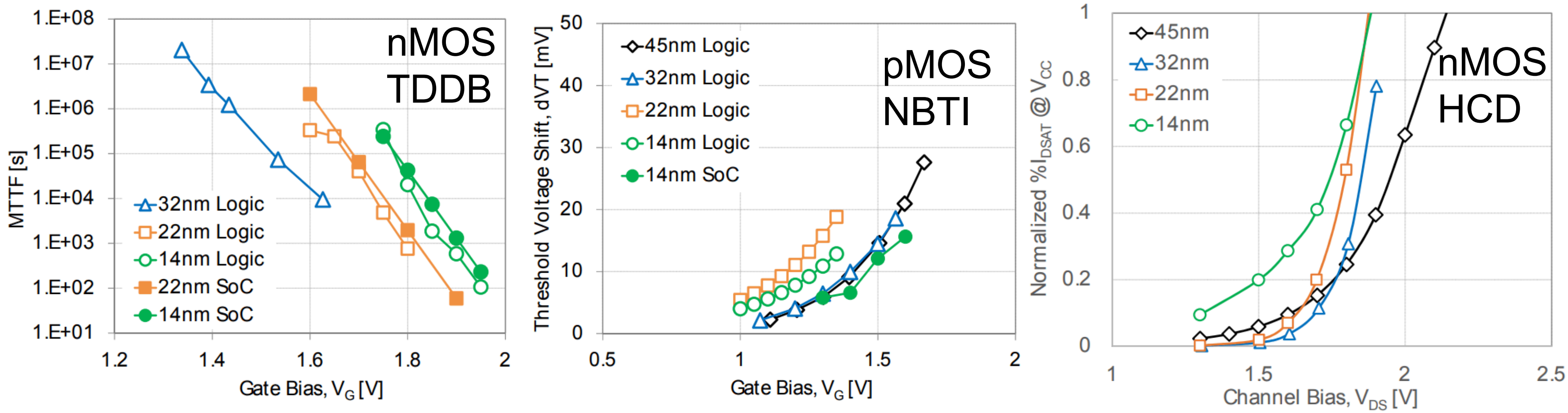


M. G. Bardon (IMEC) *ICICDT* (2015)



Uppal (GF), *IIRW* (2016)

Reliability Outlook



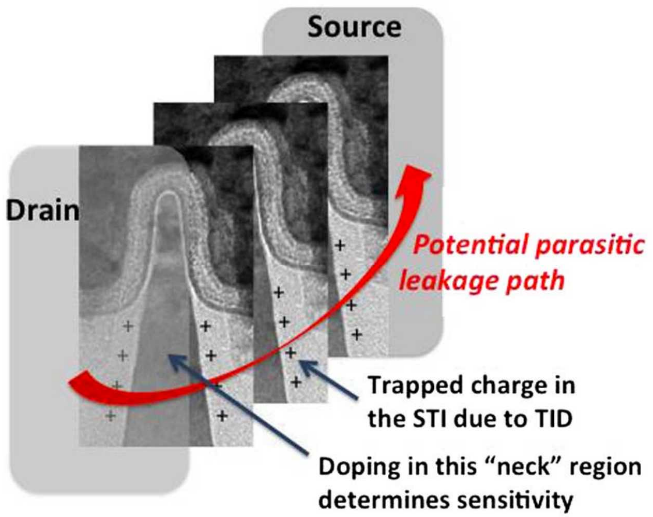
- FinFET TDDB shows improvement over planar
- pMOS FinFET NBTI did show some regression; improved in second gen. overall BTI improved
- HCD does degrade some for FinFETs

Brief review

RADIATION EFFECTS IN SEMICONDUCTORS

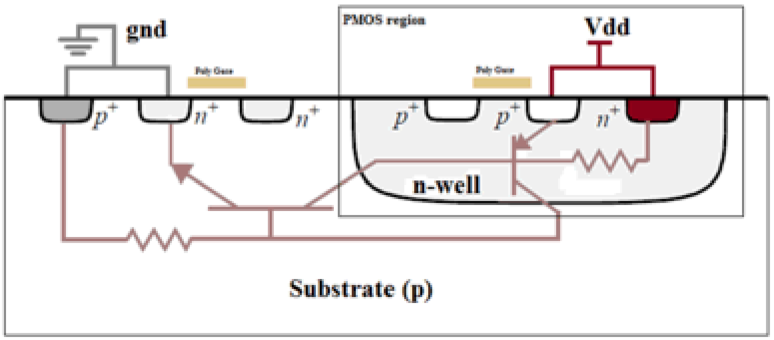
Total Ionizing Dose Degradation Mechanisms

- Gate degradation from interface traps and positive charge trapping in oxide bulk
- Leakage current (and gate control component) from charge trapping in STI



Chatterjee, *IEEE TNS,* 2013.

Single Event Latchup (SEL)



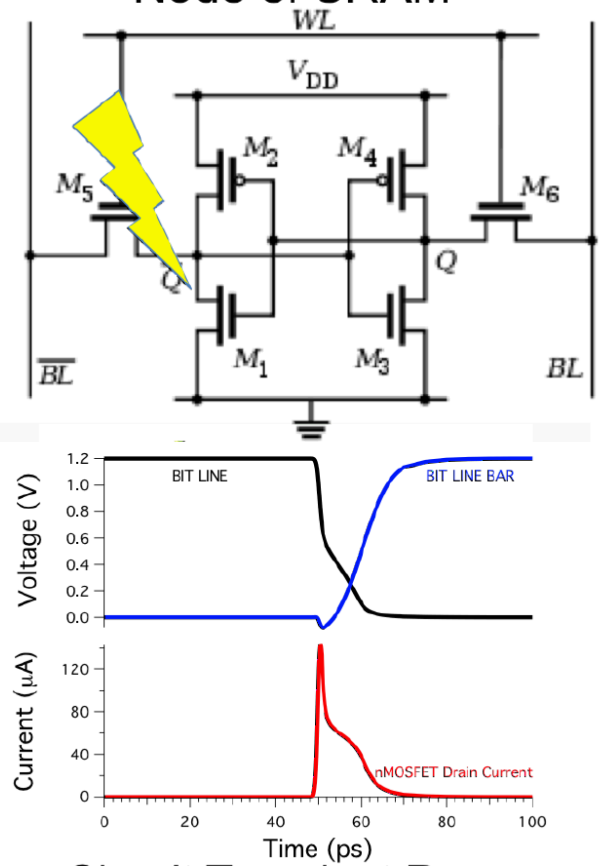
Why do we care?

- Well it requires a power-down event to quench
- Can be destructive if not handled quickly
- Parts that exhibit such behavior are *high risk*

- A high current state sustained by a positive feedback loop in a n-p-n-p junction resulting from charge injection in cross-coupled bipolar junction transistor
- Similar to electrical latchup except initiated by a charged particle interaction

Single Event Upset (SEU)

Particle Strikes Sensitive Node of SRAM



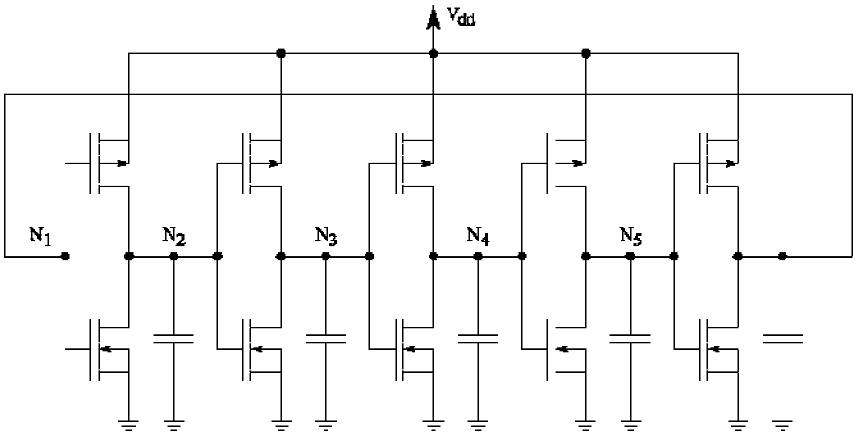
Circuit Transient Response Results in Error

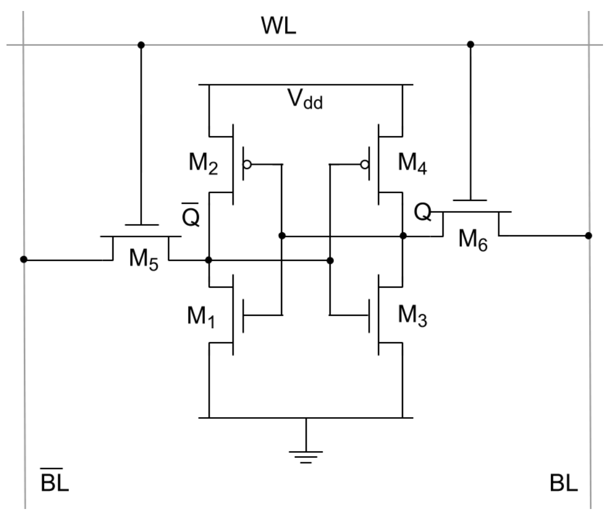
- A possible circuit response to a charged particle interacting in specific regions of a memory (SRAM depicted) leading to an erroneous data state
- Problem because of data integrity and fault propagation up to the system level

And now for some data…

RESULTS

Description of Test Structures



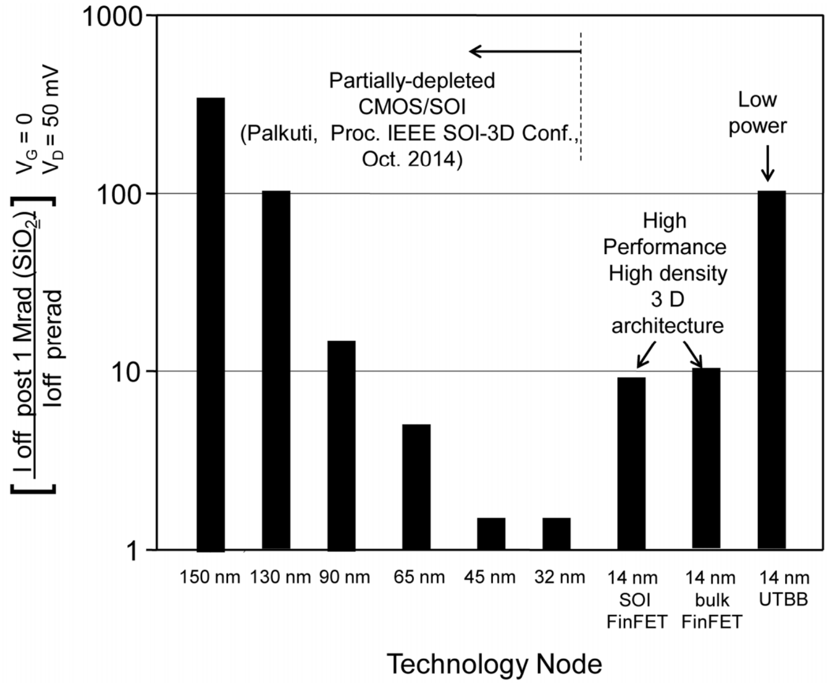


- Single logic and IO transistors in all V_{th} flavors
- Special Structures
  - Ring oscillator (RO) (RF) transistors
  - Static random access memory (SRAM) transistors

Experimental Methods

- Information extracted from I_{ds}-V_{gs} curves
  - V_{th} – linear region approximation
  - $g_m = dI_{ds}/dV_{gs}$
  - $I_{ds,on} = I_{ds}$ @ V_{gs} = 0.9 V, V_{ds} = 50 mV
  - $I_{ds,off} = I_{ds}$ @ V_{gs} = 0 V, V_{ds} = 50 mV
- Bias Conditions
  - Off-state: V_d = 1.0 V, $V_g = V_s = V_b$ = 0 V
  - On-state: V_g = 1.0 V, $V_d = V_s = V_b$ = 0 V
  - Half-on-state: V_g = 0.5 V, $V_d = V_s = V_b$ = 0 V
- Devices irradiated at 525 rad(SiO_2)/s

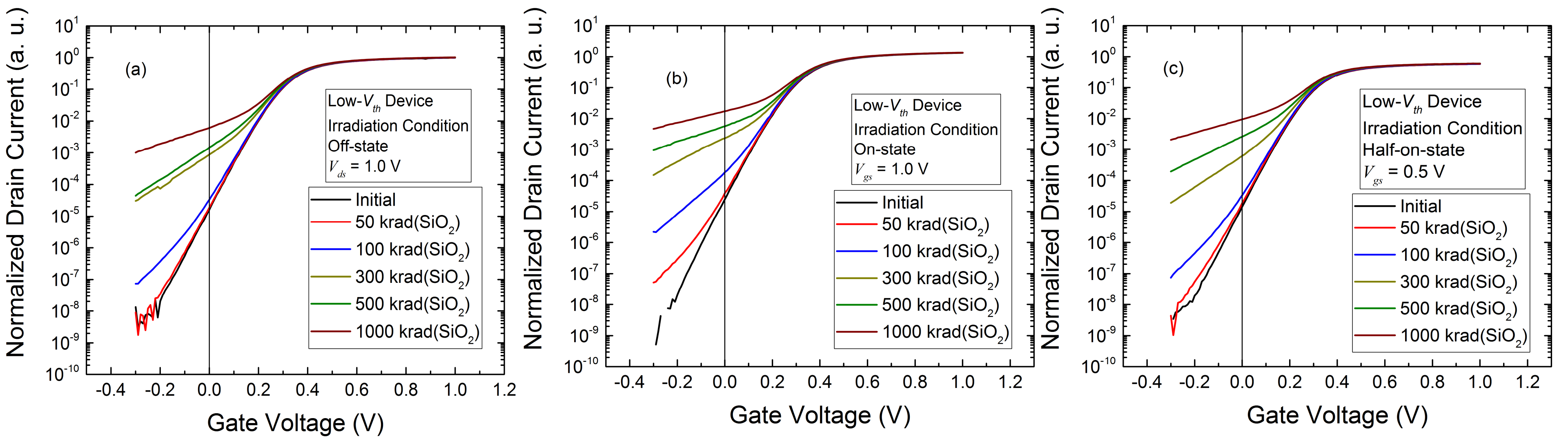
TID vs Technology Scaling



Hughes (NRL) REDW NSREC (2015)

- Scaling trends of off-state leakage vs technology node
- PDSOI exhibits very low leakage for 45- and 32-nm at 1 Mrad
- Migration to FinFETs resulted in a dramatic increase in post-irradiation leakage (early look)
- FDSOI shows leakage comparable to older technologies

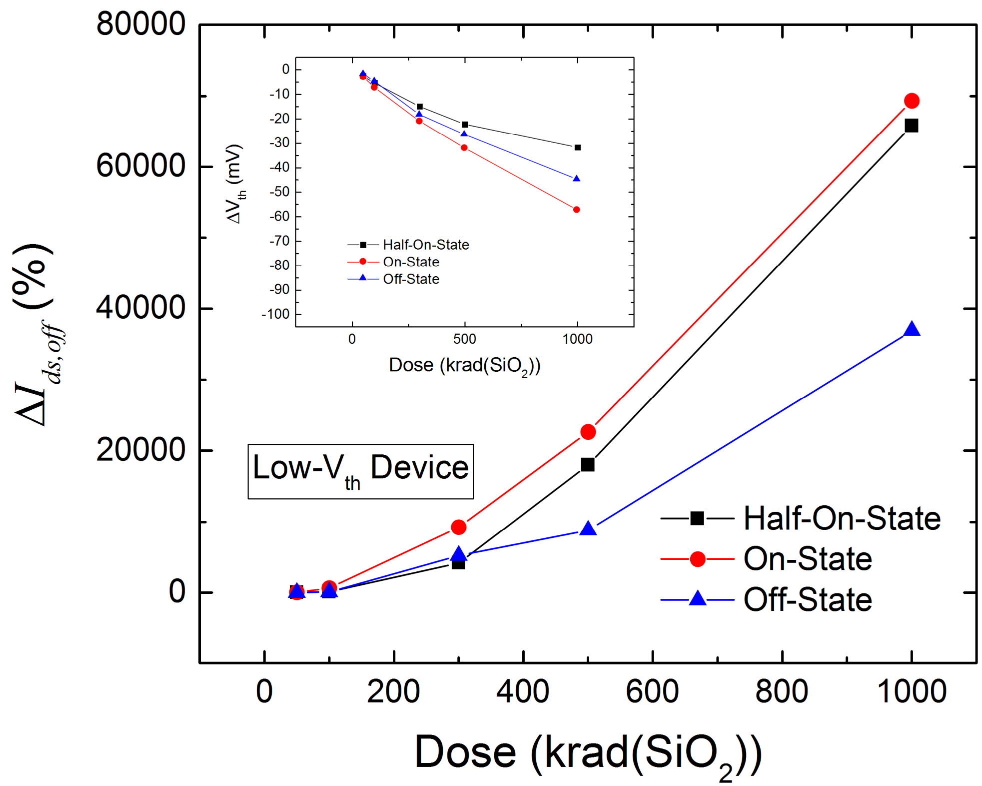
Low-V_{th} Device Bias Dependence



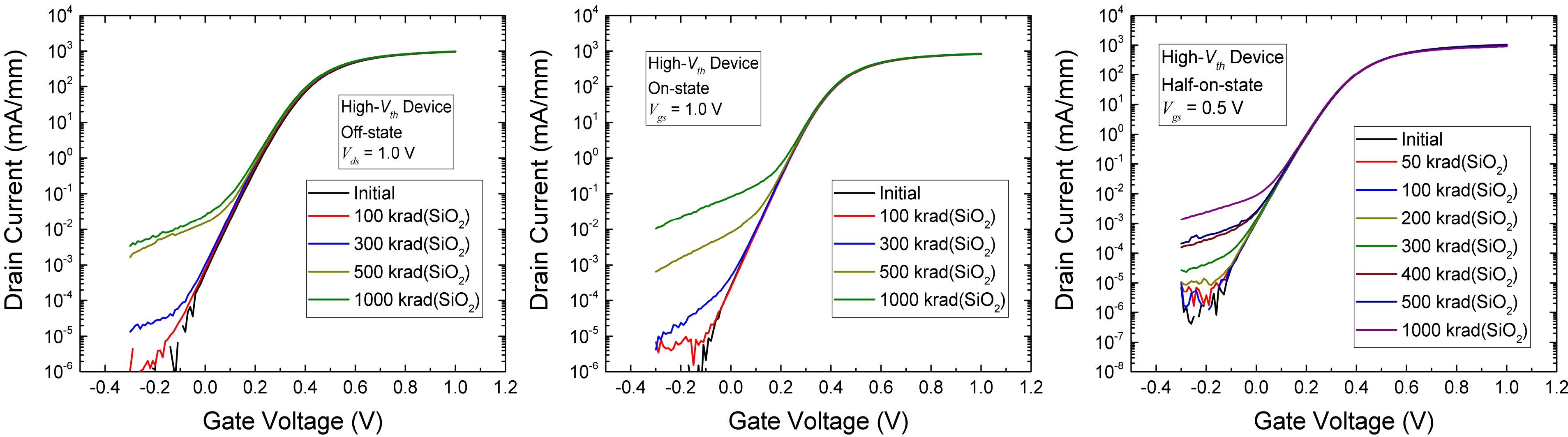
- Large changes in $I_{ds,off}$
- Gate-controlled leakage component
- *On*-state condition gives largest degradation
- Minimal change in V_{th}

TID Irradiation Bias Dependence

- $\Delta I_{ds,off}$ shows most degradation for on-state condition
- ΔV_{th} fairly similar for all bias conditions (and small)
- Lower operating voltage (half-on-state) shows marginal improvement in $\Delta I_{ds,off}$ and ΔV_{th} compared to full on-state



High-V_{th} Device Bias Dependence



- Less off-state leakage compared to low-V_{th} device
- Reduced operating voltage has a greater impact on TID degradation for higher V_{th}device

Different V_{th} Devices – On-State

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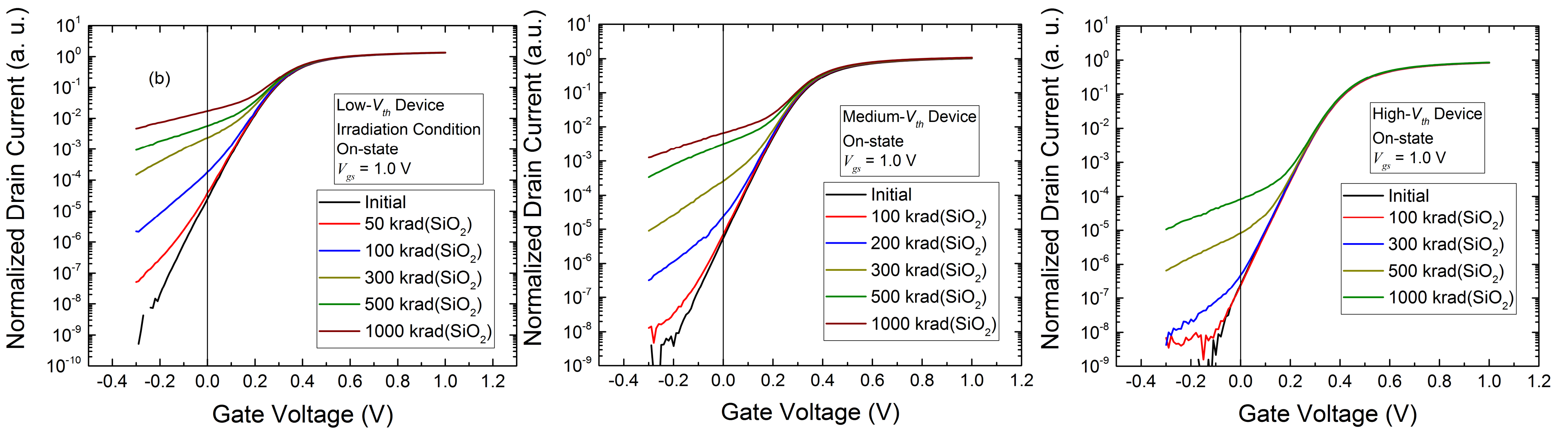
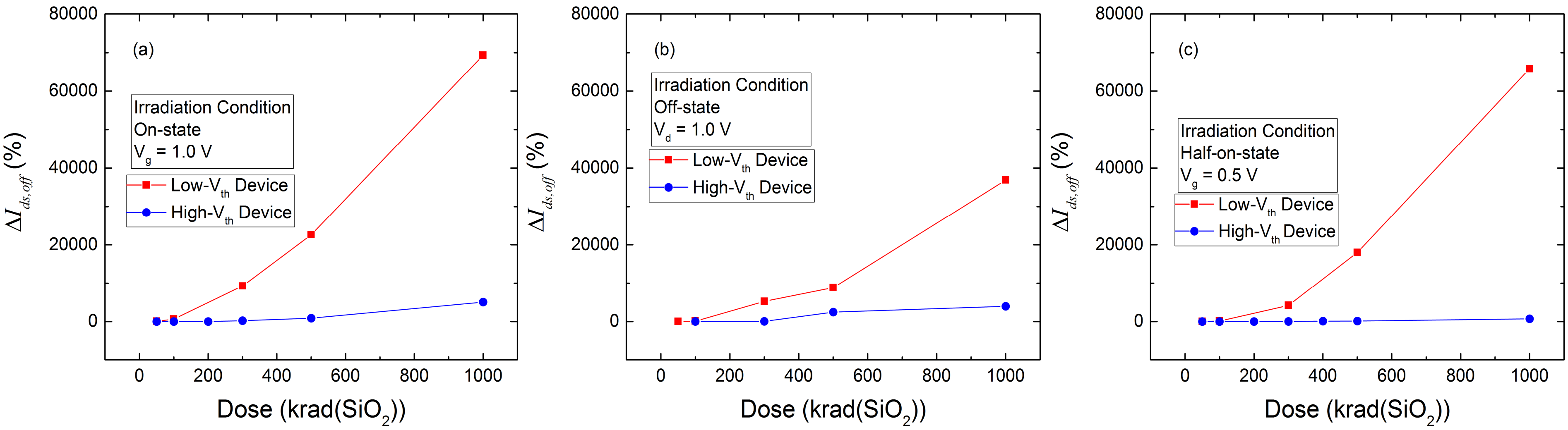


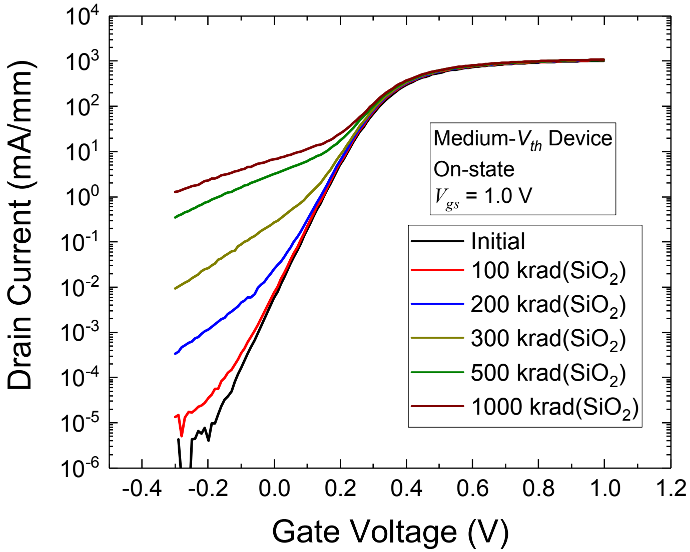
- Increasing V_{th} shows less $I_{ds,off}$ degradation for equivalent dose
- Process level decisions will clearly impact TID impact on devices, circuits, and ICs

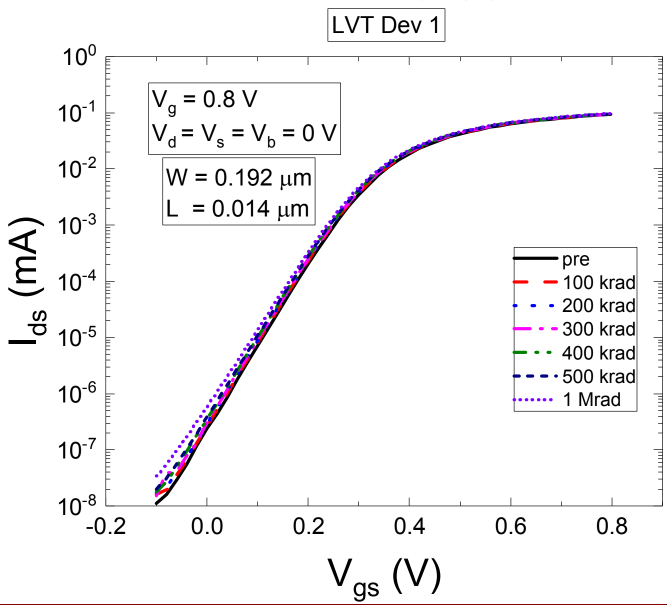
Comparison of TID Variability for Different V_{th}



- High-V_{th} device shows less $\Delta I_{ds,off}$ compared to Low-V_{th} devices
- On-state appears to be the worst case for device leakage response

A Tale of Two Commercial Processes

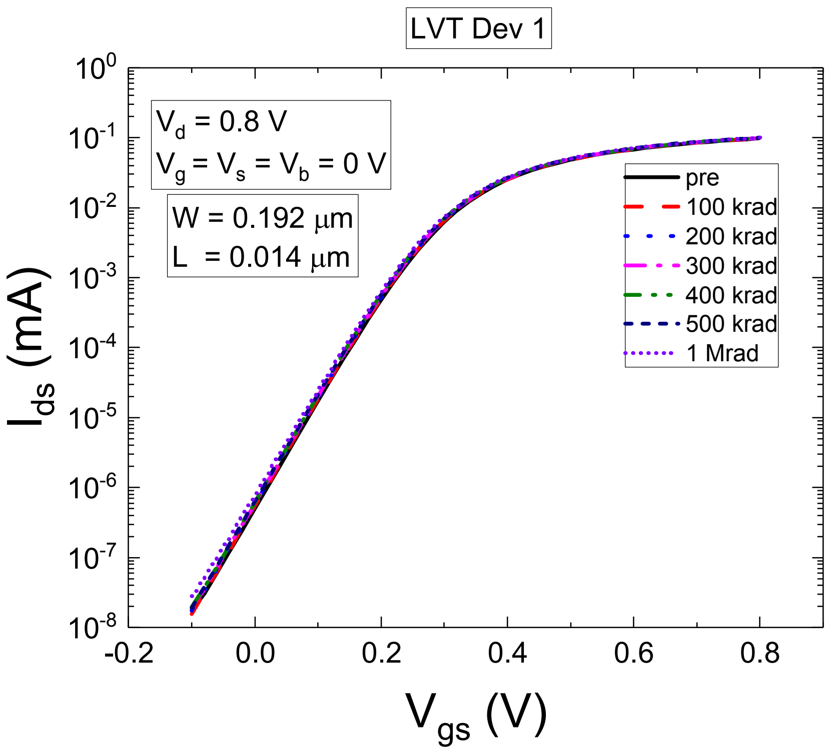


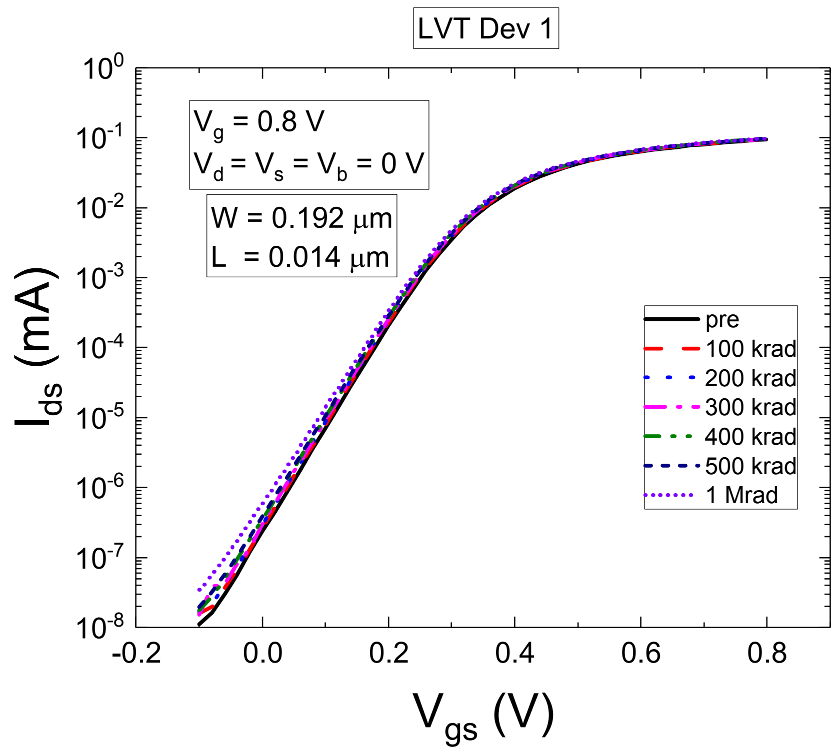


- Typically comes about when they fix a leakage problem
- Impossible to say if TID resilience remains a permanent feature of the technology going forward

Two snapshots of a commercial 14/16-nm FinFET technology show *very* different TID results

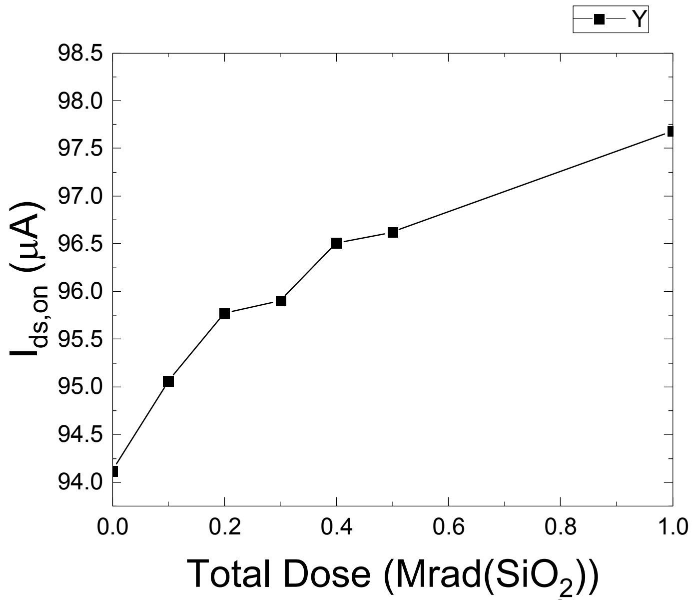
Narrow width nFET

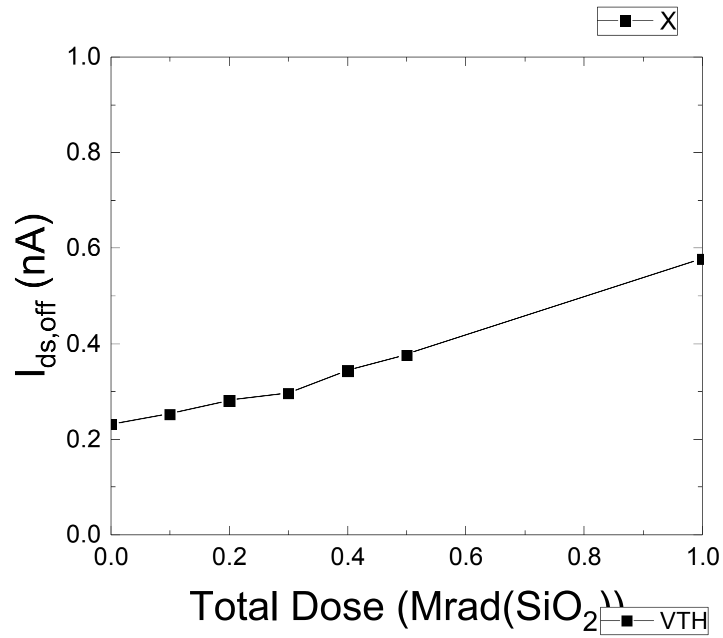


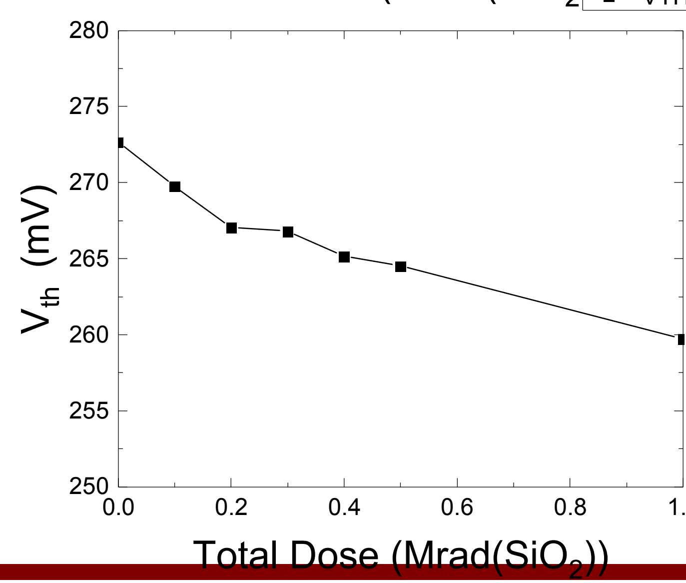


- Device shows more leakage in the on-state consistent with previous experimental results
- Response to TID is much less severe than original observations

Change in irradiated leakage and V_{th}

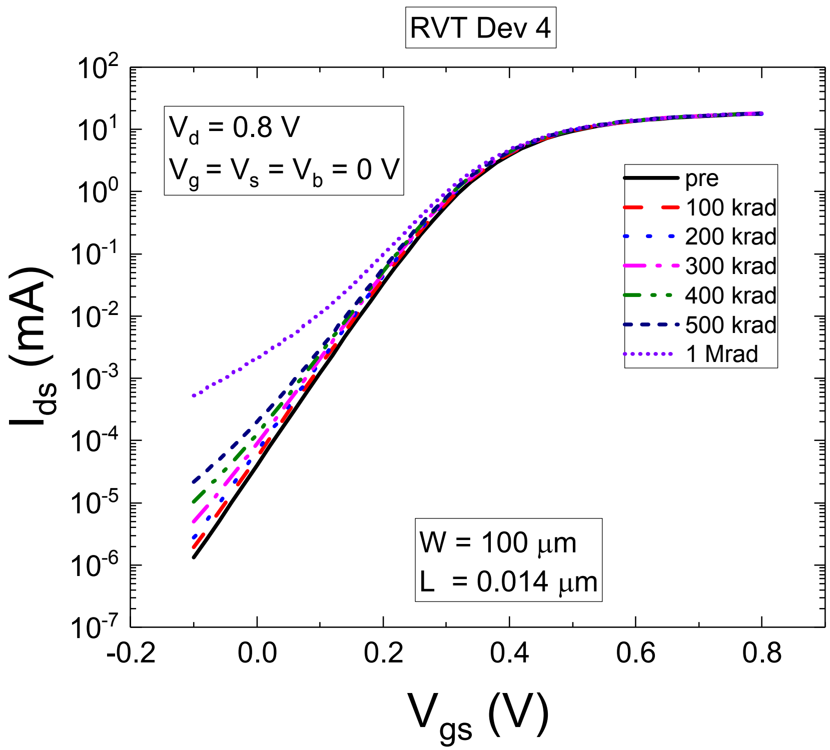


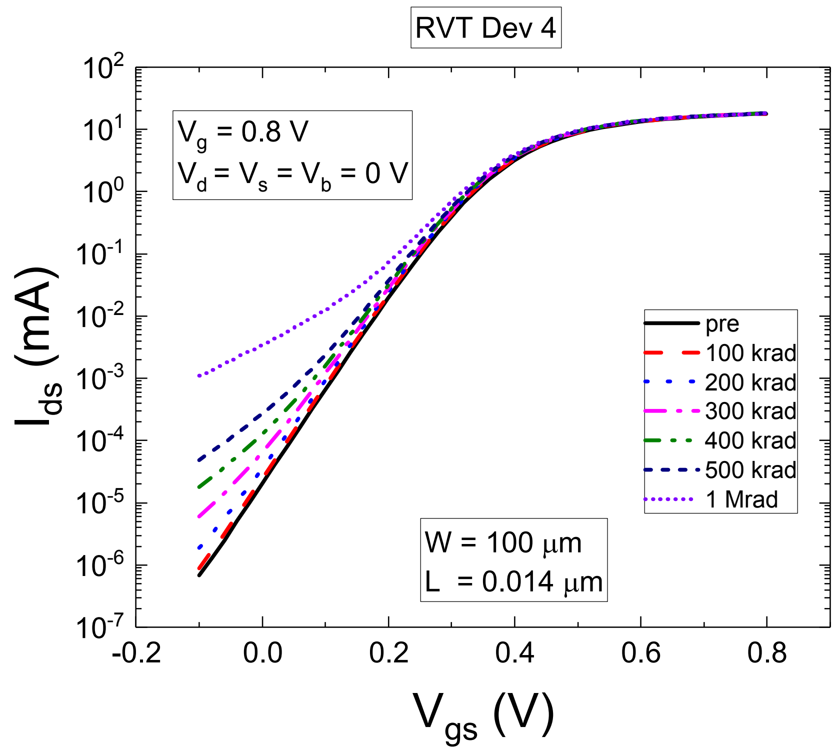




- Drive current tracks V_{th} with irradiation
- Leakage current shift smaller than previous evaluations
- Results not consistent between foundries! – recent VU paper at NSREC

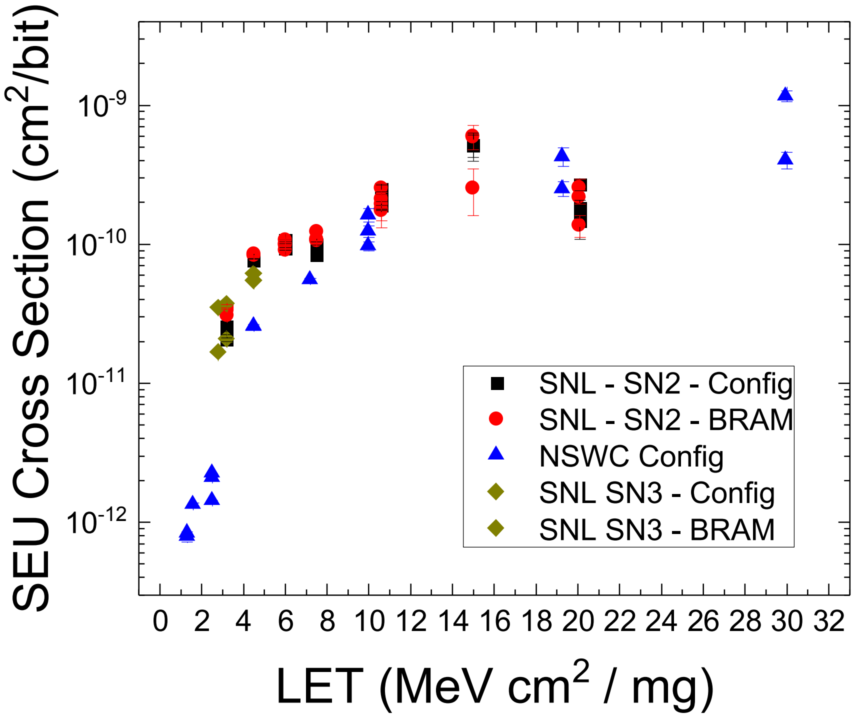
Not all is well in the land of Oz





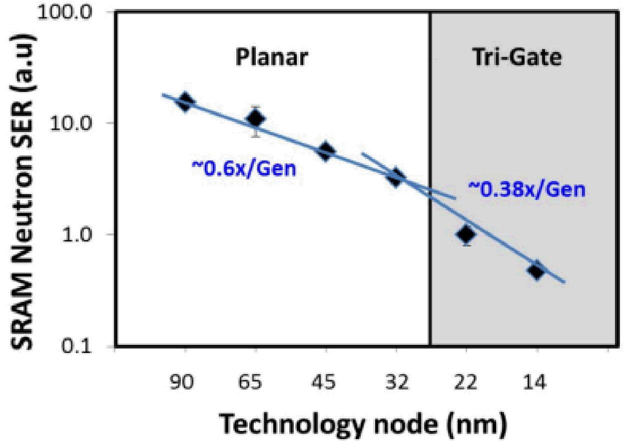
- Largest device shows much more leakage than either of previous two devices
- May be some dependence on total width/number of fingers

Xilinx UltraScale+ (16-nm) FPGA - SEU

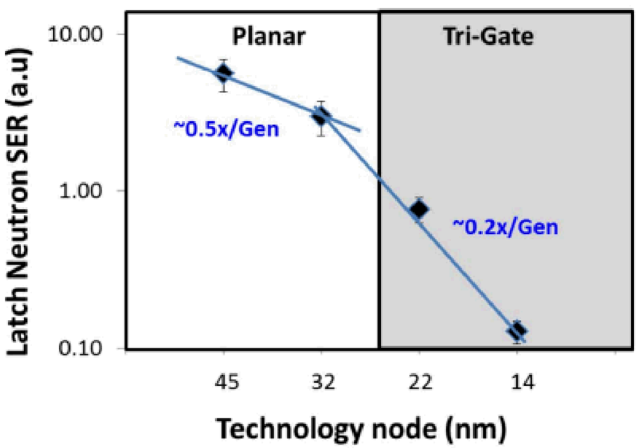


- Parts exhibit a fairly low SEU cross section

Early Neutron SER Report



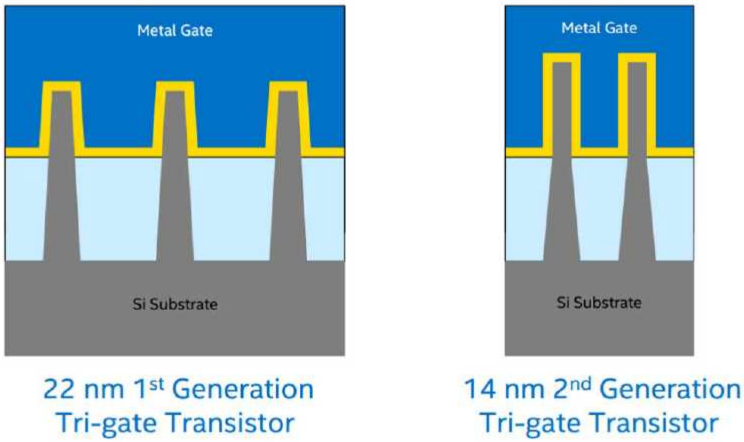
(a)

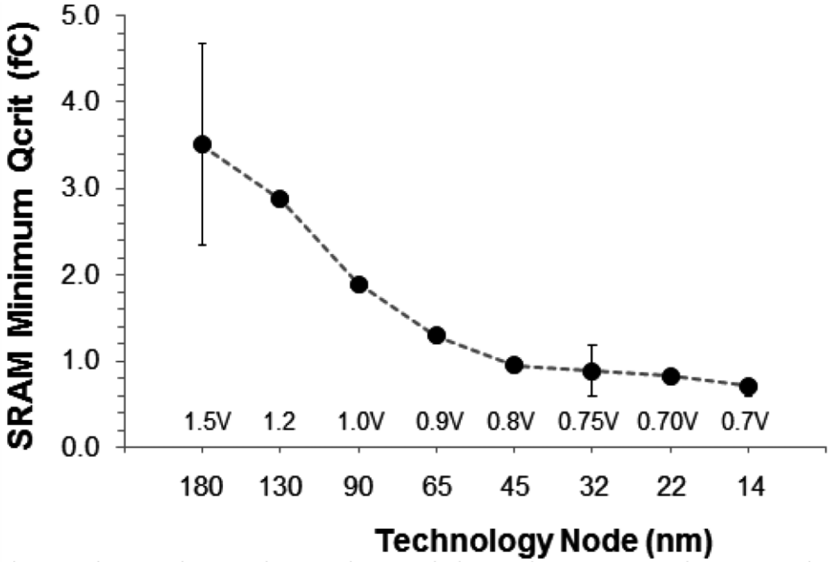


(b)

- Industry looks at SER from alphas, muons, and neutrons for terrestrial environment reliability
- Several reports of reduced SER from geometry change in FinFET vs planar
- No reports of destructive effects due to neutrons to 10^9 n/cm^2 from Broadcom or Intel

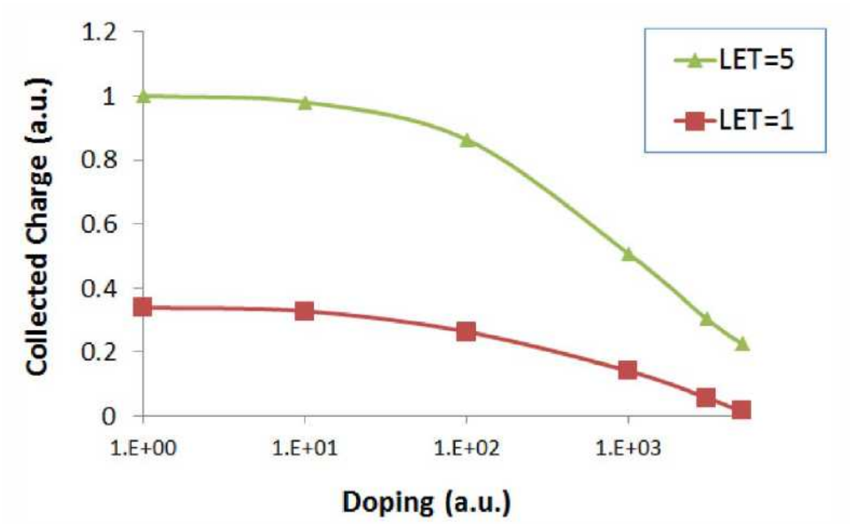
Mechanisms of SEU in FinFETs

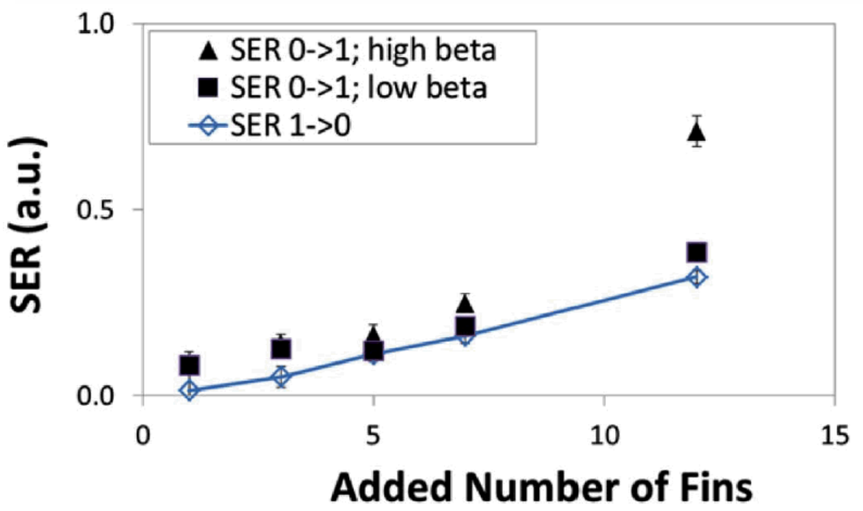




- 3D geometry allows increasing drive without increase in Drain-Body/Well area
- Most charge is collected from subfin/well region this implies a higher Q_{crit} without impacting the sensitive volume dimensions

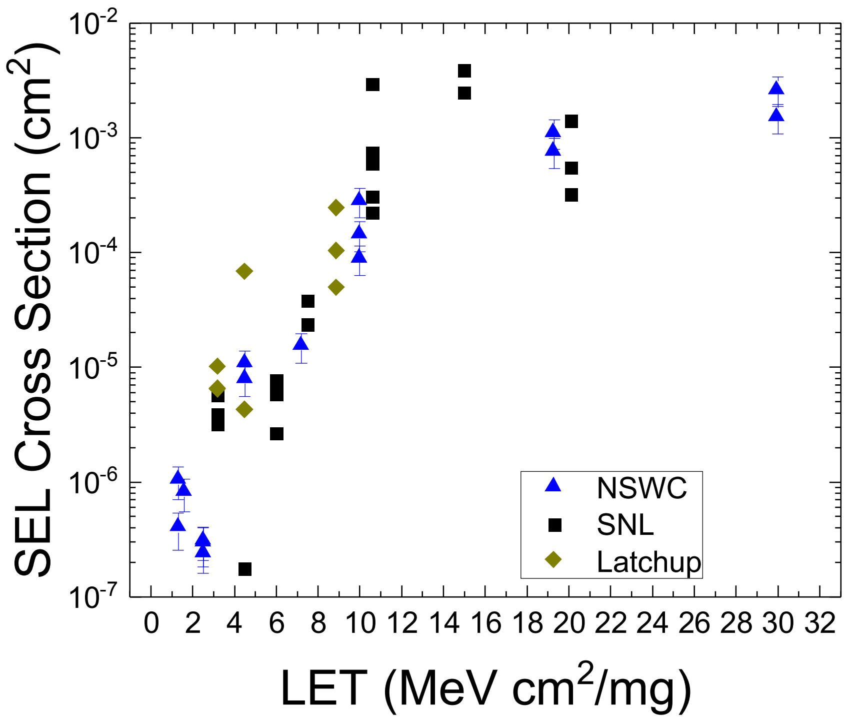
Additional SEU Mechanisms





- SER/SEU response ultimately will depend on things beyond our control
  - Channel stop doping
  - Well doping
- Some control from layout and memory architecture
  - Effective transistor width
  - Spatial separation of critical nodes
  - DICE vs regular latch

Xilinx UltraScale+ (16-nm) FPGA – "SEL"



- Parts exhibit SEL-like behavior at relatively low LET
- Unclear if this is a circuit design issue or actual latchup
- There are reports of SEL in 14/16-nm that exhibit the correct temperature dependence but *none* have such low threshold LET

Conclusions

- High-V_{th} devices give a lower post-irradiation $I_{ds,off}$ than Low-V_{th} devices
- On-state bias condition appears to be the worst case for $I_{ds,off}$ for all the transistor variations evaluated in this work
- Lower voltage operating conditions (half-on-state) (near-threshold computing) remain of interest as a means to reduce TID degradation of FinFET devices
- We saw SEL and were not happy about it