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Design and Control Methodology for Improved Operation of a HV Bipolar Hybrid Switched Capacitor Converter

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***Abstract*— In this work, a novel dc-dc converter topology, an adaptation of the Hybrid Switched Capacitor Circuit (HSCC), is considered for use in high-gain, high voltage applications that also require high efficiency and superior power density. In particular, a bipolar HSCC design is described, and a candidate control methodology is set forth and developed analytically. The converter performance is demonstrated to be consistent with analysis. In addition, the converter is demonstrated to step 460V up to 8.63 kV (gain of 19) at 3.63 kW and nearly 97.0% efficiency.**

Keywords*— *WBG, High-gain DC-DC converters, MVDC applications, PV, switched capacitor

I. INTRODUCTION

Recent advances in wide-bandgap (WBG) semiconductor power devices have begun to realize improved power density and efficiency in power converters for military, transportation, and grid applications; several instances of converters have been demonstrated in an R&D setting to achieve between 50 to over 200 W/in^3 power densities while maintaining superior efficiency [1]. However, very high power density and efficiency has been demonstrated only at relatively low voltages (i.e. 100s of volts) and often with extensive complexity. Recently, in [2], the authors achieve "…200 V to 966 V conversion at 900 W output power with 93.7% peak efficiency" in a very compact package. However, the circuit is complex in its control of six GaN MOSFETS and not scalable to medium voltages. Extreme power density has yet to be accomplished in medium to high voltage converters. Realizing this capability will require new advances in packaging [3] and the design of new converters that exploit the capabilities of WBG based devices [4]. Herein, a new converter is evaluated to enable high-gain DC-DC power conversion at medium voltage (>5 kV), while maintaining high conversion efficiency.

In prior work, a prototype bipolar HSCC was built and demonstrated to boost an input voltage of 600V to an output voltage of over 10 kV at 2.57 kW and 95.3% efficiency [4]. In addition, corresponding high-fidelity models predicted a California Energy Commission (CEC) efficiency of that converter of over 94%. However, the circuit gain and applied duty cycle were not consistent with that predicted by the analysis under idealized assumptions, and a power regulation scheme had not been identified.

In this work, some revisions were applied to the circuit, with improvements realized in gain, efficiency, and power density. In addition, a method of control is developed and evaluated. In particular, the desired power flow maps to a reference input inductor peak current. Using the analysis, switching may be controlled to minimize turn-on losses and to realize the peak inductor current and thus achieve the desired power flow with high efficiency. This, however, results in a variable frequency control scheme.

The next section describes the HSCC and the bipolar HSCC which is the subject of this study. In Section III, the hardware prototype featured in this work is presented with a discussion of the parameters selected. Section IV develops the analysis in support of a preferred method of control. Section V presents the results of several hardware experiments, evaluating efficiency, gain, and correspondence with the analysis. Section VI provides conclusions and highlights the areas to focus future work.

II. BIPOLAR HYBRID SWITCHED CAPACITOR CONVERTER

In this section, the HSCC circuit topology and general operation are described, and the reasons why WBG devices are particularly suited to this converter are discussed.

A. HSCC and Bipolar HSCC

The HSCC is a combination of the traditional boost converter topology and a switched capacitor (SC) circuit, which in this case includes a "diode-capacitor ladder", to act as a voltage multiplier, and thus provide additional gain [4]-[6]. In this topology, there is only one controlled switch. A bipolar HSCC effectively contains two HSCC converters; it has a positive pole and a negative pole wherein the diode direction is reversed, as shown in Figure 1. In this case, there are two controlled switches that must be synchronized. For the analysis presented in the next section, focus is placed on the operation of the positive pole, and symmetric operation of the two poles is assumed (i.e. $i_{L1} = i_{L2}$). Thus, only components necessary to the analysis and discussion (i.e. primarily in the positive pole), are labeled in Figure 1.

To achieve high voltage, high efficiency, and high power density, the circuit relies on the use of WBG semiconductor devices.

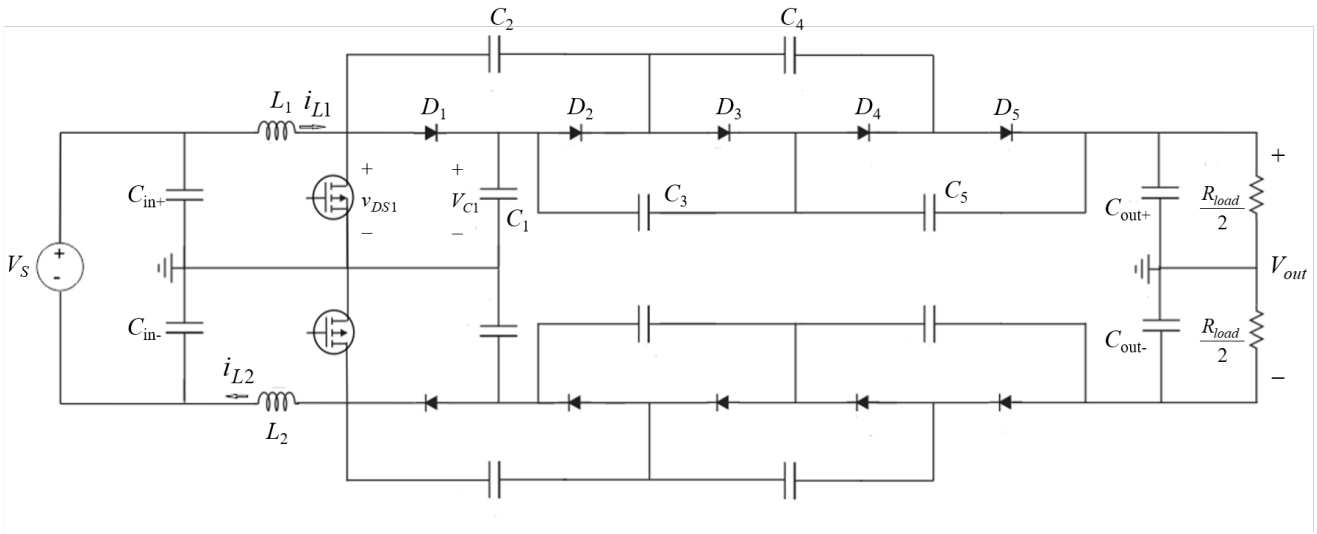

Fig. 1: Bipolar HSCC schematic for an example implementation with N=2 stages on each pole

B. Wide Band Gap Devices for Switched Capacitor Circuits

WBG semiconductor devices, especially Silicon Carbide (SiC) and vertical Gallium Nitride (v-GaN) are ideal materials systems for high voltage power converter applications that demand high power density and efficiency. While SiC is a relatively mature device type, v-GaN power devices have been developed comparably recently. In these devices, voltage is dropped across a thick vertical drift region, rather than along the surface as in conventional lateral GaN devices, enabling competition with silicon (Si) devices in voltage regimes above 1200 V.

Rapid progress in growth and fabrication of both SiC and v-GaN diodes has been made in the past few years, with unipolar figures of merit for realized devices significantly exceeding those of Si [7],[8]. Additionally, several materials properties of WBG devices make inclusion into these types of power converters ideal, lowering power dissipation, enabling higher temperature operation, and allowing higher switching frequencies.

WBG devices have higher critical electric field values compared to traditional Si. This allows thinner layers of material to hold off a given voltage. As the thickness of material is typically significantly larger than the resistance of the packaging [9], thinner devices yield lower intrinsic resistance in the forward conduction regime, especially as forward current density increases. The decrease in bulk material reduces the intrinsic capacitance of the device. This, combined with significantly faster carrier mobilities, enable significantly faster switching frequencies which directly enable the reduction of passive elements sizes and the increase in system-level power density.

In addition to lower power dissipation, WBG devices also exhibit higher temperature operation and higher thermal conductivity compared to Si. The larger bandgap compared to Si reduces the amount of thermally activated free carriers at a given temperature. Thus, WBG devices can operate at a higher temperature for a given specified leakage current. This, paired with higher thermal conductivity, significantly decreases the requirements for system-level cooling, decreasing system cost and size.

While the unique characteristics of WBG devices are instrumental to the construction of a compact, high efficiency, and high voltage prototype, the unique characteristics of the HSCC enable the incorporation of next-generation devices. The diode-capacitor ladder topology of the HSCC relies heavily on two-terminal devices. These types of devices are much easier to fabricate, more reliable, and cheaper than three terminal devices. Additionally, next-generation materials are much more readily available as two-terminal devices, meaning circuit topologies such as the HSCC can readily incorporate next-generation semiconductor materials, consistently improving system-level power density. The next section describes the prototype evaluated in this work.

III. HARDWARE PROTOTYPE DESCRIPTION

A prototype bipolar HSCC circuit was designed for high voltage, high power operation. The circuit includes $N = 5$ stages on the diode-capacitor ladder. The circuit design was based on a previous prototype [4], and informed by simulation and analysis, to achieve higher efficiency and gain. Figure 2 shows a photo of the prototype, and key components are listed in Table I.

The dimensions of the prototype are approximately 15.7”x7.4”x2”, for a volume of 232 in^3 (3808 cm^3), with a demonstrated power density of about 15.5 W/in^3 (0.945W/cm^3) based on the peak power achieved in this study; see Section V. As part of the test bed for this circuit, a custom resistive load was manufactured by *HVR Advanced Power Components* and adjusted to 25 kΩ. High-voltage isolation and heat dissipation were important safety considerations for the design and construction of the test bed. The entire test bed was placed inside an interlocked box for protection of personnel.

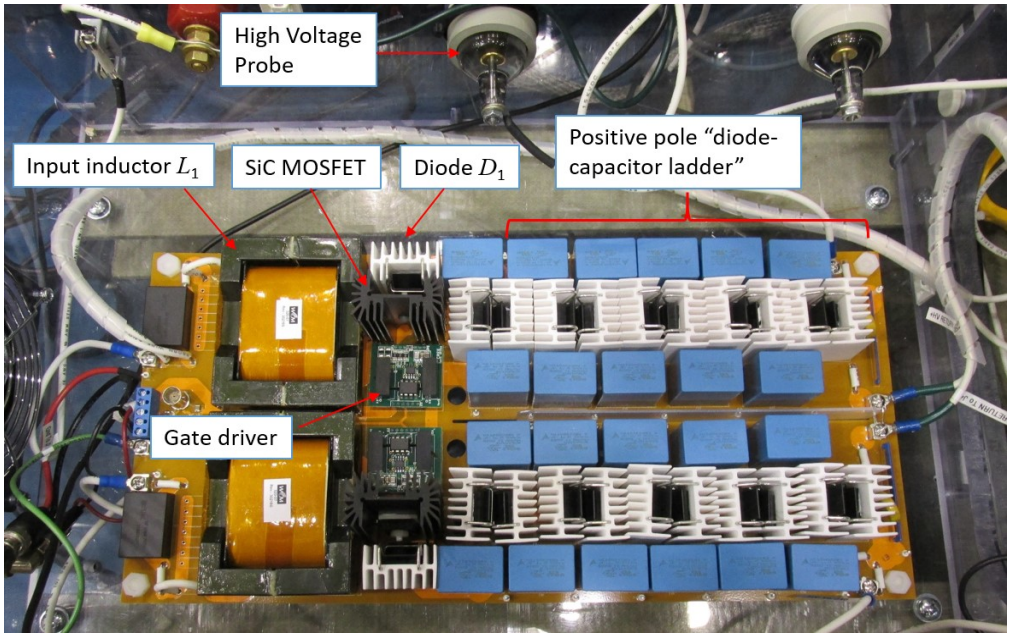

Fig. 2: Bipolar HSCC prototype with N=5 stages; the circuit layout corresponds closely to the converter schematic with the positive pole at the top side of the board; input voltage is supplied at the left of the converter, and the high voltage output is supplied to the load at the right

Table I: Key components used in prototype

Description	**Manufacturer/ Part Number**
SiC Diode, 1.7 kV, 14.4 A	Wolfspeed C3D10170H
SiC FET, 1.7 kV, 72 A	Wolfspeed C2M0045170D
Film capacitor, 1 µF, 1.5 kV	EPCOS B32024A3105M000
MLCC, 0.1 µF, 2 kV	Knowles 2220Y2K00104-KXTWS2
Inductor, 16.2 µH, 56 A	West Coast Magnetics 320-07
SiC Gate driver board	Wolfspeed CRD-100
Load Resistor, R_{load}, 25 kΩ	HVR Advanced Power Comp

The circuit could achieve the desired voltage and power levels with only four stages, but five stages were used to reduce the voltage stresses on the components, particularly the MOSFETs and diodes, and thus increase system-reliability. In addition, the circuit design lends itself much easier to removing stages than adding them, so the prototype can be reduced to four stages with minimal modification.

If the stage capacitor values are too small, the stages will become imbalanced (stages closer to the inductor will have higher voltages, and thus put higher stresses on the switching components). The stage voltages would also see higher ripple. In this prototype, film capacitors were used as stage capacitors, which allow much higher capacitance for voltage rating and cost compared to ceramic capacitors. The film capacitors also avoid the loss of capacitance at high voltage exhibited by some ceramic capacitors. To allow fast switching of the diodes, ceramic capacitors were used in parallel with the film capacitors, since the ceramic capacitors have lower equivalent-series-inductance (ESL).

As is shown in the next section, the peak inductor current largely determines the power throughput; so, the inductor was selected accordingly.

IV. HSCC Analysis and Method of Control

Herein, a method to regulate the input power to the converter is considered while mitigating switching loss. In particular, the MOSFET switches *on* as the inductor current is rising through the i_L=0 crossing (when the switch voltage is also near zero) and then switches *off* when a reference peak current is reached. The proposed mode of control deals with regulating input power and thus allows for the focus to be on the input stage of the converter. In addition, the analysis is described in terms of the positive pole, and symmetrical operation is assumed.

Since the proposed control requires the definition of a peak current, and since most applications would have a fixed output voltage, the quantities will be expressed in terms of the peak current $I_{L,pk}$ and the output voltage V_{out} as well as the source voltage V_S and any parameters assumed to be constant. In addition, for the bipolar HSCC with N stages on each pole and assuming perfect balancing across the capacitors, the steady-state average voltage of the capacitor proximal to diode D_1 is given as

$$V_{C1} = \frac{V_{out}}{2(N+1)} \tag{1}$$

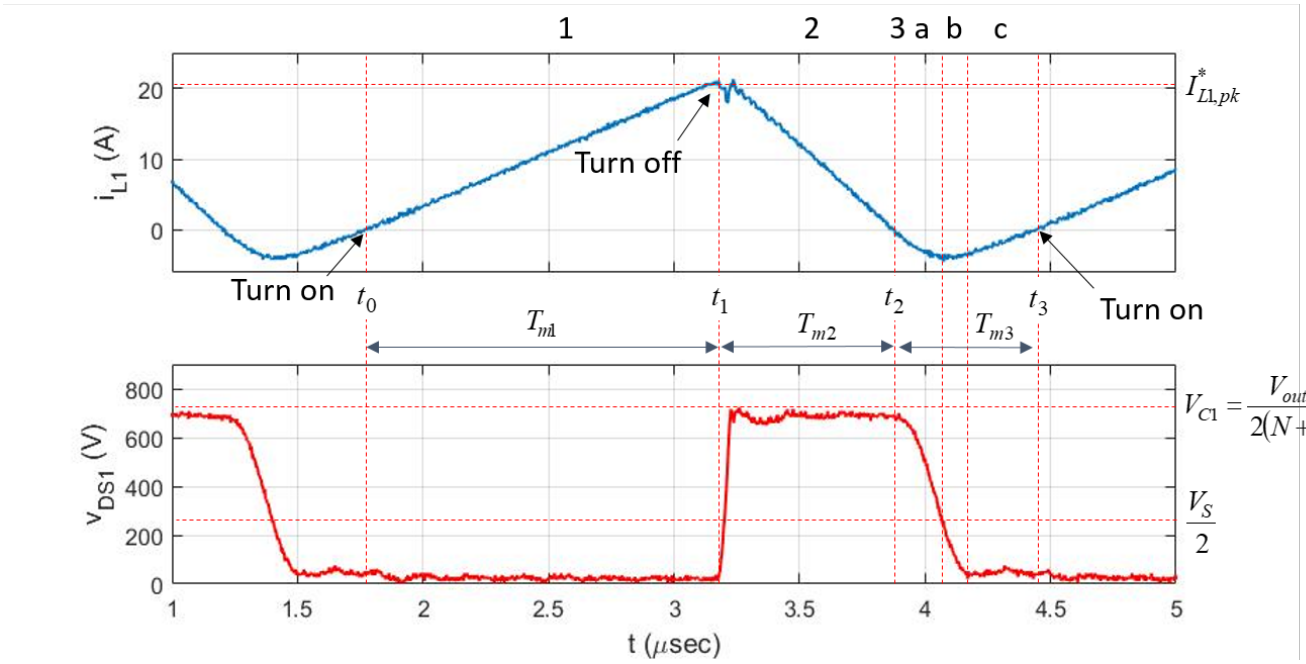

Fig. 3: Characteristic inductor current and drain-source voltage for top pole of 5-stage HSCC prototype; the modes of operation are labeled at the top

During HSCC operation, the inductor current and switch voltage exhibit a distinctive operational characteristic. Figure 3 shows this for the hardware prototype presented in Section III. The switch cycle has three distinct modes which are labeled at the top of Figure 3 and discussed below. Times are also labeled, t_0 … t_3, to mark transitions. For the analysis presented herein, it is noted that quantities written in upper case are assumed constant over a switching cycle, while quantities that are written as lower case are time varying.

A. Switch modes

In Mode 1, the MOSFET switch is turned *on* just as the inductor current crosses zero. The inductor current increases linearly while the switch is *on*. Based on the time the MOSFET stays in the *on* state, the peak inductor current may be computed. Neglecting the series resistance of the inductor, the time spent in Mode 1 for a given peak inductor current is computed according to the following.

Mode 1 (MOSFET *on*):

$$\frac{di_{L1}}{dt} = \frac{V_S}{2L} \tag{2}$$

$$T_{m1} = I_{L1,pk}\frac{2L}{V_S} \tag{3}$$

where V_S is the source voltage for the entire converter, L is the input inductance, T_{m1} is the time the MOSFET switch is in the *on* state.

The charge transferred during Mode 1 is given as the integral of inductor current over the interval. Assuming a triangular waveform, the charge Q_1 is given simply as

$$Q_1 = \int_{t_0}^{t_1} i_{L1}(t)dt = \frac{I_{L,pk}T_{m1}}{2} = \frac{L}{V_S}I_{L,pk}^2 \tag{4}$$

When the peak current $I_{L1,\mathrm{pk}}$ reaches the reference value $I^*_{L1,pk}$, the MOSFET switch turns *off*, diode D_1 begins conducting, and the inductor current falls. This is Mode 2, and it continues until i_{L1} crosses zero again. Neglecting again the inductor series resistance and the diode voltage drop (i.e. assuming v_{DS1}=V_{C1}), the rate of change in the inductor current and the time spent in mode 2 (T_{m2}) may be computed as follows.

Mode 2 (MOSFET *off*, i_{L1}>0):

$$\frac{di_{L1}}{dt} = \frac{1}{L}\left(\frac{V_S}{2} - V_{C1}\right) \tag{5}$$

$$T_{m2} = \frac{2L}{2V_{C1} - V_S}I_{L1,pk} = \frac{2L(N+1)}{V_{out} - V_S(N+1)}I_{L1,pk} \tag{6}$$

where V_{C1} is given by (1). Again, assuming a triangular waveform, the charge transferred in Mode 2 may be computed as follows

$$Q_2 = \int_{t_1}^{t_2} i_{L1}(t)dt = \frac{I_{L,pk}T_{m2}}{2} = \frac{L(N+1)}{V_{out} - V_S(N+1)}I_{L,pk}^2 \tag{7}$$

In Mode 3, the inductor current becomes negative, causing the diode to stop conducting. In this mode, the switch voltage v_{DS1} begins falling as the even-numbered diodes in the charge pump output stage begin conducting in sequence, quickly pushing the switch node voltage down. To facilitate the analysis, Mode 3 is divided into three steps designated a, b, and

c. In Mode 3a, the switch node voltage is above the input voltage $v_{DS1}>V_S/2$, and the inductor current continues reducing.

The diode switching in the diode-capacitor ladder is sequential; thus, the rate at which v_{DS1} falls is computed assuming there is a charge-pump time constant τ_{CP} that may be calculated from the number of stages, the capacitor values, the capacitor equivalent series resistance (ESR) values, and an equivalent resistance value attributed to the SiC diodes. The time spent in the $v_{DS1}>V_S/2$ condition defines the length of time spent in Mode 3a, T_{m3a}. Finally, the minimum inductor current $I_{L1,\min}$, may then be computed. The calculation is as follows.

Mode 3a (MOSFET *off*, $i_{L1}<0$, $v_{DS1}>V_S/2$):

$$\tau_{CP} = \sum_{n=1}^{N+1} C\left(r_C + \frac{r_D}{2n+1}\right) \tag{8}$$

$$\frac{dv_{DS1}}{dt} = -\frac{V_{C1}}{2.75\tau_{CP}} \tag{9}$$

$$T_{m3a} = 2.75\tau_{CP}\left(1 - \frac{V_S(N+1)}{V_{out}}\right) \tag{10}$$

$$\begin{aligned} i_{L1,\min} &= \frac{1}{L}\int_{t_2}^{t_2+T_{m3a}} \left(\frac{V_S}{2} - v_{DS1}(t)\right)dt \\ &= \frac{1.375\tau_{CP}}{L}\left(V_S - \frac{V_{out}}{2(N+1)} - \frac{V_S^2(N+1)}{2V_{out}}\right) \end{aligned} \tag{11}$$

where C is the capacitance in each capacitor, r_C is the ESR value in Ohms, r_D is the equivalent series resistance of the diode, calculated using the datasheet IV characteristic [10], and the $2.75\tau_{CP}$ term in (10) is assumed based on a 10%-90% change in 2.2 time constants and a linear extrapolation.

When $v_{DS1}=V_S/2$, the inductor current slope is zero, and the inductor current is at minimum. The switch voltage v_{DS1} continues to fall monotonically until it is near zero. When $v_{DS1} < V_S/2$, the inductor current begins again to rise. While $0<v_{DS1}< V_S/2$, the converter is in Mode 3b. The time spent in Mode 3b and current at the end of Mode 3b are computed below.

Mode 3b (MOSFET *off*, $i_{L1}<0$, $0<v_{DS1}<V_S/2$):

$$T_{m3a} + T_{m3b} = 2.75\tau_{CP} \tag{12}$$

$$i_{L1,m3b} = \frac{1.375\tau_{CP}}{L}\left(V_S - \frac{V_{out}}{2(N+1)}\right) \tag{13}$$

When the switch node voltage has reached approximately zero, the converter is in Mode 3c. The rate of change in the current and the time spent in Mode 3c are computed as follows.

Mode 3c (MOSFET *off*, $i_{L1}<0$, $v_{DS1}=0$):

$$\frac{di_{L1}}{dt} = \frac{V_S}{2L} \tag{14}$$

$$T_{m3c} = -\frac{2Li_{L1,m3b}}{V_S} = \frac{1.375\tau_{CP}}{V_S(N+1)}V_{out} - 2.75\tau_{CP} \tag{15}$$

For Mode 3, the charge is computed over the sub-intervals and summed. After much algebraic manipulation, the result is given in (16).

$$\begin{aligned} Q_3 &= \int_{t_2}^{t_2+T_{m3a}+T_{m3b}} i_{L1}(t)dt + \int_{t_3-T_{m3c}}^{t_3} i_{L1}(t)dt \\ &= \frac{{\tau_{CP}}^2}{L}\left(0.6301\frac{V_{out}}{(N+1)} - 0.4727\frac{{V_{out}}^2}{V_S(N+1)^2}\right) \end{aligned} \tag{16}$$

The time spent in Mode 3 is computed as the sum of the three intervals as follows.

$$T_{m3} = T_{m3a} + T_{m3b} + T_{m3c} = \frac{1.375\tau_{CP}}{V_S(N+1)}V_{out} \tag{17}$$

The switch cycle period is given by the sum of the times spent in the three modes as follows

$$\begin{aligned} T_{sw} &= T_{m1} + T_{m2} + T_{m3} \\ &= \left(\frac{2L}{V_S} + \frac{2L(N+1)}{V_{out} - V_S(N+1)}\right)I_{L,pk} + \frac{1.375\tau_{CP}}{V_S(N+1)}V_{out} \end{aligned} \tag{18}$$

It thus follows that the switching frequency is given as

$$f_{sw} = \frac{1}{\left(\frac{2L}{V_S} + \frac{2L(N+1)}{V_{out} - V_S(N+1)}\right)I_{L,pk} + \frac{1.375\tau_{CP}}{V_S(N+1)}V_{out}} \tag{19}$$

B. Power Flow

Assuming both poles of the converter operate symmetrically, the input power to the converter may be calculated by the product of the input voltage and the average inductor current I_{L1}, averaged over the three modes of the switch cycle

$$P_{in} = V_S I_{L1} = V_S \frac{(Q_1 + Q_2 + Q_3)}{T_{sw}} \tag{20}$$

wherein the quantities in (20) are expressed in the preceding equations as functions of input voltage, output voltage, key circuit parameters, and peak inductor current.

V. Hardware Results

To demonstrate the performance of the bipolar HSCC prototype and validate the analysis presented above, the prototype was tested at several operating points. Specifically, the input voltage was supplied by an Ametek / Sorenson SGI 600/8 power supply and varied. The gating signals were controlled using a waveform generator to accomplish the proposed switching scheme. The RMS input and output voltages and currents were measured using Fluke digital multi-meters. The results for five experiments are summarized in Table II. The waveform in Figure 3 was taken during experiment 5.

Of particular note is that the converter is demonstrated to boost 460 V to 8.63 kV at 3.63 kW with an efficiency of nearly 97%. In fact, the average efficiency for the operating points is over 97.5%. This is a higher efficiency than what was reported in [4]. Furthermore, the converter is demonstrated to switch at a much higher frequency than what was reported in [4]. This high efficiency is attributed to the method of control which turns the MOSFET on at i_L=0, and thus significantly reduces switching loss in the MOSFET.

In addition, the converter behavior is found to be consistent with analytical prediction. Figure 4 illustrates both the P_{in} versus $I_{L,pk}$ characteristic and the switching frequency versus $I_{L,pk}$ characteristic. The analysis in Section IV is used to create a family of curves assuming constant input and output voltages from the five experiments. The measured values are then included. Both comparisons show good agreement with measured values lying on or very close to their respective curves.

VI. Conclusions and Future Work

In this paper, a high voltage, high-gain DC-DC boost converter is realized using a novel bipolar hybrid switched capacitor topology with WBG devices. In particular, a method of control is developed that reduces the *on* transition switching losses and controls power into the converter through control of a peak current. Experiments are done to demonstrate operation of the converter and to validate the analysis. This analysis is intended to support the development of a hardware controller.

Hardware experiments were done at several operating points. In particular, the converter was demonstrated to step 460 V up to 8.63 kV at 3.63 kW with an efficiency of nearly 97%. Comparison with measured results show that the converter power and switching frequency were consistent with analytical prediction, and the average conversion efficiency was greater than 97.5%.

Future work will focus on methods to further improve efficiency, to optimize for power density, and to evaluate performance for various applications.

A. Future Work

To increase the efficiency further, future efforts will include parameter optimization, use of v-GaN diodes, adjustments to the topology, and advanced packaging approaches.

Vertical GaN diodes are available in a pseudo-production stage as pin-diodes. These diodes exhibit increased unipolar figures of merit compared to SiC and would be expected to exhibit lower switching and conduction losses in a wide variety of usage scenarios, decreasing HSCC losses in future converter instantiations.

Regarding the topology, a method to further reduce switching loss in the MOSFET would be to include a capacitor in parallel with the main inductor to absorb charge during the sharp transitions between operating modes. This has been shown in SPICE simulations to decrease the switching losses in the MOSFET.

Converter size can be reduced considerably by taking advantage of advanced packaging technology. Some additional size reduction can be achieved by pushing

Table II: Measured Hardware data

Exp.	V_S (V)	$I_{L,pk}$ (A)	V_{out} (V)	P_{in} (W)	Eff (%)	Gain	f_{sw} (kHz)	$I_{L,min}$ (A)
1	100	5.52	2142	190.4	97.88	21.44	310	-1.44
2	200	10.5	4247	766.2	97.56	21.26	330	-2.56
3	300	14.1	5911	1543.8	97.64	19.72	364	-3.12
4	400	18.6	7788	2855.6	97.63	19.47	365	-3.60
5	460	20.3	8630	3632.6	96.93	18.77	375	-3.92

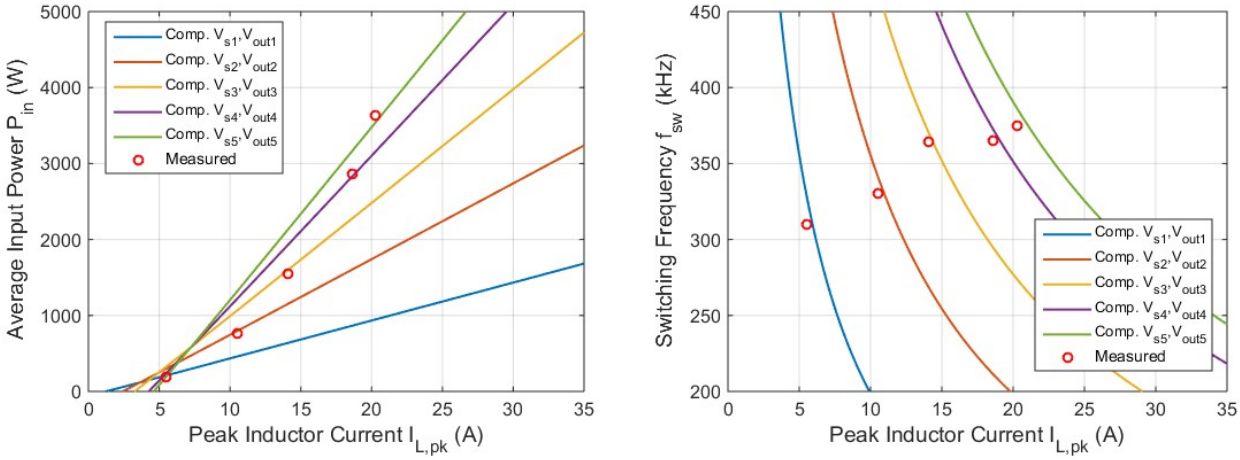

Fig. 4: Comparison of measurements and analytical prediction for (left) P_{in} vs $I_{L,pk}$ and (right) switching frequency vs $I_{L,pk}$

components more closely together; however, maintaining voltage hold-off and achieving good thermal management are a challenge with standard printed circuit board based designs. To achieve significant size reduction, new packaging paradigms will be investigated.

Finally, the net circuit performance will be evaluated for select applications. For applications in photovoltaics there is the California Energy Commission (CEC) weighted efficiency [11]. In this qualification, the efficiency of a power electronic converter is calculated based on a weighted average of the efficiency at different loading levels. Efforts are under way to optimize the circuit for CEC efficiency. For military applications, such as naval electric ship or pulsed power systems, the circuit will be evaluated over select operational vignettes [12].

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