SAND2017-9889C

Prediction of Pareto-Optimal Performance Improvements in a Power Conversion System using GaN Devices

B. Zhang, S. Sudhoff, S. Pekarek, R. Swanson
Electrical and Computer Engineering
Purdue University
West Lafayette, Indiana, USA

J. Flicker, J. Neely, J. Delhotal, R. Kaplar
Sandia National Laboratories
Albuquerque, New Mexico, USA

***Abstract*—Gallium Nitride (GaN) semiconductors have extremely low switching loss, high breakdown voltage, and high junction temperature rating. These characteristics enable improved device performance and thus improved switch mode power converter designs. This paper evaluates the Pareto-optimal performance improvements for a DC generation system with predicted GaN loss characteristics and a rigorous multi-objective optimization based design paradigm. The optimization results show that the application of GaN can achieve a 6.4% mass savings relative to Silicon Carbide (SiC) and 40% mass savings relative to Silicon (Si) at the same loss level for a 10 kW application.**

Keywords—GaN; DC generation system; optimization-based design

I. INTRODUCTION

Several power converter size (power density) and efficiency targets have been set by government agencies and corporate entities for power electronics used in military systems, electric vehicles, and renewable energy applications [1]. The use of wide bandgap (WBG) devices has resulted in considerable performance improvement in power converters, meeting and sometimes surpassing these targets. In general, the properties of WBG devices, which allow faster switching frequency and higher junction temperatures, enable improvements to power density and efficiency; however, an exact mapping has not been identified. It is valuable to consider how the use of a WBG device with prescribed characteristics will affect the design space for a given application.

The motivation of this research is to develop the capability to predict the Pareto-optimal performance of a given power converter topology, for a given device type. In particular, this effort aims to identify, quantitatively, the expected Pareto-optimal performance improvement from the utilization of vertical GaN (v-GaN) transistors and GaN Junction Barrier Schottky (JBS) diodes, as compared to solutions based on Si and SiC based designs.

This work was supported by Sandia National Laboratories Contract Agreement 1701331 and the Office of Naval Research Grants N000141410160 and N000141612956.

Sandia National Laboratories is a multi-mission laboratory managed and operated by National Technology and Engineering Solutions of Sandia, LLC., a wholly owned subsidiary of Honeywell International, Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525.

Rapid progress in growth and fabrication of v-GaN diodes has been made in the past few years, with device unipolar figures of merit exceeding those of SiC. As the voltage is dropped across a thick vertical drift region, rather than along the surface as in conventional lateral GaN devices, v-GaN devices can operate in systems requiring higher voltage hold-off. This enables competition with SiC and Si devices in voltage regimes above 1200 V.

In [2], the Pulse Width Modulation (PWM) converter power density limit is achieved by optimizing the heatsink and passive components separately. But the impact of such optimizations on the system efficiency is not considered.

In [3], a multi-objective optimization design paradigm of a DC generation system is set forth. This paradigm is applied herein to quantify the potential advantages, in terms of mass and efficiency, that GaN devices provide relative to Si and SiC devices. To support a rigorous comparison, conduction and switching loss models are integrated with generator and converter design models to form a single multi-objective optimization of a 10 kW DC generation system. An evolutionary optimization approach is then used to establish the theoretically achievable performance boundary between mass and loss for the entire system.

II. SYSTEM DESCRIPTION

The DC generation system considered consists of a Permanent Magnet Synchronous Machine (PMSM), a passive rectifier, a filter inductor and capacitor, and a DC-DC converter. The system topology is shown in Fig. 1. The passive rectifier is chosen here because of its low cost and robustness. To simplify the system design, the rectifier diodes are the same as the DC-DC converter diodes. Permanent magnet inductors (PMIs) [4] are used for input inductor L_{in} and output inductor L_{out} in order to reduce size. Since L_{in} sees a low frequency current ripple, a Hiperco steel is used as the core material to reduce mass. Since L_{out} sees the switching frequency, a ferrite is used as the core material to reduce high-frequency loss. Polypropylene capacitors are used for C_{in} and C_{out} because of their bandwidth and lifetime.

The design approach is based on full load operation. At full load, the output inductor waveform is assumed to be as in Fig. 2. Because the output inductor current is always positive, only

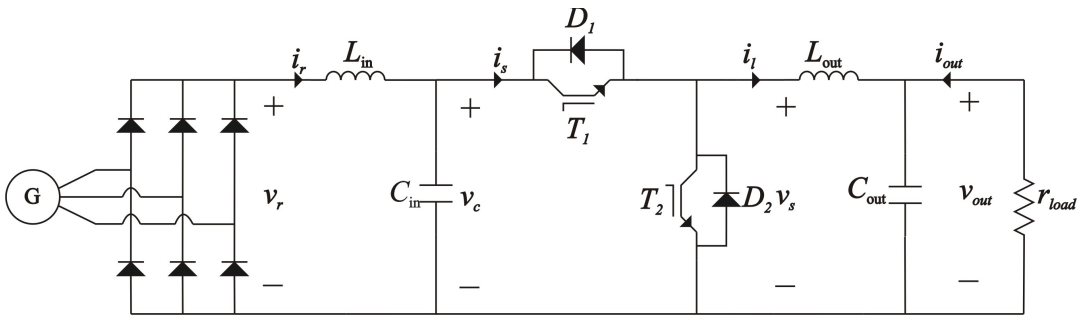

Fig. 1. System topology

transistor T_1 and diode D_2 conduct under full load condition. The function of T_2 and D_1 is to avoid the discontinuous conduction mode [5] under light load. In Fig. 2, d is the duty cycle, i_{mn} and i_{mx} are the minimum and maximum output inductor current, T_{sw} is the switching period, $\overline{i_l}$ is the average output inductor current, Δi_l is the output inductor current ripple. The current extrema i_{mn} and i_{mx} may be expressed as $i_{mn} = \overline{i_l} - \Delta i_l / 2$, $i_{mx} = \overline{i_l} + \Delta i_l / 2$.

III. Semiconductor Models

In this section, a generic semiconductor loss model is established based on [3]. Then the loss model is applied to Si, SiC, and GaN with variances based on different semiconductor materials and types.

A. Semiconductor Loss Model

The transistor loss model contains the conduction loss and the switching loss. The instantaneous conduction loss of the transistor is expressed as

$$p_{t,cd}\left(i_{t,cd}\right) = \alpha_{t,cd} i_{t,cd} + \beta_{t,cd} \left(i_{t,cd} / i_b\right)^{\gamma_{t,cd}} \tag{1}$$

where $i_{t,cd}$ is the transistor current during the transistor conduction period, and $\alpha_{t,cd}$, $\beta_{t,cd}$ and $\gamma_{t,cd}$ are model parameters. The base current i_b =1 A.

The switching energy is expressed as

$$E_{t,y}(i_{t,sw}, v_t) = (\alpha_{t,y} {i_{t,sw}}^2 + \beta_{t,y} i_{t,sw} + \gamma_{t,y}) v_t / v_{t,b} \tag{2}$$

where $v_{t,b}$ is the base voltage, v_t is the off-state voltage, $i_{t,sw}$ is the current at the instant prior to the switching event, $\alpha_{t,y}$, $\beta_{t,y}$ and $\gamma_{t,y}$ are model parameters, and the subscript *y* is either "on" or "off" to designate turn on or turn off energy loss, respectively.

The diode loss model contains the conduction loss and reverse recovery loss. The instantaneous conduction loss is expressed as

$$p_{d,cd}(i_f) = \alpha_{d,cd} i_f + \beta_{d,cd} \left(i_f / i_b\right)^{\gamma_{d,cd}} \tag{3}$$

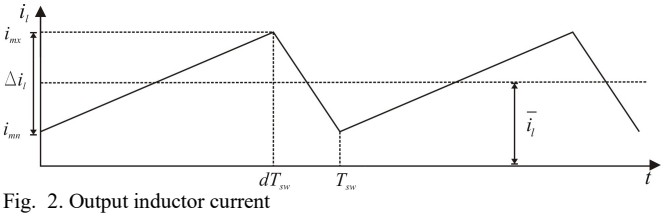

Fig. 2. Output inductor current

where the i_f is the forward conduction current and $\alpha_{d,cd}$, $\beta_{d,cd}$ and $\gamma_{d,cd}$ are model parameters.

The diode reverse recovery loss is established in [4] which can be approximated using the sequence

$$I_{rr0}(i_{mn}) = \alpha_{irr} i_{mn} + \beta_{irr} \left(i_{mn} / i_b\right)^{\gamma_{irr}} \tag{4}$$

$$t_{rr}(i_{mn}) = \alpha_{trr} i_{mn} + \beta_{trr} \left(i_{mn} / i_b\right)^{\gamma_{trr}} \tag{5}$$

$$P_{d,rr} = v_c^2 I_{rr0}(i_{mn}) t_{rr}(i_{mn}) / (4 v_{d,b} T_{sw}) \tag{6}$$

where v_c is the input capacitor voltage, $v_{d,b}$ is the diode base voltage, $\alpha_{trr}, \beta_{trr}, \gamma_{trr}, \alpha_{irr}, \beta_{irr}, \gamma_{irr}$ are model parameters.

With the loss model just set forth and the current waveform shown in Fig. 2, the DC-DC converter semiconductor loss can be calculated. The average transistor conduction loss $P_{t,cd}$ can be expressed as

$$P_{t,cd} = d\left(\frac{\alpha_{t,cd}(i_{mx} + i_{mn})}{2} + \frac{\beta_{t,cd}\left(i_{mx}^{\gamma_{t,cd}+1} - i_{mn}^{\gamma_{t,cd}+1}\right)}{(\gamma_{t,cd}+1)(i_{mx} - i_{mn}) i_b^{\gamma_{t,cd}}}\right) \tag{7}$$

The transistor switching loss is given by

$$P_{t,sw} = f_{sw} E_{t,on}(i_{mn}, v_t) + f_{sw} E_{t,off}(i_{mx}, v_t) \tag{8}$$

where f_{sw} is the switching frequency.

The average diode conduction loss $P_{d,cd}$ is expressed as

$$P_{d,cd} = (1-d)\left(\frac{\alpha_{d,cd}(i_{mx} + i_{mn})}{2} + \frac{\beta_{d,cd}\left(i_{mx}^{\gamma_{t,cd}+1} - i_{mn}^{\gamma_{t,cd}+1}\right)}{(\gamma_{d,cd}+1)(i_{mx} - i_{mn}) i_b^{\gamma_{t,cd}}}\right) \tag{9}$$

For the rectifier loss analysis, since the switching frequency of the rectifier diode is low, the reverse recovery loss is neglected. The rectifier operation is divided into a commutation interval and conduction interval. During the commutation interval, the DC link current $i_r(t)$ is shared between two diodes and a third one completes the return path.

During the conduction interval, $i_r(t)$ travels through two diodes. Neglecting the commutation period the rectifier loss is approximated as

$$P_{rec,cd}(i_r(t)) = 2\left(\frac{1}{2\pi/\omega_r}\int_0^{2\pi/\omega_r} p_{d,cd}(i_r(t))dt\right) \quad (10)$$

where ω_r is the generator electrical speed and $i_r(t)$ can be achieved based on the waveform reconstruction algorithm [3]. In (10), the integration is evaluated numerically.

B. Si Semiconductor loss

The Si IGBT conduction loss and switching loss can be calculated based on (7) and (8), respectively. The Si PN junction diode conduction loss and reverse recovery loss can be calculated based on (9) and (6), respectively. The Si rectifier loss can be calculated based on (10). Thus the total Si semiconductor loss is expressed as

$$P_{Si,semi} = P_{t,cd} + P_{t,sw} + P_{d,cd} + P_{d,sw} + P_{rec,cd} \quad (11)$$

The model parameters used in (6)-(10) are achieved by fitting the Microsemi APT13GP120B IGBT datasheet [6] and Powerex CS241250D diode datasheet [7]. The parameters are listed in Table I and Table II.

C. SiC Semiconductor Loss

The SiC MOSFET conduction loss and switching loss can be calculated based on (7) and (8), respectively. Since the SiC Schottky diode is a majority-carrier device, there are no minority carriers stored during forward conduction. Thus, the DC-DC converter diode reverse recovery loss is neglected herein. The diode conduction loss can be calculated from (9). The rectifier loss can be calculated from (10). Thus the SiC semiconductor loss is expressed as

$$P_{SiC,semi} = P_{t,cd} + P_{t,sw} + P_{d,cd} + P_{rec,cd} \quad (12)$$

The model parameters used in (7)-(9) and (10) are achieved by fitting the Cree C2M0080120D MOSFET datasheet [8] and Cree C4D20120A diode datasheet [9]. The parameters are listed in Table III and Table IV.

D. Predicted GaN Semiconductor loss

While v-GaN diodes have been fabricated in a quasi-production mode [10][11], more advanced two terminal (JBS diodes) or three terminal (MOSFETs) devices are still in the early research phase due to, for example, limitations of GaN selective-area doping. Therefore, since advanced v-GaN semiconductor devices are under development, a predicted loss model is proposed based on GaN's material properties [12]-[15] in advanced topologies with conduction/switching loss calculated based on similar devices fabricated from SiC.

For the losses of a theoretical future GaN JBS diode, an optimization program described in [16] was utilized to optimize a GaN SBD for a minimized power dissipation in a power conversion system. The GaN SBD was optimized for reverse biased voltage of 1200V, forward current density of 500 A/cm^2, switching frequency of 200 kHz, duty cycle of

TABLE I. SI IGBT LOSS MODEL PARAMETERS

$\alpha_{t,cd}$	1.1119 V	$\gamma_{t,on}$	$6.1034\cdot10^{-5}$ J
$\beta_{t,cd}$	0.3468 W	$\alpha_{t,off}$	$1\cdot10^{-8}$ J/A^2
$\gamma_{t,cd}$	1.7135	$\beta_{t,off}$	$5.396\cdot10^{-5}$ J/A
$\alpha_{t,on}$	$6.337\cdot10^{-8}$ J/A^2	$\gamma_{t,off}$	$1.0779\cdot10^{-4}$ J
$\beta_{t,on}$	$4.945\cdot10^{-5}$ J/A	$v_{t,b}$	600V

TABLE II. SI DIODE LOSS MODEL PARAMETERS

$\alpha_{d,cd}$	0.4131 V	γ_{trr}	0.1275
$\beta_{d,cd}$	0.2799 W	α_{irr}	$1.7636\cdot10^{-6}$
$\gamma_{d,cd}$	1.3553	β_{irr}	4.1159 A
α_{trr}	$3.1\cdot10^{-9}$ s/A	γ_{irr}	0.6493
β_{trr}	$2.609\cdot10^{-7}$ s	$v_{d,b}$	600V

TABLE III. SIC MOSFET LOSS MODEL PARAMETERS

$\alpha_{t,cd}$	1.3028 V	$\gamma_{t,on}$	$2.7409\cdot10^{-5}$ J
$\beta_{t,cd}$	0.0064 W	$\alpha_{t,off}$	$2.454\cdot10^{-7}$ J/A^2
$\gamma_{t,cd}$	2.7744	$\beta_{t,off}$	$-9.938\cdot10^{-7}$ J/A
$\alpha_{t,on}$	$5.852\cdot10^{-7}$ J/A^2	$\gamma_{t,off}$	$5.7478\cdot10^{-5}$ J
$\beta_{t,on}$	$3.752\cdot10^{-7}$ J/A	$v_{t,b}$	800V

TABLE IV. SIC DIODE LOSS MODEL PARAMETERS

$\alpha_{d,cd}$	0.9784 V	$\beta_{d,cd}$	0.0239 W	$\gamma_{d,cd}$	2.0672

50%, and a die size (A) equal to a similar SiC diode available from Cree (0.308×0.308 cm^2) [17]. From the optimization program, the ideal device thickness was found to be 6.14 μm with a doping density of $2.08\cdot10^{15}$ cm^{-3}, which yields an intrinsic device on-resistance $R_{on,d}$ of 1.22 mΩcm^2.

To calculate the power dissipated in a circuit, it is assumed that the SBD is a majority-carrier device, which effectively has no reverse recovery due to recombination of minority carriers. The total power dissipation is then approximately equal to the conduction loss in the diode and can be calculated as

$$p_{d,cd}(j_f) = j_f A\phi + Aj_f^2 R_{on,d} \quad (13)$$

where j_f is the forward current density and ϕ is the Schottky barrier height which equals to 1.12 eV [1]. Since for a certain GaN SBD, the diode size A is fixed, then (13) can be written as (3) with $i_f = j_f A$, $\alpha_{d,cd} = \phi$, $\beta_{d,cd} = R_{on}/A$ and $\gamma_{d,cd} = 2$.

The formulation of a power dissipation model for a GaN MOSFET is difficult due to the device complexity as well as the lack of devices in production. Therefore, an idealized GaN MOSFET structure is proposed based on production-level SiC MOSFET devices.

In general, the higher critical electric field of GaN compared to SiC means that thinner layers of material are needed to hold off a given voltage, yielding lower intrinsic resistance. In a MOSFET, this resistance reduction can either be used to decrease the on-resistance of a device (decrease conduction losses) or to reduce die area (and thus decrease dynamic power dissipation). In this treatment, it is assumed that GaN device conduction loss is kept constant compared to SiC device conduction loss and the increased critical electric field is utilized to decrease the die area. In order to determine the approximate switching loss in a GaN MOSFET, an optimization program was developed to extract the

characteristic dimensions of a Cree MOSFET from the datasheet [8] operational parameters (gate threshold voltage, transconductance, input capacitance, output capacitance, reverse transfer capacitance, gate to source charge, gate to drain charge, total gate charge, turn on delay time, rise time, fall time, turn off delay time) using the equations presented in [18]. These dimensions were then scaled by a factor (F) given by

$$F = \sqrt{\frac{R_{on,T}^{GaN}}{R_{on,T}^{SiC}}} \tag{14}$$

where $R_{on,T}^{GaN}$ and $R_{on,T}^{SiC}$ are the intrinsic device on-resistance ($R_{on,T}$) for GaN MOSFET and SiC MOSFET, respectively. The $R_{on,T}$ is expressed as

$$R_{on,T} = \frac{4V_{rated}}{\varepsilon \mu_n E_c} \tag{15}$$

where $\varepsilon = \varepsilon_s \varepsilon_0$ is the dielectric constant of the material, V_{rated} is the rated voltage of the device, μ_n is the mobility of majority carriers, and E_c is the critical electric field. The parameters used to calculate $R_{on,T}$ are listed in the Table V. In Table V, N_d is donor site density, and E_g is the bandgap energy.

With the scaled dimensions, new values for switching energy for the GaN MOSFET can be calculated using the equations presented in [18] for a given applied current. From that point, equations (7)-(10) can be applied to the GaN semiconductor devices with the model parameters updated. The GaN semiconductor loss is expressed as

$$P_{GaN,semi} = P_{t,cd} + P_{t,sw} + P_{d,cd} + P_{rec,cd} \tag{16}$$

The predicted loss model parameters are listed in Table VI and Table VII. It is noted that power dissipation due to packaging and device parasitics are neglected since these are typically much less than the intrinsic device power dissipation. In addition, the resistance added by ohmic contacts are neglected due to the very low resistance values that can be achieved with a suitably large contact area [19].

IV. Multi-objective Optimization Based Design

In [3], the DC generation system design is formulated as a multi-objective optimization problem.

A. Optimization Objectives

The two objectives of the optimization problem are to minimize the system mass (M) and to minimize the system loss (P). The system mass includes the generator mass (M_G), the input inductor mass, the output inductor mass, the input capacitor mass, the output capacitor mass, and the heatsink mass. The system loss include the generator loss (P_G), the passive rectifier conduction loss, the MOSFET/IGBT conduction loss and switching loss, the DC-DC converter diode loss and the input and output inductor DC loss.

TABLE V. MOSFET ON RESISTANCE CALCULATION PARAMETERS

Parameter	GaN	SiC
V_{rated}	1380 V	1380 V
μ_n (N_d= $4 \cdot 10^{16}$ sites/cm^2) [16]	1402	743
ε_S	9.7 [20]	9.66 [21]
E_c	$1.73 \cdot 10^5 E_g^{2.5}$ [22]	$\frac{2.49 \cdot 10^6}{1 - 0.25 \log(N_d \cdot 10^{-16})}$ [21]

TABLE VI. PREDICTED GAN MOSFET LOSS MODEL PARAMETERS

$\alpha_{t,cd}$	1.3028 V	$\gamma_{t,on}$	$1 \cdot 10^{-12}$ J
$\beta_{t,cd}$	0.0064 W	$\alpha_{t,off}$	$5.23 \cdot 10^{-8}$ J/A^2
$\gamma_{t,cd}$	2.7744	$\beta_{t,off}$	$2.0175 \cdot 10^{-6}$ J/A
$\alpha_{t,on}$	$1.477 \cdot 10^{-7}$ J/A^2	$\gamma_{t,off}$	$1 \cdot 10^{-12}$ J
$\beta_{t,on}$	$3.718 \cdot 10^{-6}$ J/A	$v_{t,b}$	800V

TABLE VII. PREDICTED GAN JBS LOSS MODEL PARAMETERS

$\alpha_{d,cd}$	1.03 V	$\beta_{d,cd}$	0.0136 W	$\gamma_{d,cd}$	2

B. Optimization Constranits

There are thirty-three constraints imposed on this optimization problem. These include generator geometry constraints; generator magnetic field constraints to avoid overly saturating the rotor and stator steel and avoiding permanent magnet (PM) demagnetization; converter ripple constraints to limit the rectifier DC current (i_r) ripple, rectifier DC voltage (v_r) ripple, output current (i_l) ripple, and output voltage (v_{out}) ripple; a rectifier under voltage constraint; a rectifier mode constraint; a system full load operation constraint which ensures the output inductor current is always larger than zero; input and output capacitor thermal constraint; heat sink constraint to ensure a valid heatsink design; system dynamic constraints (DyC) which are added here to guarantee the system transient performance. Although these constraints are described in more detail in [3], it is appropriate to describe the DyC in detail herein because they have a significant impact on performance.

The DyC are based on system frequency domain impedance analysis. In particular, in order to address the ability of the converter output voltage to be stiff with respect to load disturbance, a constraint is placed on the converter output impedance. In particular, the magnitude of the converter output impedance is required to be less than 5% of the converter output base impedance, defined as the ratio of rated output voltage over rated output current, over the 1-1000 Hz frequency range. Another DyC constraint is that the system is stable.

V. Case Study

With the optimization based design paradigm introduced in [3], a case study is set forth. The design variables and their range are listed in Table VIII. These include the number of pole pairs P_p, radius of the stator teeth r_{st}, air gap length g, permanent magnet depth d_m, depth of rotor back iron d_{rb}, depth of stator tooth base d_{tb}, depth of stator back iron d_{sb}, tooth fraction α_t, PM fraction α_{pm}, PM residual flux density B_r, machine active length l, peak phase conductor density N_{s1}, switching frequency f_{sw}, input inductor inductance L_{in}, output

TABLE VIII. DESIGN SPACE

Parameter	Min	Max	Units
P_p	2	7	N/A
r_{st}	1.4	36.25	cm
d_{rb}	0.1	15	cm
d_m	0.1	5	cm
g	1	2.5	mm
d_{tb}	0.1	5	cm
α_t	0.1	0.9	N/A
d_{sb}	0.1	5	cm
α_{pm}	0.1	0.9	N/A
B_r	0.5	1.3	T
l	1	20	cm
N_{sl}	1	$1.0\cdot10^4$	cond/rad
f_{sw}	$1.0\cdot10^3$	$1.0\cdot10^6$	Hz
L_{in}	$1.0\cdot10^{-6}$	$1.0\cdot10^{-1}$	H
J_{Lin}	$7.5\cdot10^4$	$7.5\cdot10^6$	A/m^2
L_{out}	$1.0\cdot10^{-6}$	$1.0\cdot10^{-1}$	H
J_{Lout}	$7.5\cdot10^4$	$7.5\cdot10^6$	A/m^2
C_{in}	$1.0\cdot10^{-6}$	$1.0\cdot10^{-2}$	F
C_{out}	$1.0\cdot10^{-6}$	$1.0\cdot10^{-2}$	F
$\bar{i}_{r,0}$	0.01 $i_{r,max}$	$i_{r,max}$	A

TABLE IX. SYSTEM SPECIFICATIONS

Specification	Value	Specification	Value
v_{out}	750 V	J_{max}	$7.5\cdot10^6$ A/m^2
$v_{r,min}$	775 V	ΔT_{max}	30°C
$i_{r,max}$	13 A	ω_{rm}	9000 RPM
P_{out}	10 kW	m_s	JFE 10JNEX900
δ_{vout}	0.001	m_r	JFE 10JNEX900
δ_{il}	0.2	m_c	Copper
δ_{vcin}	0.05	k_{pf}	0.42
δ_{ir}	0.2	n_{spc}	1
δ_{imp}	0.05	r_{rs}	0.01 m
n_{spp}	2	$T_{d,j}$	175°C (SiC/GaN) 150°C (Si)
$T_{t,j}$	150°C	v_t	2V
α^*	-0.5	k_{max}	20
$d_{e,max}$	0.0001	$v_{e,max}$	0.01

inductor inductance L_{out}, input inductor current density J_{Lin}, output inductor current density J_{Lout}, input capacitor capacitance C_{in}, output capacitor capacitance C_{out} and the initial value of rectifier DC current $\bar{i}_{r,0}$. The system specifications are listed in Table IX. In Table IX, v_{out} is the rated output voltage, $v_{r,min}$ is the minimum rectifier DC voltage, $i_{r,max}$ is the maximum rectifier DC current, P_{out} is the rated output power, δ_{ir}, δ_{vcin}, δ_{il}, and δ_{vout} are specifications of converter ripple constraints, δ_{imp} is the impedance specification index of the DyC, n_{spp} is the number of stator slots per pole per phase, $T_{t,j}$ is the maximum transistor operating temperature, α^* is the commanded firing angle relative to back EMF, $d_{e,max}$ and $v_{e,max}$ are the error criteria of the system steady state analysis [3], k_{max} is the maximum iterations of the steady state analysis, J_{max} is the maximum current density of input inductor, output inductor, and generator, ΔT_{max} is the maximum temperature rise of the capacitors allowed, ω_{rm} is the generator mechanical speed, m_s is the stator material, m_r is the rotor material, m_c is the generator conductor material, k_{pf} is the stator slot packing factor, n_{spc} is the number of strands per conductor, r_{rs} is the rotor shaft radius, $T_{d,j}$ is the maximum diode operating temperature, and v_t is the assumed rectifier diode forward voltage drop.

The Genetic Optimization System Engineering Toolbox (GOSET) [23] is used here to solve this optimization problem. The population size and the generation size are both set as 3000. The optimization yields a Pareto-optimal front (a set of designs characterizing the trade-off between, in this case, system mass and system loss). Each individual of the Pareto-optimal front represents a complete system design. Six studies are performed here to assess the advantage of GaN devices. They have the same system specifications. The six studies include a Si based system design with DyC, Si based system design without DyC, SiC based system design with DyC, SiC based system design without DyC, GaN based system design with DyC and GaN based system design without DyC. The studies without DyC are implemented here to demonstrate the effect of transient analysis to the system design, especially to the system's passive components design. The Pareto-optimal fronts are shown in Fig. 3. The optimization results show that the GaN-based system designs dominate the Si-based and SiC-based system designs. This advantage becomes more pronounced after the DyC are added. The switching frequency versus system mass is shown in Fig. 4. From this figure, it can be noticed that the system mass decreases as switching frequency increases and the GaN based system with DyC has the highest switching frequency which goes up to 200 kHz.

In Fig. 3, six designs are selected from six Pareto-optimal fronts, respectively. The system efficiency of each of the selected designs is close to 97.09% which is equivalent to a system loss of 300W. The design parameters of each design are listed in Table X. In Table X, M_C is the converter mass, P_C is the converter loss. From Table X, the GaN with DyC design converter mass is 92.5% of the SiC with DyC converter mass and 30.5% of the Si with DyC converter mass. The mass reduction is mainly due to the increase in switching frequency which results in a reduced size for the output inductor and output capacitor. The GaN with DyC design converter loss is 87.8% of the SiC with DyC design converter loss and 65.5% of the Si with DyC design converter loss. The loss reduction is due to the extremely low switching loss and relatively low conduction loss in the GaN diode. The loss reduction also contributes to the heat sink mass reduction.

The system mass stacked bar plot of the designs in Table X is shown in Fig. 5. Therein, from 0-4 kg is generator mass in all cases so it can be seen that the generator dominates the mass. Interestingly, WBG semiconductors yield a modest decrease in generator size, probably through their impact on converter loss. Recall that since these designs all have the same loss, reducing converter loss allows the machine loss to increase which translates to reduced machine size.

Unexpectedly, while in percentage terms the machine sizes were similar; the difference that did exist between the generators was a significant contributor to the difference between the total system masses.

Next, it can be seen that the mass of the input inductor is relatively stable across all designs, except in the case of the Si based design with DyC. This is most likely because of the constraint on the inductor current ripple. The input capacitor made an almost insignificant contribution to the total system masses in all cases.

In the output stage, the mass of the output inductor was similar for all WBG designs; though these were smaller than for the Si based designs. The output capacitor contributed little to total system mass for those designs w/o DyC; but did

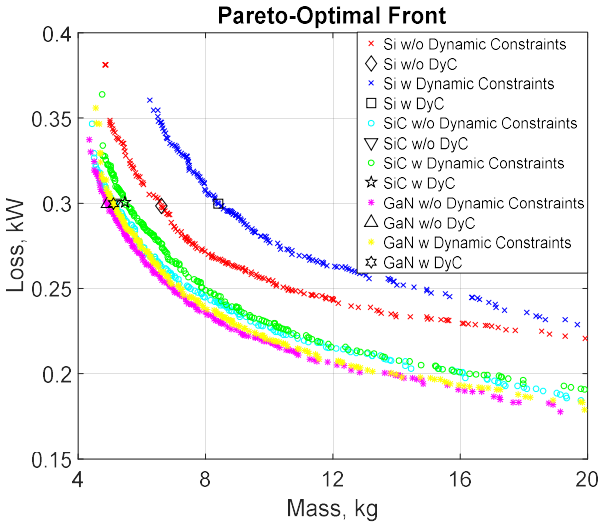

Fig. 3. Pareto-optimal fronts

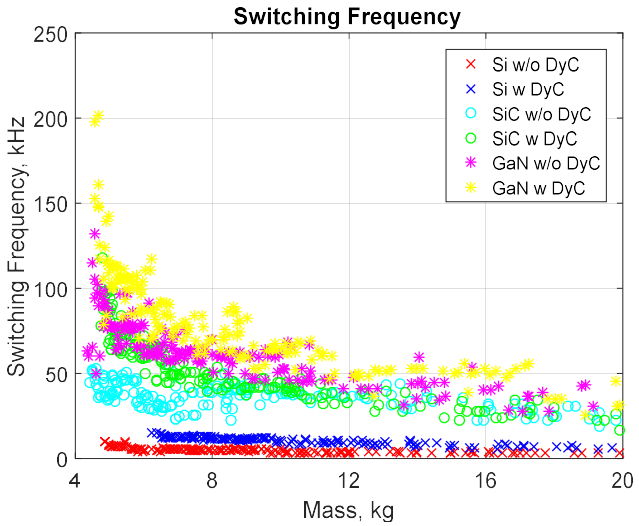

Fig. 4. Switching frequency versus system mass

TABLE X. EXAMPLE DESIGNS

Parameter	Si w/o DyC	Si w DyC	SiC w/o DyC	SiC w DyC	GaN w/o DyC	GaN w DyC
M(kg)	6.61	8.41	5.17	5.46	4.91	5.11
P(W)	299	300	299	301	300	300
M_C(kg)	1.24	2.57	0.514	0.848	0.600	0.784
P_C(W)	93.8	109	77.6	81.0	69.3	71.1
M_G(kg)	5.37	5.86	4.66	4.61	4.31	4.33
P_G(W)	205	191	221	220	232	229
P_o	6	6	7	7	7	7
r_{st}(cm)	8.65	8.47	8.21	8.74	8.91	8.30
d_{rb}(mm)	7.22	8.01	6.27	6.60	7.17	6.57
d_m(mm)	3.20	2.86	2.47	2.98	2.49	2.43
g(mm)	1.88	2.34	2.19	2.44	2.06	1.97
d_{tb}(mm)	11.0	11.5	13.6	10.6	11.5	12.2
α_t	0.455	0.477	0.470	0.477	0.487	0.488
d_{sb}(mm)	7.83	9.26	6.91	7.31	7.44	7.03
α_{pm}	0.737	0.775	0.791	0.743	0.792	0.783
$_r$(T)	0.858	1.30	1.19	1.26	1.13	1.16
l(cm)	4.57	4.67	4.06	4.16	3.53	3.91
N_{tl}	86.8	83.4	84.9	79.1	114	123
f_{sw}(kHz)	5.60	11.2	46.0	72.7	79.9	100
L_{in}(mH)	2.57	2.32	2.01	2.33	3.14	3.30
J_{Lin}(A/mm^2)	4.46	6.62	7.50	7.30	6.48	6.81
L_{out}(mH)	1.53	2.72	0.262	0.617	1.07	0.940
J_{Lout}(A/mm^2)	3.99	4.96	3.47	5.22	6.74	6.60
C_{in}(μF)	2.29	2.86	4.88	52.9	3.26	34.5
C_{out}(μF)	76.3	864	10.1	124	11.1	81.2

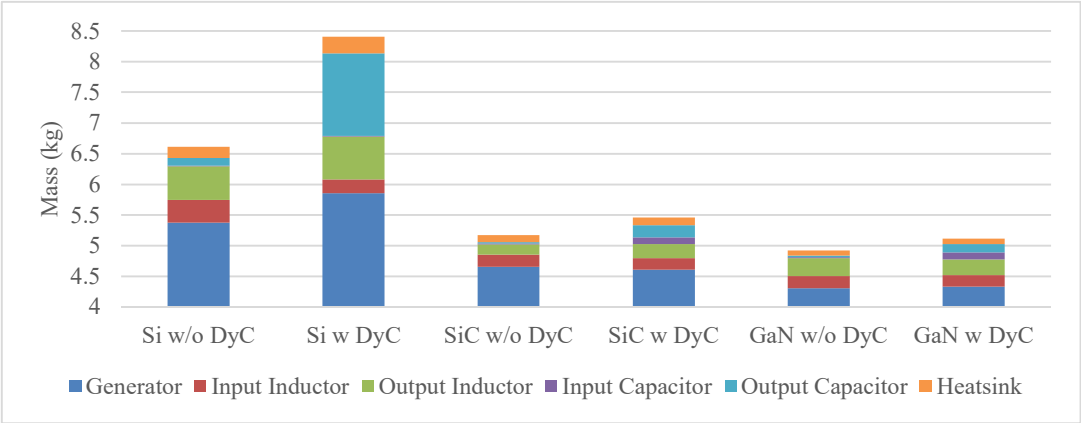

Fig. 5. System mass

contribute to the mass of those designs in which DyC were enforced.

It can also be seen that the heatsink mass reduced going from Si to SiC; it was further reduced in terms of going from SiC to GaN.

VI. CONCLUSIONS

This paper presents a predictive GaN loss model for computing the losses in a candidate vertical GaN MOSFET device. This paper also provides quantified predictions for converter performance using the candidate device in place of state-of-the-art Si and SiC devices. For a given system loss, the GaN based with DyC system mass is 93.6% of the SiC based with DyC system mass and 60.8% of the Si based with DyC system. This theoretical result indicates the value of GaN based power conversion system with regard to increasing power density and efficiency.

REFERENCES

[1] R. J. Kaplar, J. C. Neely, D. L. Huber and L. J. Rashkin, "Generation-After-Next Power Electronics: Ultrawide-bandgap devices, high-temperature packaging, and magnetic nanocomposite materials," in *IEEE Power Electronics Magazine*, vol. 4, no. 1, pp. 36-42, March 2017.

[2] J. W. Kolar et al., "PWM Converter Power Density Barriers," *2007 Power Conversion Conference* - Nagoya, Nagoya, 2007, pp. P-9-P-29.

[3] B. Zhang, S. Sudhoff, S. Pekarek and J. Neely, "Optimization of a Wide Bandgap Based Generation System," *2017 IEEE Electric Ship Technologies Symposium (ESTS)*, Arlinton, VA, 2017.

[4] G.M.Shane, (2012), Permanent magnet inductor design for reduced mass inductive components. (Doctoral Dissertation). Retrieved from ProQuest (3556646).

[5] N.Mohan, T.M.Undeland, and W.P.Robbins, *Power Electronics: Converters, Applications and Design,* 3rd ed. New York, NY, USA: Wiley, 2002.

[6] Micorsemi, Inc, "APT13GP120B Power MOS 7 IGBT Datasheet." Available: microsemi.com.

[7] Powerex Power Semiconductor Solutions. "CS241250 Datasheet." Availabel: pwrx.com

[8] Cree, Inc, "C2M0080120D Datasheet." Available: cree.com/power.

[9] Cree, Inc, "C4D20120A Datasheet." Available: cree.com/power.

[10] I. C. Kizilyalli, A. P. Edwards, O. Aktas, T. Prunty, and D. Bour, "Vertical Power p-n Diodes Based on Bulk GaN," *IEEE Transactions on Electron Devices,* vol. 62, no. 2, pp. 414-422, 2015.

[11] A. M. Armstrong *et al.*, "High voltage and high current density vertical GaN power diodes," *Electronics Letters,* vol. 52, no. 13, pp. 1170-1171, 2016.

[12] M. Sun, Y. Zhang, X. Gao and T. Palacios, "High-Performance GaN Vertical Fin power Transistors on Bulk GaN Substrates," I*EEE Electron Device Letters*, vol. 38, no. 4, pp. 509-512, April 2017.

[13] O. Tohru, U. Yukihisa, I. Tsutomu, and H. Kazuya, "Vertical GaN-based Trench Metal Oxide Semiconductor Field-effect Transistors on A Free-standing GaN Substrate with Blocking Voltage of 1.6kV," *Applied Physics Express*, vol. 7, no. 2, p. 021002, 2014.

[14] H. Tetsuro, N. Takuma, F. Akihiko, and Y. Mikio, "Vertical GaN Merged PiN Schottky Diode with A Breakdown Voltage of 2kV," *Applied Physics Express*, vol. 10, no. 6, p. 061003, 2017.

[15] Koehler, Andrew D., et al, "Vertical GaN Junction Barrier Schottky Diodes," *ECS Journal of Solid State Science and Technology* 6.1 (2017): Q10-Q12.0

[16] J. Flicker and R. Kaplar, "Design Optimization of GaN Vertical Power Diodes and Comparison to Si and SiC," in *Wide Bandgap Power Devices and Applications Conference* (WiPDA 2017), 2017.

[17] Cree, Inc, "CPW4-1200-S020B Datasheet." Available: cree.com/power.

[18] B. J. Baliga, *Fundamentals of power semiconductor devices*. Springer Science & Business Media, 2010.

[19] G. Greco, F. Iucolano, F. Roccaforte, "Ohmic contacts to Gallium Nitride materials," *Applied Surface Science*, vol. 383, 2016, pp. 324-345, ISSN 0169-4332.

[20] M. E. Coltrin and R. J. Kaplar, "Transport and breakdown analysis for improved figure-of-merit for AlGaN power devices," *Journal of Applied Physics,* vol. 121, no. 5, p. 055706, 2017.

[21] T. Kimoto and J. A. Cooper, *Fundamentals of Silicon Carbide Technology: Growth, Characterization, Devices and Applications*. John Wiley & Sons, 2014.

[22] J. L. Hudgins, G. S. Simin, E. Santi, and M. A. Khan, "An assessment of wide bandgap semiconductors for power devices," *IEEE Transactions on Power Electronics,* vol. 18, no. 3, pp. 907-914, 2003.

[23] Genetic Optimization System Engineering Tool (GOSET) For Use with MATLAB, Manual Version 2.6, School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN, with United States Naval Academy, Annapolis, MD, 2014. Available:https://engineering.purdue.edu/ECE/Research/Areas/PEDS/go_system_engineering_toolbox.