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MilliKelvin HEMT Amplifiers for Low Noise, High Bandwidth Measurement of Quantum Devices

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Abstract

We demonstrate ultra-low power cryogenic high electron mobility transistor (HEMT) amplifiers for measurement of quantum devices. The low power consumption (few uWs) allows the amplifier to be located near the device, at the coldest cryostat stage (typically less than 100 mK). Such placement minimizes parasitic capacitance and reduces the impact of environmental noise (e.g. triboelectric noise in cabling), allowing for improvements in measurement gain, bandwidth and noise. We use custom high electron mobility transistors (HEMTs) in GaAs/AlGaAs heterostructures. These HEMTs are known to have excellent performance specifically at mK temperatures, with electron mobilities that can exceed 10^6 cm^2/Vs, allowing for large gain with low power consumption. Low temperature measurements of custom HEMT amplifiers at T = 4 K show a current sensitivity of 50 pA at 1 MHz bandwidth for 5 mW power dissipation, which is an improvement upon performance of amplifiers using off-the-shelf HEMTs.

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1. INTRODUCTION

Solid-state quantum bits consisting of the spin of a single particle in a semiconductor, such as an electron on a donor or in a quantum dot, are seen as a promising path to extensible quantum computing. Measurement of the spin state in these devices involves resolving the tunneling of a single electron. The signals from these events are small and typically occur in a device located at the lowest temperature stage of a dilution refrigerator, at temperatures ~ 100 mK. Detection of these events with a large signal to noise ratio is important for high fidelity measurements of the state of the qubit and it is desirable to perform the readout rapidly. For single shot measurement of an electron tunnel event, the measurement must respond faster than the electron tunnel time.

We address this problem of rapid measurement of small signal events at mK temperatures by developing ultra-low power cryogenic amplifiers based on custom HEMTs fabricated at Sandia and Purdue. The low power consumption allows for placement of the amplifier near the qubit device, reducing parasitic capacitance and noise. We leverage Sandia and Purdue's unique capabilities in fabrication of ultra-high mobility channels in GaAs/AlGaAs heterostructures. HEMTs fabricated in these heterostructures are known to have excellent performance specifically at mK temperatures, with electron mobilities that can exceed 10^6 cm^2/Vs [1,2]. High mobilities should provide an advantage over commercial HEMTs in terms of gain at low power.

There are several approaches to cryogenic preamplification of signals from spin qubit devices. RF reflectometry requires optimization of a tank circuit, which can be challenging due to device parasitics [3]. Readout with excellent SNR was recently demonstrated using a Josephson parametric amplifier [4]. However, this approach requires embedding the device in a superconducting resonator, which may be problematic for operation in a magnetic field (as required for spin qubits). In a recent demonstration, a single off-the-shelf heterojunction bipolar transistor (HBT) was used to amplify the current through a quantum dot at low temperatures [5]. However, one limitation in this case was that the voltage drop across the quantum dot source-drain leads was not well-controlled. Further research on using HBTs for cryogenic preamplification is ongoing at Sandia. Using a commercial HEMT at an intermediate cryostat stage is bandwidth limited by cable capacitance [6], motivating placement of the HEMT circuit at the lowest cryostat stage. Initial results obtained at Sandia using commercial discrete HEMTs operated at the lowest cryostat stage showed promising, allowing a single shot readout bandwidth increase from ~10 kHz to ~100 kHz for a Si spin qubit [7]. The use of custom HEMTs and integrated circuits lead to further improvements in the measurement gain, bandwidth, and noise as compared to off-the-shelf discrete parts.

A final motivation for pursuing a HEMT based amplifier is straightforward compatibility with existing quantum dot fabrication processes, allowing for on-chip integration. Quantum dots made in Si/SiGe or GaAs/AlGaAs heterostructures are fundamentally HEMT device structures with additional in-plane confinement created by surface depletion gates [8,9].

2. DEVICE DESIGN

Our HEMTs are fabricated using Si modulation doped GaAs/AlGaAs heterostructures specifically designed to create electron channels for low temperature operation with extremely high mobilities (> 10^6 cm^2/Vs at temperatures below 4 K). Devices are fabricated using these heterostructures via standard semiconductor processing techniques.

2.1. Heterostructures

The starting material for the HEMT fabrication process is Si modulation doped GaAs/AlGaAs heterostructures grown via molecular beam epitaxy. The data shown are from devices fabricated using two different wafers. For both samples, the electron channel is formed at a single GaAs/AlGaAs heterojunction, as shown in Fig. 1a. Information about the channel depth and quality are shown in Table 1. The electron density and mobility are measured at a temperature of 0.3 K.

Table 1. Heterostructure Data

Wafer ID	Channel depth (nm)	Electron density (10^{11} cm^{-2})	Electron mobility (10^6 cm^2/Vs)
VA0171	100	1.6	2.9
5-21-15-1	57	2.5	3.3

2.2. HEMT Design

After growth, standard semiconductor processing techniques are used to create HEMT devices. First mesa regions are defined using photolithography and wet etch. Next, NiAuGe alloy areas are patterned to create Ohmic contacts to the channel. Finally, a metal gate is deposited over the channel region. We fabricated devices with gate lengths varying from 3 to 7 μm. A cross section and top down view of the final HEMT device is sketched in Fig. 1.

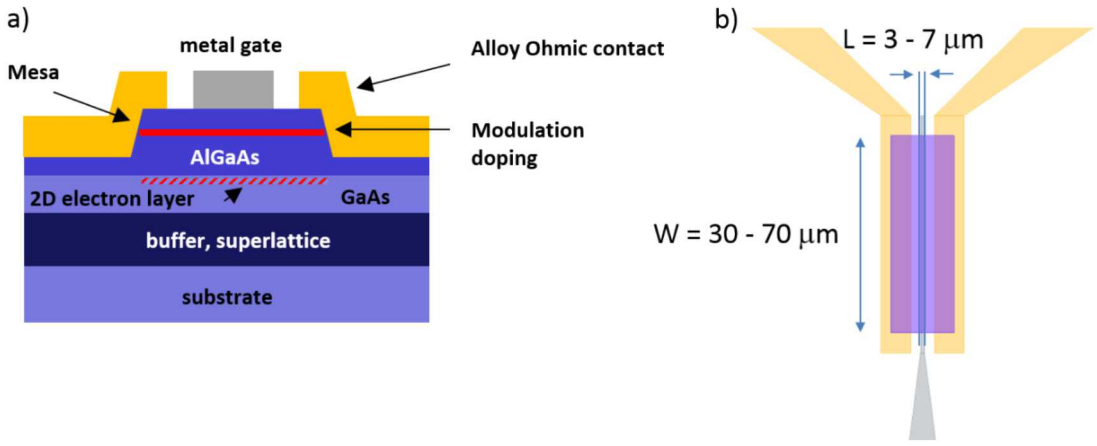

Figure 1. Modulation doped HEMT design. a) Cross-sectional view of modulation doped HEMT (not to scale), showing epitaxial layers and doping, mesa, Ohmic contacts and gate. b) Top down view of HEMT showing layout of mesa (purple), Ohmic contacts (gold), and gate (grey).

2.3. Integration

In the final devices, amplifiers are integrated with quantum dots on a single GaAs chip. Images of the quantum dot device are shown in Fig. 2. Figure 2a is an optical microscope image of the quantum dot device, showing an overview of the dot device design, including mesa, gates, and Ohmic contacts. Figure 2b shown a scanning electron microscope image of the nanoscale depletion gates used to define the quantum dot. The amplifier consists of a HEMT integrated on chip with resistors and capacitors. Resistors are fabricated using thin NiCr films, patterned into meander line structures using electron beam lithography. Capacitors are metal-insulator-metal structures with an alumina dielectric deposited via atomic layer deposition.

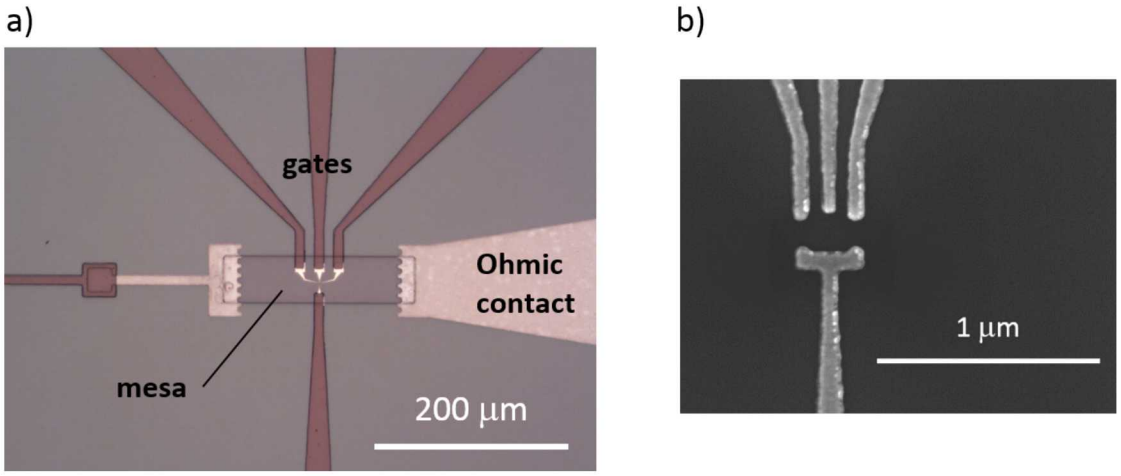

Figure 2. Quantum dot device layout. a) Optical microscope image of quantum dot device showing mesa region, Ohmic contacts, and gates. b) Scanning electron microscope image of nanoscale depletion gates used to define quantum dot.

3. CRYOGENIC DEVICE PERFORMANCE

Next we discuss low temperature transport measurements of individual HEMTs and performance of integrated HEMT amplifier devices.

3.1. HEMT Transport

Individual transistor performance was initially characterized via DC transport at T = 4 K. Results for two different devices from two different wafers are shown in Fig. 3. The two devices show overall similar transport behavior, with device current dropping rapidly from ~100 μA to zero in a gate voltage range of ~20 mV, for a source-drain voltage of 100 mV. Saturation of current versus source-drain voltage is also similar for the two devices, but can be seen most clearly in the individual traces shown in Fig. 3b.

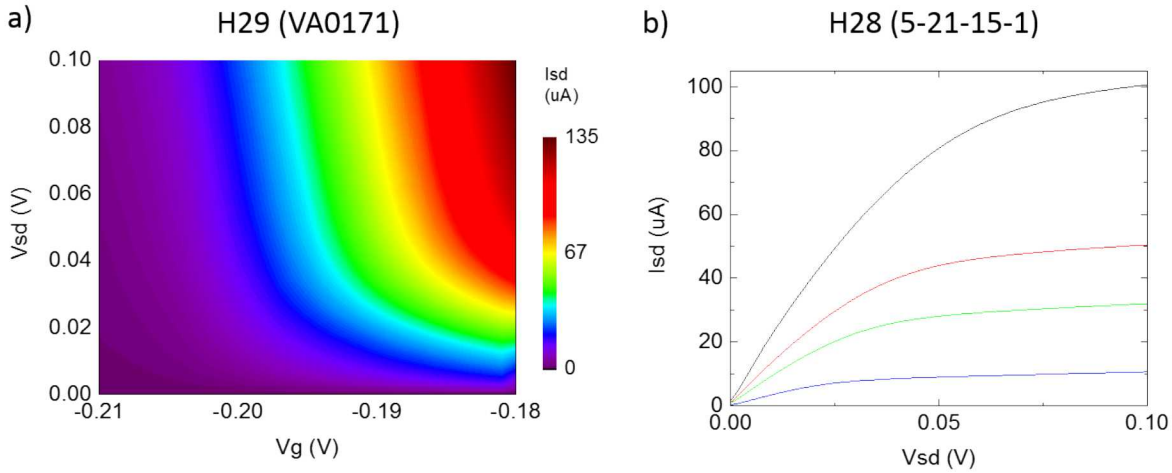

Figure 3. Electrical transport through HEMTs at T = 4 K. a) Transport for device H29 from wafer VA0171 showing source-drain current (Isd) vs. gate voltage (Vg) and source-drain voltage (Vsd). b) Transport for device H28 from wafer 5-21-15-1 showing individual Isd vs. Vsd curves for various gate voltages (Vg = -0.123, -0.134, -0.139, -0.147 V).

3.2. Gain, Bandwidth and Noise

Next we consider the performance of the entire amplifier circuit. A diagram of the complete circuit is shown in Fig. 4. The voltage across resistor R2, due to current through quantum dot, is ac coupled through capacitor C1 to the gate of the HEMT. The bias resistor R1 allows independent dc biasing of the HEMT gate. The HEMT drain current is sent to a room temperature bias tee and current preamplifier (Femto model HCA-10M-100k-C).

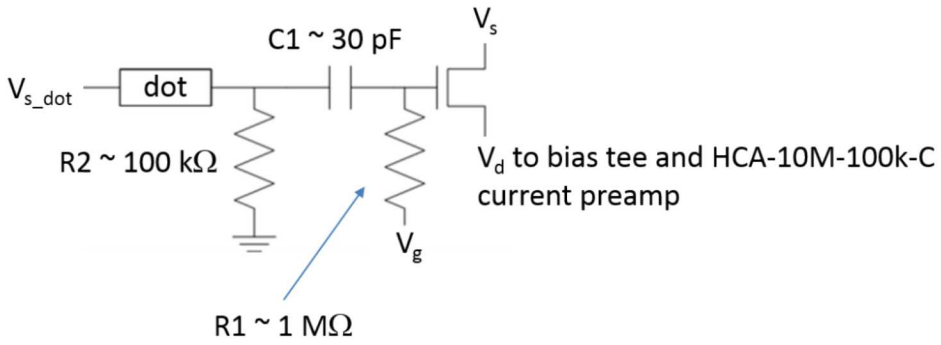

Figure 4. Amplifier and quantum dot circuit showing HEMT, resistors, capacitor, and quantum dot.

Figure 5 shows the current gain of the amplifier circuit at T = 4 K for two integrated devices (H28 and H29), with the quantum dot conductance tuned to a resistance of ~100 kΩ. Also shown for comparison is the gain of the same circuit implemented with the off-the-shelf transistor ATF-36163 (Broadcomm) and surface mount capacitors and resistors. For all three circuits, the source-drain voltage was set to 100 mV and the gate voltage was biased such that the source-drain current was 50 μW, (5 μW power dissipation). From the data of Fig. 5, it can be seen that the 3 dB bandwidth of the integrated parts (H28 and H29) is greater than that of the ATF-36163 circuit (~5 MHz, vs ~4 MHz). The gain of the custom parts is also greater than for the off-the-shelf part, ~300x vs. 230x.

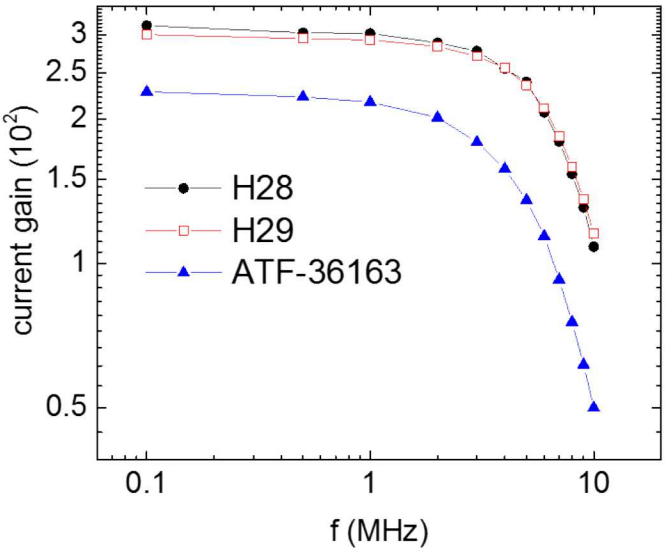

Figure 5. Current gain versus frequency at T = 4 K for HEMT amplifier devices H28 (wafer 5-21-15-1), H29 (VA0171), and same circuit using COTS HEMT ATF-36163 and surface mount resistor and capacitor

Figure 6 shows the current noise referred to input for the same HEMT circuits at T = 4 K at the same biasing conditions as described above for the gain and bandwidth tests. All devices show a current noise of ~43-45 fA/Hz$^{1/2}$ near 1 MHz. Much of this noise is likely Johnson noise (we estimate ~31-33 fA/Hz$^{1/2}$ for a dot conductance ~100 kΩ) and will likely decrease upon further cooling to dilution fridge temperatures. Device H29 appears to have a larger 1/f type noise. Presumably, this is due to the details of the heterostructure design and growth, which are known to play an important role in determining noise in mesoscopic devices at low temperature [10].

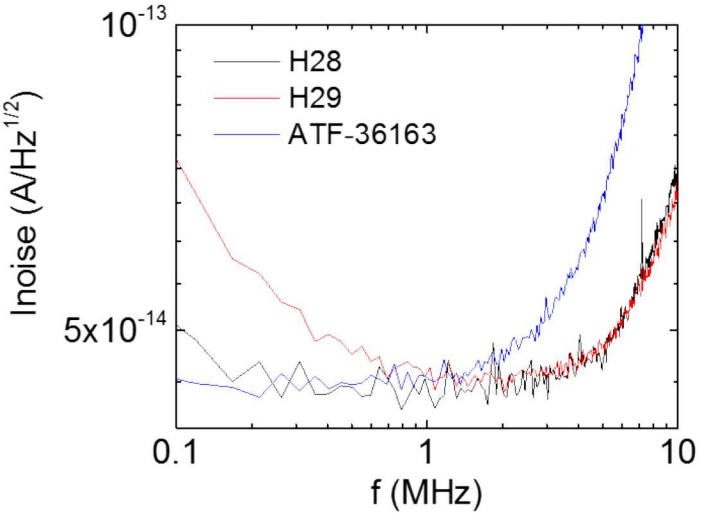

Figure 6. Noise versus frequency at T = 4 K for at T = 4 K for HEMT amplifier devices H28 (wafer 5-21-15-1), H29 (VA0171), and same circuit using COTS HEMT ATF-36163 and surface mount resistor and capacitor.

Figure 7 shows the gain and noise performance for the three devices versus power dissipation. For operation at milliKelvin temperatures, it is essential to have low power dissipation in order to avoid heating of the quantum dot. For devices where the transistor and quantum dot are not integrated on the same chip it is known that power levels of a few microwatts can be tolerated [7,11]. Although the gain continues to increase as the power consumption rises, at T = 4 K, the noise performance does not improve dramatically as the power is increased above 3 μW.

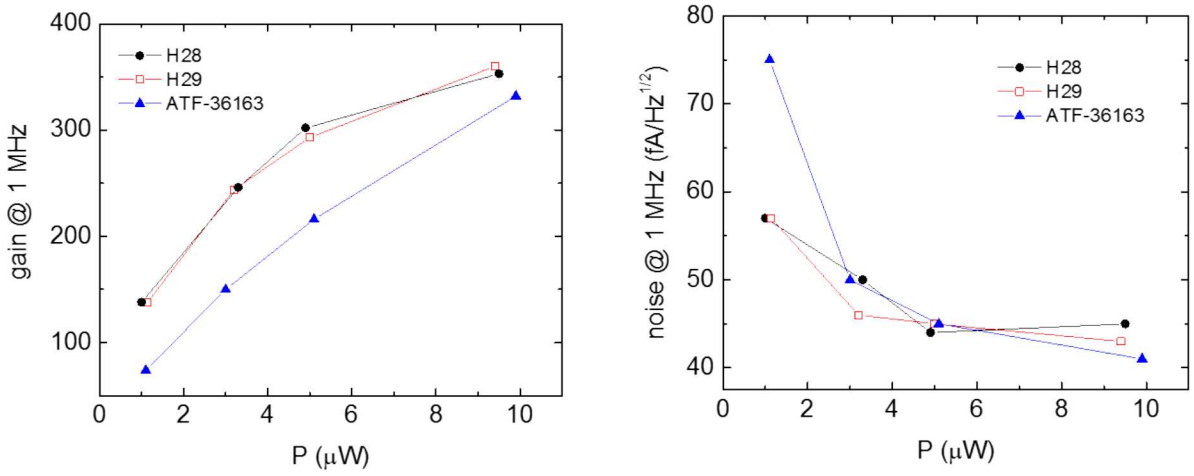

Figure 7. Gain and noise performance at 1 MHz versus power, T = 4 K, for HEMT amplifier devices H28 (wafer 5-21-15-1), H29 (VA0171), and same circuit using COTS HEMT ATF-36163 and surface mount resistor and capacitor.

3.3. Homodyne Detection

We next demonstrate how the amplifier circuit could be used for detection of an electron tunnel event using homodyne detection. A diagram of the measurement setup is shown in Fig. 8a. An ac voltage bias at 2 MHz is applied to the quantum dot source lead. After amplification by both the cryogenic preamp and room temperature current preamp, the signal is mixed down to dc, filtered down to a 1 MHz bandwidth, and digitized. To simulate a single electron tunnel event, we apply a 100 μs, 380 pA current pulse through the dot and digitize the amplified output, as shown in Fig. 8b. At this bandwidth, the noise is ~50 pA rms,

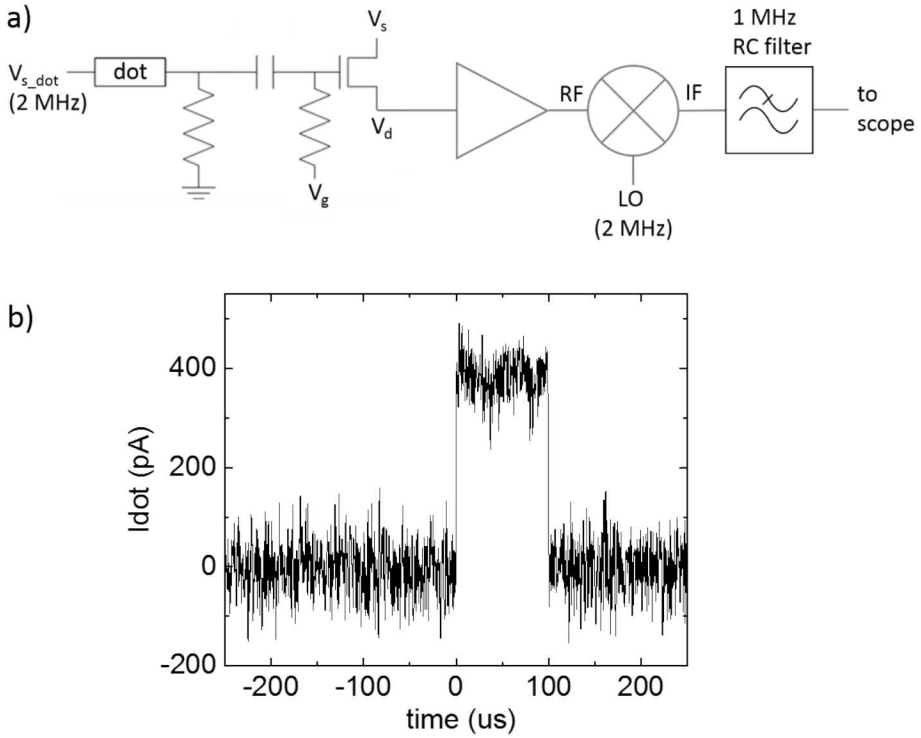

Figure 8. Homodyne detection of dot current pulse with HEMT circuit. a) Circuit diagram for homodyne detection. b) Detection of 100 μs, 380 pA dot current pulse using homodyne circuit.

4. SUMMARY

In conclusion, we have demonstrated a single HEMT cryogenic amplification circuit integrated on chip with a quantum dot device with ~5 MHz bandwidth. Initial tests at a temperature of 4 K show that for 1 – 10 μW power consumption, we achieve a current gain of ~140-360x and noise at 1 MHz of 43 – 57 fA/Hz$^{1/2}$. Using homodyne detection we demonstrate a current sensitivity of ~50 pA rms for a 1 MHz bandwidth. For future work, it would be of interest to characterize these devices at lower temperatures (sub Kelvin) to determine the ultimate noise performance when Johnson noise is reduced, and whether operation of the on-chip HEMT leads to heating of the quantum dot device.

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