SAND2017-9661C

Failure Analysis and Process Verification of High Density Copper ICs Used in Multi-Chip Modules (MCM)

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Abstract

Manufacturing of integrated circuits (ICs) using a split foundry process expands design space in IC fabrication by employing unique capabilities of multiple foundries and provides added security for IC designers [1]. Defect localization and root cause analysis is critical to failure identification and implementation of corrective actions. In addition to split-foundry fabrication, the device addressed in this publication is comprised of 8 metal layers, aluminum test pads, and tungsten thru-silicon vias (TSVs) making the circuit area > 68% metal. This manuscript addresses the failure analysis efforts involved in root cause analysis, failure analysis findings, and the corrective actions implemented to eliminate these failure mechanisms from occurring in future product.

Introduction

High density copper ICs manufactured using a split-foundry process offer challenges for front or back side failure analysis. Efforts to localize defects in an 8 to 10-layer IC with TSVs and test pads become more difficult the higher the metal density. When defects are present in the middle of the stack, they become obscured by metallization and difficult to localize.

The fabrication flow of the IC discussed in this publication has foundry 1 responsible for the Front End of Line (FEOL) processes. This includes the device layer, metal layers 1-4 (M1-M4) and a protective capping layer. Foundry 2 is responsible for the Back End of Line (BEOL) processes. This includes TSVs for 3D integration, metal layers 5-8 (M5-M8) and pads. Both foundries use a dual damascene process for deposition of copper metal lines and vias [2]. A tantalum liner is deposited prior to copper deposition to prevent copper diffusion into the dielectric and device layer. Excess copper is removed via Chemical Mechanical Polishing (CMP) to leave a smooth, planarized surface for further processing. As shown Fig. 1, a Secondary Electron Microscope (SEM) image of a Focused Ion Beam (FIB) cross-section shows all 8 metal layers, top level passivation, and a TSV for 3D integration.

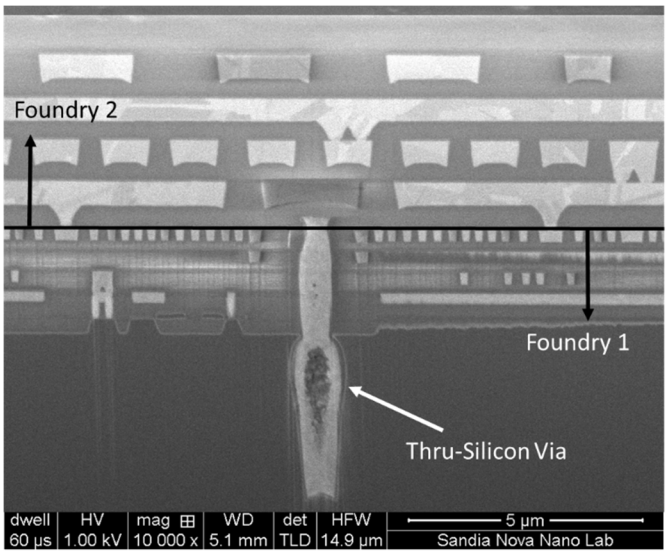

Fig. 1. FIB cross-section showing the boundary between the two foundries' processing.

In addition to the high metal density, numerous test pads and their unique orientation make electrical testing and manual probing very challenging. A single die contains 6016 test pads. Each die consists of 32 tiles in a 4 x 8 array. Each tile contains 188 test pads with each pad tested to assess functionality. An optical image of the die is shown in Fig. 2. A high magnification image of an individual tile is shown in Fig. 3. Excluding the fiducial located in tile 1 (iron cross in the upper left corner shown in Fig. 2), each tile layout is identical.

Initial electrical testing identified open and short failures resulting in 0% yield. Many dice contained both failure mechanisms. Non-destructive FA techniques such as thermal imaging [3] and lock-in thermography [4] were used with limited success. Optical beam-based techniques such as Thermally-Induced Voltage Alteration (TIVA) [5] and Optical Beam Induced Resistive Change (OBIRCH) [6] did not identify defects when used with low laser power and low drive current.

Fig. 2. Optical image of a fully processed die consisting of 32 tiles in a 4x8 array. Tile 1 is located in the upper left corner, tile 32 is located in the bottom right corner.

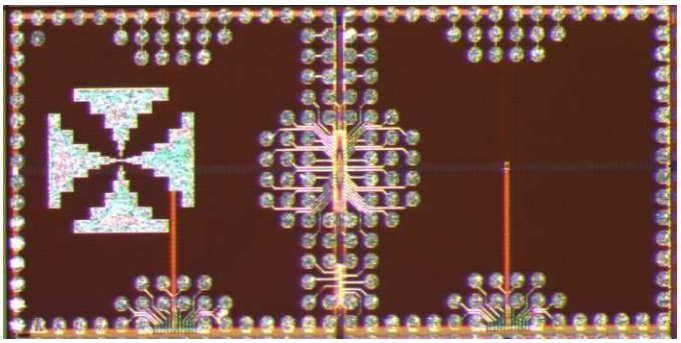

Fig. 3. Optical image of tile 1 with metal pads for testing.

Electrical Testing

Fully fabricated wafers were shipped to Sandia for electrical testing using automated test equipment (ATE). These wafer level tests were performed on individual dice with an ATE interfaced to a prober. A probe card using foundry compatible materials was designed and fabricated to our specifications. This allowed the wafers to be re-introduced into the foundry after testing for 3D hybridization. In testing, a quiescent power supply is used to monitor the device current (μA) and ensure in-specification conditions. The quiescent current test sets a maximum voltage on the power supply pin [7]. A pre-condition pattern is applied to the input pins to supply power and ensure the device is in a steady-state mode. Failure occurs if; a) the measured current is greater than the specified current for that pin or b) measured current is equivalent to an open circuit.

Every die on every wafer failed in either an open condition a short condition or both. Short circuit failures measured significantly more quiescent current than specified. Control wafers were used to validate the test set up and test program. We determined the wafers contained defects causing the open and short circuit failures. These failures were determined by setting all the input pins and power supplies to zero while monitoring the current. The voltage on one power supply was slowly elevated in 0.1V increments while keeping the other power supplies at 0V. For shorting failures, the observed current caused the power supply to reach compliance well before its operational voltage range. For open failures, the observed current was well below specification when the power supply reached its designated voltage output.

After identifying the failures were not attributed to test, two wafers were provided for failure analysis. Select test pads were manually probed. Open and short failures identified from ATE testing were verified from manual probing. Dice located in the center of the wafer contained open failures. Dice located on the perimeter of the wafer contained short failures. Dice located in between contained both open and short failures. After failure validation was performed, efforts identifying the root cause of failure resulting in 0% yield were initiated.

Open Circuit Failure Identification

Each die contains several common V_{dd}, Gnd, and signal pads. These functions are interconnected within a tile and between tiles. In the center of the wafer, common power and ground pins failed open. Time Domain Reflectometry (TDR) was used to determine the relative distance of the open failure from the test point. In this test, TDR contacts were placed on a calibration standard to establish a continuity baseline. The TDR probes were raised off the calibration standard to obtain and open state at the probes. Six test pads with known open failures were tested. A fast rise time was observed on these six test pads indicating an open circuit failure. Using a velocity factor of 0.4 [8], the distance from the test pad to the open failure measured approximately 1.5 mm. These results were presented to the design engineers where circuits of interest matching that distance from the test pads were identified and selected for guided FIB cross-sectional analysis. As shown in Fig. 4, numerous metal-via issues were observed in M5/M6 and M6/M7 interconnect sites. These vias were identified as being partially or completely open. EDS analysis of M5/M6 and M6/M7 vias shown in Fig. 5 revealed a tantalum liner conforming to the partial and incomplete via profile. This indicates the partial and incomplete via issues occurred prior to tantalum liner deposition. Identification of partial and completely open vias from guided FIB cross-sectioning showed the via/metal defects are present in significant quantity. These findings were sufficient for the manufacturer to move forward with corrective actions and did not warrant further investigation. Possible causes for this failure include; residual and/or marginal resist fill during trench patterning, damage to the SiN or top of the previous copper layer, or SiN punch-thru causing copper oxidation.

Root cause analysis was performed at the manufacturer's facility. A design of experiments (DOE) consisting of multiple short loop processed wafers focused on M5/M6 etch and cleaning processes. These processes are used for M6/M7 and

M7/M8 via/metal interfaces. Results from these short loop experiments showed SiN was fully and partially removed after a post-etch high temperature ash process. As shown in Fig. 6, bright contrast spots at the bottom of the vias indicate the SiN etch-stop layer is intact. Vias with bright and dark contrast show partially intact SiN. Vias with dark contrast show SiN has been completely removed. In vias missing SiN, crystalline features are observed at the bottom of every. These results are shown in Fig. 6b. Cross-sectional analysis of an open via verified the SEM results and is shown in Fig. 7. The crystalline features were identified as copper oxide occurring at the via/metal interface. SiN punch-thru exposed the underlying copper layer to a high temperature ash process resulting in oxidation of the copper at the damage site. This copper oxide prevented the tantalum liner from contacting the underlying copper layer.

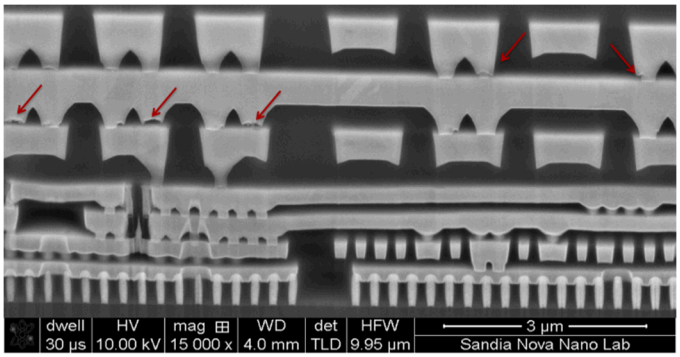

Fig. 4. FIB cross-sectional analysis revealed partial and incomplete vias between M5/M6, and M6/M7.

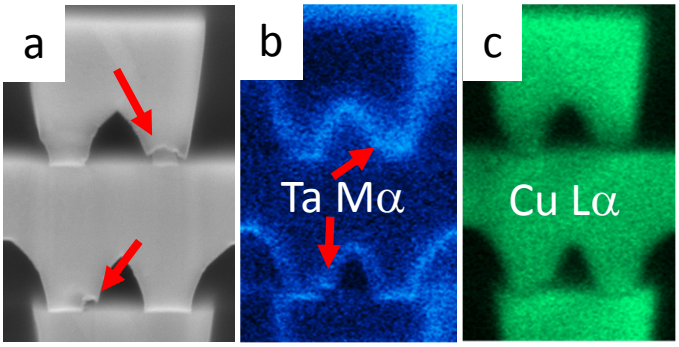

Fig. 5. a) SEM image of M5/M6 and M6/M7 vias. EDS maps of b) Tantalum liner Mα x-ray and, c) Copper La x-ray.

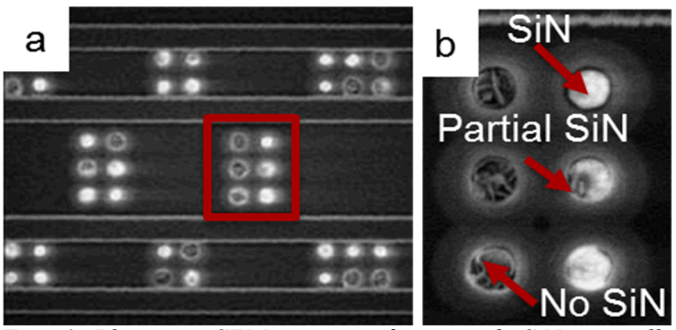

Fig. 6. Plan-view SEM images of vias with SiN, partially missing SiN and no SiN a) low mag., and b) high mag after high temperature ash processing.

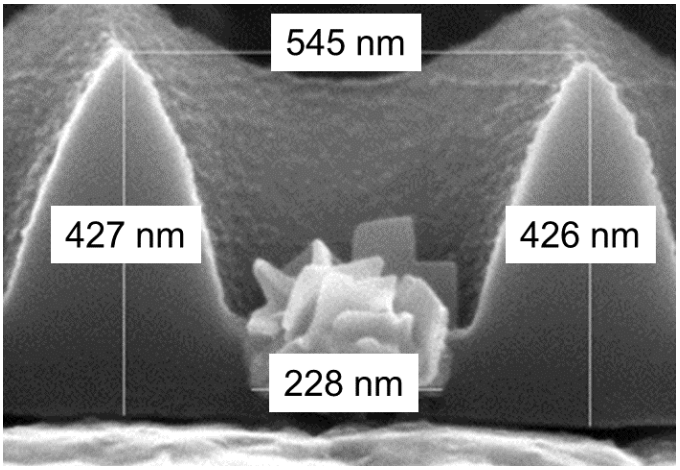

Fig. 7. FIB cross-section showing recrystallized copper oxide (CuO) at the bottom of a via.

Based on initial FA results and short loop findings, corrective actions were developed and implemented to prevent open failures. By increasing the thickness of the SiN layer, damage and/or punch-thru failures resulting in copper oxidation were eliminated. These results are shown in Fig. 8. In addition to the SiN layer corrective action, the via-metal dual damascene stack and etch processes were modified to improve sidewall conformity. A two-stage oxide etch process was implemented to selectively land on the SiN. This corrective action enables better, high-temperature ash processes for photoresist removal to be used. A mid-layer SiN etch stop was also implemented to prevent the vias from flaring. Newly fabricated vias have much less side wall tapering and no CuO build-up indicating the corrective actions resolved the root cause of open via failures.

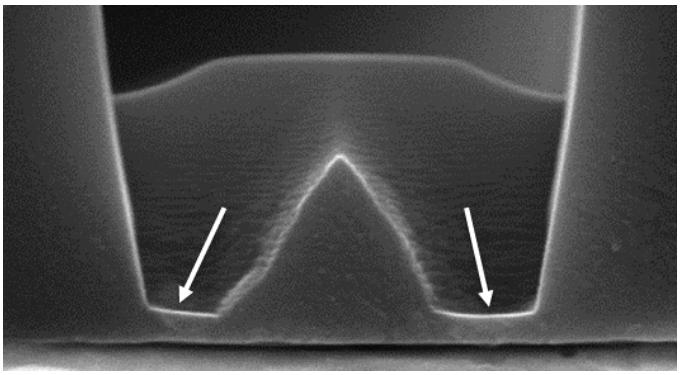

Fig. 8. FIB cross-section of a via post thicker SiN deposition. No copper oxidation is observed.

Short Circuit Failure Identification

Failure analysis of perimeter dice revealed multiple shorting failures between power, ground and various signal lines. Each tile is interconnected. A short on one tile would be electrically identified on every tile in that die. Manual probing of 20+ pads on multiple tiles confirmed the initial ATE results and identified the shorting failures were interconnected. Power, ground and other signal lines were shorted with resistances of $\leq 6\Omega$.

FA techniques such as thermal imaging, lock-in thermography and optical beam based methods revealed regions of interest but did not localize a defect site. Thermal imaging and lock-in thermography were performed on several shorted dice, each revealing a different region of interest. This result was critical during the early stages of FA as it eliminated a systemic design issue as the root cause.

The high copper density of this die effectively acted as a heat sink, dispersing much of the thermal signature during lock-in thermography. Initial lock-in thermal analyses taken at 100 mV and 30 mA showed significant heating across a very large area in the die. This sample was probed between power and ground on two separate tiles. A large thermal bloom spanning 3 tiles (6 mm) is shown in Fig. 9. The hottest spot (noted by the arrow in Fig. 9) was selected for cross-sectional analysis. Results (not shown) did not reveal any defects or shorted lines. Thermal images were taken on several failed dice using the same probe configuration. In each instance, the thermal signatures varied die to die with hot spots in different locations.

Efforts to perform backside lock-in thermography at wafer level produced similar results. Thermal blooms like those from the front side were observed. Backside thermal images helped narrow the location of the defect but did not contain any fiducials for alignment. Manual alignment of a back-side thermal image with a top side image revealed an area ~ 2 mm^2 spanning two tiles (*Fig. 10*).

Other shorting failed dice were selected and examined using optical beam based fault localization techniques. To expedite analysis, several dice were removed from the wafer, packaged and wire bonded for front and backside analysis. In parallel, other dice were probed from the front side only. Dice containing hard shorts (< 6Ω) were selected for investigation. Dice prepared for front and backside analysis were thinned to 100 µm then packaged and wire bonded.

Initial TIVA analysis of both packaged and free standing dice was performed using a 1340 nm laser at 5–10 mW power, and a device stimulus of 0–1 mA. These parameter ranges are typical for most CMOS product FA. Front and back side analyses using these parameters did not localize the defect. Under these conditions, the high metal density with test pads and tungsten TSVs strongly shielded the laser from heating and/or stimulating any defects. These results were consistent when examined from the front or back side. During electrical testing and thermal imaging, the failures appeared stable up to 50 mA. To improve our chances of stimulating and detecting defects, the laser power was increased from 5 mW to 50 mW at low magnification and 1 mA to 50 mA. These are atypical laser power and device stimulus conditions elevating the risk of compromising the failure mechanism. Under these conditions, we were successful in localizing defect sites from both the front or backside without impacting the failure mechanism.

Investigation of a failing die probing power to ground using 50 mA drive current and 50 mW laser power revealed a TIVA signal located in tile 22. Three different power/ground pads were probed in 3 separate tiles. Each time, the TIVA signal from each test occurred in the same location. This TIVA site is observed in tile 9 is shown in Fig. 11. Multiple signals were shorted to power and ground. Probing revealed TIVA sites in tile 9, same location. This failure has compromised multiple copper lines. High magnification of the power to ground short using elevated laser power and device stimulus revealed a TIVA signal near a bank of test pads (Fig. 12).

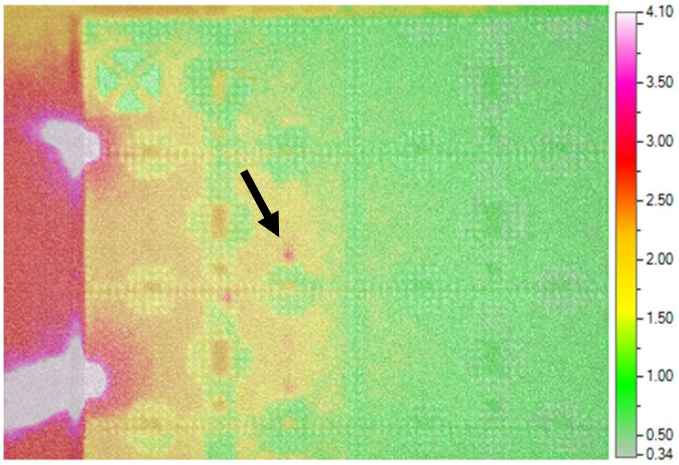

Fig. 9. Lock-in thermal image of a power/ground short taken at 100 mV and 30 mA.

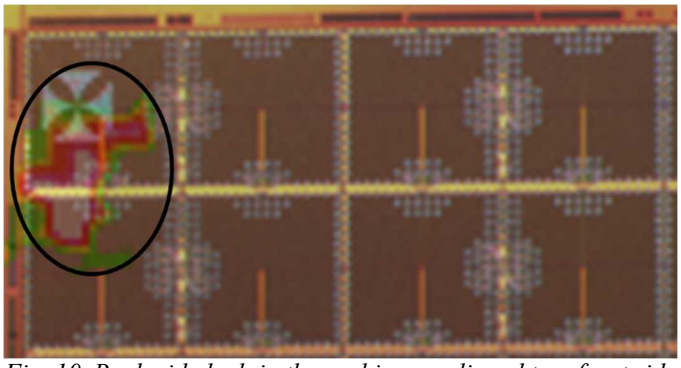

Fig. 10. Back-side lock-in thermal image aligned to a front side optical image shows a region of interest spanning 2 tiles.

FIB cross-sectional analysis performed at the TIVA site is shown in Fig. 12. Initial findings revealed thickness variations in M5, dielectric cracking, and cavities in the inter level dielectric (ILD). Fig. 13a shows thinning at M5 (circle) at the beginning of the TIVA signal. Comparing this region to the design reveals M5 should have extended to the end of the metal line with the fabricated M5 thickness of ~ 600 nm. In addition, the FIB cross-section shows M5 thickness variation of 90 nm or 15% of the nominal M5 thickness. In Fig. 13b, a cross-section taken 3 µm further into the sample (from 13a) shows a copper globule forming at M5. In addition to the copper globule, the dielectric above M4 appears to be missing allowing this defect to bridges multiple M4 lines. Other defects include lateral M5 bridging, copper pooling causing M6 bridging and in one instance, shorting to a TSV. These findings explain why under multiple shorts across multiple signal lines were observed in the same area.

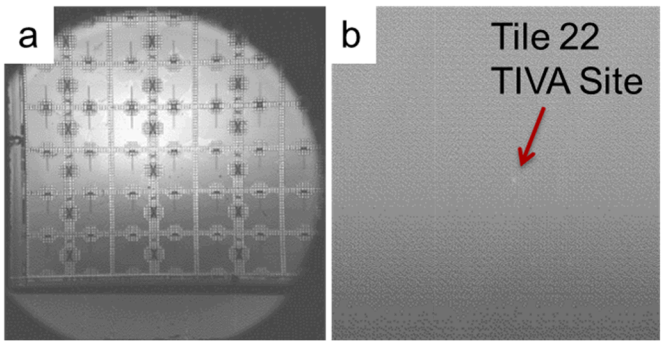

Fig. 11. a) reflected light image of a failed device, b) a TIVA site located in tile 22, ~ 6 mm from the stimulus site.

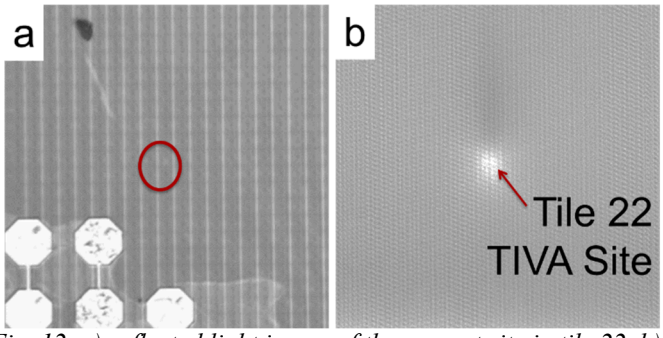

Fig. 12. a) reflected light image of the suspect site in tile 22, b) TIVA image located ~ 240 µm north of a test pad.

In addition to the dense metallization, the large copper globule (10 µm – 20 µm) acted as another heat sink requiring more laser power and drive current to stimulate the defect. The root cause of this failure was attributed to a backside wafer roughening step. Two issues contributing to this failure are: a) back-side roughening process adding particles to the device surface, and b) damage to the capping layer introduced by particles or use of a vacuum chuck. After foundry 1 completes M4 processing, a 35 nm SiN protective cap is blanket deposited on the wafer prior to shipping. Upon receipt at foundry 2, the wafers were cleaned and placed device side down on a vacuum chuck for backside roughening. The placement of wafers device side down damaged the SiN film resulting in exposure of M4. Particle contamination introduced from back side roughening further exasperated this problem. To address this issue, foundry 1 modified their protective stack (35nm SiN) to 70nm SiN/300nm SiO2/100nm SiN. Foundry 2 removed the vacuum chuck in favor of a perimeter contact holder for backside roughening. Implementing these corrective actions reduced the number of particles and defects.

TIVA analysis of another die using elevated drive current and laser power revealed two TIVA signals located in tiles 3 and 11. These two TIVA signals shown in Fig. 14 were observed when power and ground were probed in tiles 15 and 26 respectively. Other signal pads probed to ground produced one TIVA signal at the same location as the power/ground signal produced in tile 11. These individual TIVA signals are shown in Fig. 15. The TIVA signal in 15b only occurs during power/ground probing. The TIVA signal in tile 11 (15b) appears stronger in the upper left portion of the test pad. FIB cross-sectional analysis of the TIVA site in tile 11 (15d) revealed a similar copper globule as the failure mechanism. Here, the copper globule occurred in M7 and extended upwards bridging multiple M7 and M8 lines. In addition, the copper globule caused several M8 lines to fail open. These features are shown in Fig. 16.

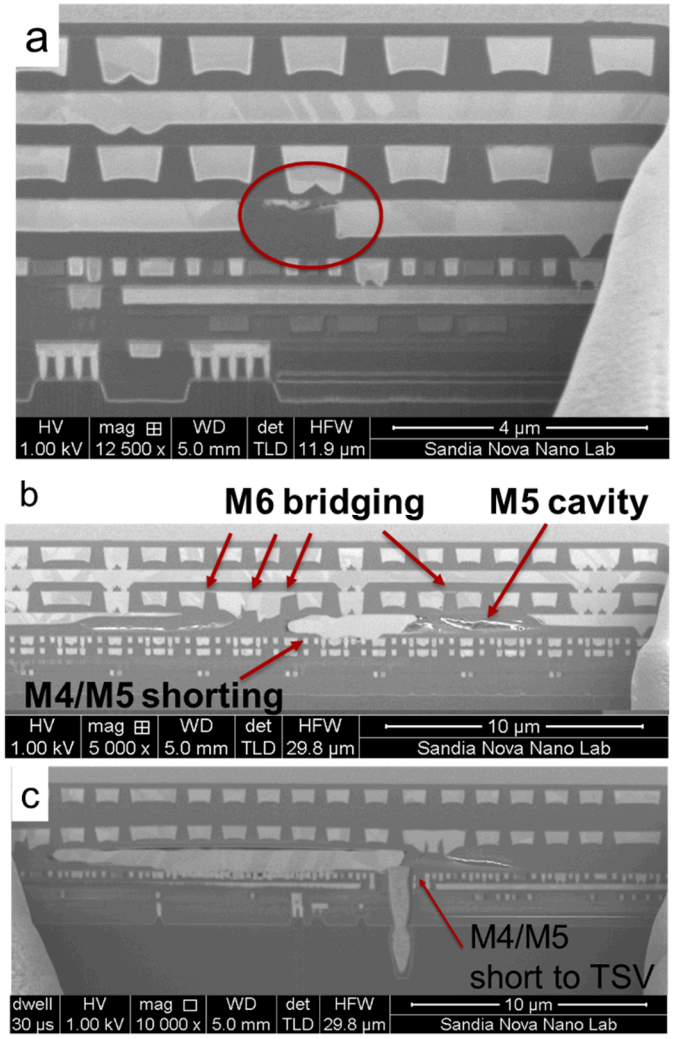

Fig. 13. FIB cross-sections a) near the beginning of the TIVA signal reveals thickness variations and damage in M5, b) 3 µm further into the sample shows an M5 copper globule bridging M4, M5 and M6 traces, and c) M4/M5 short to a TSV.

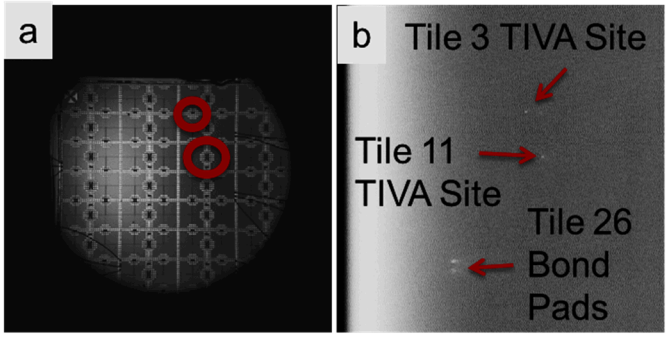

Fig. 14. a) reflected light image with circles indicating tiles where TIVA signals were observed, b) TIVA signals in tiles 3 and 11 after testing power/ground in tile 26.

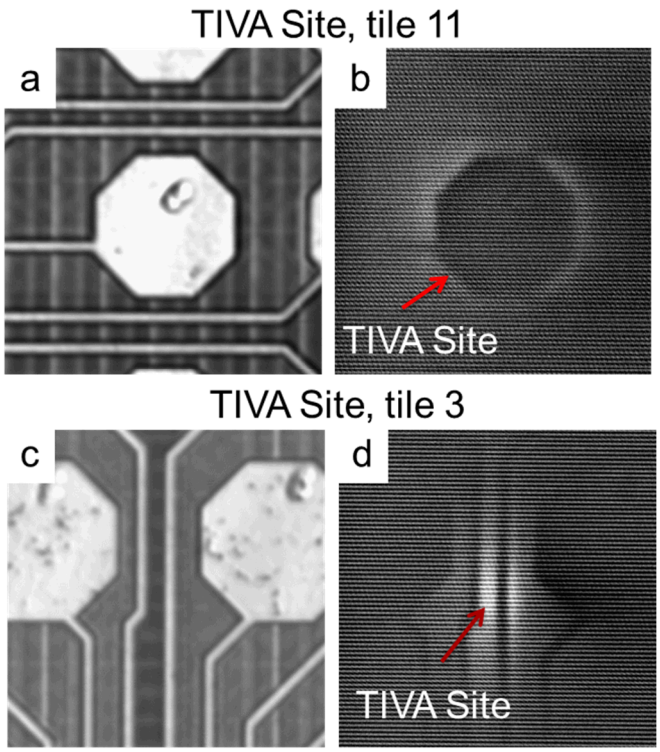

Fig. 15. TIVA signals observed during power to ground probing in tile 26 show a) reflected light image and b) TIVA image directly underneath a test pad in tile 11 and c) reflected light image and d) TIVA image between 2 pads in tile 3.

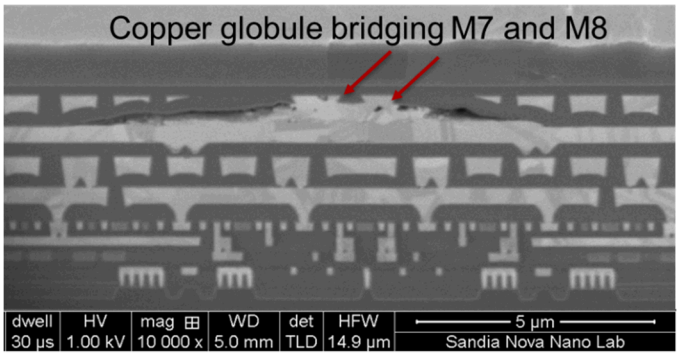

Fig. 16. FIB cross-section of a copper globule bridging adjacent M7 and M8 lines.

The TIVA signal observed in tile 3 (15d) was FIB cross-sectioned. Initial analysis revealed two hollow M4 lines but no shorting defect as shown in Fig. 17. Chemical analysis of the interior of these lines revealed the tantalum liner is intact but the line completely lacking copper. As the cross-section progressed closer to the TIVA site, one hollow trace ended while the shape of the other hollow trace changed. Fig. 18 shows a collapsed trace resulting in deformation of the upper level ILD. This deformation caused a dip in the ILD creating an uneven surface. Subsequent copper deposition resulted in a low point causing a thickness variation of ~ 200 nm in M5 above the collapsed M4 line. During CMP processing, the excess copper was not cleared resulting in a pool of copper bridging two M5 lines. This defect is shown in Fig. 19 where three cross-sections taken at the end of one M5 line (a), in the ILD (b) and at the beginning of the next M5 line show the copper above the collapsed M4 trace bridging both M5 lines resulting in a small, localized power/ground short.

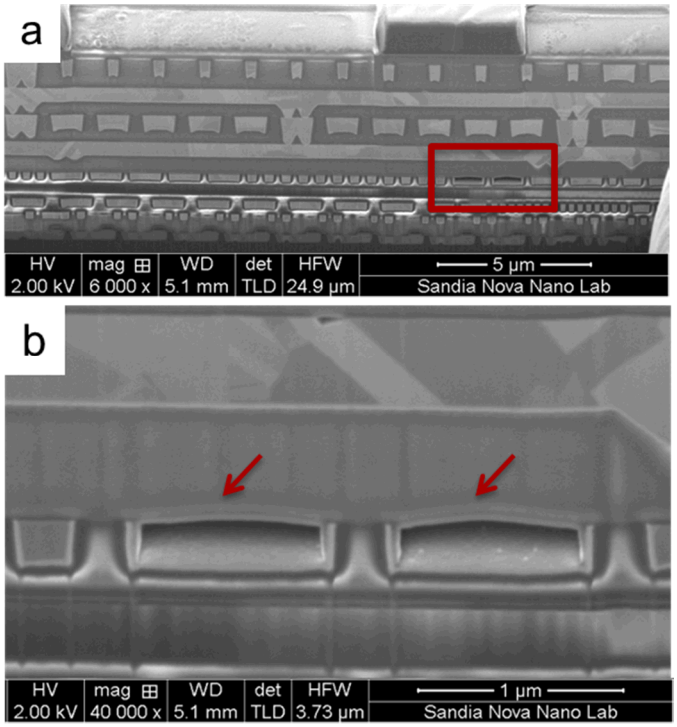

Fig. 17. FIB cross-section revealed a) two hollow M4 traces, b) higher magnification showing a convex structure.

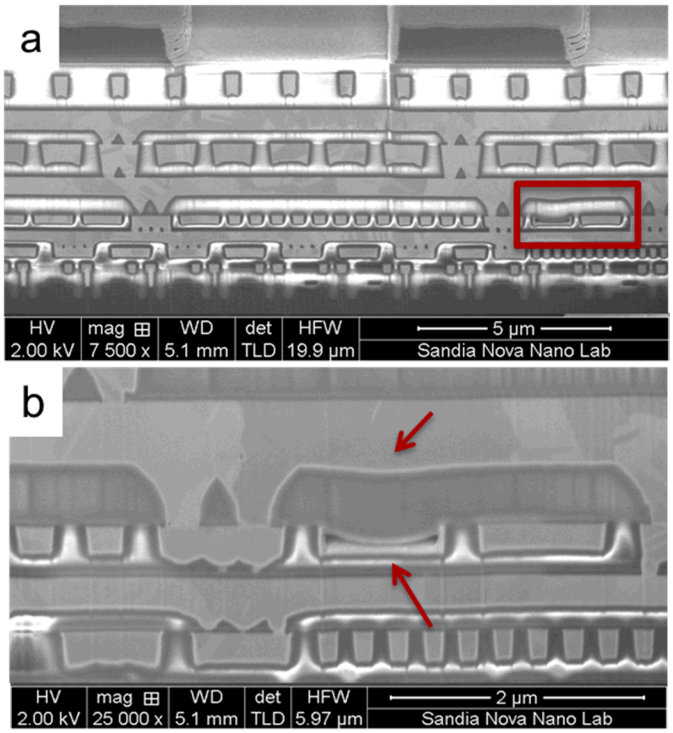

Fig. 18. FIB cross-section further showed a) hollow M4 trace with concave structure, b) higher magnification showed concave structure and the effect on the upper level ILD.

We believe the copper in M4 was removed due to pin holes and damage in the SiN. Aggressive cleans attacked M4 and etched the copper. Subsequent rinse and cleaning processes removed the copper leaving the tantalum liner intact. When the hollow trace collapsed creating an undulation in the ILD, copper was pooled creating a thicker region above the hollow M4 line. This copper was not removed during CMP resulting in a puddle bridging adjacent M5 lines. Similar corrective actions were taken to address the SiN film and protect the underlying copper layers.

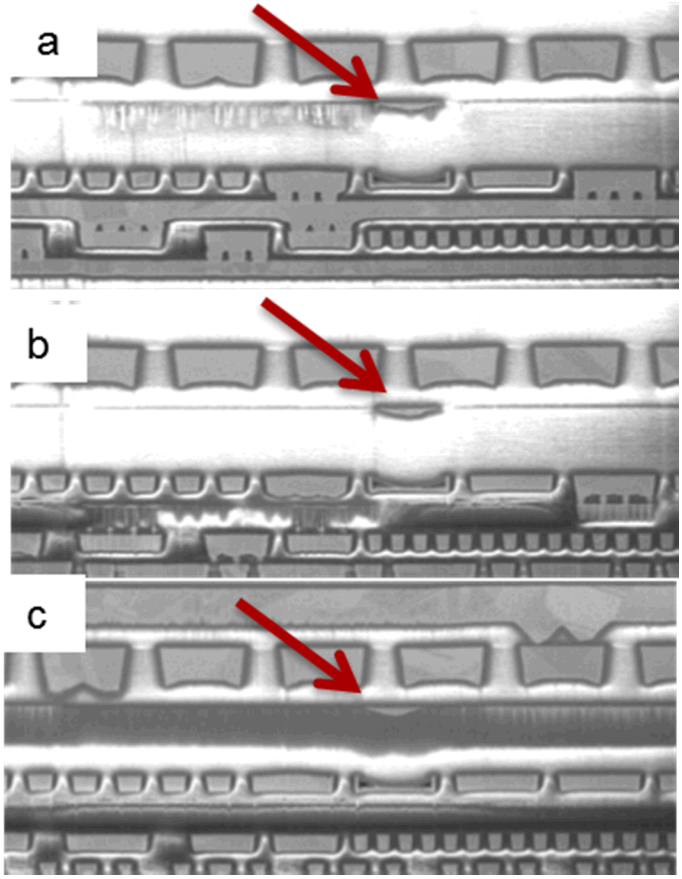

Fig. 19. FIB cross-sections showed a) concave M4 trace with M5 ending, b) ILD with a small copper film present after CMP, c) the small copper film contacting an adjacent M5 trace resulting in a power/ground short.

Conclusions

Several processing deficiencies resulting in open and short circuits were examined, analyzed and resolved. Corrective actions have been developed and implemented to reduce the occurrence of these failures. Corrective actions implemented to address the open via failures proved beneficial, eliminating the formation of copper oxide, improving the via sidewall profile and eliminating open via failures. Efforts addressing the short circuit failures are in progress. Short-loop experiments modifying wafer cleaning, rinsing and CMP processes have shown promise and are being incorporated into the process flow. In addition to the short circuit corrective actions, defect screening and inspection steps have been incorporated into the process. These steps will help identify any contamination or defects after key processes and to evaluate the corrective actions implemented.

Acknowledgments

The authors would like to thank the wafer processing technology staff at Novati for their efforts, Darlene Udoni and David Cordova for probing and wafer level testing, Kathy Myers, Ken Mcguire and Kira Fishgrab for wafer dicing, packaging and wire bonding, and Alex Pimentel for FIB analysis. Sandia National Laboratories is a multimission laboratory managed and operated by National Technology and Engineering Solutions of Sandia, LLC., a wholly owned subsidiary of Honeywell International, Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525.

References

[1] Intelligence Advanced Research Projects Activity (IARPA). Trusted Integrated Circuits Program, https://www.iarpa.gov/index.php/researchprograms/tic/baa

[2] C. K. hu and J.M. E. Harper, "Copper Interconnections and Reliability," Mater. Chem. Phys., vol. 52, pp. 5-16, 1998

[3] Tessier, G., M. Bardoux, C. Boue, C. Filloy, and D. Fournier. "Back side thermal imaging of integrated circuits at high spatial resolution." *Applied physics letters* 90, no. 17 (2007): 171112.

[4] O. Breitenstein, J.P. Rakontoniaina, F. Altmann, J. Schulz, G. Linse, "Fault localization and Functional testing of ICs by lock-In Thermography", *Proceedings of the 28th International Symposium for Testing and Failure Analysis (ISTFA)*, pp. 29 – 38, ASM International, 2002.

[5] Cole, EI Jr, Paiboon Tangyunyong, and Daniel L. Barton. "Backside localization of open and shorted IC interconnections." In *Reliability Physics Symposium Proceedings, 1998. 36th Annual. 1998 IEEE International*, pp. 129-136. IEEE, 1998.

[6] Nikawa, K., 2003, October. Optical beam induced resistance change (OBIRCH): Overview and recent results. *Lasers and Electro-Optics Society, 2003. LEOS 2003. 16th Annual Meeting of the IEEE* (Vol. 2, pp. 742-743). IEEE.

[7] Hawkins, C.F., Soden, J.M., Fritzemeier, R.R. and Horning, L.K., 1989. Quiescent power supply current measurement for CMOS IC defect detection. *IEEE Transactions on Industrial Electronics*, *36*(2), pp.211-218.

[8] Cao, L., Venkata, M., Tay, M.Y., Qiu, W., Alton, J., Taday, P. and Igarashi, M., 2012, November. Advanced Fault Isolation Technique using Electrooptical Terahertz Pulse Reflectometry (EOTPR) for 2 & 2.5D Flip-chip Package. *Proceedings of the 38th International Symposium for Testing and Failure Analysis (ISTFA)* (pp. 21-25).