Dead-time Optimization for SiC Based Voltage Source Converters Using Online Condition Monitoring

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***Abstract*—This paper introduces a dead-time optimization technique for a 2-level voltage source converter (VSC) using turn-off transition monitoring. Dead-time in a VSC impacts power quality, reliability, and efficiency. Silicon carbide (SiC) based VSCs are more sensitive to dead-time from increased reverse conduction losses and turn-off time variability with operating conditions and load characteristics. An online condition monitoring system for SiC devices has been developed using gate drive assist circuits and a micro-controller. It can be leveraged to monitor turn-off time and indicate the optimal dead-time in each switching cycle of any converter operation. It can also be used to specify load current polarity, which is needed for dead-time optimization in an inverter. This is an important distinction from other inverter dead-time elimination/optimization schemes as current around the zero current crossing is hard to accurately detect. A 1kW half-bridge inverter was assembled to test the turn-off time monitoring and dead-time optimization scheme. Results show 91% reduction in reverse conduction power losses in the SiC devices compared to a set dead-time of 500ns switching at 50 kHz.**

***Key words*—Condition monitoring (CM), silicon carbide (SiC), voltage source converter (VSC), body diode, current sensing, dead-time**

I. Introduction

VOLTAGE source converter (VSC) is a common topology used in power electronic converter design. Its basic building block is a phase-leg, which is two series-connected power semiconductors. Then the various types of converters are enabled with a dc voltage source across the lower and upper terminals of the phase-leg and an inductor, as the dc or ac current source, connected to the middle point of the phase leg. In recent years, a shift has been taking place where silicon carbide (SiC) power semiconductors have replaced traditional silicon (Si) power semiconductors in VSCs [1]. This is because SiC offers faster switching capabilities, increased junction operating temperature, increased blocking voltages, and lower on-resistance. However, in order for power electronic engineers to use these devices effectively, the SiC trade-offs must be considered and compensated. One example of this is the device body diode characteristics and their effect on reverse conduction loss. SiC devices have higher body diode forward voltage compared to other anti-parallel diodes connected to the switching devices, which produces more reverse conduction energy losses according to equation 1,

$$P_{dt} = V_f \times I_d \times 2 \times t_{dt} \times f_{sw} \quad (1)$$

where V_f is the forward voltage, I_d is the drain current, f_{sw} is the switching frequency and t_{dt} is the dead-time. The SiC intrinsic V_f value cannot be changed and SiC applications require higher power ratings and switching rating (i.e. higher I_d and f_{sw}); therefore, the dead-time parameter set in the control stage needs to be actively adjusted for ideal performance.

For a phase-leg configuration of switching devices used in VSCs, the dead-time between the two devices is a critical parameter. The dead-time is necessary to prevent both devices from turning on and causing shoot-through failures; however, it causes issues in converter performance. Dead-time adds power loss in the form of body diode conduction loss, as previously mentioned, and adds voltage distortion at the output of the converter. Therefore, adaptive dead-time regulation schemes can become beneficial by enhancing reliability (i.e. reduce heat from losses) and improving converter efficiency.

One traditional approach is trying to eliminate the dead-time needed in a phase-leg of a converter [2-4]. All three works state that precise current detection around the zero-crossing of a VSI is inaccurate. Chen *et al.* [2] adds complexity to their dead-time elimination system to avoid this issue. Wang *et al.* [3] and Yuan *et al.* [4] change their dead-time correction schemes around the zero crossing, which again avoids the issue of zero-current crossing. There is a need to design a dead-time correction scheme that successfully accounts for the switching cases around the zero-current crossing without added complexity. Other works have the same goal in mind as this proposed work in optimizing the amount of dead-time in a switching cycle [5-7]. Yousefzadeh *et al.* [5] designed a control algorithm for DC-DC converters using traditional output voltage regulation feedback along with incremental change in dead-time each switching cycle to obtain the optimal dead-time and duty cycle. Lee *et al.* [6] also optimizes the dead-time in DC-DC converters but uses dead-time error voltage sensing circuits. An issue with these works is they are limited to only DC-DC converters, where the current doesn't change from switching cycle to switching cycle, and cannot be applied to all 2-level VSCs.

In this paper, an online condition monitoring system for SiC is used to adaptively set the optimal dead-time for every

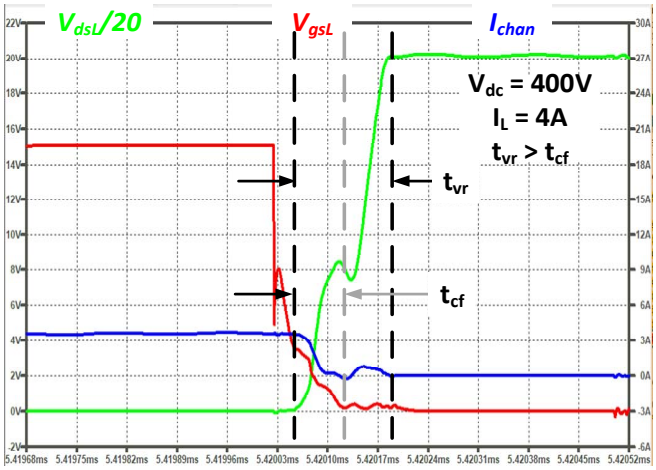
switching cycle (even those around the zero-crossing) during a VSI operation without modifying anything around the zero-current crossing. In section II, the model for optimal dead-time between two SiC devices centered on the device turn-off transition is presented. In section III, the online turn-off condition monitoring system is detailed to show precise and accurate turn-off time sensing as well as elimination for current sensing. Section IV will show experimental results using a VSI as the converter to show power loss reduction from reverse body diode conduction.

II. Dead-time Optimization in VSCs

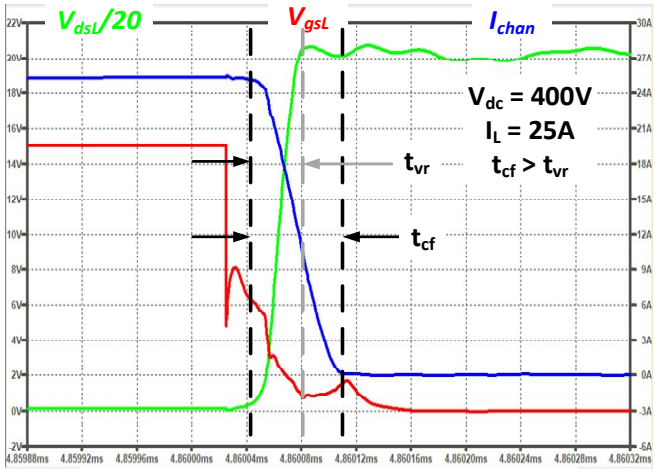
The dead-time optimization scheme is based on a model designed in previous work [7]. This model will be summarized in the following section with special considerations for VSI applications

A. Dead-time optimization scheme

Optimal dead-time is stemmed from the turn-off transition of a power semiconductor device in a phase-leg configuration. For SiC phase-legs, the turn-off time (t_{off}) is sensitive to operating conditions and converter load characteristics [8, 9]. An example



(a) at low currents, voltage rise takes longer ($t_{vr} > t_{cf}$)



(b) at high currents, current fall takes longer ($t_{cf} > t_{vr}$)

Fig. 1. Switching waveforms during the turn-off transient

of this is looking at the hard turn-off transition of the low side SiC device, where the current is flowing into the phase-leg. This is simulated in LTSpice with the Wolfspeed C2M0080120D SiC MOSFET model used in a half-bridge inverter with switching transition results shown in Fig. 1. When load current is smaller, *dv/dt* of the drain-source voltage is limited by the power loop. All of the low I_L current is used to charge the output capacitance of the device, which causes the channel current to fall to zero faster than it takes to raise V_{ds} to the DC bus voltage. This means voltage rise time (t_{vr}) is longer than current fall time (t_{cf}), as shown in Fig. 1(a), and this case is called the power loop dominated turn-off. For the case of higher load current, only a portion of the load current is needed in the power loop to charge the output capacitance, whereas the rest of the load current travels via the gate loop. This means current fall time (t_{cf}) is longer than voltage rise time (t_{vr}), as shown in Fig. 1(b), and this case is called the gate loop dominated turn-off. Therefore, the optimized dead-time for the case of a hard-turn off is dependent upon t_{vr} and t_{cf}, which are dependent upon load current. Now the online monitoring system, which will be discussed in more detail in section III, can obtain the t_{vr} value for any switching cycle. However, it is difficult to monitor channel current and therefore know t_{cf}. So, Fig. 2 shows the model used for optimized dead-time ($t_{dt(opt)}$) for the hard turn-off case, where monitored t_{vr} is used as $t_{dt(opt)}$ until the max t_{cf} value is reached and used as $t_{dt(opt)}$ [7].

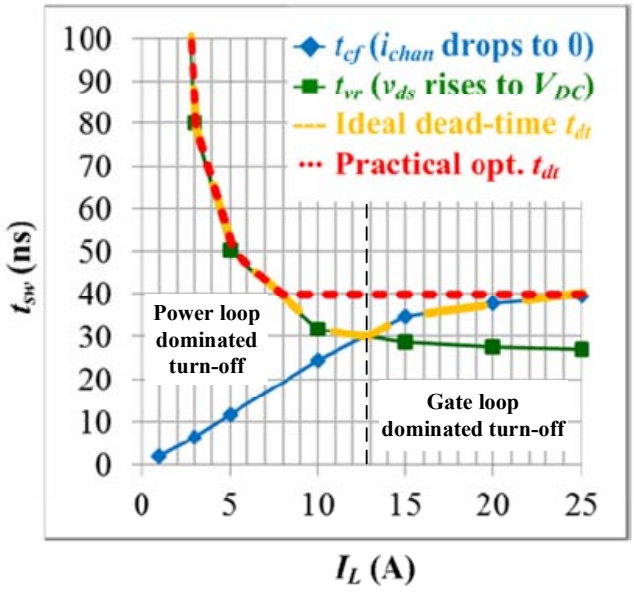
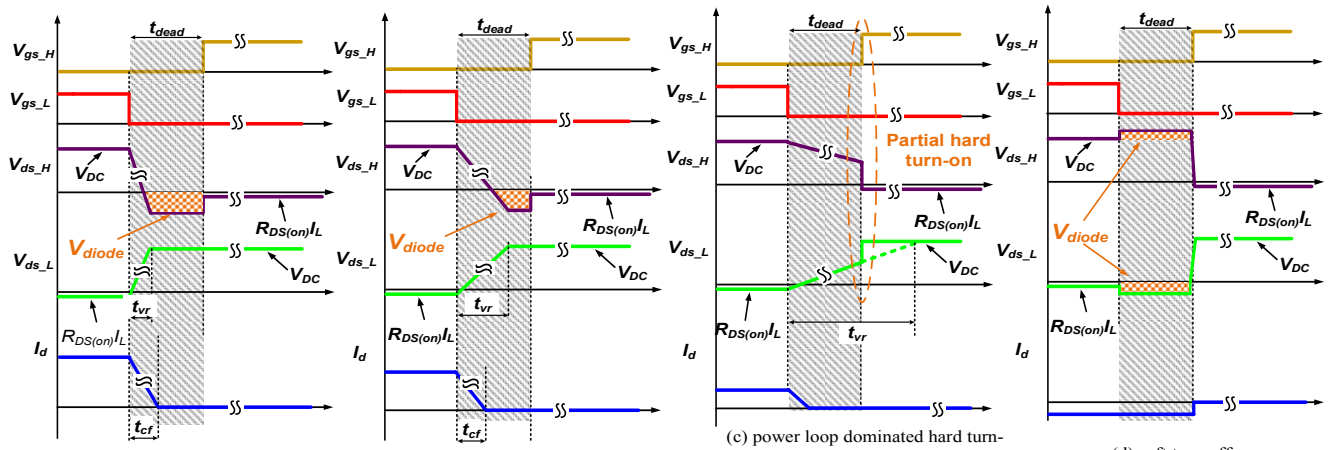


Fig. 2. t_{cf} vs. t_{vr} determining optimal dead-time for hard turn-off case

B. Specific VSI considerations for dead-time optimization

The analysis for dead-time optimization is not complete yet because the previous section only looked at a hard turn-off case for the low side device in a phase-leg configuration. This was because, in previous works, the converter topology chosen was a buck converter configured to have the DC load current flowing into the phase-leg, which makes the low side device the operating device and makes the upper SiC device be the



(a) gate loop dominated hard turn-off $t_{dt} > t_{cf} > t_{vr}$ (b) power loop dominated hard turn-off $t_{dt} > t_{vr} > t_{cf}$ (c) power loop dominated hard turn-off with partial hard turn-on $t_{vr} > t_{dt} > t_{cf}$ (d) soft turn-off

Fig. 3. Diagram of all possible turn-off switching waveforms in a VSI application, showing diode losses in the dead-time

synchronous device. However in a VSI application, the load current is AC and thus both devices can be the operating device and synchronous device depending on the current polarity, which means there are special considerations needed to be analyzed for full dead-time optimization.

1) Soft turn-off case: A power switching device experiences a soft turn-off when the load current is flowing in the direction of source to drain (i.e. the device is acting as the synchronous device). The turn off transition for this case can be seen in Fig. 3(d). For a VSI application, both switches can be the synchronous device so it would seem there is a need for current sensing to indicate the current polarity for each switching cycle. However, the monitoring system can be leveraged to indicate current polarity and this detail will be shared in section III. The optimal dead-time in this case is just the time it takes for the gate-source voltage to drop to 0 V to prevent both channels turning on and causing a shoot-through current spike.

2) Partial hard turn-on from synchronous device: Another type of turn-off transition that can be seen in VSI operation is the partial hard turn-on for the synchronous device. This type arises when dead-time is set too aggressively and becomes shorter than the drain-source voltage rise time as shown in Fig. 3(c). This eliminates the reverse conduction losses but causes switching power loss in the synchronous device when it experiences a partial hard turn-on, which doesn't solve the problem of optimizing dead-time to reduce power loss. There is not an easy way to mitigate this through monitoring though as it would take knowing the voltage value the V_{ds} rose to before the partial hard turn-on to know how long the dead-time should be in this switching cycle case. The best way to avoid this case is conservatively set the dead-time in initial VSI operation.

In summary, the switching transition experienced in a VSI application during dead-time can be seen in Fig. 3. This figure also shows where the reverse conduction power loss (i.e. case (a), (b), (d)) or switching losses (i.e. case (c)) occur.

III. Turn-off Time Acquisition in VSIs

The best way to achieve dead-time optimization is through condition monitoring of the critical parameters discussed in section II. However, further analysis can show that it is sufficient to just make assumptions for some of the parameters. First, it was mentioned earlier the difficulty to monitor the t_{cf} time. Also, when t_{cf} is greater than t_{vr}, it isn't by much so an assumption can be made to just add a small margin to the monitored t_{vr} time for dead-time optimization under the hard turn-off cases. Second, for the soft turn-off cases, the gate-source voltage fall time doesn't change; therefore, we can determine that value offline and use it as $t_{dt(opt)}$ value under the soft turn-off cases. This leaves t_{vr} as the only critical parameter left to be monitored and the next section will detail this designed online monitoring system. Also, before that system is explained, there needs to be some clarification on the labeling of pieces during the turn-off transition. When looking back at Fig. 1, there is a section of time between the start of the fall of the gate-source voltage and the start of t_{cf} and t_{vr}. This time is called the turn-off delay time (t_{d_off}) and it is one of the times this online monitoring system can capture. It will come into play in section III(B) looking at the elimination for a need of current sensing. Also, the online monitoring system can capture both drain-source voltage rise and fall times so the labeling is simplified to denote that time as voltage commutation time (t_{vc}).

A. Online condition monitoring system

The system, published in [10], starts with gate drive assist circuits which detect critical moments in the turn-off transition.

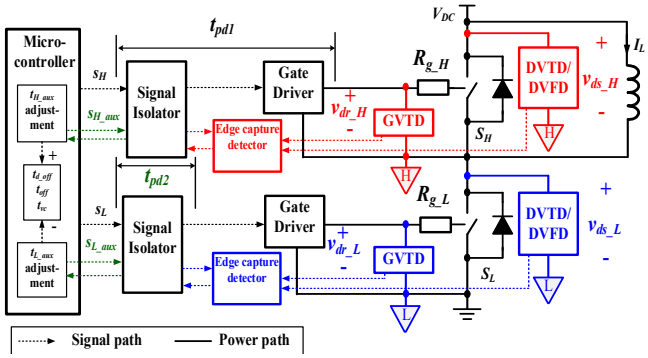


Fig. 4. Online t_{off} monitoring system [9]

The first one is called gate-source voltage transient detector (GVTD) that detects the moment when the gate-source voltage begins to fall. The second one is called drain-source voltage transient detector (DVTD) that detects the moment when the opposite device drain-source voltage begins to fall (i.e. when the monitored device drain-source voltage begins to rise). The third gate drive assist circuit is the drain-source fall detector (DVFD), which detects the moment when the opposite device drain-source voltage reaches 0 V (i.e. when the monitored device drain-source voltage reaches V_{DC}). This detection data is captured with a high resolution PWM (HRPWM) auxiliary signal from the micro-controller. This HRPWM functionality of the TMS320F28335 micro-controller enables very accurate measurement of the timing conditions by using the small 0.104 ns capture step in the PWM signal [11]. The micro-controller is then able to process the time in between the detection signals. This system diagram is shown in Fig. 4, where the devices are connected to the gate driver and gate drive assist circuits. The gate drive assist circuit send their signals to the edge capture detector, which also receives an isolated HRPWM auxiliary signal. The output is an indicator of edge detection that gets isolated and sent back to the MCU to process the monitored times during the turn-off transition of both devices. It is also important to note that the monitoring process accounts for the propagation delay of the signal isolator and gate driver IC, which could lead to time sensing error especially in the high switching frequency applications for SiC devices.

B. *Elimination of need for current sensing*

The monitoring system can also be leveraged to indicate load current polarity as shown in Fig. 5. The concept behind this ability is the different drain-source voltage waveforms for a hard turn-off and soft turn-off. The parameter that can clearly be used to indicate current polarity is turn-off delay time (i.e. the time from the start of the fall of the gate-source voltage to the start of the drain-source voltage rise). This ability to online know the current polarity without a dedicated current sensor turns out to be advantageous for a number of reasons. First, in a VSI application, some form of current sensor is necessary to know the type of switching transition (i.e. hard vs. soft switching) during monitoring. Second, traditional dedicated current sensors struggle to precisely know the load current

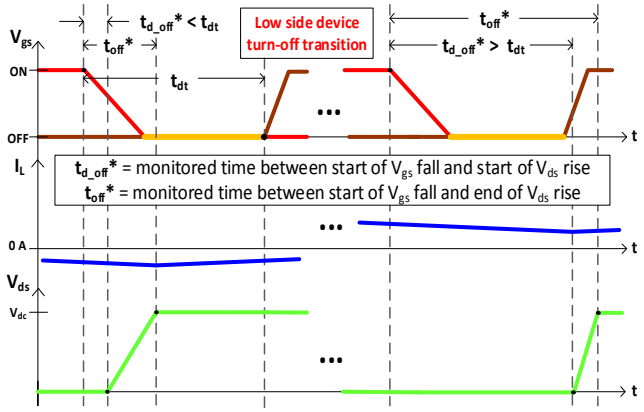


Fig. 5. Difference in monitored turn-off delay time (t_{d_off}) for positive and negative load current which can indicate the two categories for optimized dead-time.

value during a switching transition (i.e. limited bandwidth) [12]. This distinguishes this research work from other dead-time optimization/elimination schemes that deal with the issue of precise current sensing, especially around the zero current crossing. Therefore, this online system is able to accomplish multiple tasks, in current polarity sensing and accurate t_{off} monitoring, towards the objective of dead-time optimization in any VSC.

IV. Simulation and Experimental Results

A. *1kW half-bridge inverter test results*

Experimental verification was also conducted to show improved performance from dead-time optimization. A 1 kW half-bridge inverter, shown in Fig. 6, was constructed using two Wolfspeed C2M0080120D SiC devices in a phase-leg configuration, a 400 V dc input, switching frequency of 50 kHz, fundamental frequency of 360 Hz, and modulation index of 0.8. The AC load included a 400 µH inductor connected to the middle point of the phase-leg as well as a 4.8 µF capacitor and 10 Ω resistor in parallel on the output. The inverter was run and the monitoring system accurately captured the turn-off time for the critical switching cycles during inverter operation as shown through an oscilloscope capture in Fig. 7. This figure used the persistence feature on the oscilloscope to portray the auxiliary signal capturing the end of the turn-off time for multiple switching cycles. The monitored data, processed in the micro-controller, updates the dead-time to the optimized value to

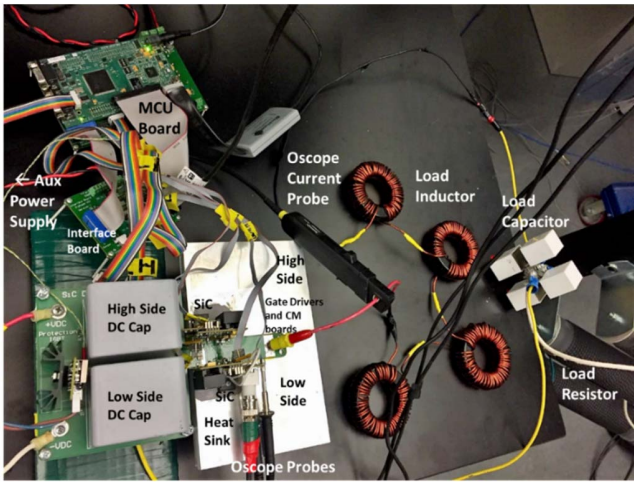


Fig. 6. 1 kW half-bridge inverter test setup with labeled components

increase converter efficiency and reduce power loss in the SiC devices. A summary of the power loss analysis is shown in Table I, where four dead-time situations are tested in the inverter. The related body diode reverse conduction loss is calculated using equation 2,

$$P_{diode} = V_f \times I_{rms} \times (t_{dt} - t_{off}) \times 2 \times f_{sw} \qquad (2)$$

where V_f is the diode forward voltage from the datasheet, I_{rms} is the RMS load current, and f_{sw} is the switching frequency. The partial hard turn-on loss (P_{ps}) is calculated using equation 3,

$$P_{ps} = \left(\frac{-V_1 \times I_d}{3} \times t_{sw} + \frac{V_1 \times I_d}{2} \times t_{sw}\right) \times f_{sw} \qquad (3)$$

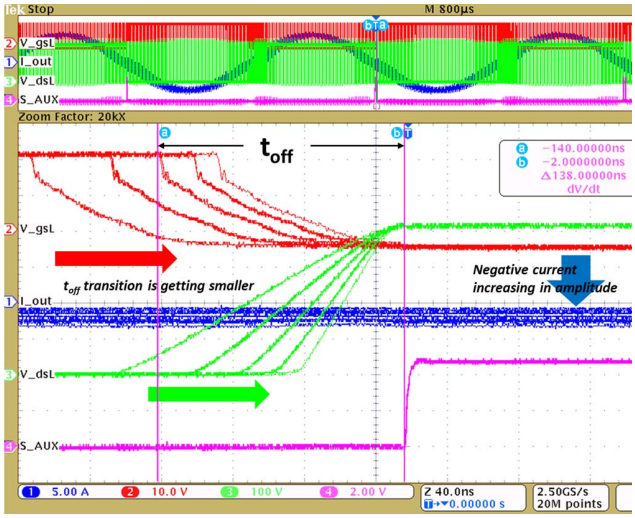


Fig. 7. Turn-off time monitoring for multiple switching cycles during HB inverter operation.

where V_1 is the voltage level of V_{ds} at the time of the partial hard turn-on, I_d is the drain current, and t_{sw} is the switching time. The last column does an energy comparison inside of 1 µs, where the first case is just the reverse conduction energy loss during dead-time and the other cases feature other forms of energy loss less than the reverse conduction loss. E_{ps} is the energy lost from a partial hard turn-on and E_{chan} is the energy lost during the SiC channel conduction. Clearly the dead-time optimization approach presents the best performance and reduces the body diode power conduction loss on the devices by 91% when compared to the 500 ns case.

Table I. Power loss analysis for dead-time implementations on the 1 kW HB inverter

Operation	Body diode reverse conduction loss	Partial hard turn-on loss	Energy loss in 1 µs (E_{dt} + E_{ps} + E_{chan})
Dead-time = 1 µs	2.852 W	0 W	57.04 + 0 + 0 = 57.04 µJ
Dead-time = 500 ns	1.417 W	0.133 W	28.34 + 2.66 + 8.36 = 39.36 µJ
Dead-time = 100 ns	0.08 W	1.06 W	1.6 + 21.2 + 17.14 = 39.94 µJ
Dead-time Optimization	0.1267 W	0 W	2.53 + 0 + 16.57 = 19.1 µJ

V. Conclusion

A dead-time optimization scheme is proposed for any VSC using online turn-off monitoring for the two SiC devices in a phase-leg configuration. Dead-time optimization is needed for SiC based converters because of higher reverse conduction loss, faster switching frequency, and the turn-off time's increased sensitivity to operating conditions and load characteristics. The online monitoring system distinguishes itself by also detecting current polarity based on the V_{ds} switching waveform, which eliminates the need for a current sensor that can be unreliable around the zero current crossing. A 1 kW half-bridge inverter experimental test, switching at 50 kHz, was conducted to compare the results of different dead-time implementations. The DTO results show clear reverse conduction power loss reduction compared to conservative dead-time settings of 500 ns (91% reduction) and 1 µs (95.6% reduction). The DTO results also show 100% reduction in the partial hard turn-on loss when compared to the aggressive dead-time setting of 100 ns. Future work would be seeing the benefits on incorporating this DTO scheme on converters outside of the 2-level VSC.

Acknowledgment

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