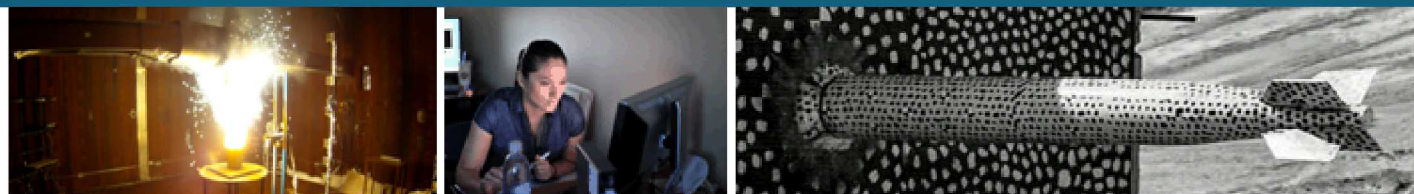
SAND2018-9355R

Summary of Total Dose Testing on IBM Bottom Oxidation Through STI (BOTS) FinFETs



PRESENTED BY

M. P. King (05268)

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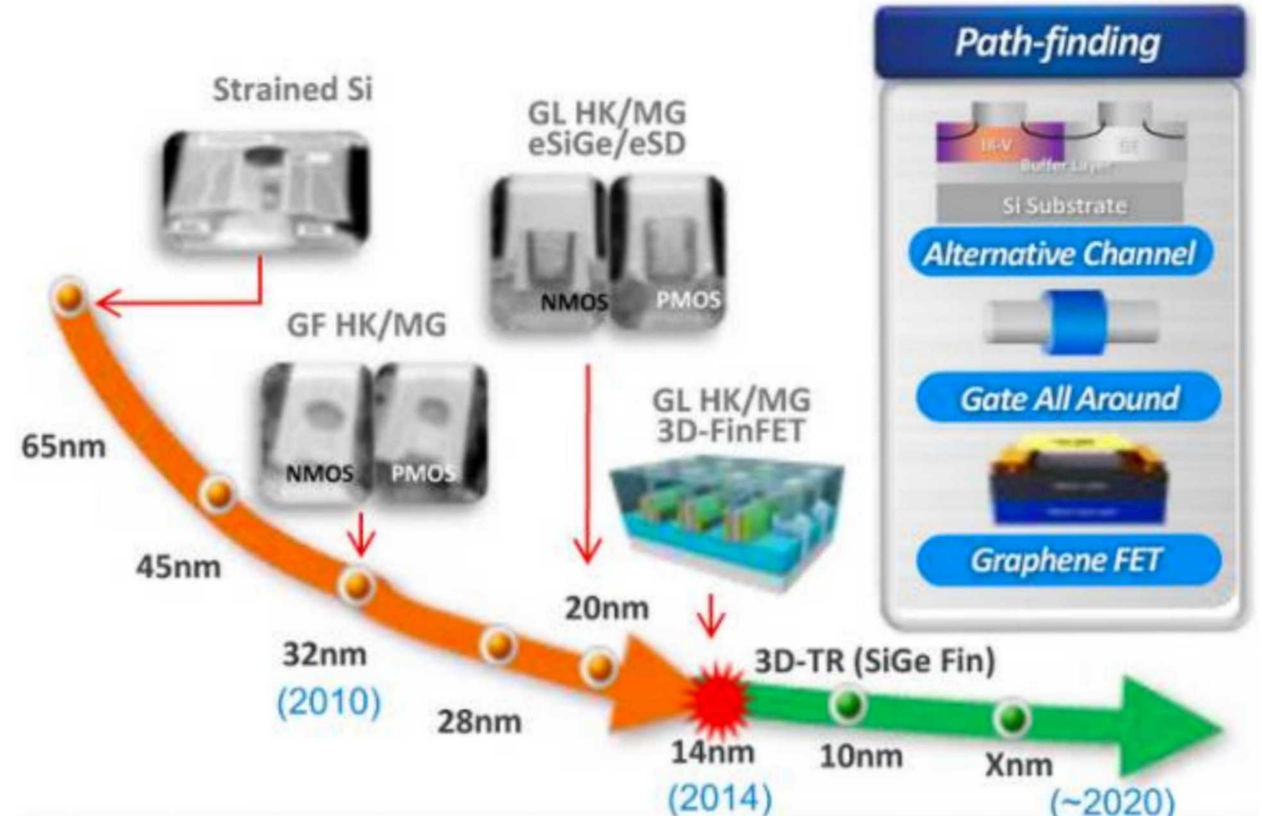
Outline

- Trends of TID in commercial technology
- Test methods and analysis used in this work
- TID results on a novel quasi-SOI(BOTS) FinFET
- Conclusions

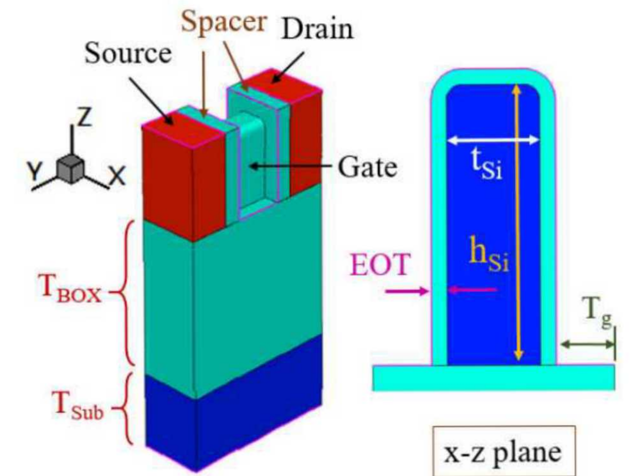


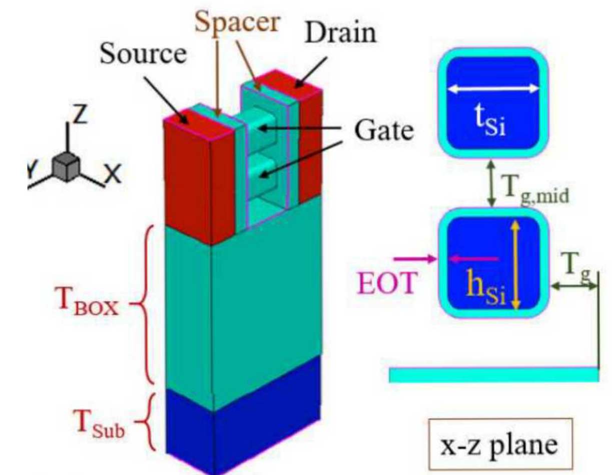
Motivation

State of the art semiconductor processes have created high performance and low power consumption technologies

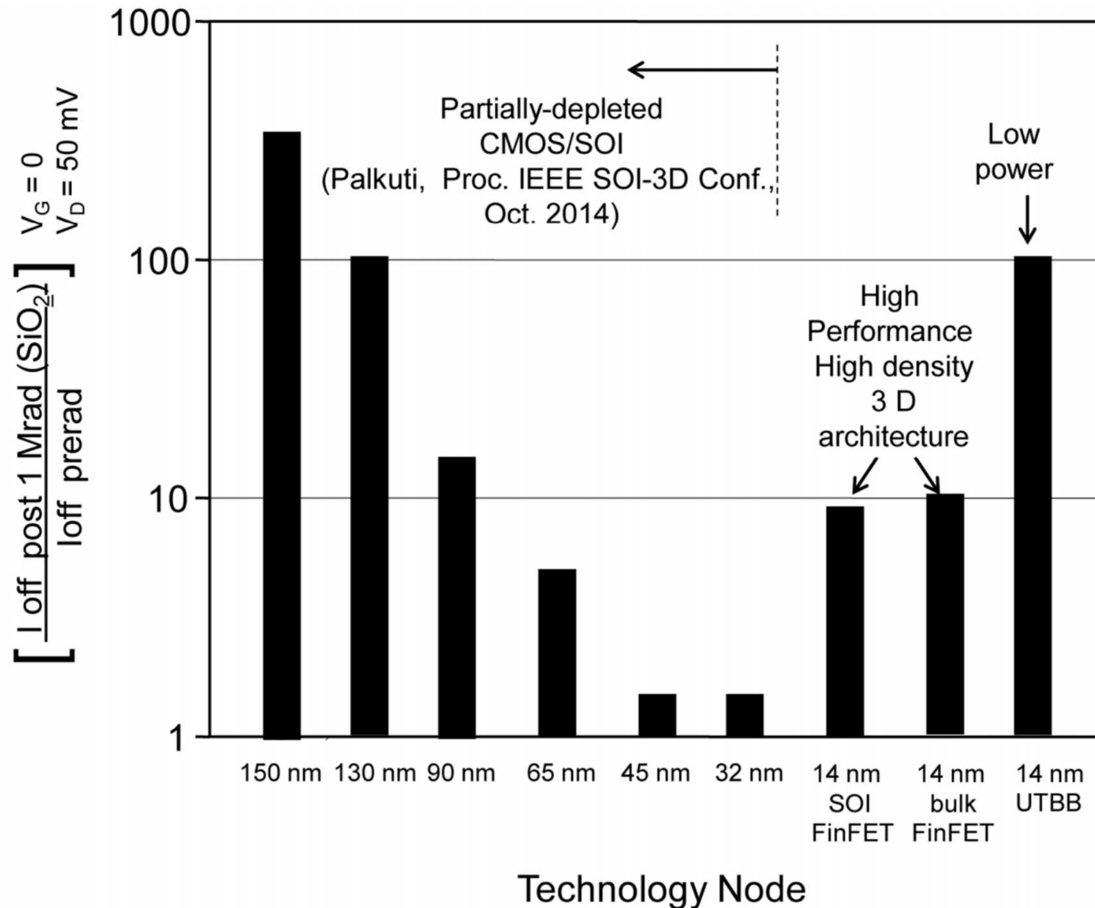
There is a drive to use these technologies for commercial space, defense, and infrastructure

- Need to understand radiation effects in leading technology nodes





Total Dose vs Technology Scaling



Hughes (NRL) REDW NSREC (2015)

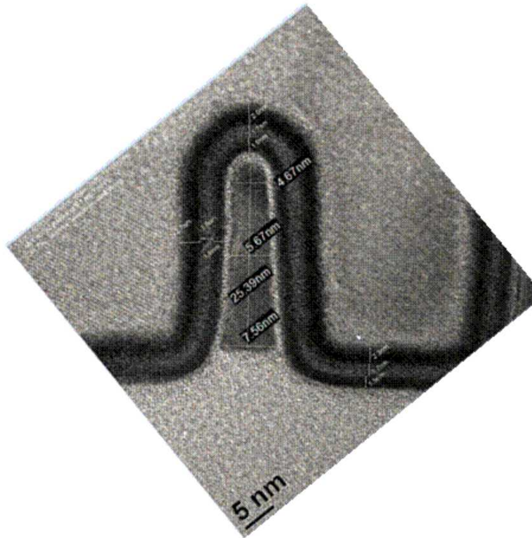
Scaling trends of off-state leakage vs technology node

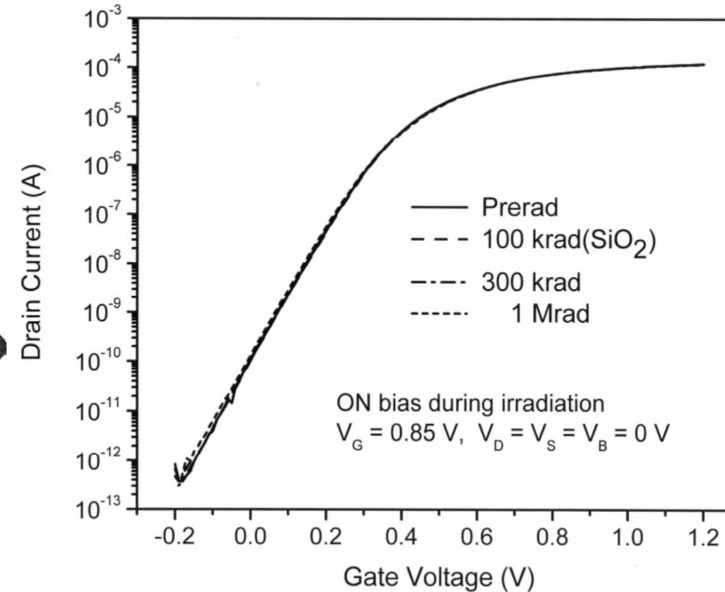
PDSOI exhibits very low leakage for 45- and 32-nm at 1 Mrad

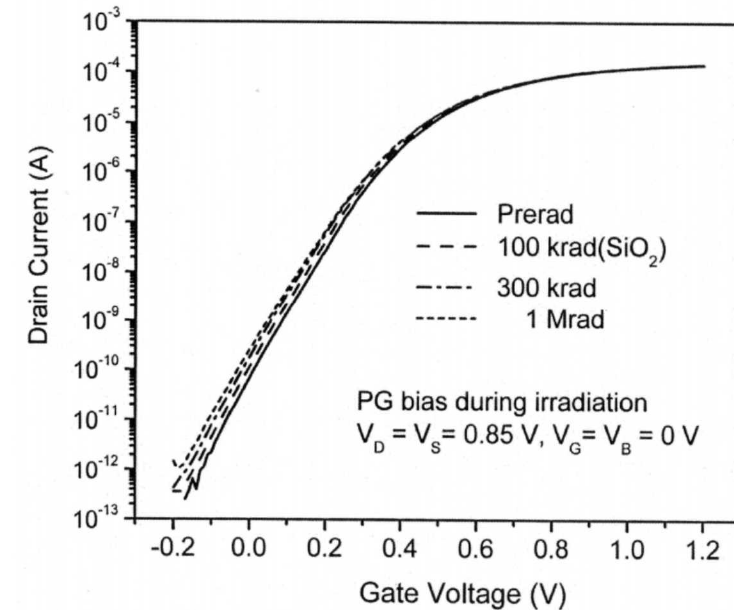
Migration to FinFETs resulted in a dramatic increase in post-irradiation leakage (early look)

FDSOI shows leakage comparable to older technologies

Return of the SOI FinFETs?







Hughes REDW 2015

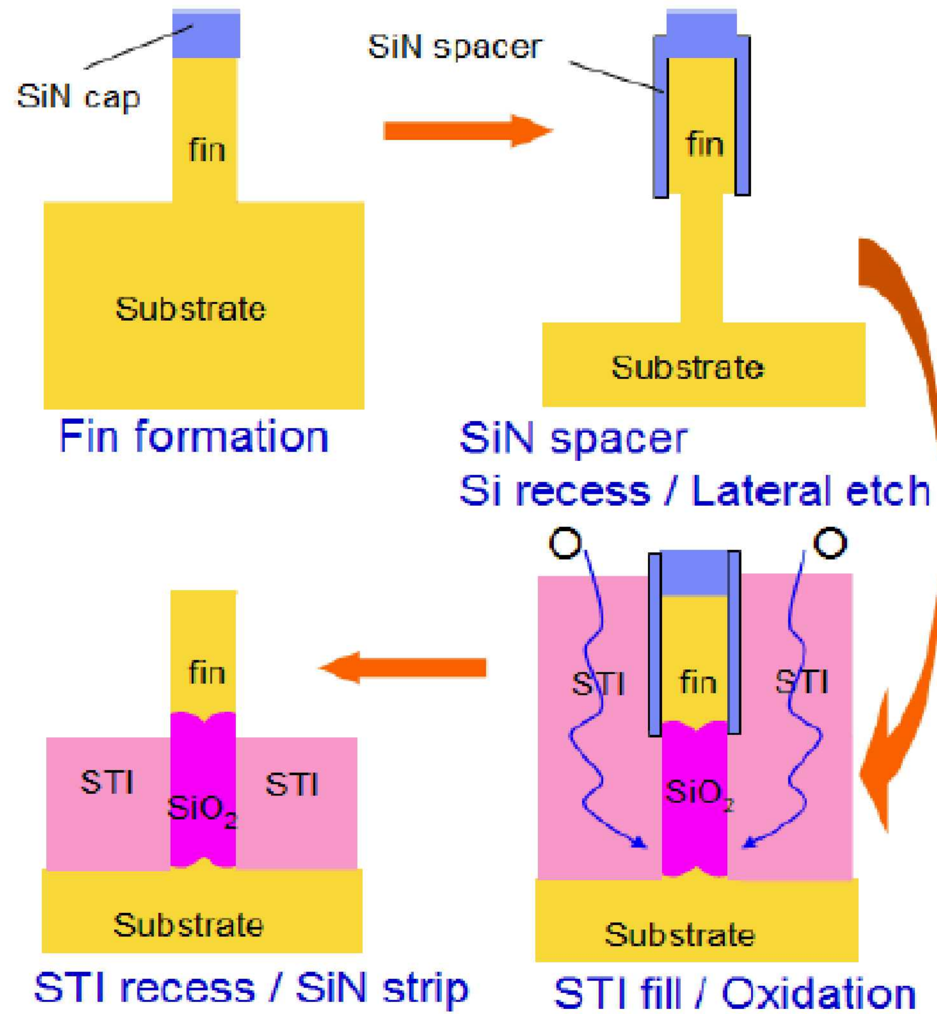
No commercial source (IBM tech)
- Made by GF for Z-server series (14HP)

Good: Latchup (electrical or radiation-induced) immune

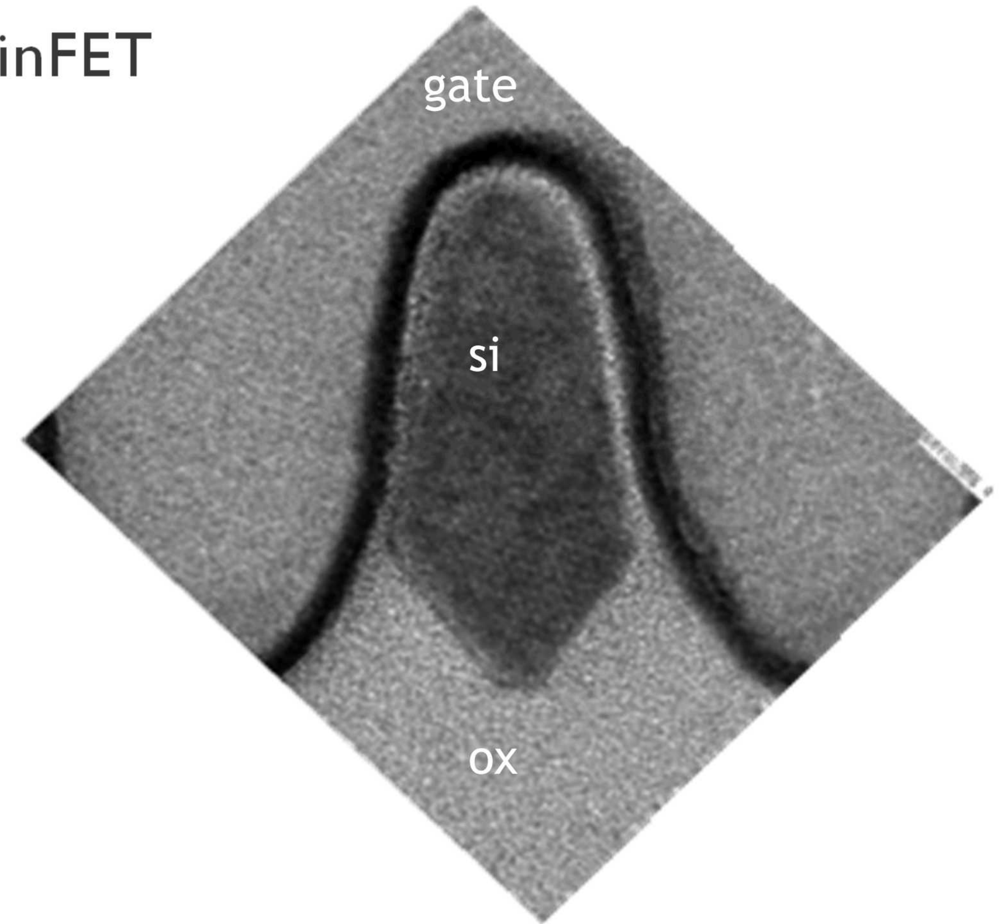
Good: Reduced charge collection volume

Bad: Increased parasitics and floating body

Bottom Oxidation Through STI – BOTS FinFET



Cheng VLSI Symposium 2014

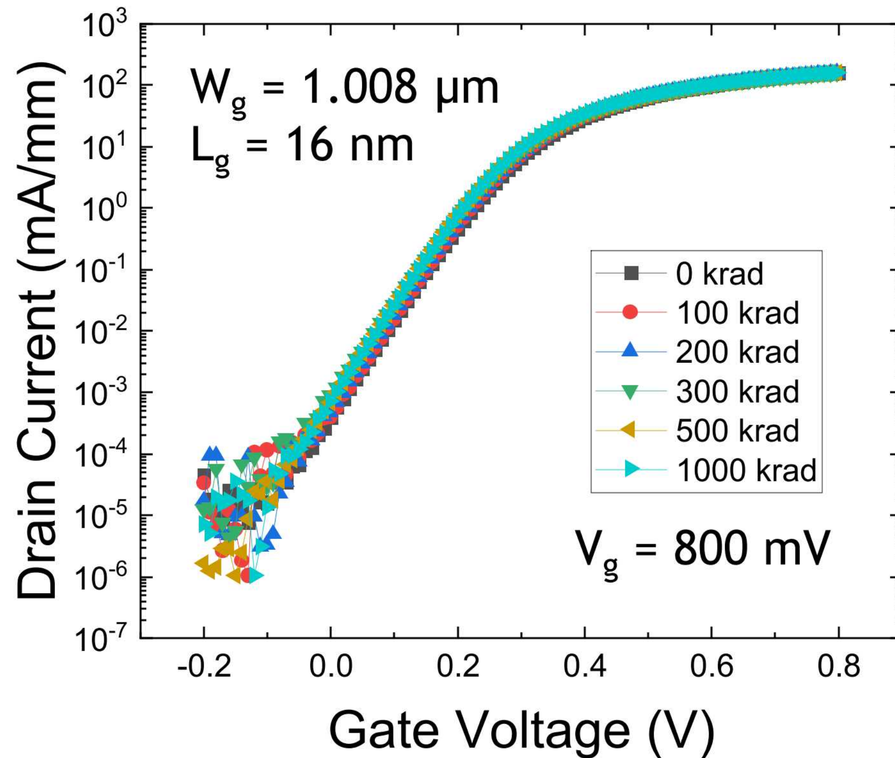


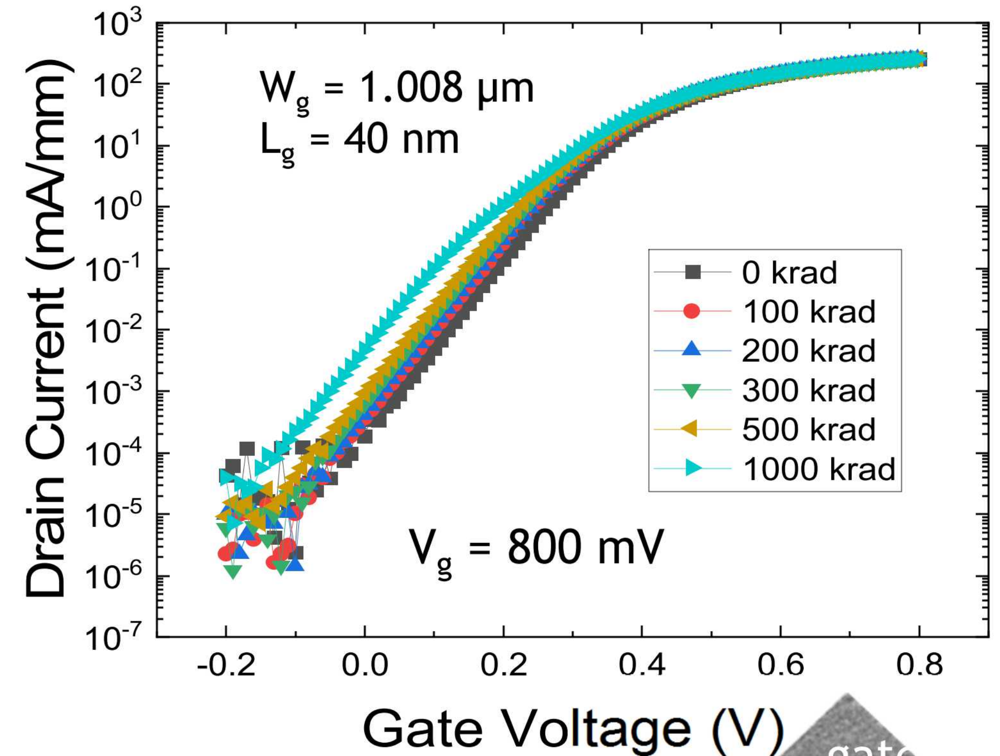
Technology compatible with bulk process flow, start material, and tools

Selective formation of SOI devices on same reticle as bulk devices

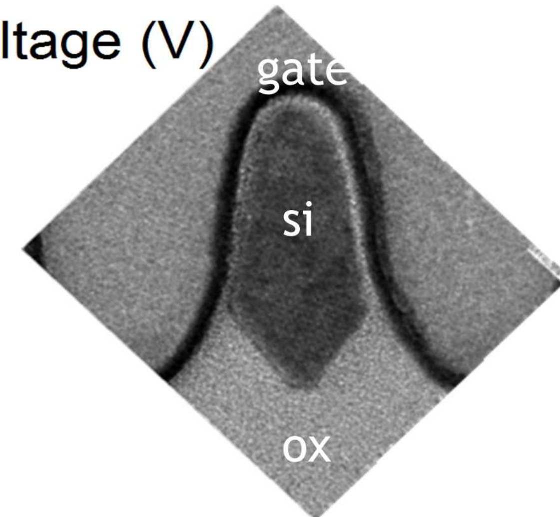
TID in BOTS-FinFETs - Transistor Length Dependence

Quasi-SOI Technology - Experimental

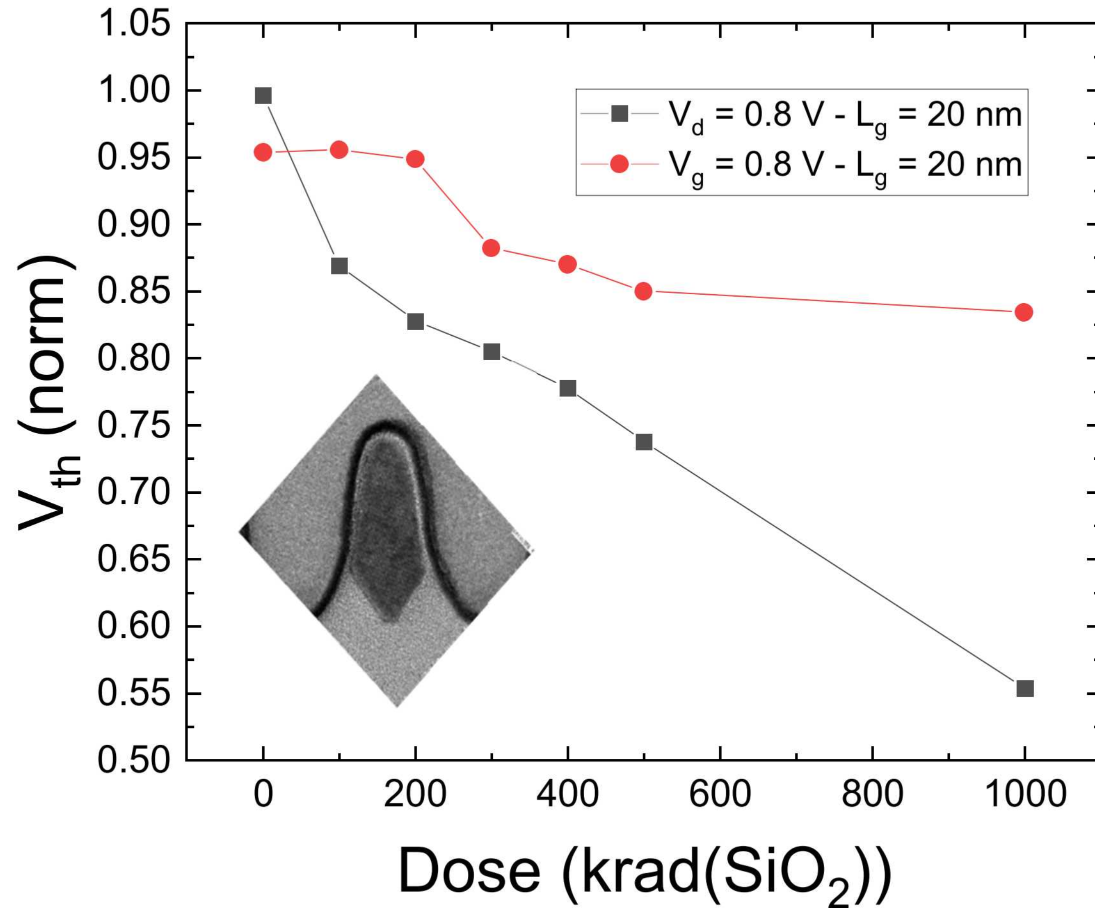




- Dielectrically isolated devices remove latchup structures limiting current technology
- Device length leads to interesting trends for threshold voltage and leakage current (ΔV_{th} due to charge trapping) – similar to reports on FDSOI



Threshold Voltage Influenced by Buried Oxide Trapped Charge

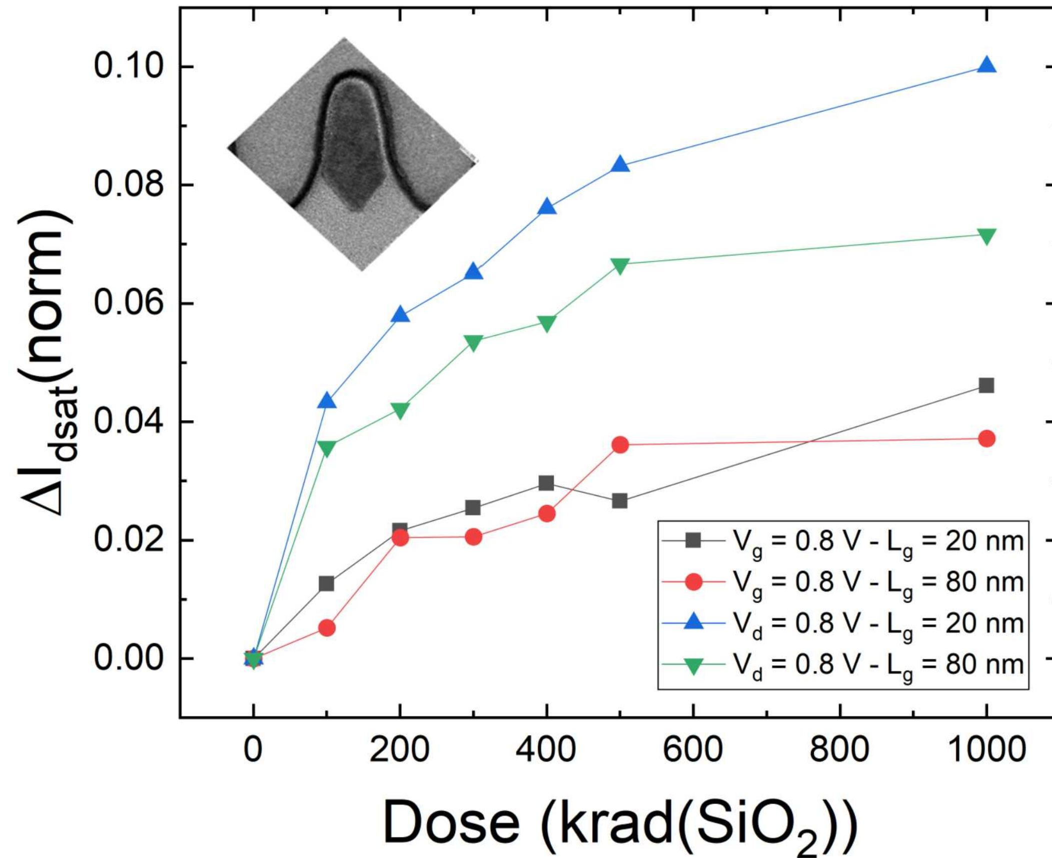


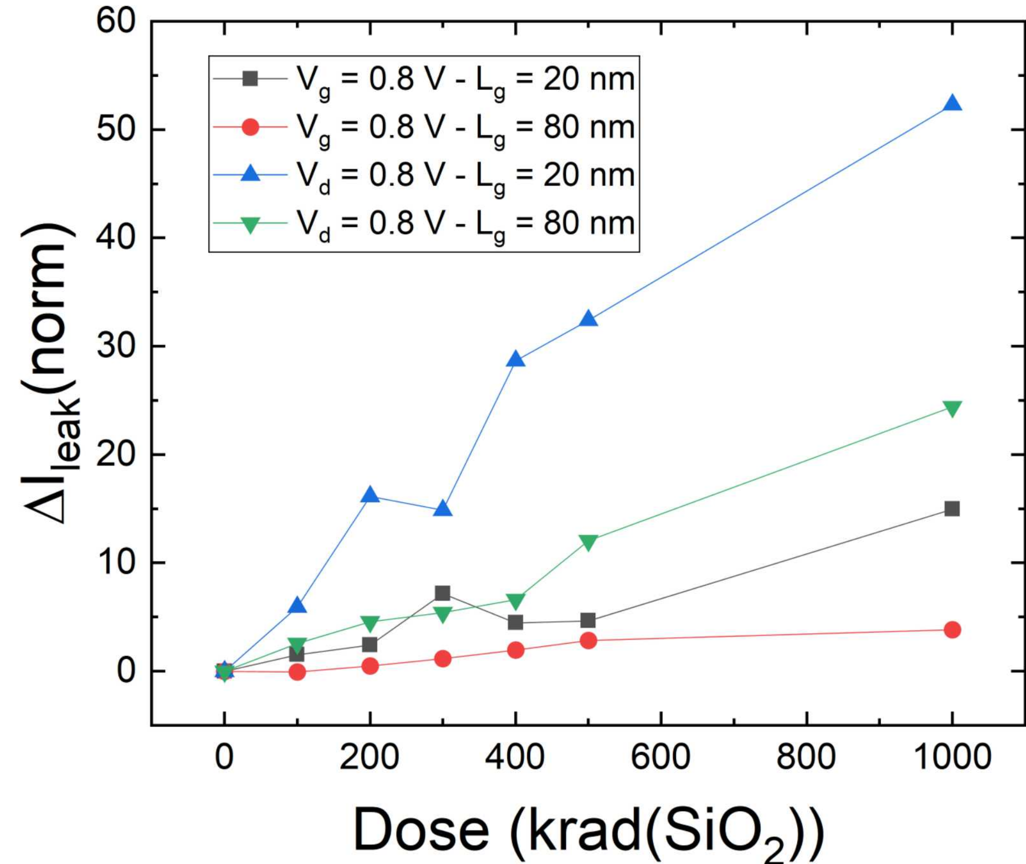
Devices irradiated in the off-state (V_d = 800 mV, $V_g = V_s$ = 0 V) exhibit substantially stronger ΔV_{th} than devices irradiated in the on-state (V_g = 800 mV, $V_d = V_s$ = 0 V)

TCAD simulations show electric field penetration of the "BOX" for the off-state irradiation

Leads to greater charge yield and larger impact on device V_{th} and I_{leak}(sat)

Saturation Response – Long vs Short Channel Devices





- Irradiation condition has more impact on post-irradiation drive current than channel length with the worst case ΔV_{th} in the *off-state*
- Leakage is highest in the off-state as well – geometry dependence ~ $1/L_g$

Conclusions

Devices irradiated in the off-state (drain at V_{dd}) exhibit substantially stronger ΔV_{th} than devices irradiated in the on-state (gate at V_{dd})

- Likely due to extension of electric field into the thermally grown buried oxide with the drain at V_{dd} (supported by TCAD)

Design width and length dependences observed in *bulk* and *quasi-SOI transistors* – leakage paths still under investigation

- BOTS shows a $1/L_g$ dependence for post-irradiation leakage indicating the presence of a parasitic transistor formed along the back-gate