An Islanding Detection Test Platform for Multi-Inverter Islands using Power HIL

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***Abstract*—When an unintentional island is formed on the electric power system, distributed energy resources (DERs) are typically required to detect and de-energize the island. This requirement may become more challenging as the number of DERs in an island rises. Thus, it is of interest to experimentally verify whether DERs can successfully detect and de-energize islands containing many DERs connected at different points. This paper presents a power hardware-in-the-loop (PHIL) platform for testing the duration of islands containing multiple inverters connected at multiple points in a network. The PHIL platform uses real-time simulation to represent islanded distribution circuits, with DER inverters connected in hardware. This allows efficient testing of a large number of island configurations simply by changing the distribution circuit model in the real-time simulator. A method for calculating the quality factor of an arbitrary distribution circuit in real time, designed for anti-islanding tests, is also presented. Experimental results are included demonstrating the use of the PHIL method to test a variety of three-inverter islands.**

***Index Terms*— Anti-islanding, Power hardware-in-the-loop, Distributed energy resources, Inverters.**

I. Introduction

RAPIDLY increasing deployment of distributed energy resources (DERs) such as photovoltaic (PV) generation on electric power systems has recently led to renewed interest in islanding detection (anti-islanding) for two reasons. First, DERs are often now required to remain connected during (or "ride through") a wide range of grid voltage and frequency events [1]–[3], and they may also be required to perform various functions designed to help regulate system voltage and frequency to their nominal operating ranges, which may interfere with island detection. Second, there is concern that some anti-islanding methods may become less effective in island scenarios containing multiple DERs [4] because each individual DER's efforts to detect the island may be interfered with by other DERs in the island.

These concerns have led to an increased motivation to verify that DERs can detect unintentional electrical islands and disconnect when ride-through and other grid support functions (GSFs) are enabled and when multiple DERs are present on the same circuit. Currently in the U.S., DERs are required by IEEE 1547-2003 to de-energize an island within two seconds of its formation [5], and must pass an unintentional islanding test verifying this [6]. This test places the DER in an island with a load tuned to match the DER's real and reactive power and resonate at the nominal grid frequency. As requirements arise for DERs to perform GSFs such as voltage and frequency ride-through, volt-var control, and frequency-watt control, the island test is being updated to include testing with various combinations of such functions activated [7]. It is expected that DER inverter manufacturers will be able to update their anti-islanding controls to pass the test with GSFs enabled, and this expectation is beginning to be experimentally verified [8]–[10].

Most inverter-based DERs use one or more autonomous anti-islanding control methods to comply with unintentional islanding requirements [11]–[13]. These methods vary significantly from one inverter manufacturer to another and are typically proprietary. Thus, even for inverters individually certified to disconnect from unintentional islands, it is difficult to verify analytically or through simulation that a given *combination* of several inverters will de-energize an unintentional island. Some past work has examined the ability of inverters to detect multi-inverter islands both through simulation [14]–[16], and through laboratory experiments [17]–[22]. However, past published experimental work on multi-inverter anti-islanding has been limited to cases where all inverters are connected to the grid at the same point of common coupling (PCC), sometimes called the "AC array" scenario, and has often focused on testing multiple inverters from the same manufacturer. Past testing has not covered the so-called "solar subdivision" scenario of multiple inverters connected at multiple different PCCs on the same circuit. However, some simulations have suggested that such scenarios may indeed increase island durations [23].

Much of the challenge inherent in multi-inverter, multi-PCC island testing is in physically creating the interconnecting circuit, which can be expensive and time-consuming, especially if it is desired to test a variety of possible interconnecting circuits. This work introduces a new method of testing multi-DER, multi-PCC islands. The method uses

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power hardware-in-the-loop (PHIL) simulation to represent the interconnecting circuit. PHIL simulation is a technique where a simulation running in real time is coupled to one or more hardware devices under test in such a way that the simulation incorporates the dynamics of the hardware device [24], [25]. PHIL simulation is particularly useful when accurate models of the hardware devices under test are not available. This is often the case when testing anti-islanding methods, which are typically proprietary. Using PHIL, real hardware inverters can be interconnected at multiple PCCs on a simulated island circuit, so the need to obtain and validate detailed inverter models from multiple inverter manufacturers is avoided. Simply by changing the interconnecting circuit model, a variety of topologies and interconnecting impedance values can be tested relatively rapidly without the need to reconfigure a physical interconnecting circuit.

The primary goal of this paper is to present a method for testing electrical islands with multiple DERs connected at multiple different points, as illustrated for a three-inverter island in Fig. 1. This figure uses the following acronyms: LP = low-pass, DAC = digital to analog converter, ADC = analog to digital converter. The three simulated PCC voltages are $\{V_{PCC1} \ldots V_{PCC3}\}$ and the three measured inverter currents are $\{I_{INV1} \ldots I_{INV3}\}$.

The intent of the test method is to be flexible with respect to the type and number of DERs in the island, the topology and impedances of the interconnecting island circuit, and the type and location of the loads within the island circuit. Thus the method can be used to experimentally verify whether the DERs detect and disconnect from the island within the required time, in a wide variety of multi-DER unintentional island scenarios.

This method of evaluating multi-DER islands is not intended for use in routine standards conformance testing; instead it is intended to enable targeted evaluation of island scenarios in cases of concern to industry.

PHIL methods have been used in [26]–[31] to test inverter grid support functions, including in multi-inverter, multi-PCC scenarios (but not including unintentional island scenarios).

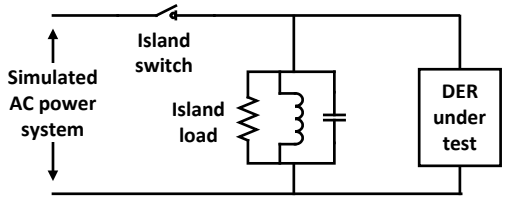

Fig. 2. Conventional unintentional islanding test setup.

PHIL methods have also been used to run traditional single-inverter anti-islanding tests where the resonant resistive-inductive-capacitive (RLC) load is represented in the real-time simulation [27], [32], [33]. However, this is the first known paper to describe in detail a hardware-in-the-loop method for multi-inverter, multi-PCC anti-islanding tests. The platform is demonstrated experimentally in Section III.

Some island tests require the load to resonate at the fundamental frequency with a prescribed quality factor such as 1.0 [6], [7], which intentionally creates a difficult condition for the DER to detect the island. In an island containing a segment of a distribution circuit, the conventional method of calculating the island quality factor [6] does not apply. As part of the PHIL test method, a novel method for calculating the quality factor of an arbitrary network of linear elements in real time is also presented here.

Considerations for complete PHIL test apparatus design make up the bulk of the paper and are discussed in Section II, including the real-time model, the test hardware, and the limitations and challenges of the platform. Experimental results from a study performed using the method are presented in Section III.

II. Anti-islanding test method

A conventional pure hardware anti-islanding test for a single DER requires four components, shown in Fig. 2:

- AC power supply or electric grid connection
- Island switch
- Island load
- Device under test (e.g. inverter-coupled DER)

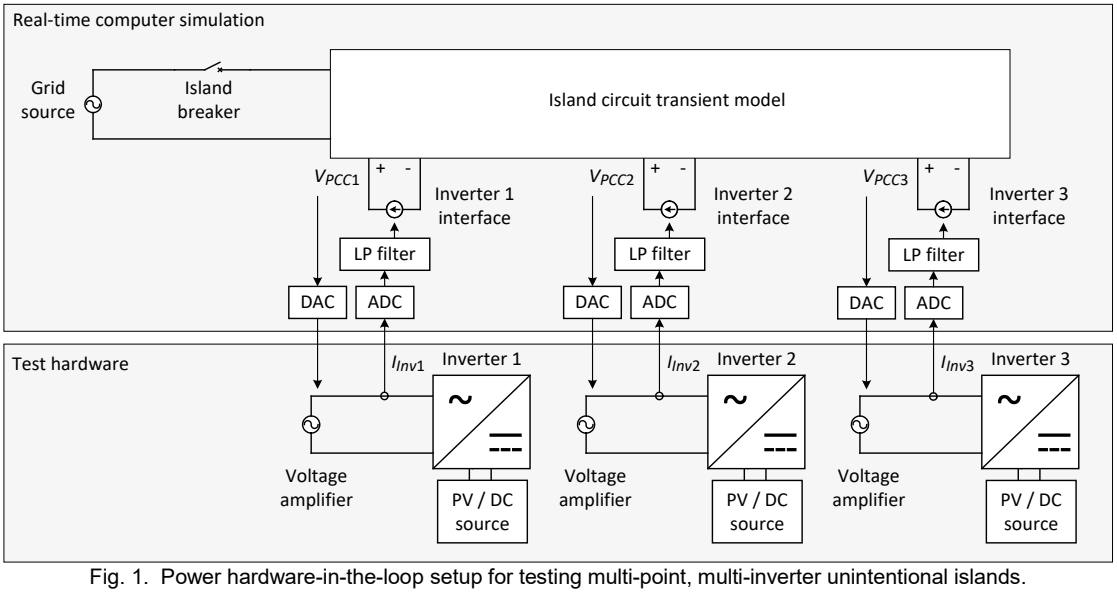

Fig. 1. Power hardware-in-the-loop setup for testing multi-point, multi-inverter unintentional islands.

More DERs and a more complex island circuit can be added to test multi-DER islands. Regardless of the number of DERs, the basic test procedure is as follows:

1. With the DER operating, tune the island load so that it consumes the fundamental frequency real and reactive power output of the DER. If required, the load tuning must also provide the desired quality factor.
2. With the DER and island load running at this steady state condition, open the island switch, creating an island consisting of the DER and the load.
3. Record voltage and current waveforms to measure the time from the opening of the switch to when the DER ceases to energize the island.

While the island circuit shown in Fig. 2 serves well for single-inverter island testing, islands on real electrical distribution feeders may take any of a number of more complicated forms. For the case of a three-DER island, three island circuit topologies are possible, seen in Fig. 3; other topologies would also be possible when considering possible additional load locations. The variable Z (with various subscripts) in Fig. 3 represents the impedances of the various lines in the interconnecting circuit. For islands with more than three DERs, the number of possible topologies expands rapidly. The case of a three-DER island was taken as a test system for development of a multi-DER, multi-point island test platform.

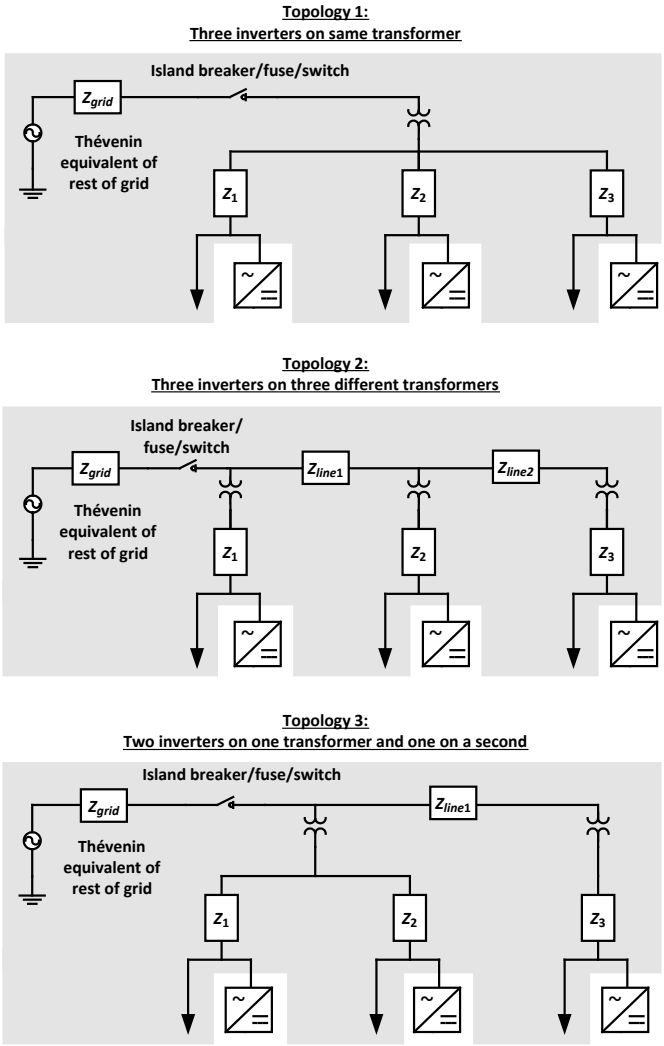

Fig. 3. Island circuit topologies for the three-inverter case. The downward arrows represent load.

A. PHIL island test design considerations

When developing any PHIL system, one must decide which components of the system will be represented in hardware and which will be simulated. Components for which accurate real-time models are available (or can be developed) *can* be represented in simulation. It is often preferable to represent as much as possible in simulation (as long as reliable models are available) because simulated components are typically much easier to modify than hardware components. The lines, loads, and transformers that make up a distribution circuit can be modeled with good fidelity and are expensive and time-consuming to physically build, and hence are good candidates to be represented in simulation. Components that cannot be easily modeled, or for which models are not sufficiently validated, should be represented in hardware. For example, the inverters that interface DERs such as PV and storage with the grid often use proprietary anti-islanding control methods for which models may not be available. Even when models are available, the purpose of the anti-islanding test is typically to verify the performance of the real hardware inverters, so using a model may not be appropriate. For these reasons, the anti-islanding test platform presented here represents the inverters under test and the DC sources supplying them in hardware, and simulates the rest of the island circuit including the loads, lines, transformers, and island switch. In Fig. 3, simulated components are shown on a gray background and hardware components are shown on a white background.

This work builds on the single-inverter PHIL anti-islanding test method first developed in [32]. As seen in Fig. 1, the ideal transformer interface method [34] is used to couple the hardware components to the real-time simulation: simulated voltages at the hardware inverter interface locations are converted to analog signals using DACs, and those analog signals are used to drive AC voltage sources acting as voltage amplifiers. Other voltage-type PHIL interface methods would require adding impedances to the hardware circuit [35], and those impedances would become part of the island circuit, which is undesirable.

The hardware inverters under test are connected to the output terminals of the voltage amplifiers, such that those inverters experience voltage dynamics as if they were connected to the circuit in the real-time model. Each output current from the inverters under test is measured, converted to a digital signal using an ADC, passed through a LP filter, and used to command a controlled current source at the inverter interface location within the real-time model. Thus, from the model's perspective, the hardware inverters are effectively part of the model. The net effect is that, while the three inverters in Fig. 1 are connected to three different voltage sources, they interact dynamically with each other through the PHIL model, and also interact dynamically with the model itself as if they were connected to the modeled circuit.

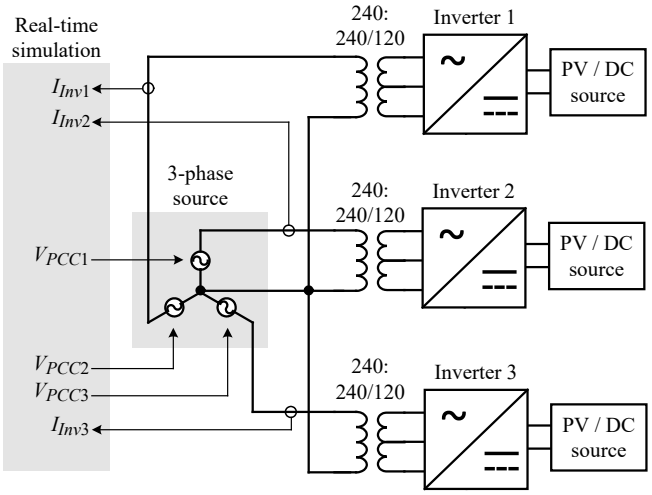

Fig. 4. Three-phase voltage source supplying three single-phase inverters. Transformers not required if inverters do not need neutral connections.

The purpose of the low-pass filter on the measured current signals is to attenuate measurement noise, which can become amplified through the closed-loop system and result in artifacts or instability of the PHIL system [25], [36]. Other methods of stabilizing PHIL systems can be found in the literature [24], [34], [35], but the simple filter used here has proven reliable in this and other work. As implemented here, it is a discrete first-order LP filter with a -3 dB bandwidth of 1.2 kHz. The effect of the phase delay introduced by the filter is discussed below. The 1.2 kHz bandwidth was selected by empirically adjusting the filter: higher bandwidths led to introduction of visible harmonics in the simulated voltage waveform, and lower bandwidths would have caused unnecessary phase delay and attenuation in the PHIL system. Those harmonics were not characteristics of the inverters under test, but rather were artifacts of the PHIL system; as the filter bandwidth was increased further, the harmonic amplitude increased until the PHIL system became dynamically unstable (and software safety limits opened the loop). It would also be possible to analytically estimate the closed-loop transfer function of the PHIL system and design the filter to maximize bandwidth while preserving dynamic stability [36]. However, for this work it is sufficient to determine an appropriate bandwidth for the low-pass filters experimentally through trial and error.

The PHIL test design must also account for the sampling rate (or time step) of the real-time simulation. The sampling rate must provide sufficient time for the real-time simulation to be solved once per time step, but must also be fast enough to capture all relevant dynamics of the system (both the components represented in simulation and those represented in hardware). For anti-islanding tests, two limiting factors may come into play:

1. Anti-islanding controls may operate on the fundamental AC frequency (e.g., by applying positive feedback on frequency or phase angle), on one or more harmonics of the fundamental (e.g., by injecting harmonics to detect grid impedance at harmonic frequencies), and/or at a sub-harmonic frequency (e.g., by modulating reactive power with a period of several line cycles). Some inverters may use more than one anti-islanding method. The real-time simulation must be sufficiently faster than the characteristic frequencies of the anti-islanding methods under test to accurately capture the dynamics of those methods.
2. The discrete nature of the simulation causes the voltage commands sent to the voltage amplifiers, which are ideally sinusoidal (or have only harmonics introduced by the inverters), to have a discrete step-wise characteristic. These small steps in the DAC output are partially filtered by the finite bandwidth of the voltage amplifier but still result in harmonics in the amplifier output at a frequency equal to the reciprocal of the real-time simulation time step (and at higher harmonics to a lesser degree). The smaller the time step, the smaller the magnitude of the harmonics. The impact of these harmonics on the PHIL test may or may not be negligible, depending on their magnitude and the impedances of the inverters under test at these harmonic frequencies.

For these reasons, the fastest feasible real-time simulation sampling rate is generally preferable – it will provide higher-fidelity representation of the true system dynamics and will also reduce the introduction of unintended harmonics.

In addition, the time step of the real-time simulation introduces a delay in the closed-loop PHIL system, which can introduce undesired dynamics and reduce accuracy. The low-pass filters on the ADC output signals introduce additional phase lag on the current signals relative to the simulation voltages; this is often the dominant delay in the system. A unity-gain, phase-lead filter can be applied to compensate for the lag, as in [37].

The maximum sampling rate of the real-time simulation is determined by the ability of the simulation platform to consistently solve the real-time model within one time step while also performing other necessary tasks (e.g. interfacing with DACs and ADCs and writing to memory).

In the test results shown below, the real-time simulation ran with 30 μs time-steps. This provides 555.5 time-steps per 60 Hz line cycle and was fast enough not to introduce appreciable harmonics into the waveforms.

The platform described here could be implemented on any of a number of commercially-available real-time computing platforms. The real-time computer must have at least one DAC and ADC channel per single-phase PCC plus three channels per three-phase PCC; an additional DAC channel is useful for triggering measurement devices. Additional ADC channels may be needed to bring in voltage or current measurements for real-time quality factor estimation, as described in Section II.B. The experiments described below used a single-processor Opal-RT real-time computing system comparable to those available in many industry and university labs. The real-time models were developed in Matlab/ SimPowerSystems and compiled in RT-Lab.

B. Hardware selection considerations

Power hardware required for multi-inverter, multi-PCC island testing includes the inverters under test and an AC voltage amplifier for each PCC. The inverters under test should not use any anti-islanding method that operates on a

frequency higher than the bandwidth of the PHIL system. In the test setup used here, the limiting factor on the PHIL system bandwidth is the 1.2 kHz low-pass filter on the measured current signals; therefore this system would not be expected to reliably evaluate anti-islanding methods operating on a time scale near 1.2 kHz or faster, corresponding to the 20th harmonic of 60 Hz. Many inverters use anti-islanding methods that operate on the fundamental frequency or low-order harmonics; this platform is appropriate for anti-islanding evaluation for such inverters. It is likely possible to modify this platform to enable fidelity at higher frequencies using PHIL stabilization methods such as that described in [36].

The voltage amplifiers used in the PHIL experiment (sometimes referred to as grid simulators) must be capable of amplifying an analog voltage command to produce the voltage waveforms expected at the DER point of common coupling. They should have sufficient bandwidth and slew rate to reproduce the dynamics of the PCC voltage. The experimental results described below were produced using an Ametek MX45-3, which has a voltage slew rate of 0.5 V/μs [38]. The voltage controller bandwidth is not specified, but the unit has been experimentally verified to accurately reproduce frequency content above the 1.2 kHz bandwidth of the low-pass filter, such that the MX45 is not the limiting factor on PHIL system bandwidth.

The voltage amplifier for each hardware-software interface must have the same number of phases as that interface. In the example presented in Fig. 1, there are three single-phase interfaces (one for each inverter under test), so three single-phase voltage amplifiers are needed. For the experimental results presented below, a single three-phase four-wire MX45-3 was used to supply all three hardware interfaces by controlling each phase independently. This allowed the three-inverter, three-PCC experiment to be conducted using a single (three-phase) voltage amplifier, as seen in Fig. 4.

Some single-phase 240 V AC grid-interactive inverters also require a neutral connection between the two power lines (often for voltage sensing purposes only). When supplying such an inverter from a single-phase voltage source, a 240:240/120 transformer can be connected in series to derive a neutral connection, as seen in Fig. 4. If used, this transformer must be accounted for when designing the interconnecting circuit and when calculating the island quality factor, as described below. Some split-phase inverters can be configured not to require a neutral connection using software parameters, which avoids the need for a transformer.

For PHIL unintentional islanding tests, representing the load in the real-time simulation avoids the need for a hardware load bank. In addition, if the hardware load(s) were to be located elsewhere in the island circuit besides at the hardware inverter PCCs, additional voltage amplifiers would be needed to create the load PCC. Representing the load in simulation allows more flexibility in the location, configuration, and tuning of the load, all of which can be easily changed between tests. A simulated load also has advantages when calculating the island quality factor, as described below. In addition, the simulated load could include models of realistic distribution circuit loads that may affect island behavior, such as motor loads. The disadvantage of representing the load in simulation is that any non-idealities or inaccuracies of the simulated load may introduce artifacts or errors into the experiment. The experimental results shown below were produced with the load represented in simulation.

C. Island load tuning

Accurate tuning of the island load helps to create an island that is difficult for the inverters to detect. One way this is accomplished is by tuning the load such that the fundamental frequency real and reactive power flowing through the island switch are nearly zero at the time of island formation. In addition, conventional unintentional islanding tests often use a parallel RLC load tuned to resonate at the nominal AC frequency with a prescribed quality factor (QF), such as $QF = 1.0 \pm 0.05$ [6]. This tends to stabilize the island, again making island detection more difficult.

Thus, careful tuning of the load's real and reactive power and its quality factor are crucial to producing replicable test results. Load tuning is a relatively simple process for conventional single-inverter tests using the equations provided in [6]:

$$quality\ factor \equiv QF = R\sqrt{\frac{C}{L}} = \frac{\sqrt{Q_C Q_L}}{P} \tag{1}$$

where R, L, and C are the effective load resistance, inductance, and capacitance respectively; P is the DER output power; and Q_L and Q_C are the inductive and capacitive reactive power consumed by the load, respectively.

However, for multi-PCC islands, the impedances of the interconnecting circuit must also be accounted for, so (1) no longer holds. Instead, the total island QF can be calculated based on the definition of quality factor: the ratio of stored energy in the island circuit, E_S, to energy dissipated per line cycle, E_D:

$$QF = 2\pi \frac{E_S}{E_D}. \tag{2}$$

The stored energy E_S can be calculated by individually considering the energy stored in each inductive and capacitive element in the island. For a circuit with N inductive elements and M capacitive elements, the total stored energy is the sum of the energy stored in the inductive and capacitive elements, E_{Li} and E_{Cj} respectively, averaged over a line cycle:

$$E_S = \sum_{i=1\ldots N} \left|E_{Li}\right|_{cycle} + \sum_{j=1\ldots M} \left|E_{Cj}\right|_{cycle}. \tag{3}$$

The average energy stored in the i^{th} inductive element with inductance L_i and RMS current I_{Li} is

$$\left|E_{Li}\right|_{cycle} = \tfrac{1}{2} L_i {I_{Li}}^2. \tag{4}$$

Similarly, the average energy in the j^{th} capacitive element with capacitance C_j and RMS voltage V_{Cj} is

$$\left|E_{Ci}\right|_{cycle} = \tfrac{1}{2} C_j {V_{Cj}}^2. \tag{5}$$

If the circuit has H resistive elements, the total energy dissipated per line cycle is the sum of the energy dissipated in each element E_{Rk}, which is equal to the power draw P_k of that element averaged over a line cycle multiplied by the line period:

$$E_D = \tfrac{1}{f} \sum_{k=1\ldots H} \left|P_k\right|_{cycle} \tag{6}$$

where f is the AC frequency. The frequency can be assumed to be at its nominal value because the QF calculation is made

before the island is created. The power draw of the k^{th} resistive element with resistance R_k and RMS voltage V_{Rk} (and RMS current I_{Rk}) is

$$\left|P_k\right|_{cycle} = {V_{Rk}}^2 / R_k = {I_{Rk}}^2 R_k \,. \tag{7}$$

Thus the quality factor can be calculated as

$$QF = \pi f \frac{\sum_{i=1\ldots N} L_i {I_{Li}}^2 + \sum_{j=1\ldots M} C_j {V_{Cj}}^2}{\sum_{k=1\ldots H} {I_{Rk}}^2 R_k} \,. \tag{8}$$

Equation (8) can be implemented in the real-time model to provide a continuously updated display of the quality factor of the island circuit to aid in tuning the load. For an accurate estimate of *QF*, all resistive, inductive, and capacitive elements (both hardware elements and simulated elements) with non-negligible energy storage or dissipation should be included in the calculation. For transformers, core loss, magnetizing inductance, winding resistance, and leakage inductance may need to be included, though the effect of some of these non-idealities may be negligible. Core losses can be captured using (7) by modeling core loss as an equivalent resistive element. Rough approximations of the effects of parasitic elements may provide sufficient accuracy in the *QF* calculation as the energy stored or dissipated in parasitic elements is typically small compared to the energy in the load(s) or voltage compensation capacitors. Once equation (8) has been developed for the circuit topology of interest, its sensitivity to changes in parasitic inductances and resistances can be evaluated. Then informed decisions can be made whether to include or neglect each parasitic element, keeping in mind that the *QF* calculation need only be accurate within about one percent. Often parasitic elements such as transformer magnetizing inductance have a small enough effect on *QF* that they can be neglected. In cases where line lengths and conductor types are known but impedances are not, impedances can be estimated from component data sheets or from sources such as [39]. For hardware elements, measurements of appropriate voltages or currents should be passed into the real-time model for use in the *QF* calculation. The losses in hardware load inductors and capacitors (such as those in Fig. 2) tend to be non-negligible. Impedances outside the island, such as Z_{grid} in Fig. 3, should not be included in the *QF* calculation.

In addition to the real-time calculation of quality factor, it is also useful to calculate the fundamental frequency real and reactive power flowing through the island switch. This helps in tuning the load to ensure that the real and reactive powers flowing through the switch are as close to zero as possible when it is opened.

Some inverters modulate reactive power periodically as part of their island detection scheme. For these inverters, the timing of the island disconnection can have a significant impact on the island duration. The real-time display of real and reactive power flowing through the island switch can be very useful in ensuring that the unintentional islanding test truly captures the worst-case island condition for inverters using this method.

Even with the continuous readouts of quality factor and real and reactive power afforded by the PHIL model, load tuning is substantially more difficult in multi-inverter islanding tests than in single-inverter tests, especially when one or more inverters are performing grid support functions that actively modulate reactive power as a function of voltage, such as volt-var control. A small change in load tuning can result in a small change in voltage at one or more inverter PCCs, which in turn results in a significant change in inverter reactive power output via the volt-var function. This in turn can both change the circuit quality factor and require a new load tuning to balance real and reactive power. Hence load tuning is an iterative process requiring significant care.

The multi-inverter, multi-point island test method described above has several inherent limitations mentioned above that the engineer must consider. If these limitations can be overcome, the techniques described here can be used to experimentally evaluate a wide array of multi-inverter, multi-point island scenarios efficiently and economically, as demonstrated in the next section.

III. Experimental results

Before beginning multi-inverter unintentional islanding tests, ten single-inverter PHIL unintentional islanding tests were run and the results were compared against 60 previously-run conventional (non-PHIL) tests of the same inverter. As seen in Table I, the average island durations and the distributions of island durations were very similar between the two test methods. The differences in duration between the two methods are due to stochastic variations in island detection time and are not statistically significant. The somewhat wider range of durations seen in the conventional tests is accounted for by the larger sample size.

TABLE I
Island Durations in PHIL and Conventional Tests

Test	Mean	Maximum	Minimum	Std. dev.
PHIL	230 ms	512 ms	88 ms	151 ms
Conventional	224 ms	668 ms	68 ms	114 ms

In addition, the voltage and current waveforms were qualitatively similar between the two test methods. Fig. 5 shows example waveforms for inverter output current, I_{inv}, and inverter terminal voltage, V_{inv}, for both test methods. Both tests examined similar scenarios: the inverters were programmed for the voltage and frequency ride-through settings that inverters interconnecting in California will soon be required to be capable of [1], and the load was tuned for a quality factor of 1.0. The variation in durations was due to stochastic factors: linear regression showed no statistically significant variation in duration between conventional tests and PHIL tests.

This comparison to conventional single-inverter tests provided confidence that the real-time model was not introducing significant artificial dynamics that affected the results of the islanding tests. A full validation of multi-inverter PHIL tests against hardware-only tests would require construction of full interconnecting circuits and hence was not performed.

The multi-inverter, multi-PCC island test method was implemented using three split-phase PV inverters from three different manufacturers. The inverter power ratings were 5.0

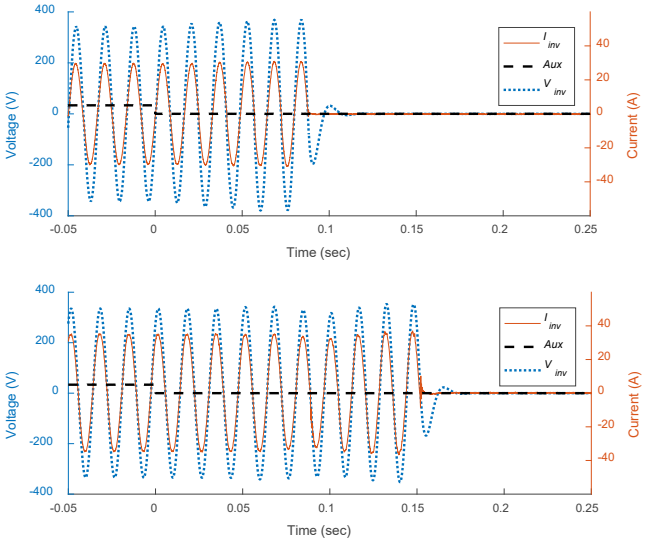

Fig. 5. Inverter voltage and current waveforms for PHIL (top) and conventional (bottom) unintentional islanding tests. The island is created at time t = 0 when the *Aux* signal goes to zero, and the inverter stops energizing the island when I_{inv} goes to zero.

kW, 6.0 kW, and 4.2 kW (referred to as Inverters 1, 2 and 3, respectively). Based on inspection of the inverter output waveforms, none of the three inverters is believed to use higher-order harmonics as part of its anti-islanding scheme. Each inverter was connected to the voltage amplifier via a split-phase transformer as shown in Fig. 4.

The real-time quality factor calculation (8) included all series and shunt impedances in the simulated interconnecting circuit and loads. The transformer shunt impedance values were not published for the hardware transformers used here. Analysis of the quality factor calculation using a wide range of plausible core loss and magnetizing inductance values found their effects to be negligible, so they were not included in quality factor calculations. Transformer conduction loss and leakage inductance were accounted for using transformer rated impedances values.

A series of 224 three-inverter island tests was run following a detailed multi-phase test plan. The tests evaluated various combinations of the following variables:

- The three island topologies seen in Fig. 3 and the location of the load relative to the inverters
- Type and length of distribution impedances making up the island, as summarized in Table II
- Inverter grid-support function settings: volt-var and frequency-watt control settings as shown in Fig. 6. All tests had the inverters set for upcoming California Rule 21 voltage and frequency ride-through requirements [1].

For all tests, the quality factor, as calculated using (8), was held to 1.0 +/- 3%. The full details of the scenarios tested and results are described in [40] (though the details of the test method are not). Due to space constraints, only one multi-inverter island test is described in detail here.

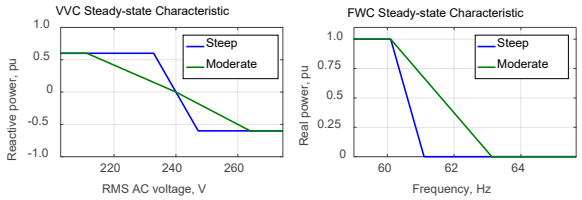

Fig. 6. Volt-var and frequency-watt curves used in island tests.

TABLE II
INTERCONNECTING CIRCUIT ELEMENT IMPEDANCES

Circuit Element	R (Ω)	X (Ω)	R pu*	X pu*
100’ 240 V overhead line	0.0059	0.0026	10	4.5
200’ 240 V overhead line	0.012	0.0052	21	9.0
300’ 240 V overhead line	0.018	0.0078	31	14
100’ 240 V underground line	0.0093	0.0028	16	4.8
200’ 240 V underground line	0.019	0.0055	32	9.6
300’ 240 V underground line	0.028	0.0083	48	14
50 kVA 7200:240 transformer	0.0077	0.015	0.0067	0.013
1 mile 7200 V overhead line	0.040	0.069	0.077	0.134

*On a 100 MVA base, except transformer on 50 kVA base

Fig. 7 shows the inverter voltages and currents for the test with the longest island duration. All inverters were operated at full power. Each inverter was on a different simulated transformer (island circuit topology 2 from Fig. 3), and the simulated island load was aggregated near the island breaker in this scenario. The load was tuned to ensure the desired power balance and quality factor, as calculated in real-time using equation (8). The total island quality factor at the time of island formation was 0.998, and the load component values were R = 5.48 Ω, L = 17.8 mH, and C = 603 µF. The

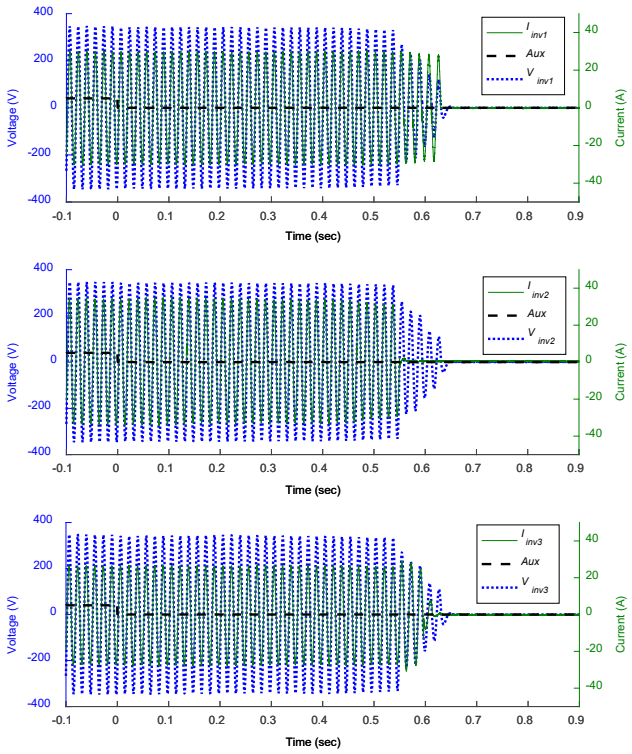

Fig. 7. Inverter voltage and current waveforms from a PHIL unintentional islanding test with three hardware PV inverters at three different points on a simulated island circuit. The island was formed at time 0.

simulated distribution secondary lines connecting two of the inverters used underground cables and the simulated lines connecting the third used overhead lines. Referencing topology 2 of Fig. 3, the impedances used for this test were Z_{grid} = 0.075+j0.10 Ω, Z_{line1} = Z_{line2} = 0.040+j0.069 Ω, Z_1 = 0.012+j0.0052 Ω, and Z_2 = Z_3 = 0.019+j0.0055 Ω. Each inverter also had its volt-var and frequency-watt controls in a configuration that had been previously found to lead to worst-case (though still sub-second) island durations: Inverter 1 had volt-var and frequency-watt disabled, Inverter 2 used the moderate curves from Fig. 6, and Inverter 3 used the moderate volt-var curve and the steep frequency-watt curve.

After the island was formed at time zero, all three inverters ran on for several cycles and tripped within a few cycles of each other, with the last one tripping at 632 ms, well below the two-second maximum required by IEEE 1547.

Fig. 8 shows the fundamental real and reactive power flowing through the island switch just before the switch opened at time zero, forming the island. The load impedance is held constant in this figure. The sharp spikes in reactive power are due to the anti-islanding mechanism of one of the inverters. Another one of the inverters exhibits steady-state fluctuations in real and reactive power output with a four-second period; half of one period is visible in Fig. 8. During the previous half-period, the reactive power flow was positive, such that the 4-second average real and reactive power are near zero, as desired in a well-balanced island. In addition, the switch was opened near the zero-crossing of the 4-second period. As detailed in the test report, creating the island near the zero-crossing of power flow through the switch tended to lead to longer island durations – not a surprising result given that near-zero power flow through the switch indicates good balance between load and generation within the island. In contrast, the timing of the island creation relative to the sharp spikes in reactive power was not found to impact island duration.

A regression analysis of the island durations for the 224 tests found that most of the variables listed above did not have statistically significant impacts on island duration. The only variable that did have a statistically significantly impact was the configuration of inverter grid support settings, and that impact was small (tens of ms). These tests found no significant evidence that variations in the interconnecting circuit configuration affect the durations of multi-inverter, multi-PCC islands. In addition, no island duration exceeded 700 ms (well within the two-second limit), and durations were no longer than those of single-inverter islands with the same inverters. Note that these findings cannot necessarily be extrapolated to greater numbers of inverters or other combinations of inverters.

Detailed test results and conclusions can be found in the authors' public report [40]. The focus of this paper is to describe the PHIL test methodology.

IV. Conclusion

This is the first known work to describe in detail a PHIL anti-islanding test method for multi-DER, multi-point islands. The method enables rapid, flexible testing of a wide variety of multi-point island scenarios, a task that would be painstaking and expensive using conventional test techniques. This paper details test design considerations for applying PHIL techniques to anti-islanding testing. It also discusses several limitations of the technique, most importantly that the PHIL system bandwidth must be sufficiently high to capture all relevant dynamics, which may be challenging in the case of island detection methods that operate well above the fundamental frequency. Experimental results produced using the proposed method, an example of which is presented here, investigated a large number of island circuits and found no problematic island durations. The general approach used here could be expanded in future work to incorporate other elements of concern, such as different types of loads and different types of generation. Additional generators and loads could be represented either within the real-time simulation (if detailed models are available) or in hardware (if detailed models are not available), subject to the limitations described in this paper. It is expected that this test method, and future iterations of it, can be used to help address utility concerns around unintentional islanding.

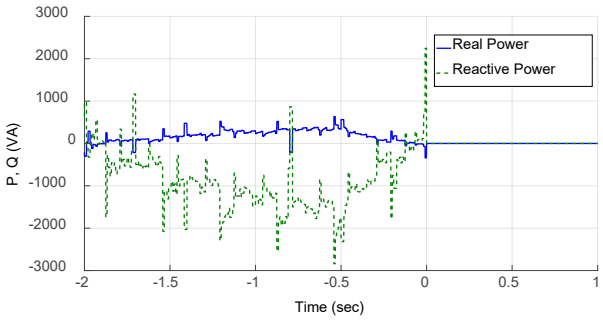

Fig. 8. Fundamental real and reactive power flowing through the island switch in the seconds leading up to the test shown in Fig. 7.

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