SAND2017-8690C

IRDS Beyond CMOS Workshop:

Connecting Emerging Devices to Circuits and Architectures

Introduction and Overview

International Roadmap for Devices and Systems

July 2017

Beyond CMOS Mission and Scope

Mission

- Identify beyond-CMOS devices for information processing and storage to enable novel computing paradigms beyond the capabilities of conventional CMOS technologies and architectures.

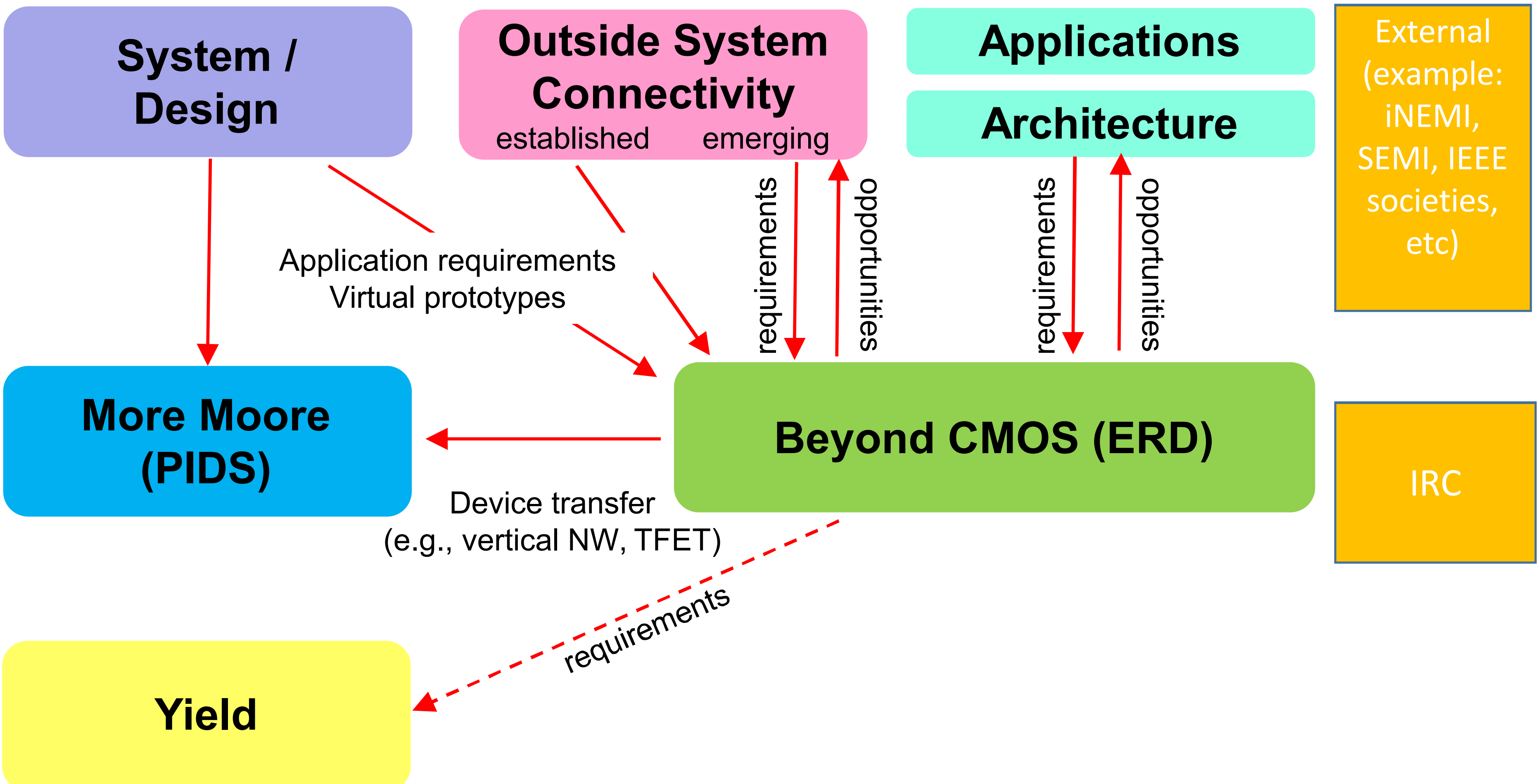
BC Scope

- The Beyond CMOS chapter will identify research opportunities for beyond-CMOS devices to enable high-performance computing, energy-efficient computing, non-von-Neumann architectures, and alternative computing paradigms (e.g., cognitive computing, quantum computing, *etc*.). Included are novel devices for information processing, sensing, and communication, novel memory and storage devices, and devices to enable functional diversification ("more than Moore"). The chapter will assess devices for different applications with recommendations of the most promising candidates and **map emerging devices with novel architectures to identify research opportunities for co-optimization**.

Team Members (Still Growing)

Member Name	Organization	Region
Geoffrey Burr	IBM	USA
An Chen	IBM/SRC	USA
Shamik Das	MITRE	USA
Matt Marinella	Sandia	USA
Paul Franzon	NCSU	USA
Erik DeBenedictis	Sandia	USA
Titash Rakshit	Samsung	USA
Douglas Holmes	BAH	USA
Sapan Agarwal	Sandia	USA
Shashi Paul	De Montfort University	Europe
Hiroyuki Akinaga	National Institute of Advanced Industrial Science and Technology (AIST)	Japan
Masami Hane	Renesas Electronics Corporation	Japan
Tetsuo Endoh	Tohoku University	Japan
Takahiro Shinada	Tohoku University	Japan
Toshiro Hiramoto	University of Tokyo	Japan
Norikatsu Takaura	Hitachi, Ltd.	Japan
Tohru Tsuruoka	National Institute for Materials Science (NIMS)	Japan
Akira Fujiwara	Nippon Telegraph & Telephone Corp.	Japan
Peper Ferdinand	National Institute of Information and Communications Technology (NICT)	Japan
Kiyoshi Kawabata	Renesas Electronics Corporation	Japan
Shintaro Sato	Fujitsu Lab	Japan
Kojiro Yagami	Sony Semiconductor Solutions Corporation	Japan
Yoshihiro Hayashi	Renesas Electronics Corporation	Japan
Shinichi Takagi	University of Tokyo	Japan
Satoshi Kamiyama	Tokyo Electron Limited	Japan

IRDS "Focus Teams"



IRDS 2017 BC Chapter Components

Beyond CMOS

Emerging memory and storage devices

- Memory devices
- Selector devices
- Storage class memory devices

Emerging logic and info. processing devices

- CMOS extension
- Beyond-CMOS charge-based
- Beyond-CMOS non-charge-based

Emerging application areas

- Neural computing
- Big data analytics
- Approximate and stochastic computing
- Hardware security
- Low-temperature electronics
- IoT

Emerging device and architecture interface

- Map Emerging architecture to suitable devices
- Define benchmarks, figure of merits (FOMs) and key challenges

Assessment

- Key FOMs
- Methodologies for quantitative benchmarking

IRDS Emerging Memory

Challenges for ReRAM/CBRAM:
Relative Maturity
Reliability/Mechanisms

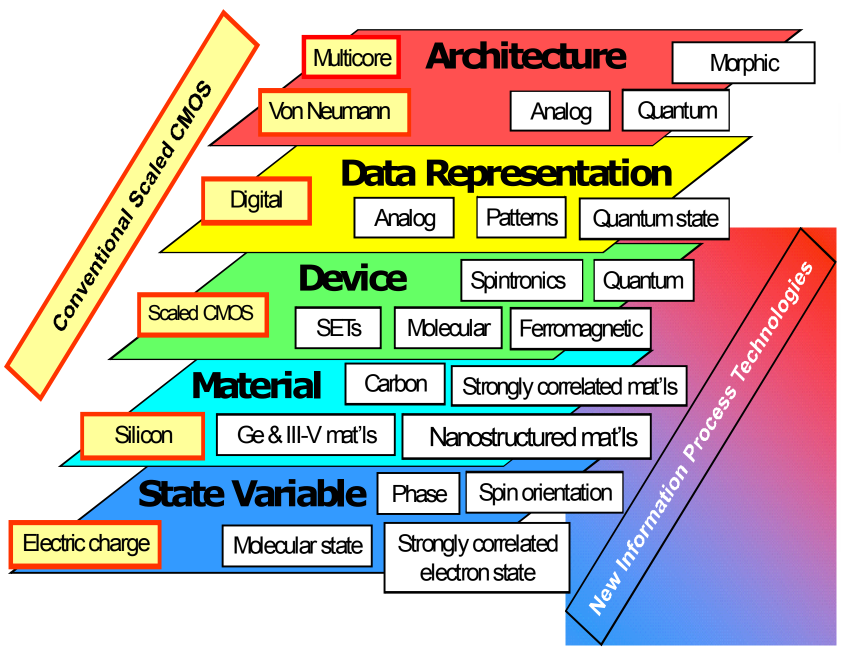
	DRAM	NAND Flash	PC-RAM	STT-MRAM	FeRAM	ReRAM	CBRAM
Maturity	Production (20 nm)	Production (16 nm)	Production (45 nm)	Production (65 nm)	Production (180 nm)	Production (180 nm)	Production (180nm)
Min device feature F (nm)	20	16	<10	16	28 nm	5	20 (5 est.)
Density (F^2)	6	10 (single layer)	4	8-20	22	4	4
Write Time (ns)	< 10	10000	50	13	<100	2	2
Write Energy (pJ/bit)	0.005	100	6	4	270	<1	<1
Endurance (W/E Cycles)	$>10^{16}$	10^4	$>10^9$	10^{12}	10^{14}	10^{12}	10^{10}
Retention	64 ms	1 - 10 y	> 10 y	weeks	> 10 y	> 10 y	> 10 y
Stackable	No	Yes	Yes	No	No	Yes	Yes
Process complexity	High/FE	High/FE	Low/BE	High/BE	High/BE	Low/BE	Low/BE

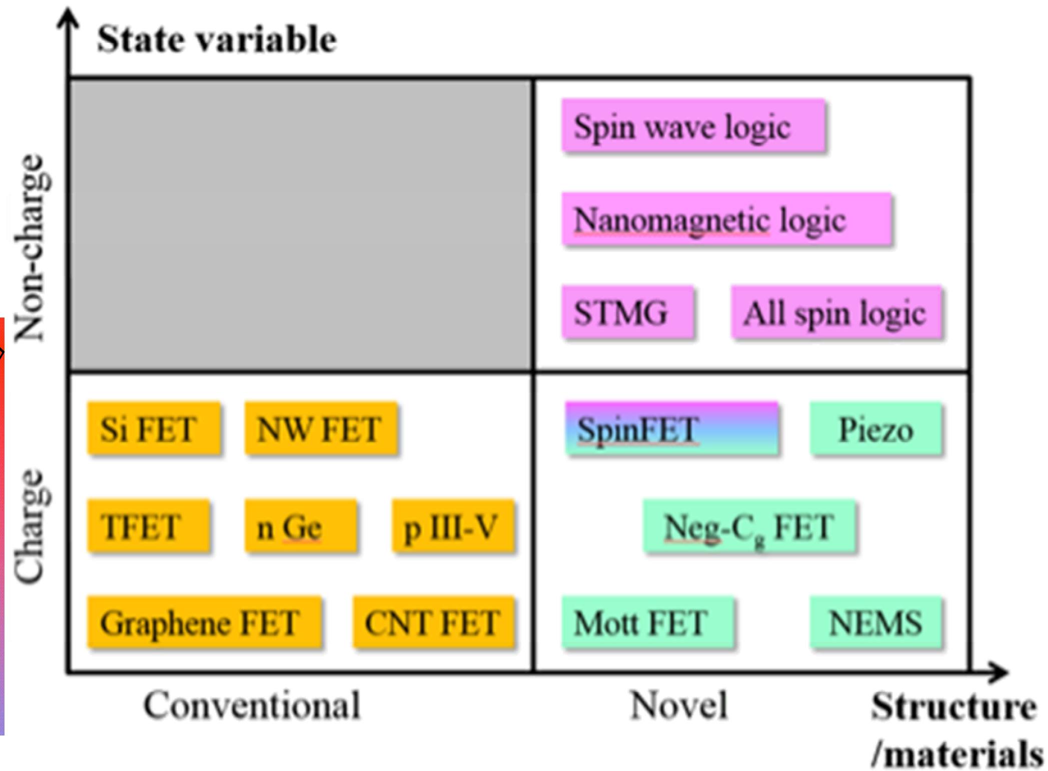
Challenges for PCM:
High erase current → Poor endurance

Challenges for STT-MRAM: Balancing Retention/Scaling/Temperature/Write current

IRDS Emerging Logic

A Taxonomy for Nano Information Processing Technologies

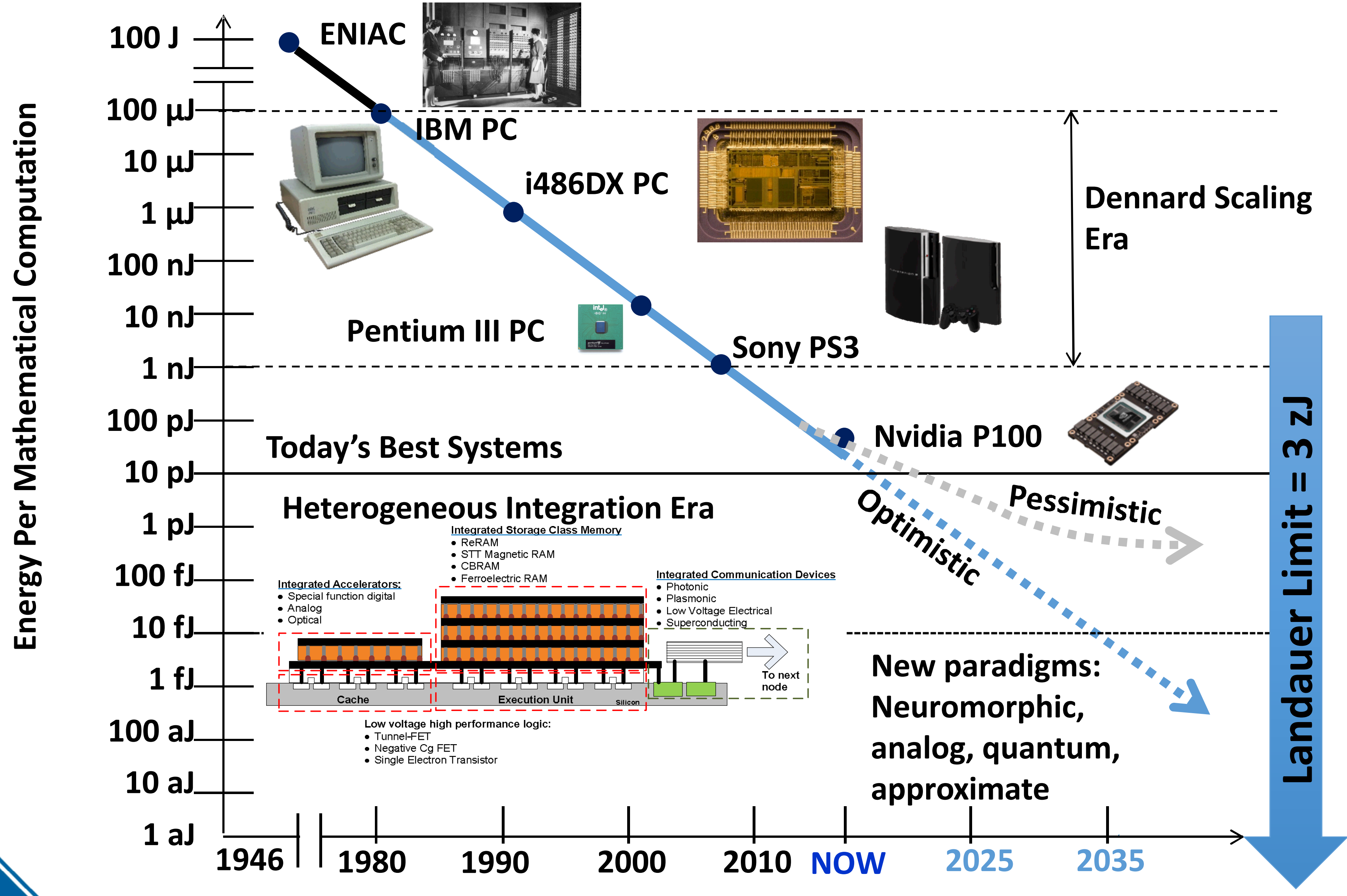




Workshop Overview

Connecting Emerging Devices, Circuits, and Architectures

Evolution of Computing Machinery



Workshop Goals

- Overarching goal: continue the improvement in computing performance, efficiency, and cost for decades
- CMOS scaling is no longer providing exponential gains in computing performance, performance/watt, or performance/area
- Emerging devices offer interesting new opportunities
- Device, circuit, and architecture communities are working toward different goals
- How can we better synergize the development of emerging devices with new circuit and architecture opportunities to ultimately enable significant gains in computing?
  - This is why we're having this workshop!

Circuit Questions

- What is the proposed circuit-block's main function and how does it fit into a system?
- How is this function implemented in CMOS? What are the relevant benchmarks for the CMOS version? What measurable advantage could the proposed block have over a CMOS version? Example benchmarks include improved performance per watt, energy per operation, energy-delay product. Circuit-level and architecture/chip level improvements should be discussed if possible.
- What system level gains and/or new functionality would be enabled by the proposed circuit block?
- Which emerging research devices are required to enable this circuit-block?
- What device properties are required for the proposed circuit-block to provide a significant advantage over CMOS?
- What are the key factors in device performance that must be addressed to make this block technologically viable?

Device Questions

- What is the proposed device's electrical functionality? What are the unique properties that are superior to a standard commercially available device (i.e. CMOS, EEPROM, DRAM)?
- Which circuit-blocks, architectures, and applications are driving development of this device?
- What are the key technical metrics by which this device currently is benchmarked? What are the current state of the art values in this device technology?
- What are the physical limits of this device technology?
- What are the major challenges to bringing this device to widespread commercial viability?

EXAMPLE OF CIRCUIT-DEVICE MAPPING

	CNT-FET	NC-FET	STT oscillator	RRAM	STTRAM	……
Conventional logic blocks						
Analog VMM (vector matrix multiply)						
Simple block FPAA (field-programmable analog array)						
True random number generator (TRND)						
Coupled oscillators						
Magnetic CNN						
TCAM						
Physical unclonable function (PUF)						

Every cross-point in the matrix quantifies the connection between the specific device and architecture: applicability, feasibility, strength/weakness measure, …

Thursday Agenda

Thursday, July 6, 2017

8:00 - 8:30 AM	Breakfast and Check in (Las Cruces Room)
8:30 - 9:00 AM	IRDS Overview, Sandia Welcome, DOE Beyond Moore Vision—Paolo Gargini, Rick McCormick
9:00 - 9:30 AM	ERD Overview and Goals for Architecture Section—Matt Marinella, ERD
9:30 - 10:00 AM	Applications/Circuit Blocks for Neuromorphic Computing—Borna Obradovic, Samsung
10:00 - 10:30 AM	Analog VMM for Neural Circuit Block/Architecture—Geoff Burr, IBM
10:30 - 11:00 AM	Break
11:00 - 11:30 AM	Resistance Switching Devices for Analog VMM and Neural Computing —J. Joshua Yang, University of Massachusetts
11:30 - 12:00 PM	Dot Product Engine: Circuit Architecture and Devices—John Paul Strachan, HP Labs
12:00 - 12:30 PM	Memristive Hardware Accelerators: From Machine Learning to High Performance Linear Algebra —Engin Ipek, University of Rochester
12:30 - 1:30 PM	Lunch
1:30 - 2:00 PM	Spin Torque Nano Oscillator Based Non-Boolean Computation—Kaushik Roy, Purdue University
2:00 - 2:30 PM	Magnetic CNN Circuit Benchmarking— Azad Naeemi, Georgia Tech University
2:30 - 3:00 PM	Magnetic Devices and Architectures— Jianping Wang, Steven Koester, University of Minnesota
3:00 - 3:30 PM	Break
3:30- 4:00 PM	Adiabatic Energy-Recycling and Charge-Conserving Mixed-Signal Arrays for Massively Parallel Cognitive Computing —Gert Cauwenberghs, University of California San Diego
4:00 - 4:30 PM	Field Programmable Analog Array Technology—Jennifer Hasler Group, Georgia Tech University
4:30 - 5:00 PM	Computing With Networks of Coupled Dynamical Systems Based on Insulator-Material Transitions — Arijit Raychowdhury, Georgia Tech University
5:00 - 5:30 PM	Non-von-Neumann Application-Specific CMOS Using Computer to Solve Combinatorial Optimization Problems —Masanao Yamaoka, Hitachi
5:30 - 6:00 PM	Materials Challenges for Non-silicon Hardware—Supratik Guha, University of Chicago
6:00 - 7:30 PM	Dinner Reception (Zuni Terrace—Poolside)
7:30 - 9:00 PM	Evening Discussion
9:00 PM	Adjourn

Friday Agenda

Friday, July 7, 2017

8:00 - 8:30 AM	Breakfast and Check in (Las Cruces Room)
8:30 - 9:00 AM	Applications—Erik DeBenedictis, Sandia National Laboratories
9:00 - 9:30 AM	Emerging Devices and Architectures—Paul Franzon, North Carolina State University
9:30 - 10:00 AM	Physically Uncloneable Functions and Content Addressable Memory —Dimitri Strukov, University of California Santa Barbara
10:00 - 10:30 AM	Random Number Generator—Kerem Camsari, Purdue University
10:30 - 11:00 AM	Memristor-Based Neural Computing—Dhireesha Kudithipudi, Roshester Institute of Technology
11:00 - 11:30 AM	Content Addressable Memory—Tarek M. Taha, University of Dayton
11:30 - 12:30 AM	Closing Discussions—All
12:30 PM	Adjourn

Thanks for being here!!

Questions?

Let's Get Started!!

Extra Slides

Challenges

- Scale volatile and nonvolatile memory technologies to replace SRAM and FLASH in appropriate applications.
- Extend ultimately scaled CMOS as a platform technology into new domains of application.
- Continue functional scaling of information processing technology substantially beyond that attainable by ultimately scaled CMOS. Enable new computing paradigms by device technology breakthroughs.
- Develop materials and devices to enable more-than-Moore solutions.

Potential Solutions

- Emerging memory and storage devices
  - Novel memory devices
  - Selector devices
- Emerging Logic and information processing devices
  - CMOS extension and beyond-CMOS devices
- Emerging application areas
  - Low-temperature electronics
  - Emerging devices for IoT
  - Emerging devices for hardware security
- The interface between emerging architectures and devices
- Assessment