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# High-Resolution Characterization of Josephson Junctions and Magnetic Multilayers for Low-Power, Superconducting Logic and Memory Devices

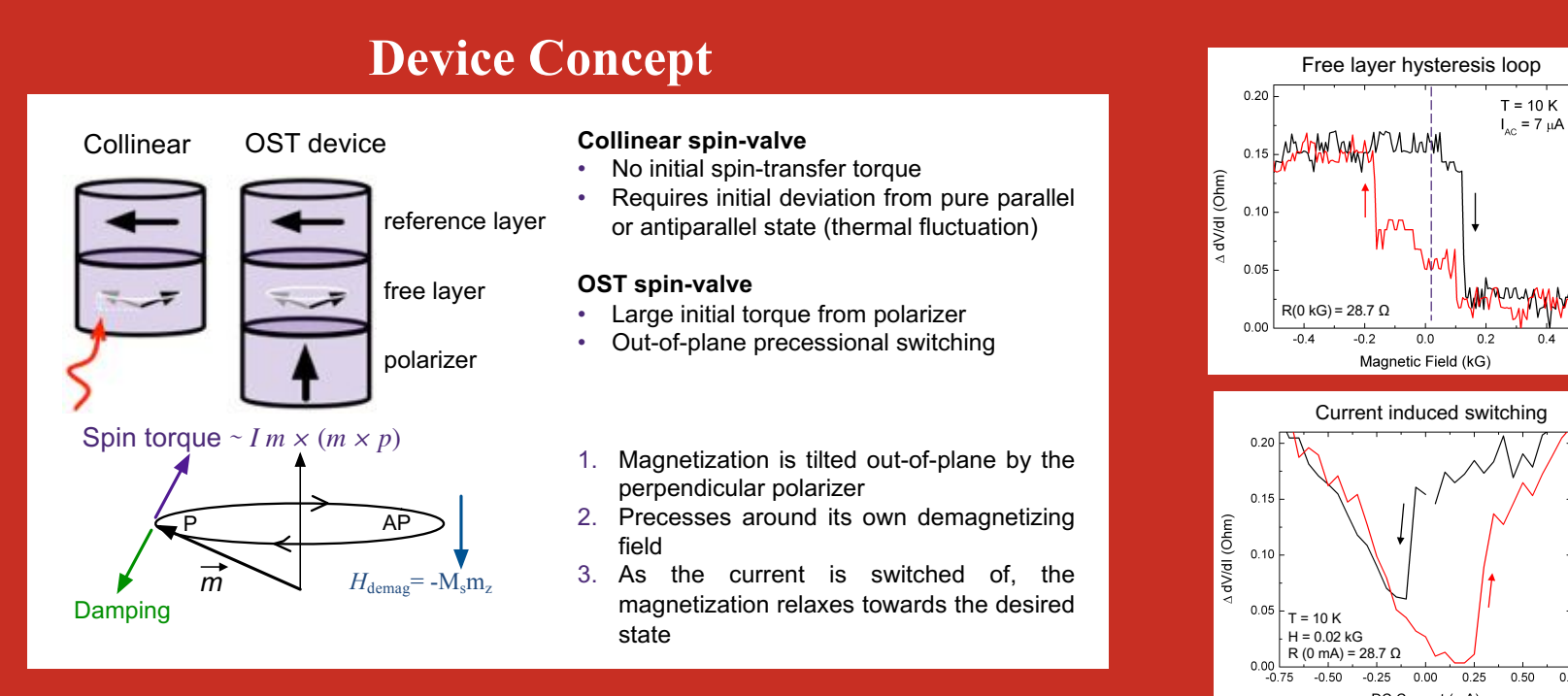
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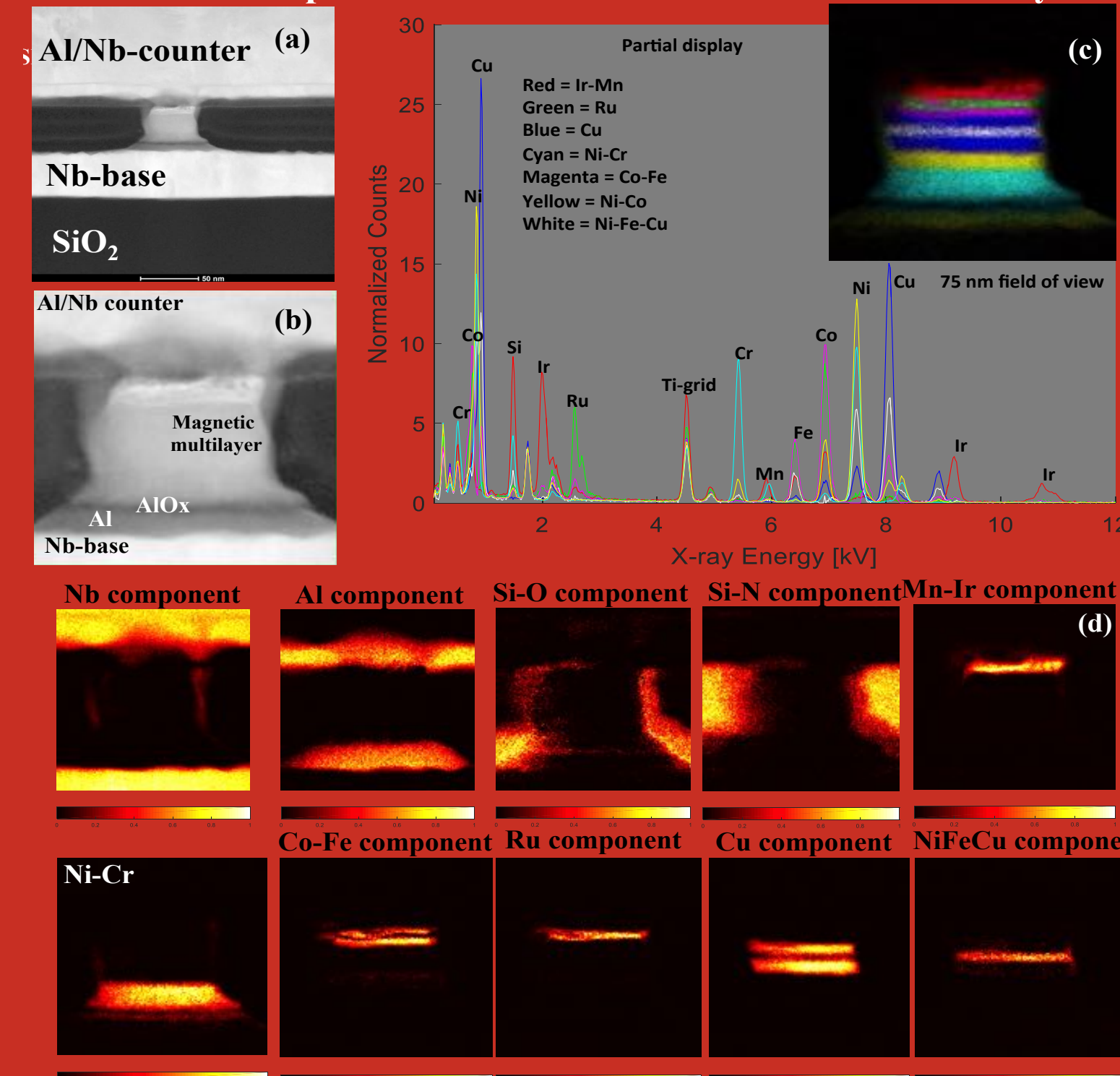
## SCE for High-Performance Computing Presents a Significant Challenge to State-of-the-Art SCE Yield

- Scaling of both logic and memory requires high yield fabrication and processing
- High yield requires uniform device characteristics
- Device characteristics depend upon properties of nanometer-scale thin films
- Microanalysis (structure, morphology, chemical composition) at these length scales can provide guidance to fabrication and processing
- Scanning transmission electron-beam microscopy (STEM) combined with energy dispersive x-ray spectroscopy (EDS) allows characterization of these parameters at the required length scales

## Template for Cryogenic Spin Transfer MRAM devices influences performance

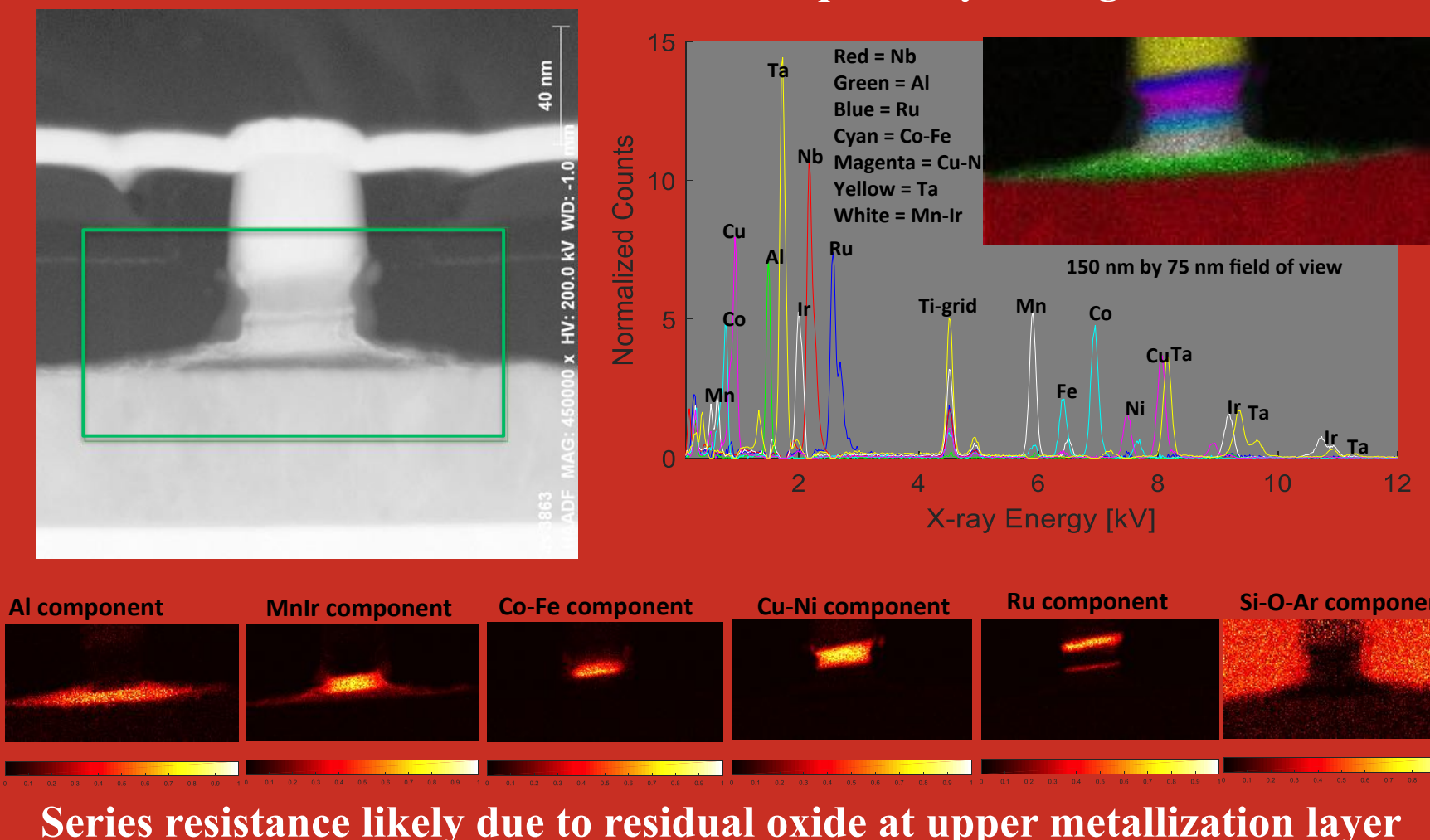


STEM/EDS : smooth, continuous, crystalline, nm-scale layers grow on Al-AIOx template with minimal interdiffusion between layers



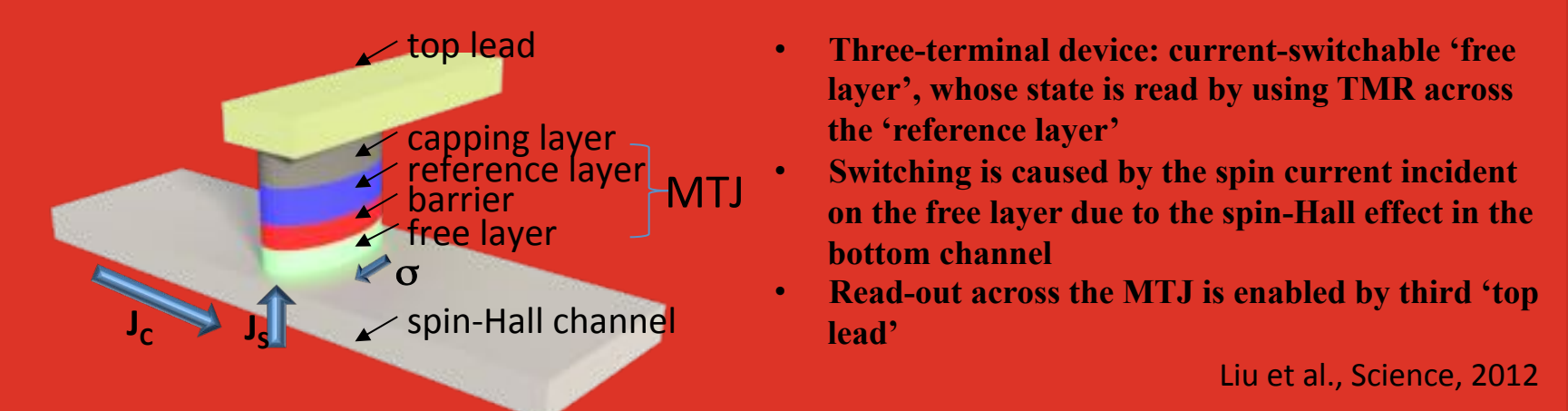
BUT: Thin AIOx adds problematic series resistance

STEM/EDS: Absence of AIOx layer and alternative layer stack results in some Al interdiffusion and subsequent layer roughness



Series resistance likely due to residual oxide at upper metallization layer

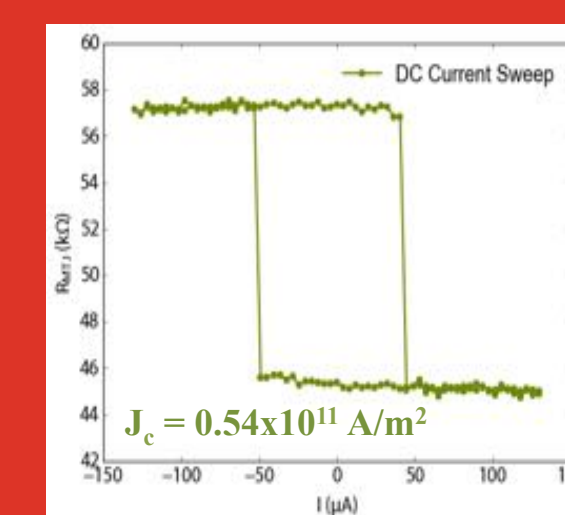
## Template for Cryogenic Spin Hall Effect devices impacts layer roughness



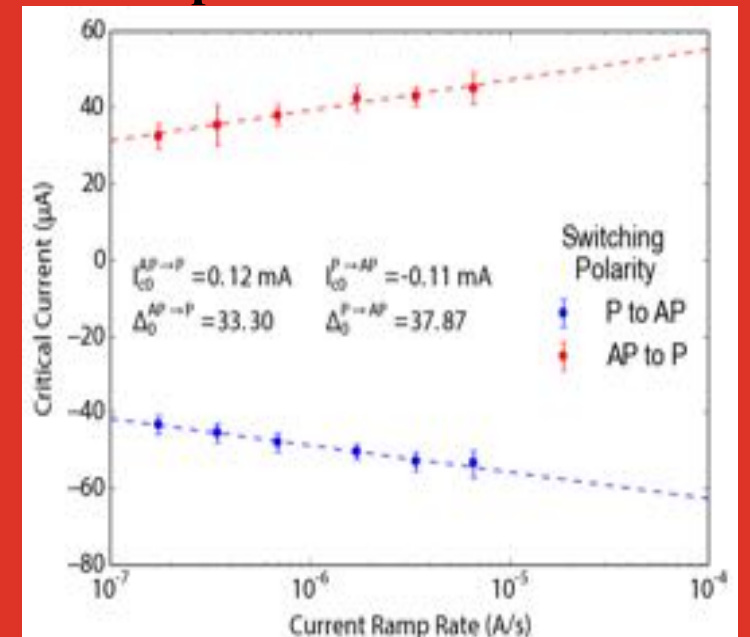
- Three-terminal device: current-switchable 'free layer', whose state is read by using TMR across the 'reference layer'
- Switching is caused by the spin current incident on the free layer due to the spin-Hall effect in the bottom channel
- Read-out across the MTJ is enabled by third 'top lead'

Liu et al., Science, 2012

DC spin torque switching curve for W based CSHE device

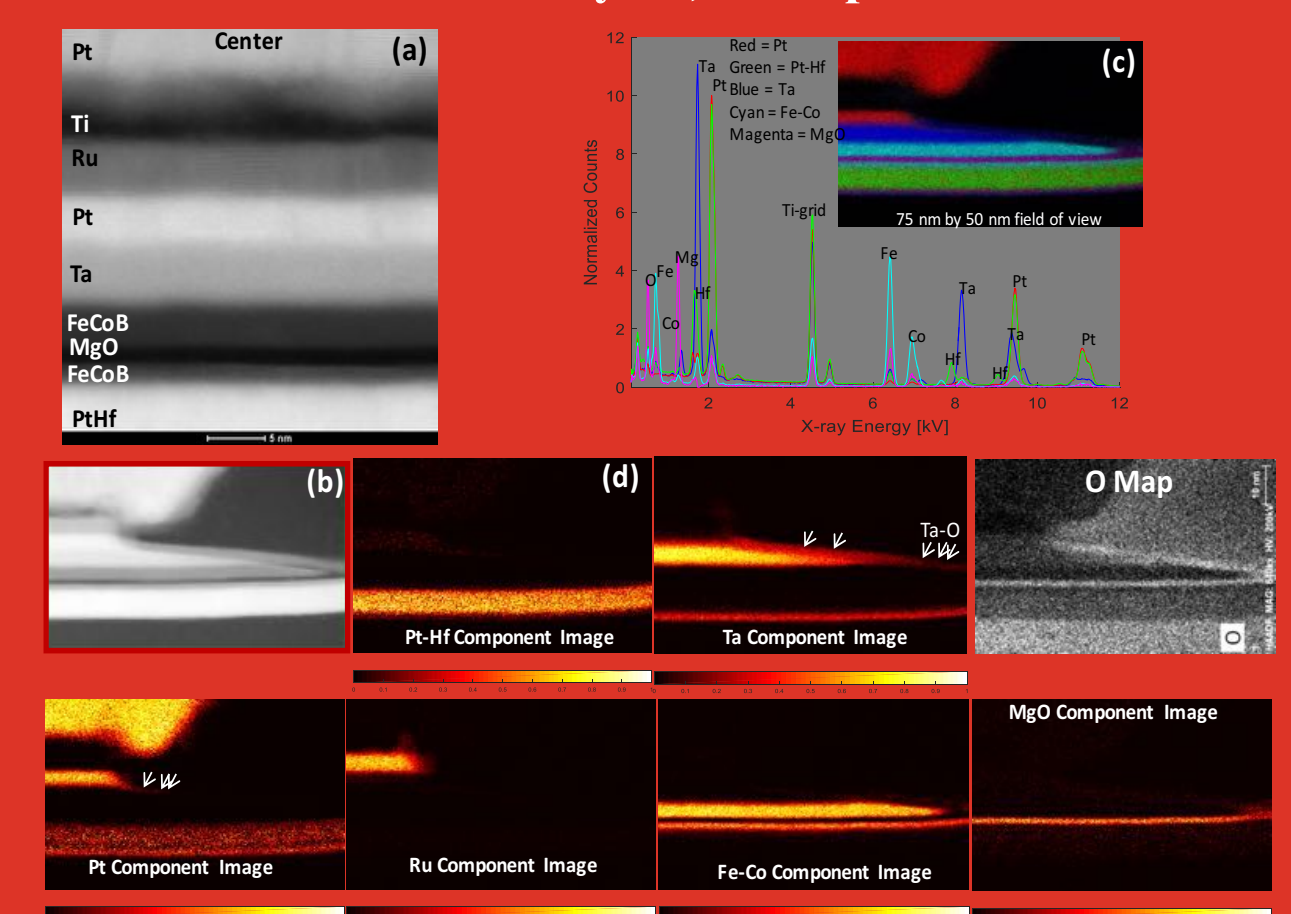


Ramp Rate Measurement

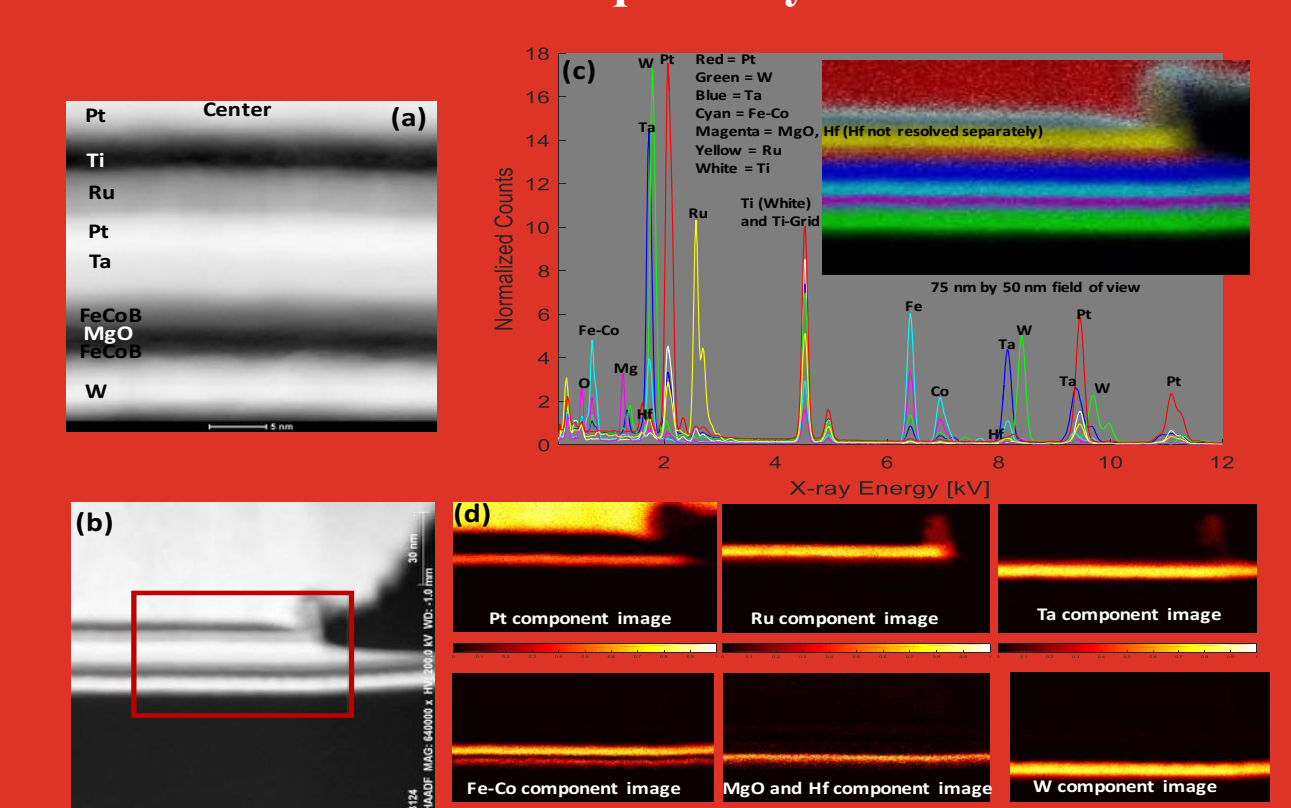


$I_c \approx 40 \mu A$  expected for optimized channel

STEM/EDS : smooth, continuous, crystalline, nm-scale layers grow with minimal interdiffusion between layers, some preferential side-wall etching

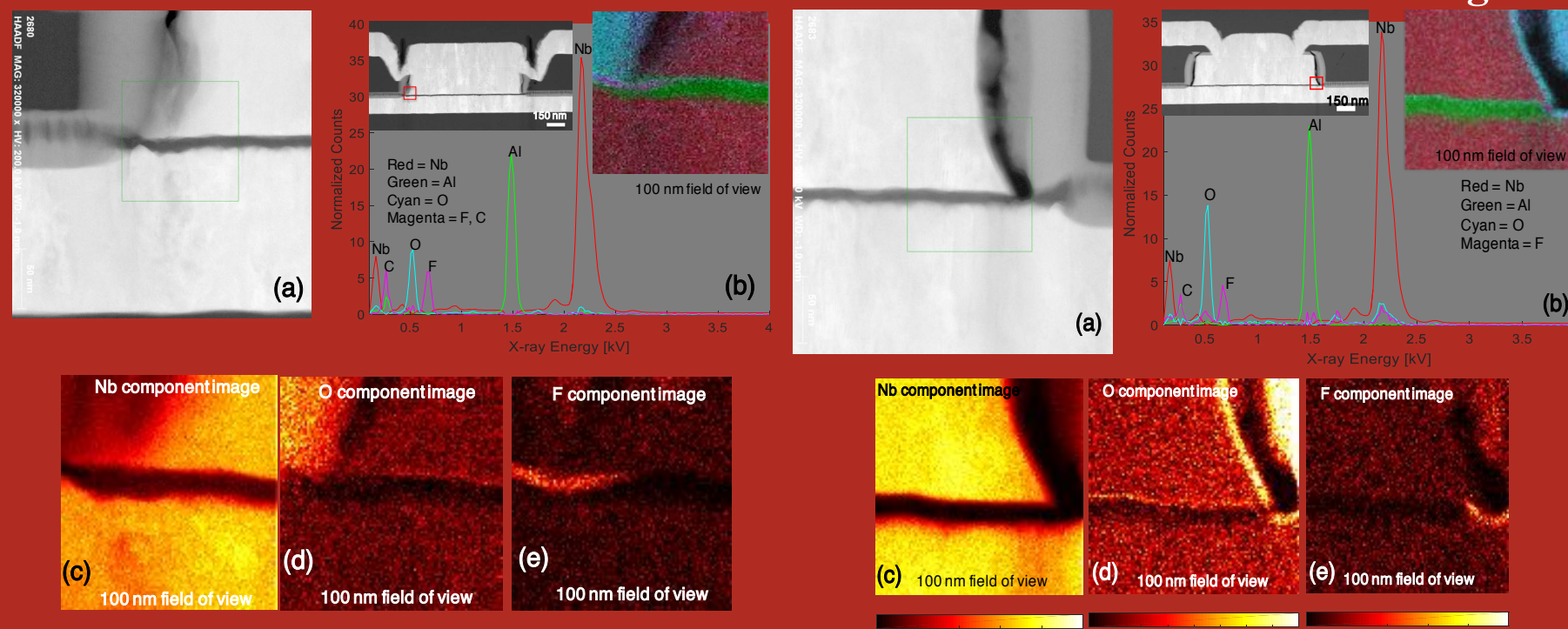


STEM/EDS : alternative W template introduces additional roughness to subsequent layers



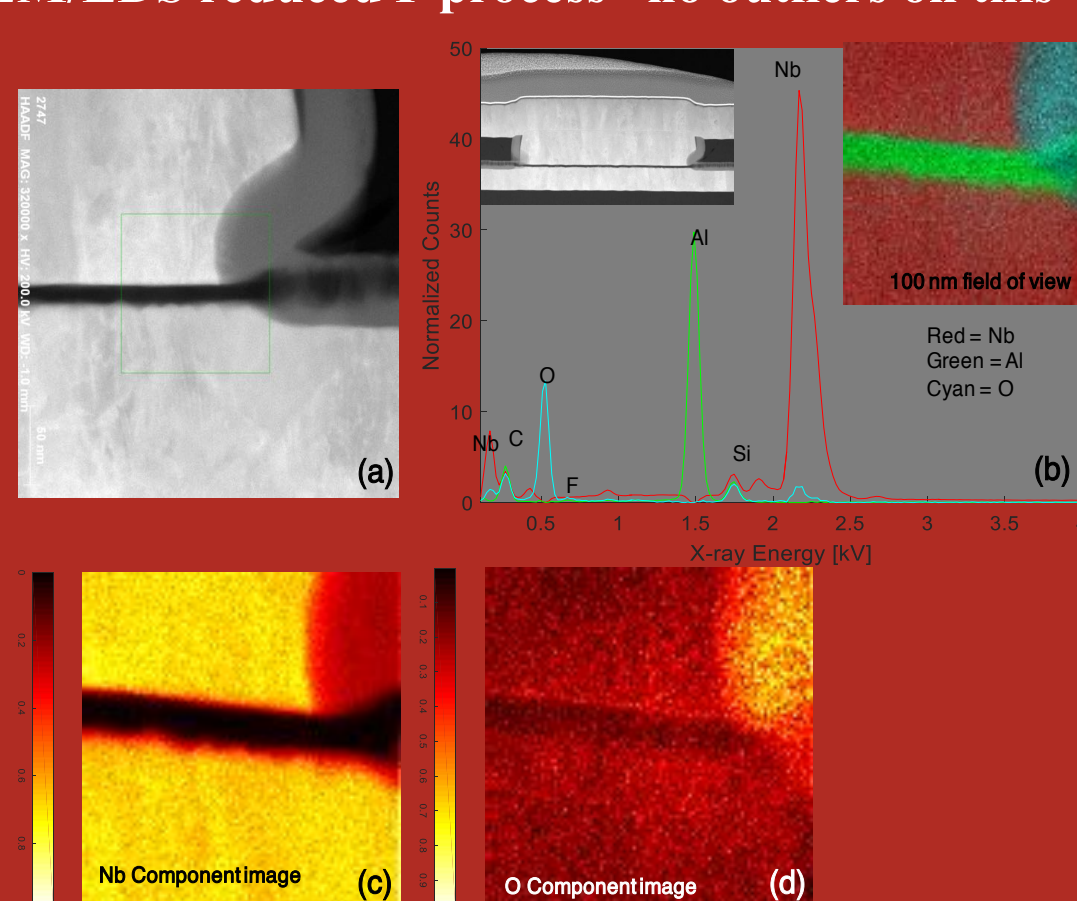
## Presence of contaminants in active area of Nb/Al-AIOx/Nb JJs correlate with electrical properties – compare “control” to “outlier” JJ

STEM/EDS “Outlier” – Low R



F observed in active JJ area correlates to low R for outlier JJs

STEM/EDS reduced F process – no outliers on this wafer



No F observed in active JJ area or at interface with anodized sidewall

**Conclusion:** FIB/STEM/EDS analysis of morphology, structure, chemical constituents can provide insight into variation in properties among specific devices and guide changes in fabrication and processing

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