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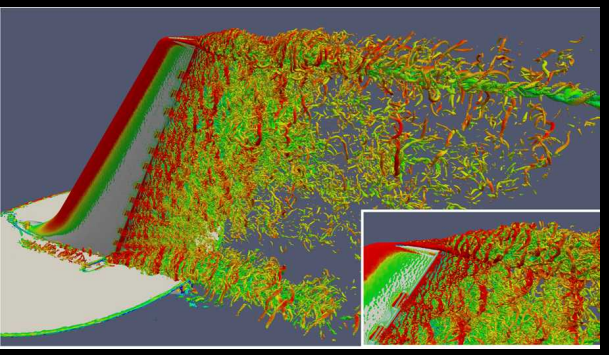
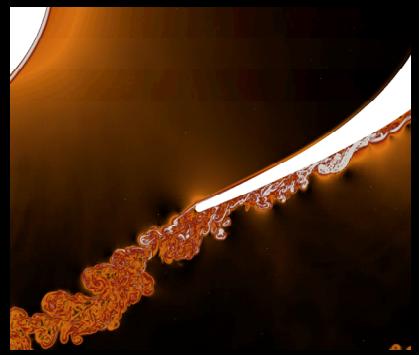
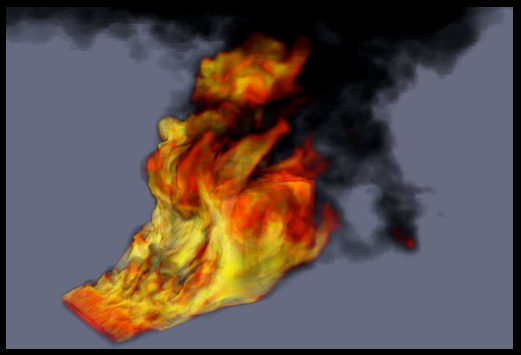
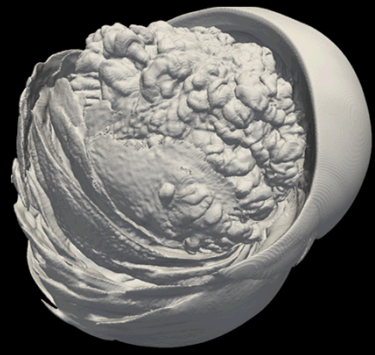

High Performance Visualization in the Many-Core Era

Kenneth Moreland Sandia National Laboratories

Computing@PNNL Seminar

August 11, 2017

CCR Center for Computing Research

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Acknowledgements

- This material is based upon work supported by the U.S. Department of Energy, Office of Science, Office of Advanced Scientific Computing Research, under Award Numbers 10-014707, 12-015215, and 14-017566.
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- **Thanks to many, many partners in labs, universities, and industry.**

Basics of Visualization

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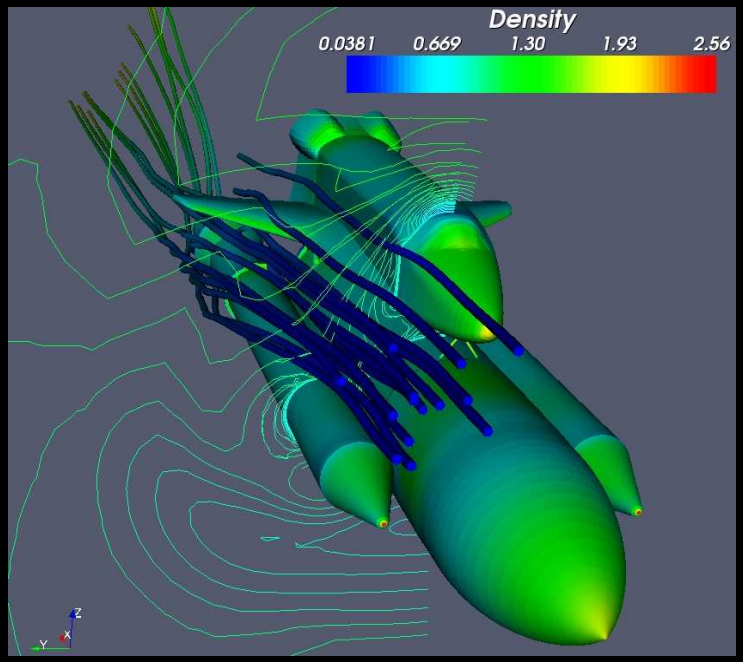

Visualization is Not Just Rendering

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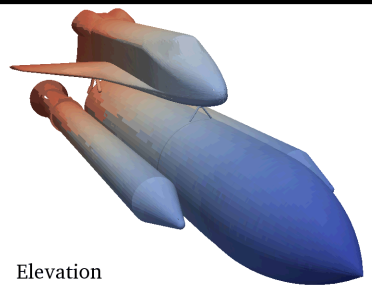
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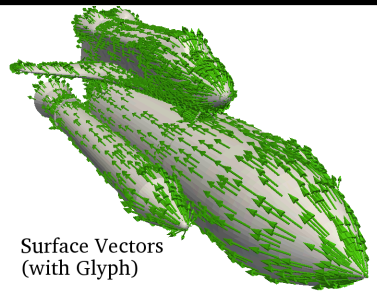
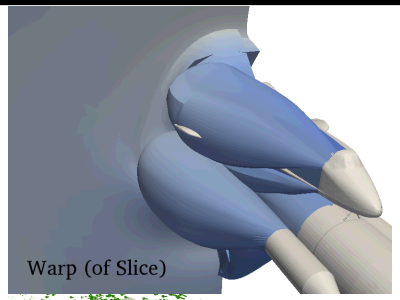
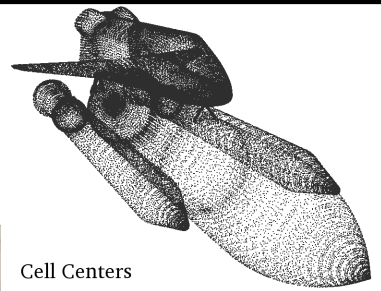

Surface Vectors (with Glyph)


Warp (of Slice)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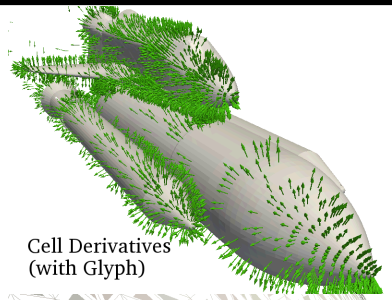
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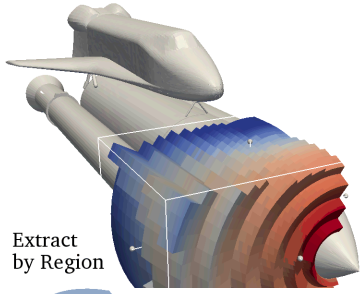
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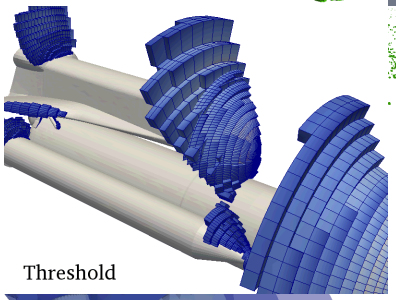
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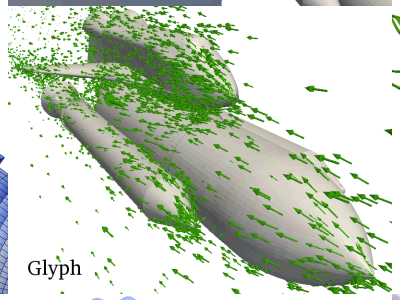
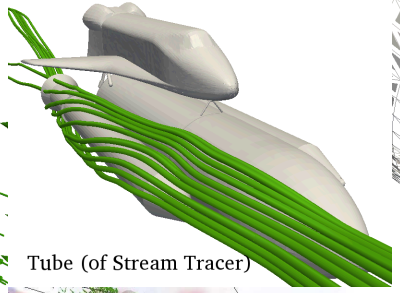
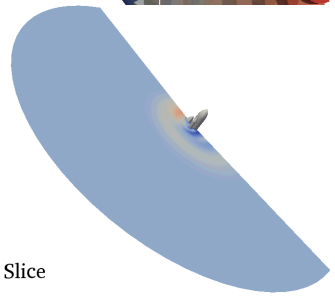

Glyph


Tube (of Stream Tracer)


Shrink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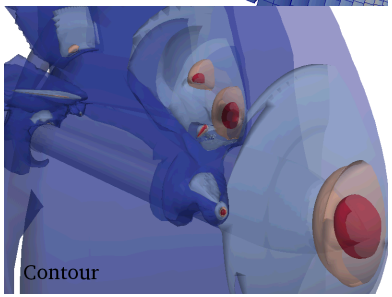
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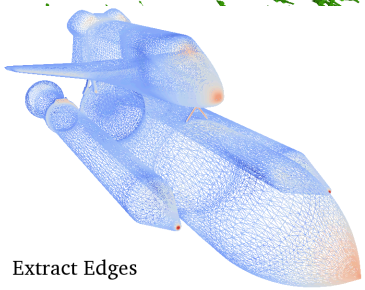
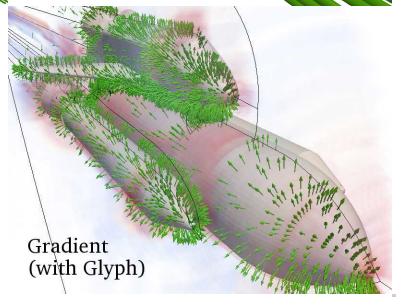
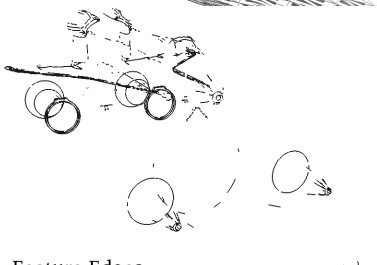

Extract Edges


Gradient (with Glyph)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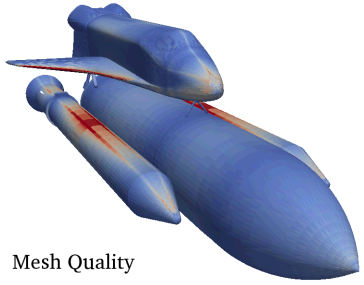
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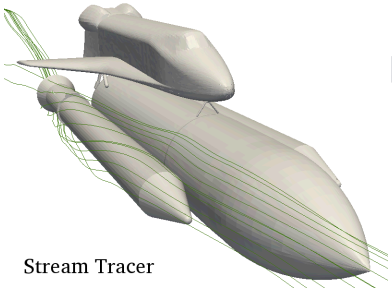
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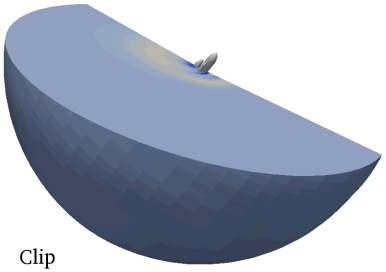
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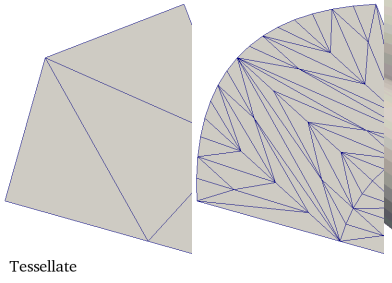
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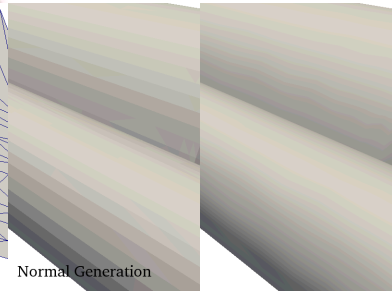
Normal Generation


A Brief History of ~~Time~~
Interactive Visualization

The Big Iron Era (circa 1995)

GPU Cluster Era (circa 2002)

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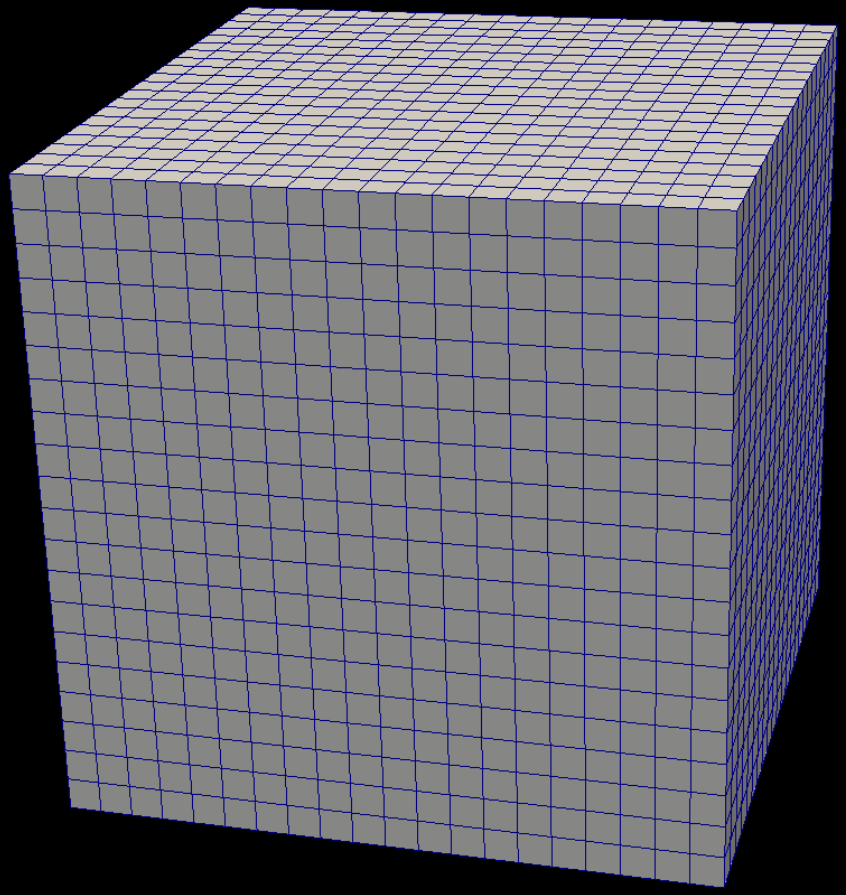
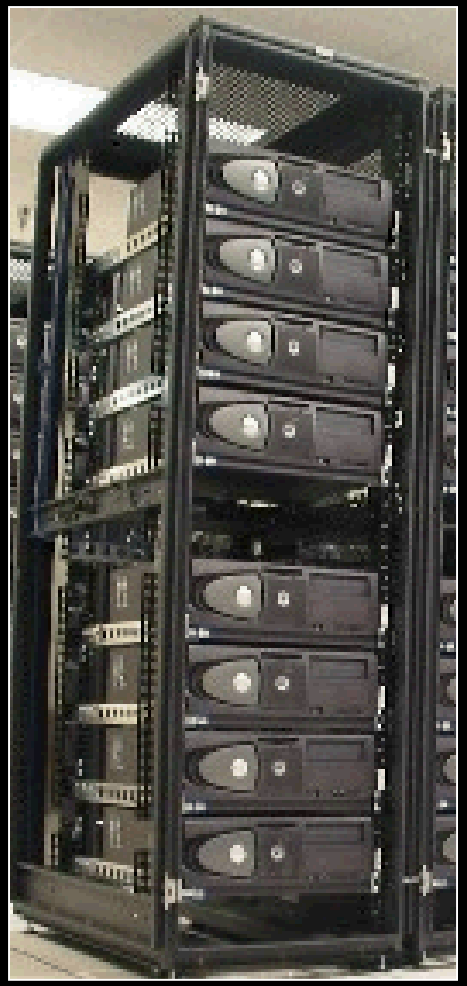
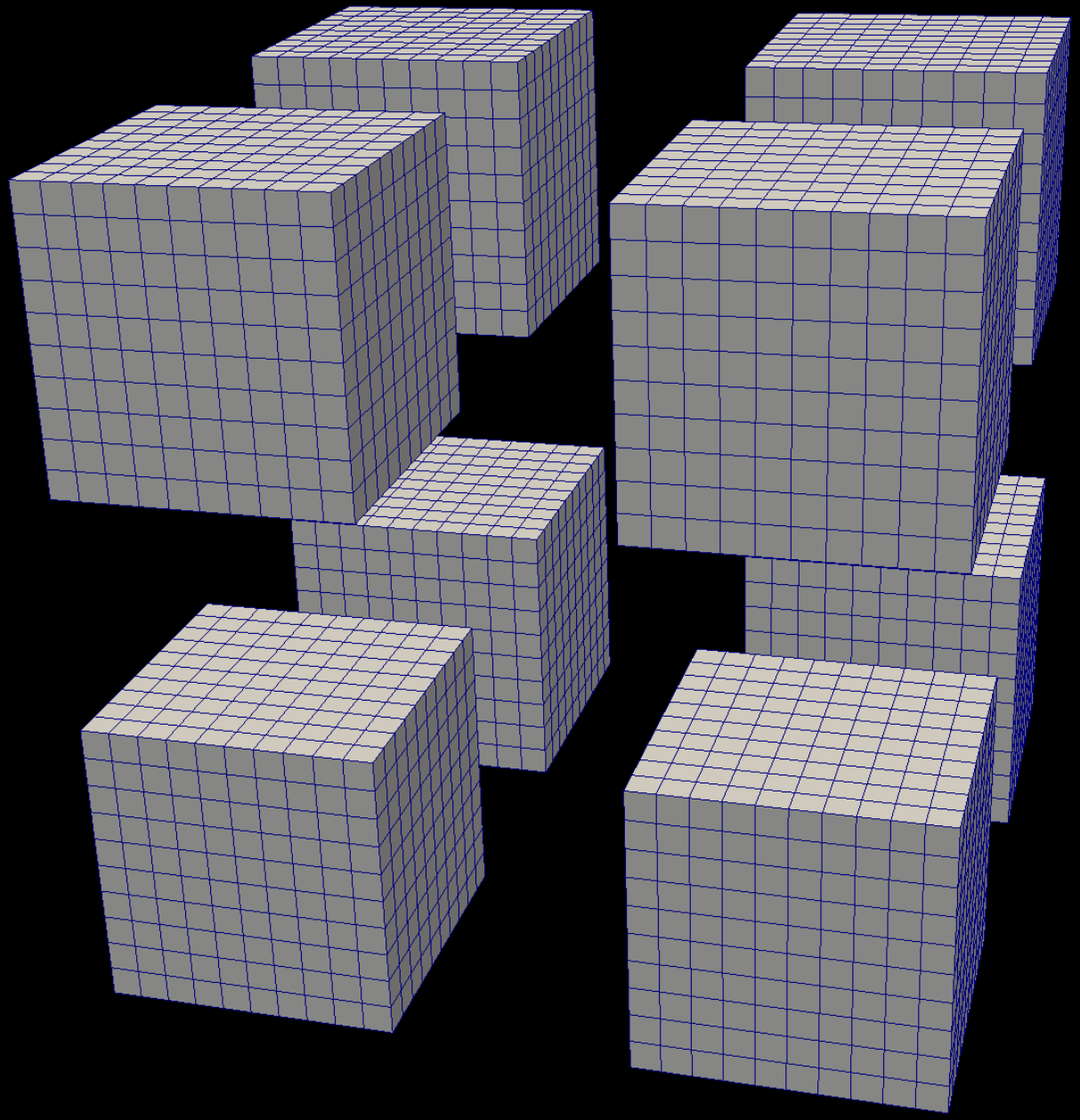
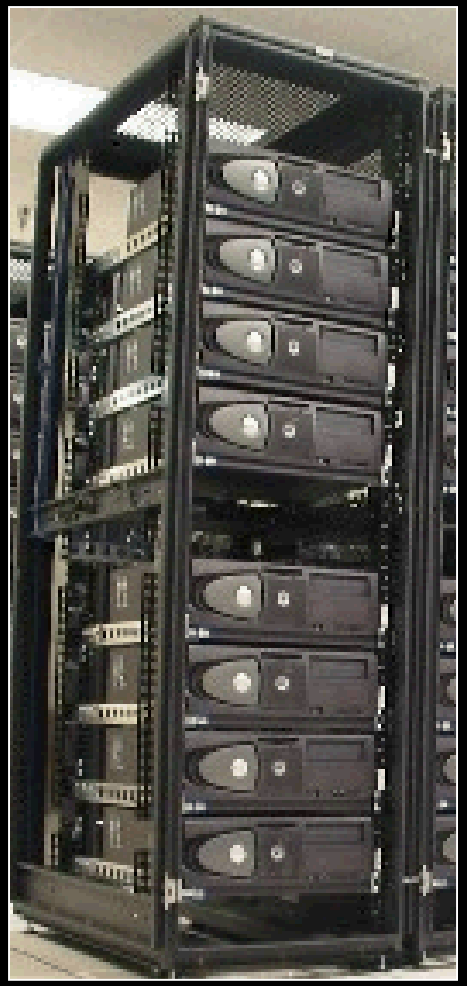
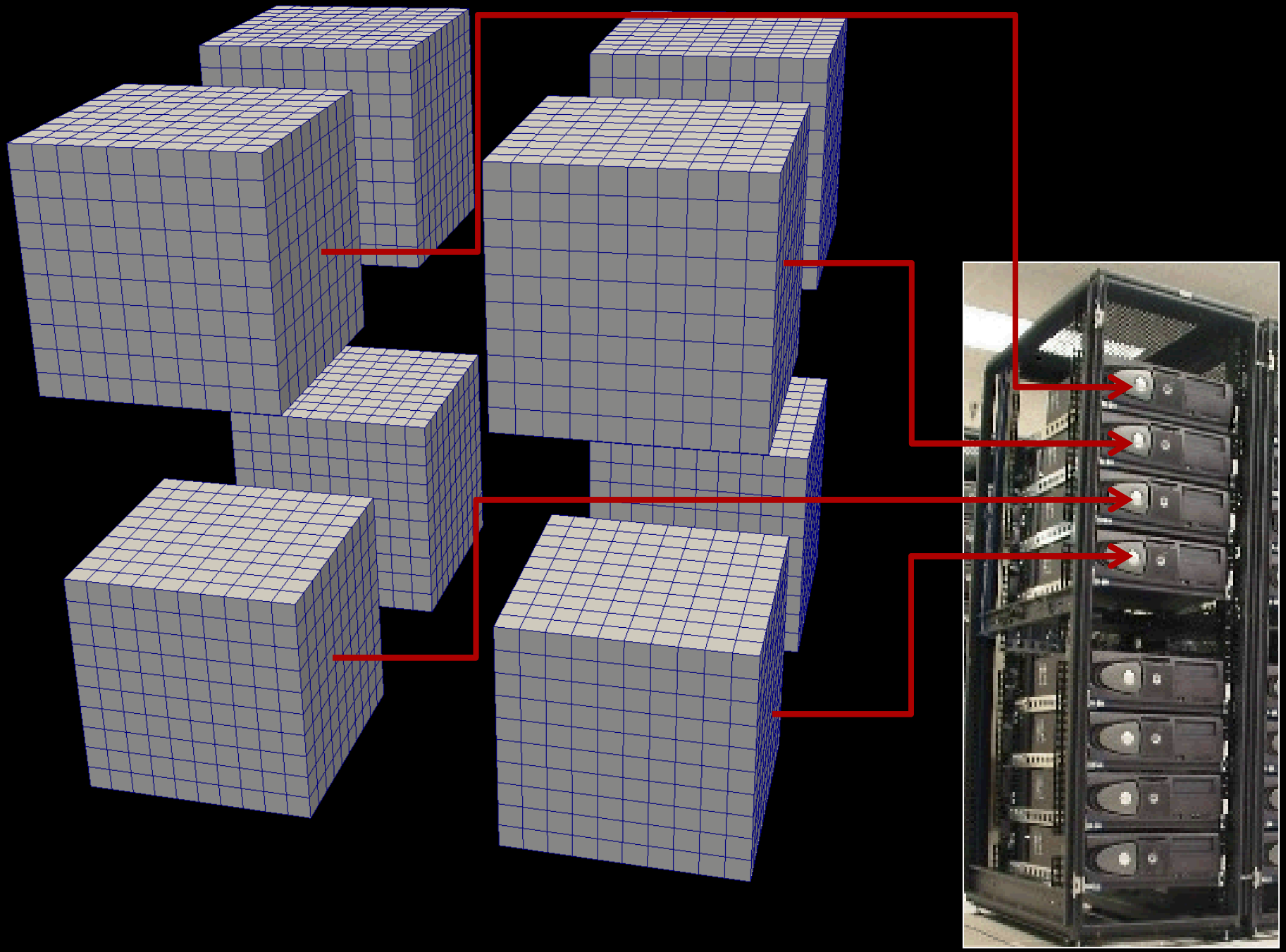
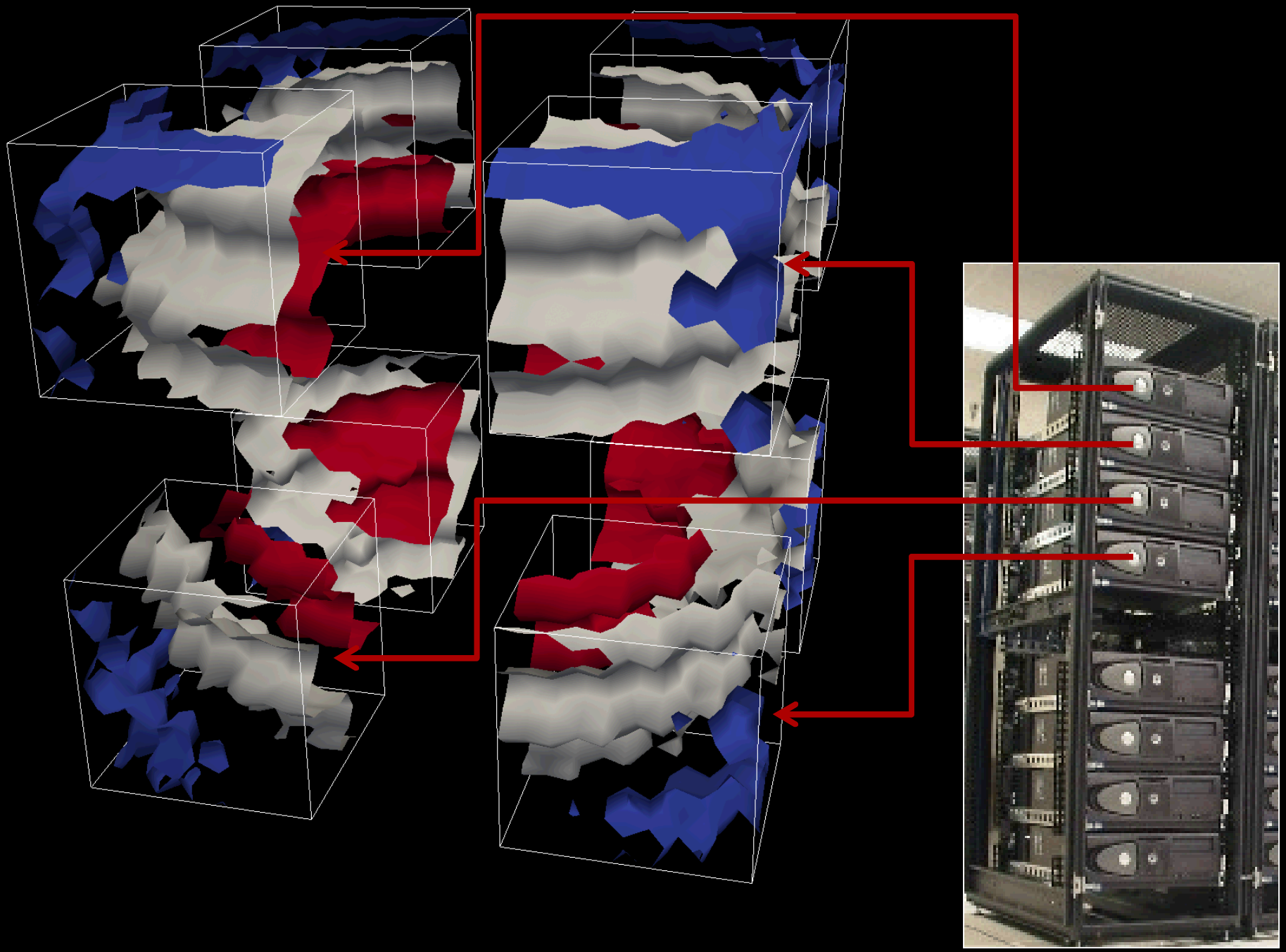




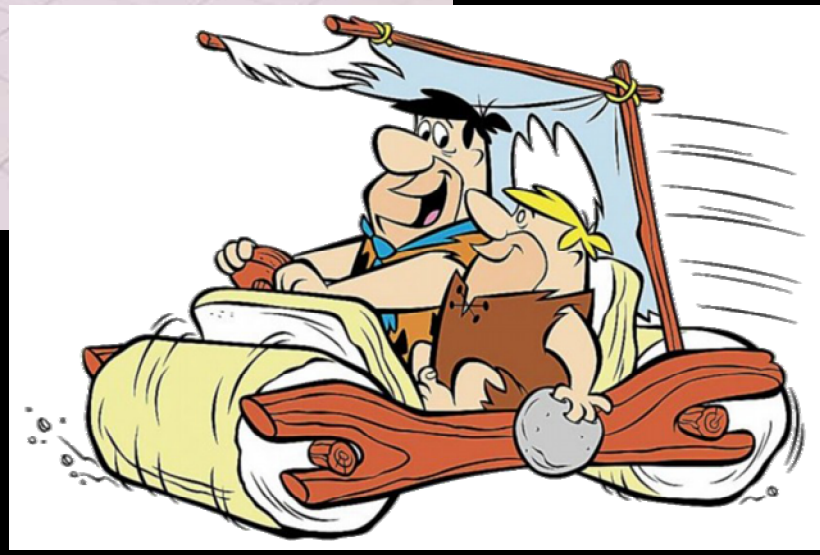








Distributed Memory Supercomputing (circa last week)



Encapsulating Large-Scale Visualization in Production Tools

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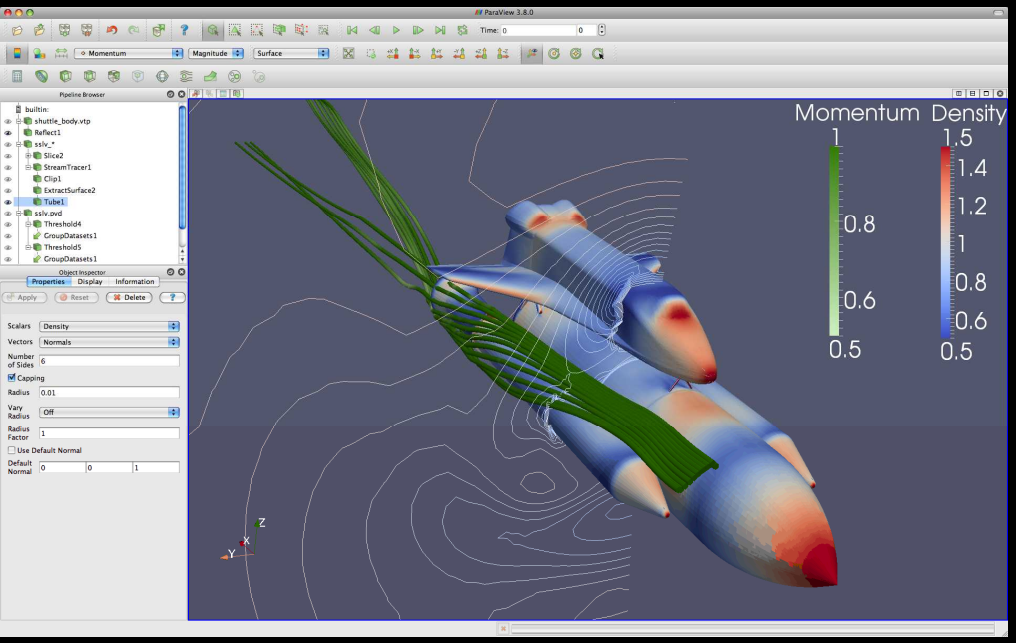
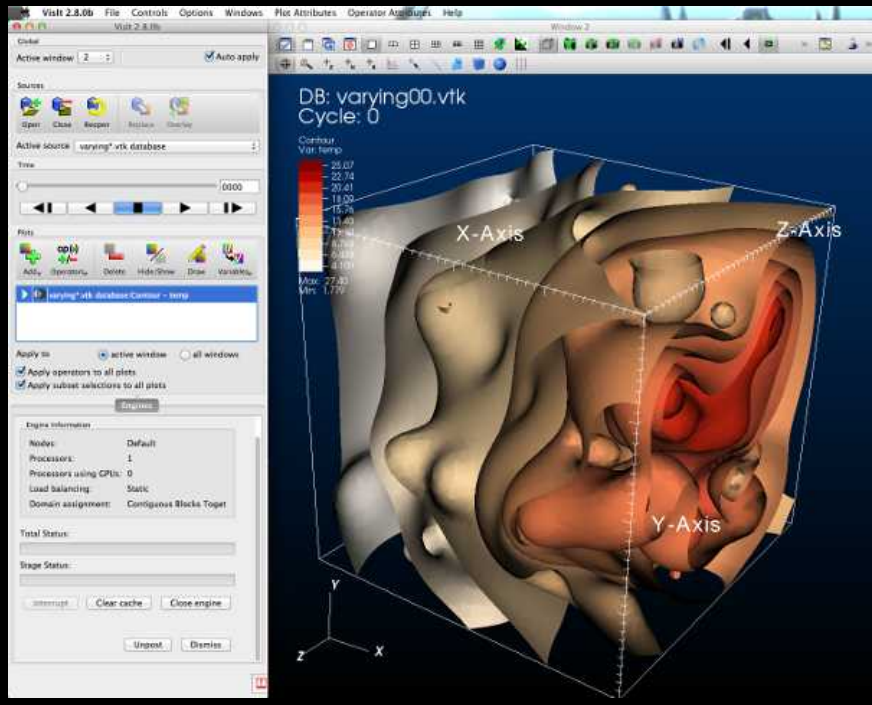


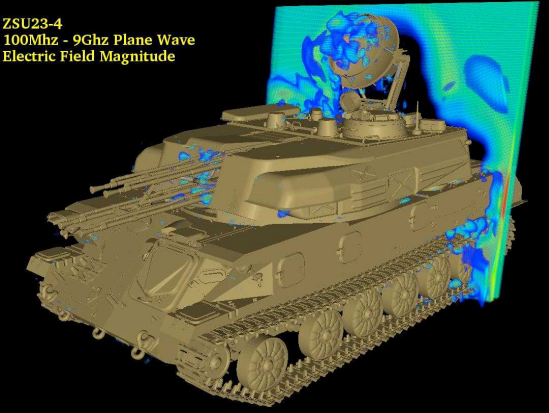
ParaView

http://paraview.org

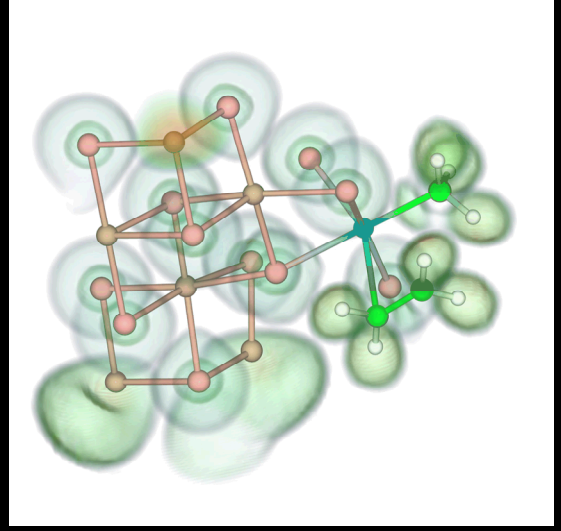


VisIt

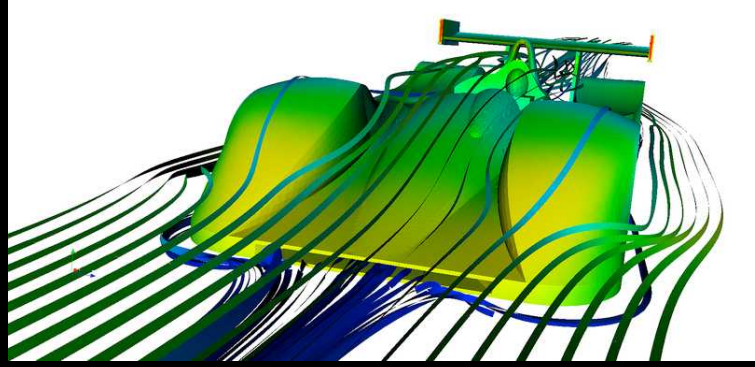
http://visit.llnl.gov/



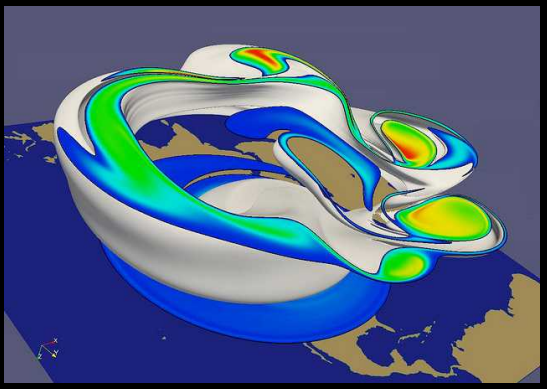
Jerry Clarke, US Army Research Laboratory

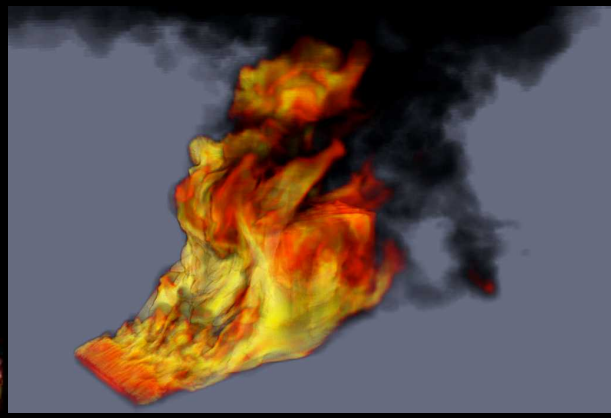


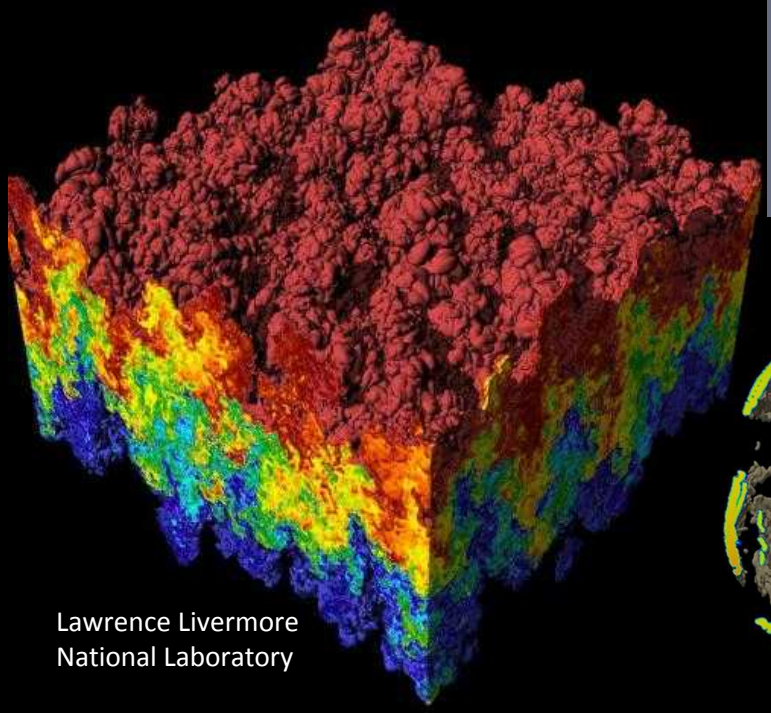
Swiss National Supercomputing Centre



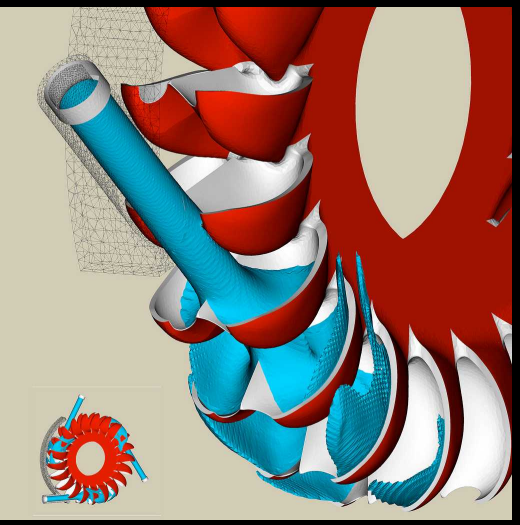
Renato N. Elias, NACAD/COPPE/UFRJ, Rio de Janerio, Brazil



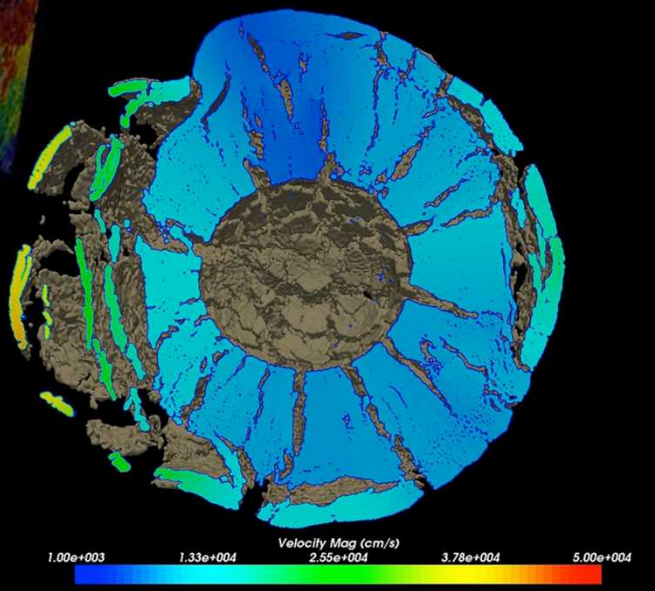


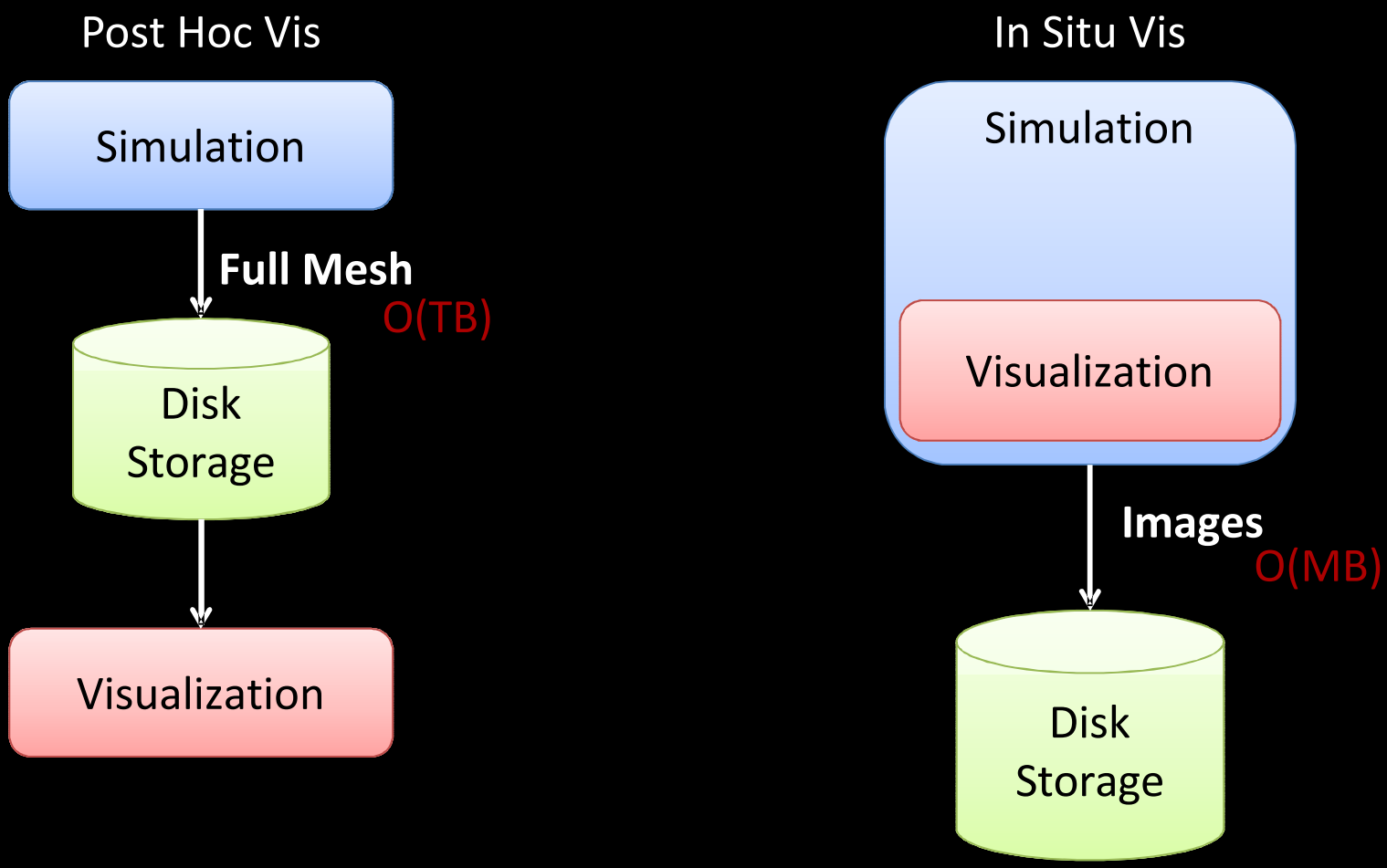


Lawrence Livermore
National Laboratory



Swiss National Supercomputing Centre

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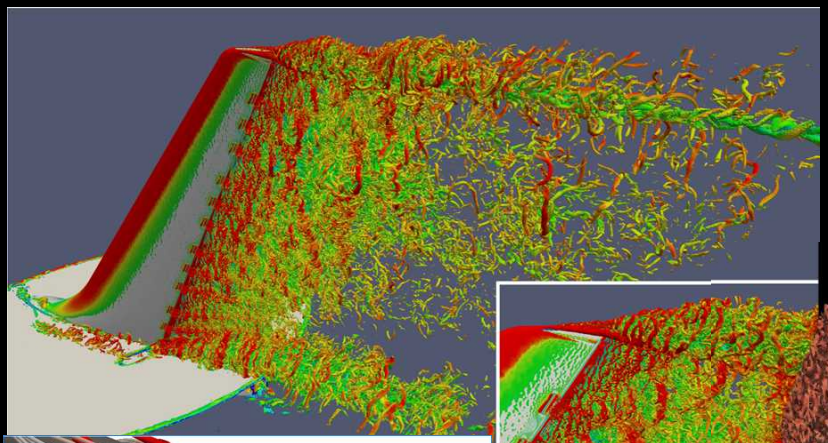
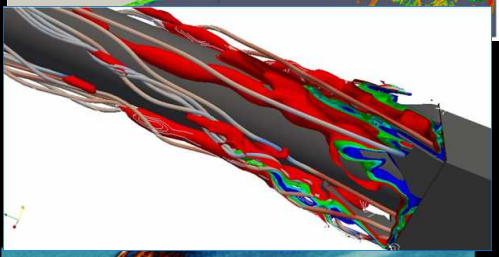
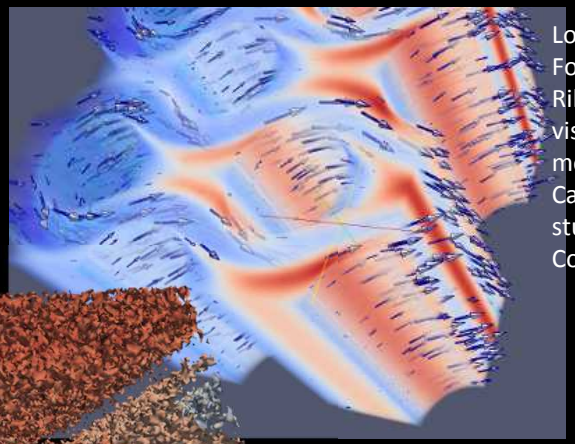
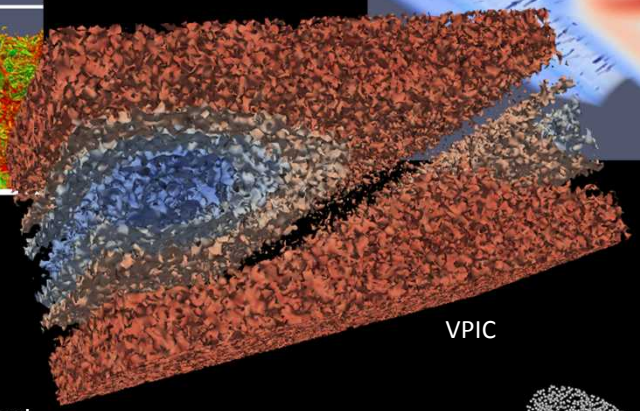






Lorendeau, Fournier, and Ribes. “In-Situ visualization in fluid mechanics using Catalyst: a case study for Code_Saturne.”



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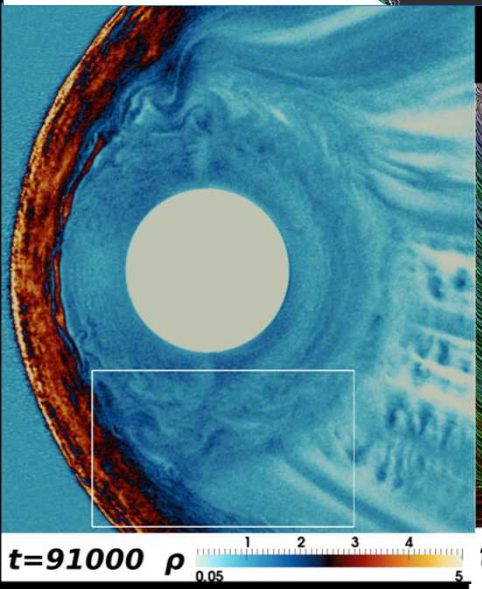
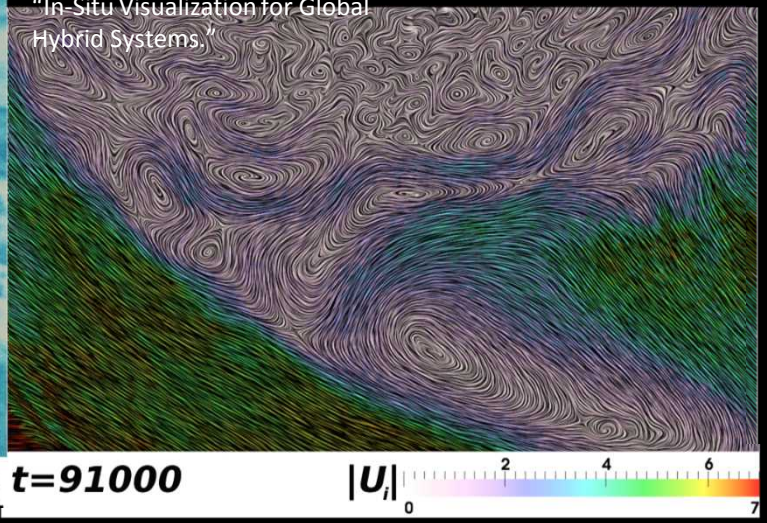
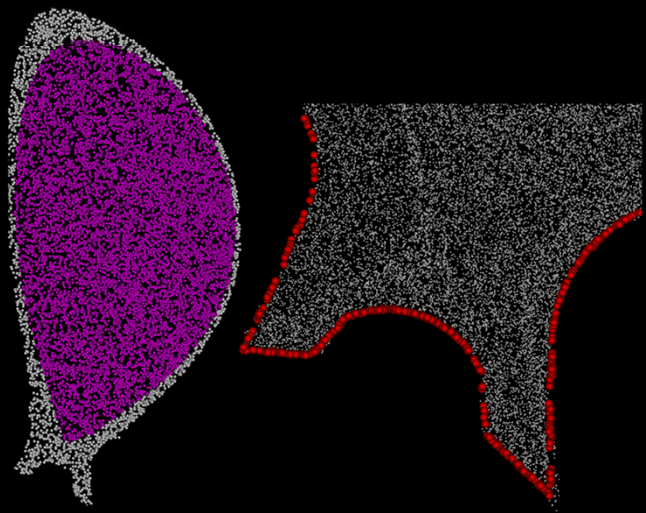


Krimabadi, O’Leary, Tatineni, Loring, Majumdar, and Geveci. “In-Situ Visualization for Global Hybrid Systems.”





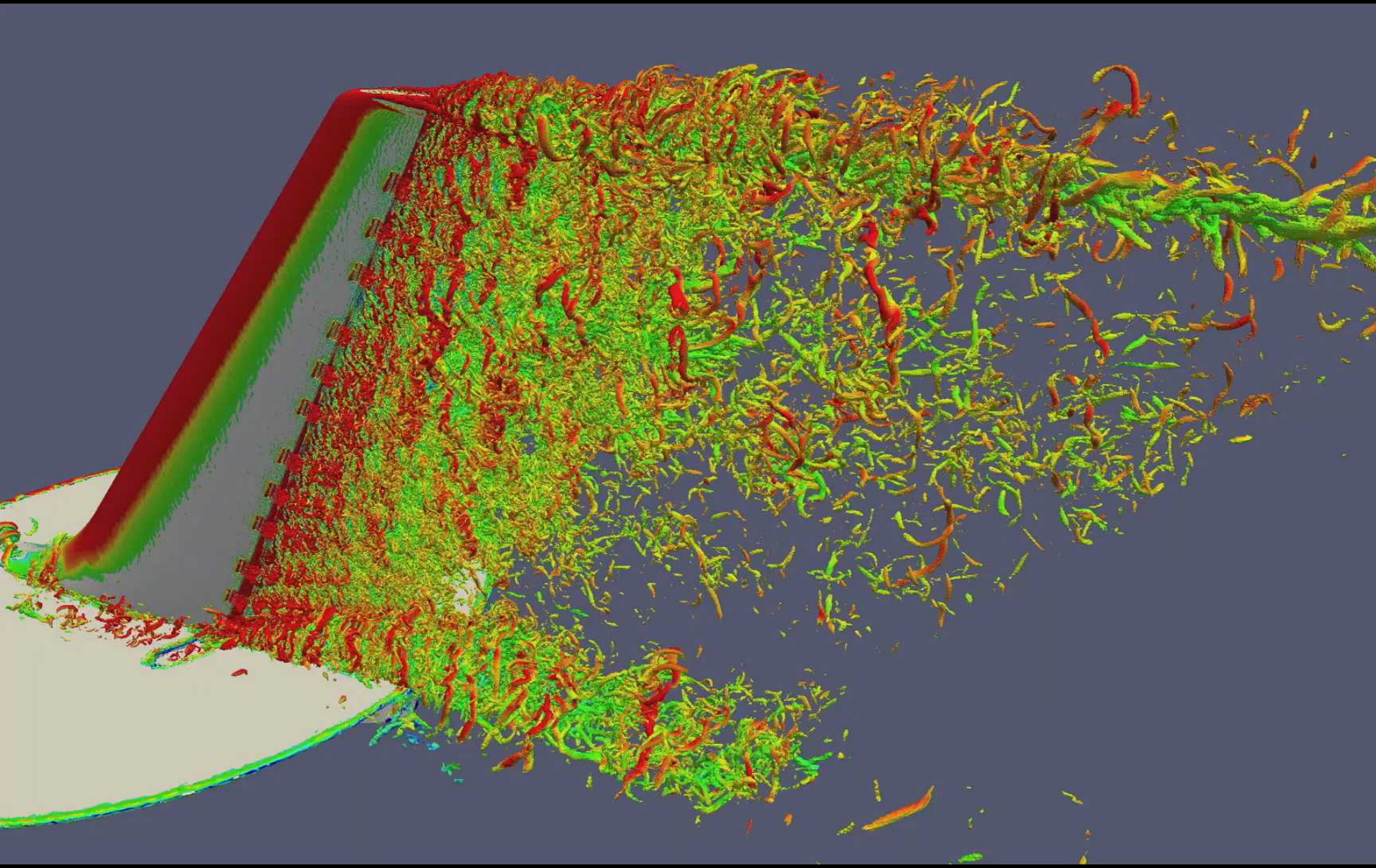


Image Credit: Jonathan Kos-Read

Extreme Scale is Threads, Threads Threads!

- A clear trend in supercomputing is ever increasing parallelism
- Clock increases are long gone
  - "The Free Lunch Is Over" (Herb Sutter)

	Jaguar – XT5	Titan – XK7	Exascale*
Cores	224,256	299,008 and 18,688 gpu	1 billion
Concurrency	224,256 way	70 – 500 million way	10 – 100 billion way
Memory	300 Terabytes	700 Terabytes	128 Petabytes

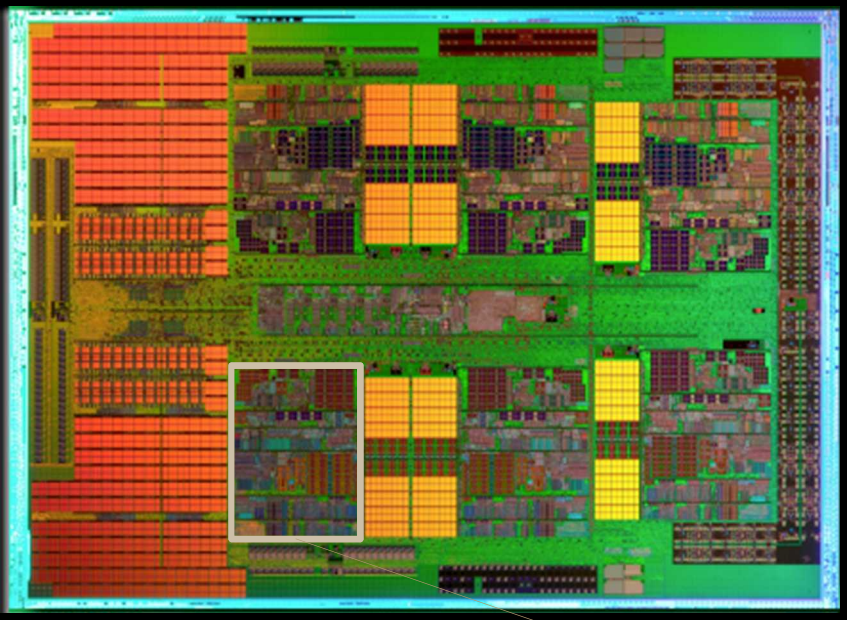
*Source: Scientific Discovery at the Exascale, Ahern, Shoshani, Ma, et al.

My new computer's got the clocks, it rocks
But it was obsolete before I opened the box

– “Weird” Al Yankovic, *It’s All About the Pentiums*, circa 1999

Moore’s Law is dead.

– Gordon Moore, circa 2005

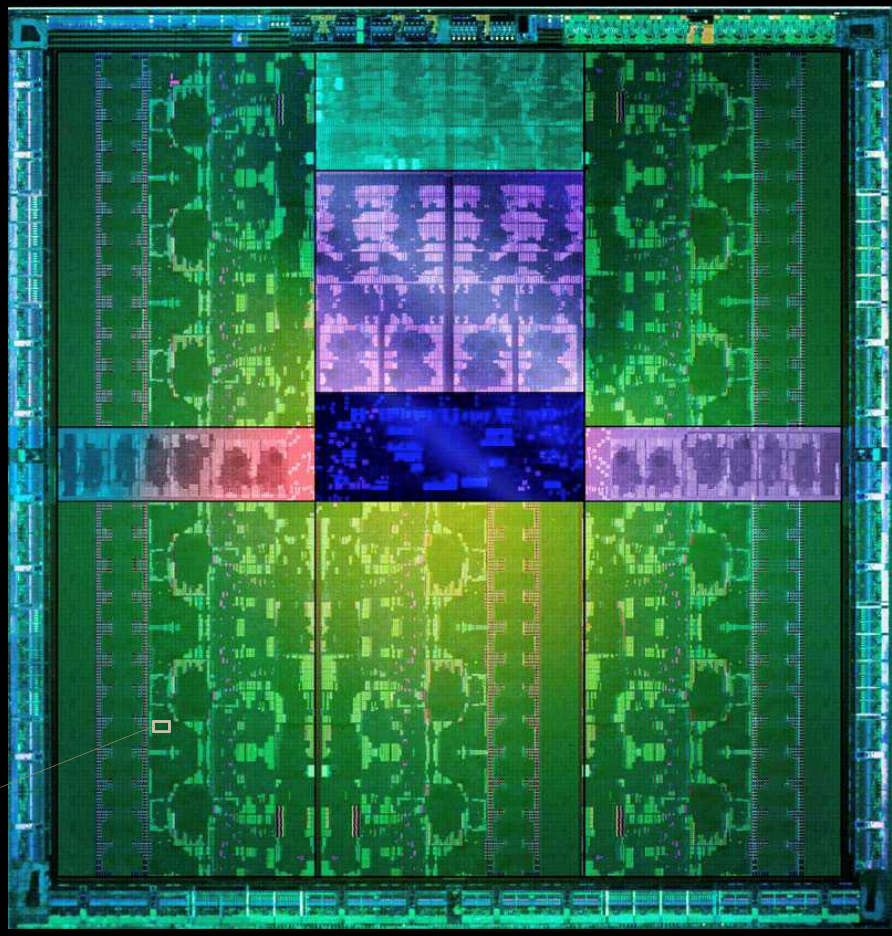


AMD x86

Full x86 Core
+ Associated Cache
6 cores per die
MPI-Only feasible

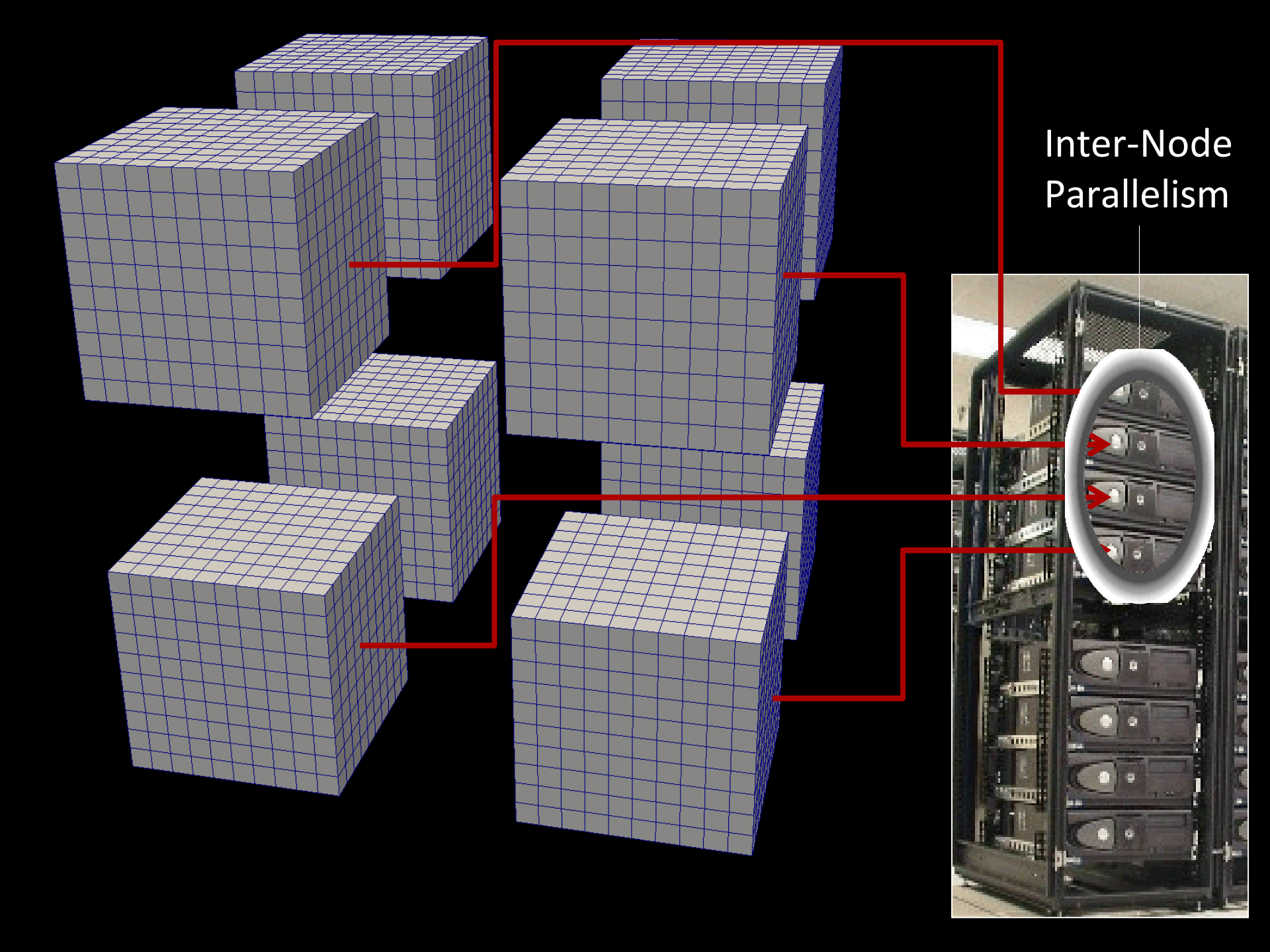
1 x86 core

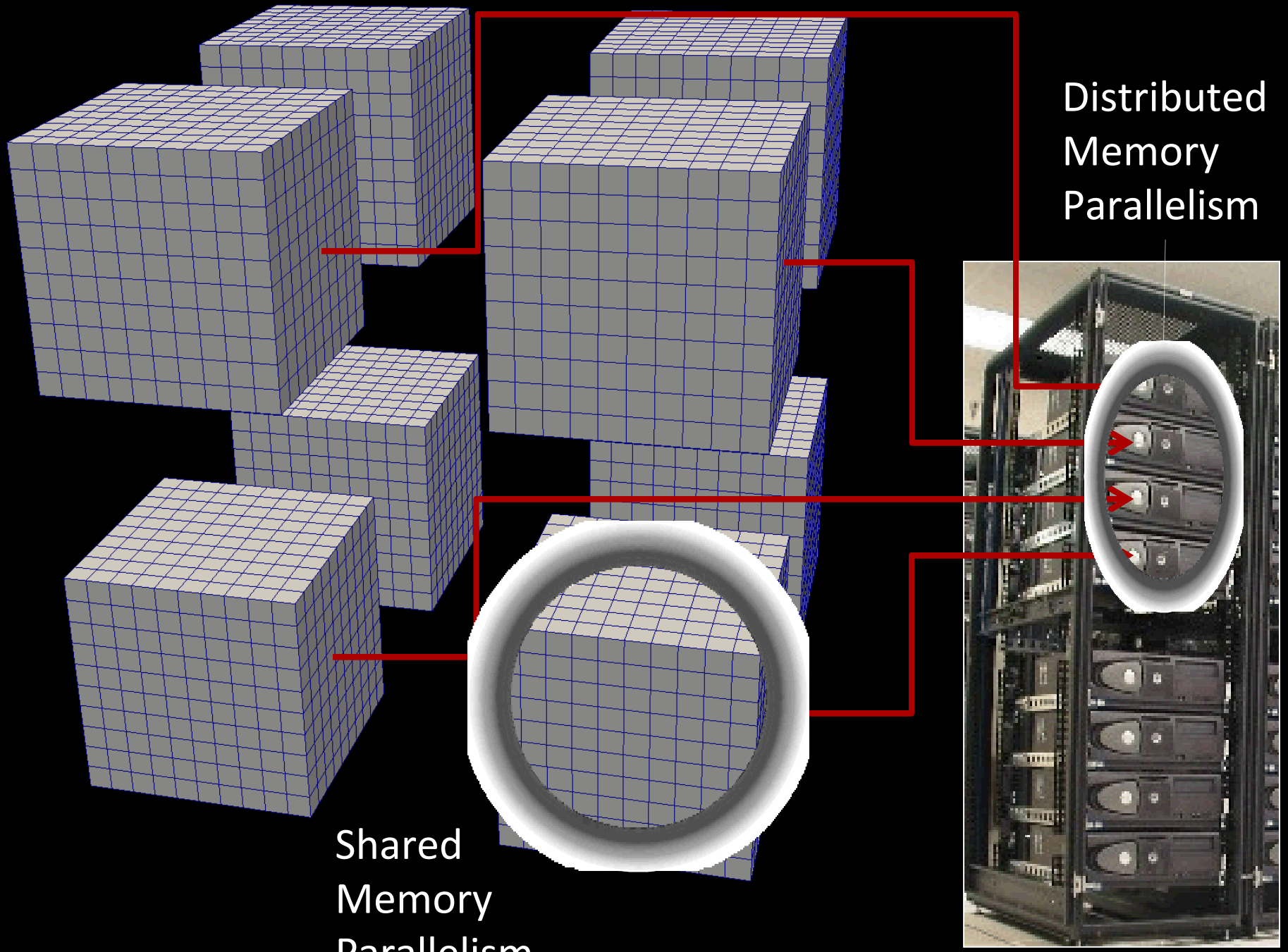
1 Kepler "core"



NVIDIA GPU

2,880 cores collected in 15 SMX
Shared PC, Cache, Mem Fetches
Reduced control logic
MPI-Only not feasible


Inter-Node
Parallelism


Distributed
Memory
Parallelism
Shared
Memory
Parallelism

VTK-m

Sandia National Laboratories

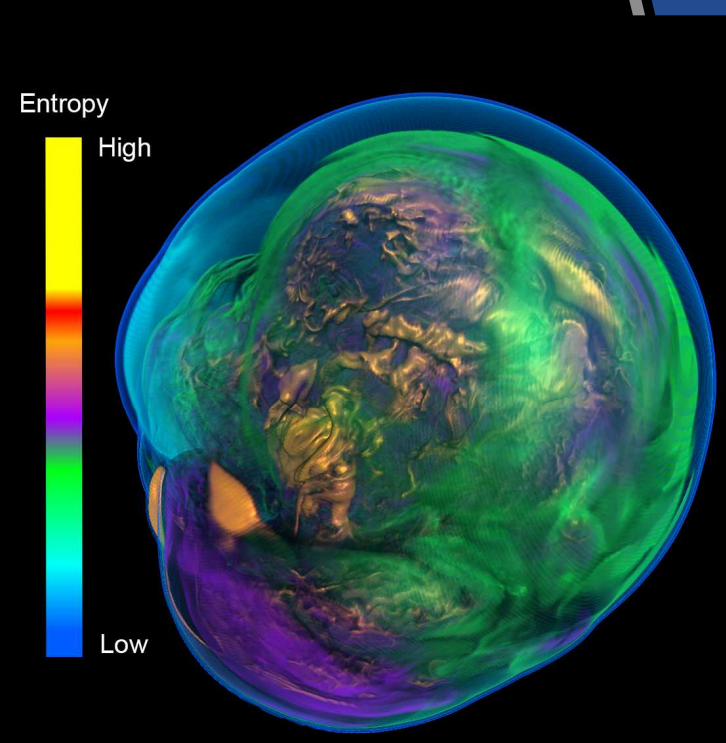
Los Alamos National Laboratory

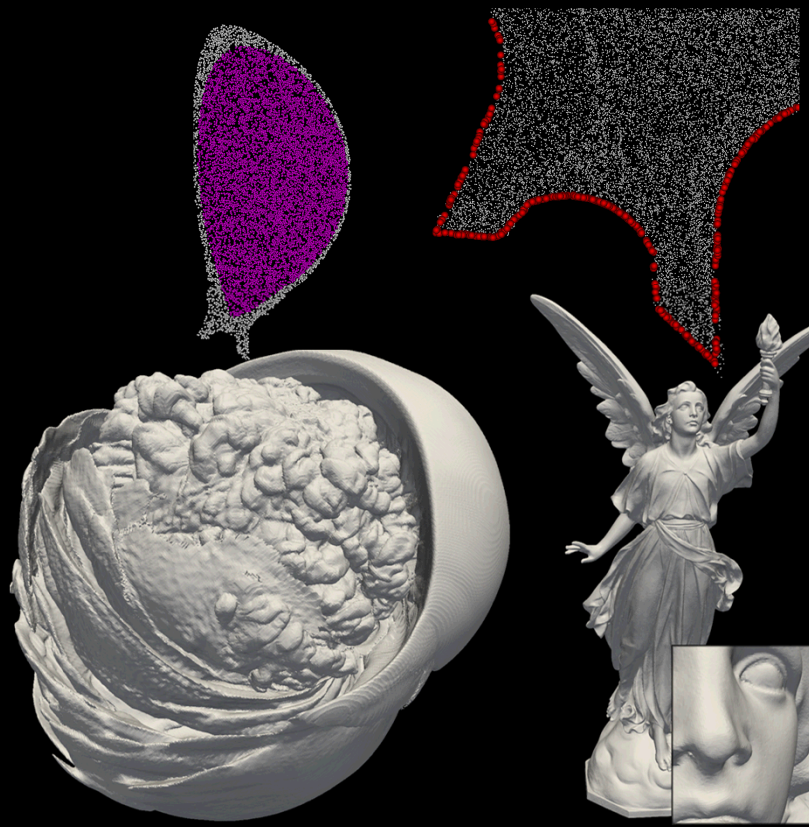
Oak Ridge National Laboratory

Kitware

University of Oregon

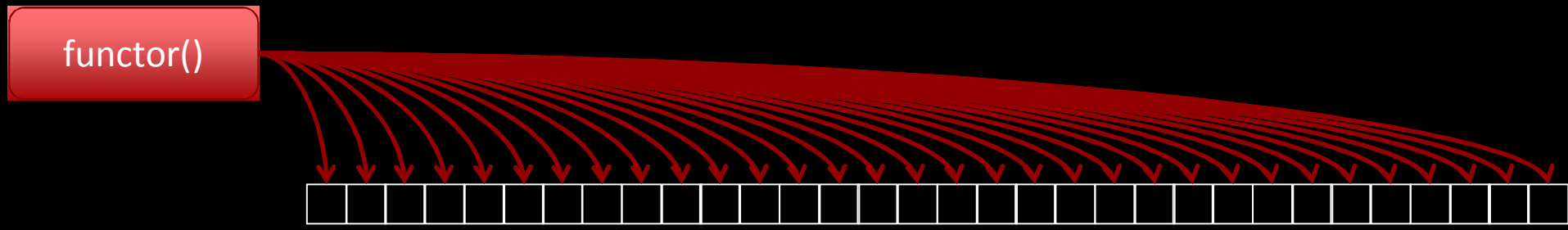
http://m.vtk.org



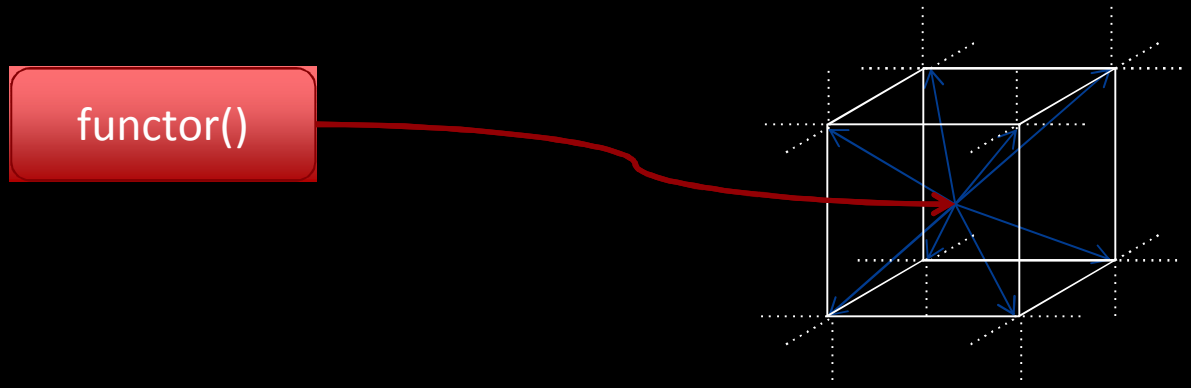


VTK-m: Basic Approach

- Functor mapping [Baker, et al. 2010]

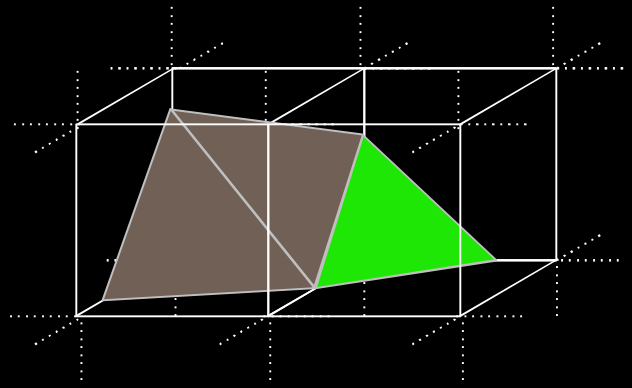


Applied to Topologies

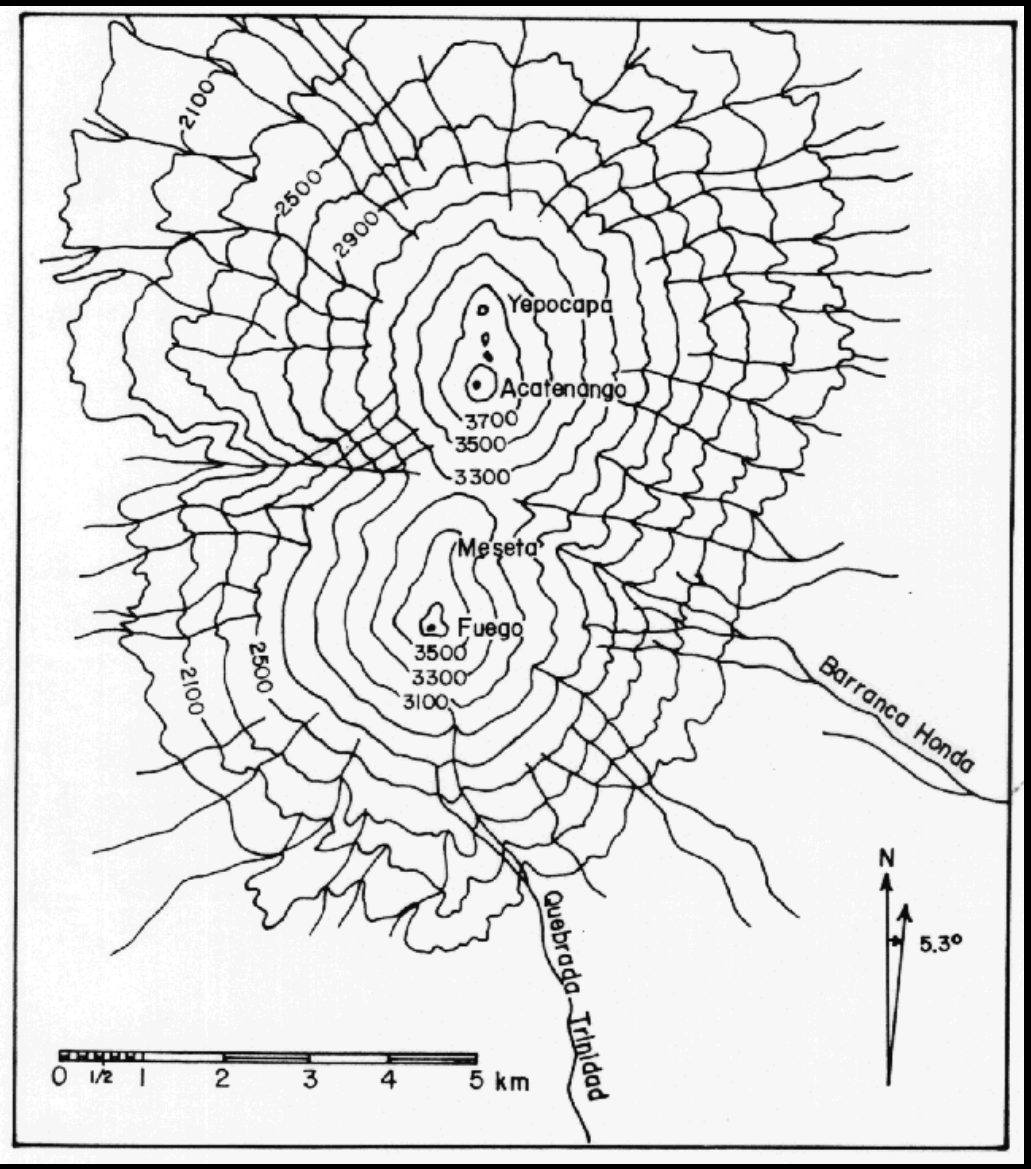


Applied to Topologies

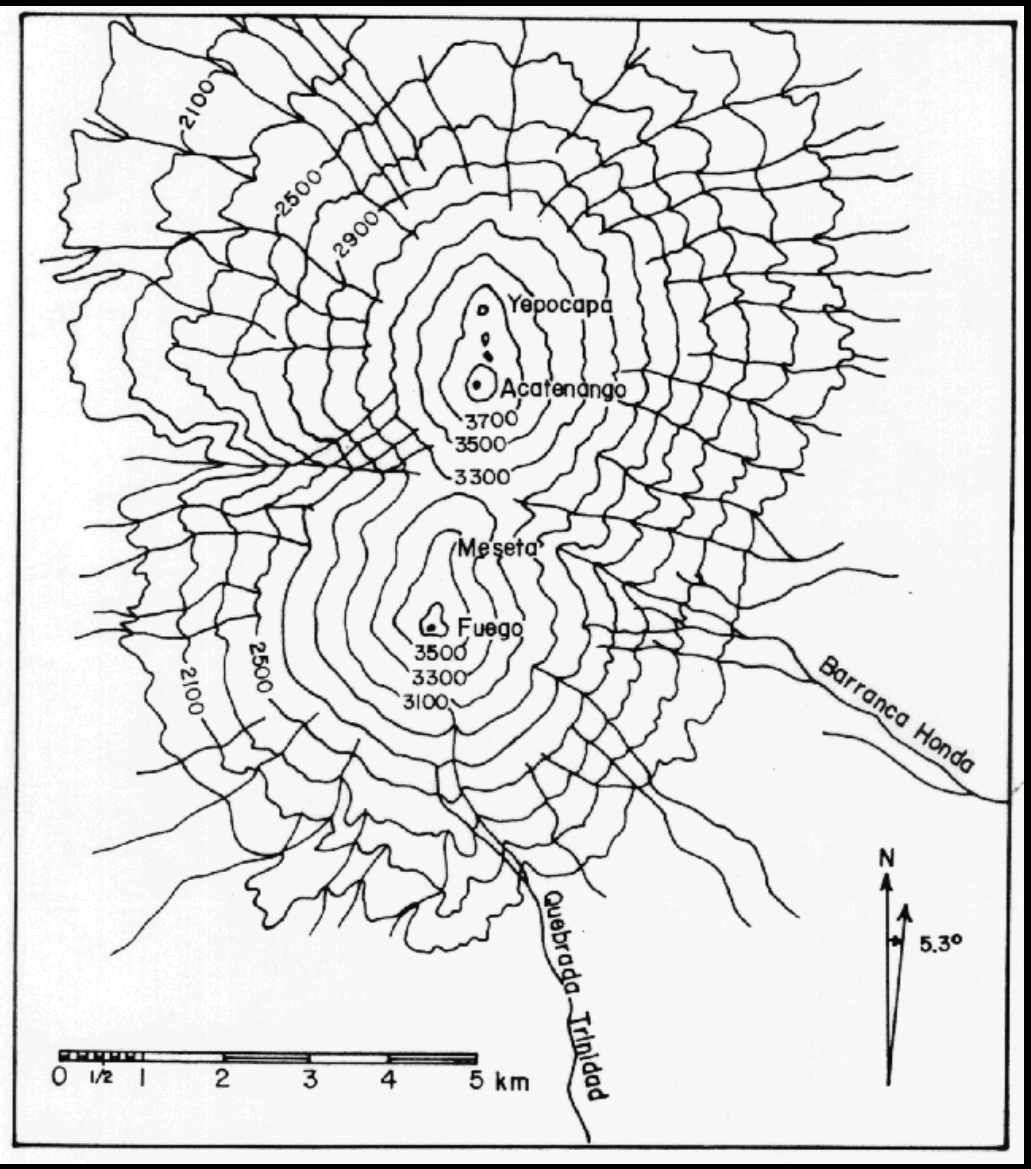
functor()

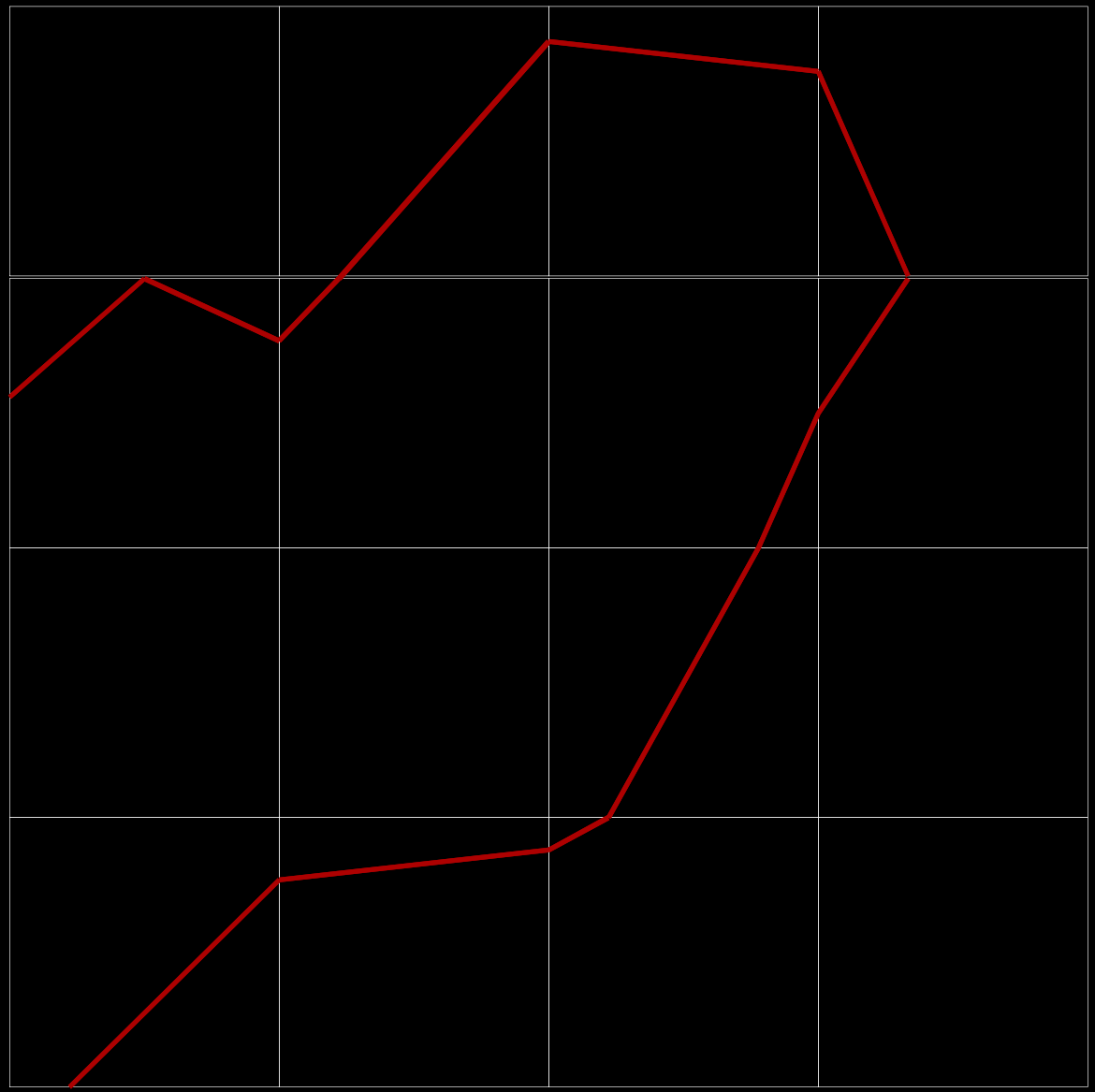


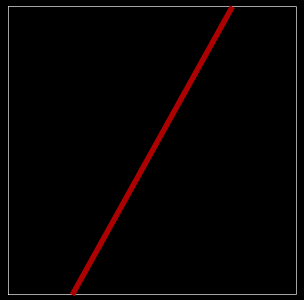
Example Algorithm: Contours

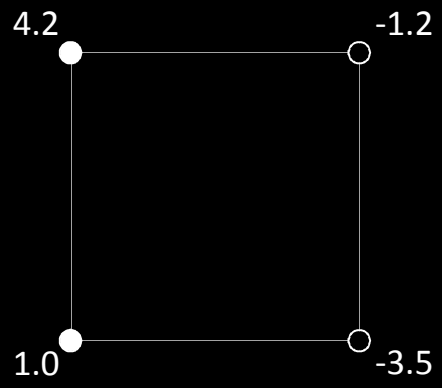


Example Algorithm: Contours





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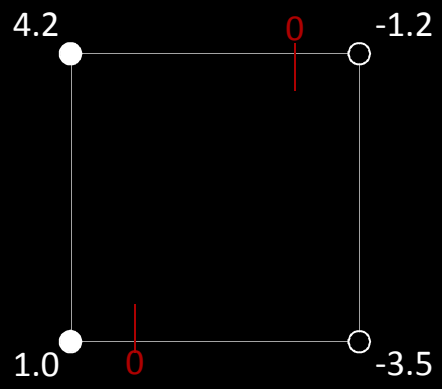
-3.5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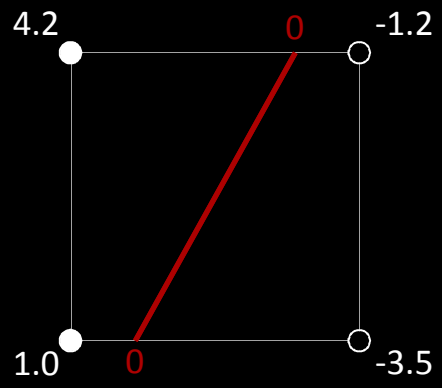
4.2
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-1.2
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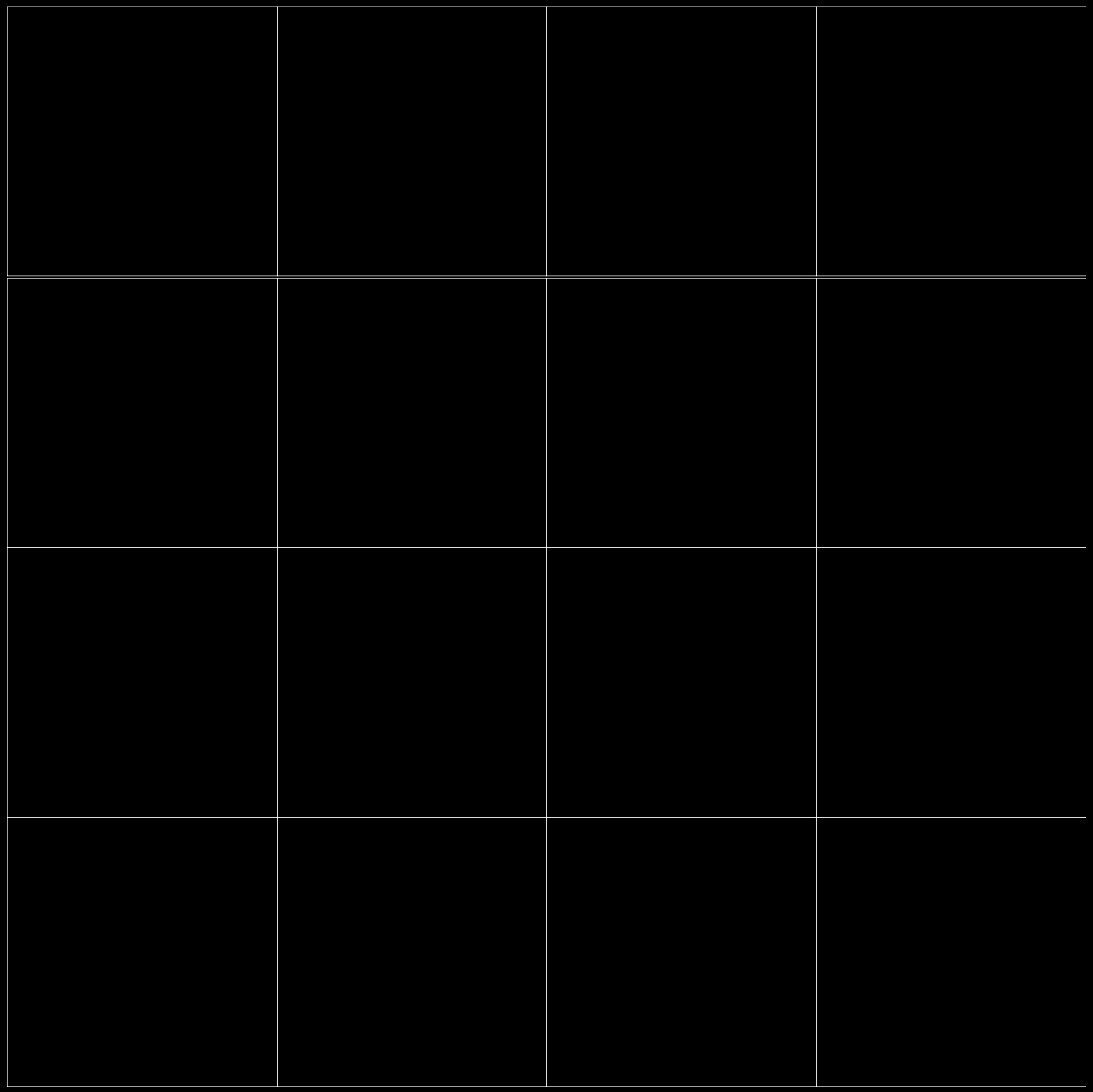

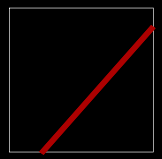

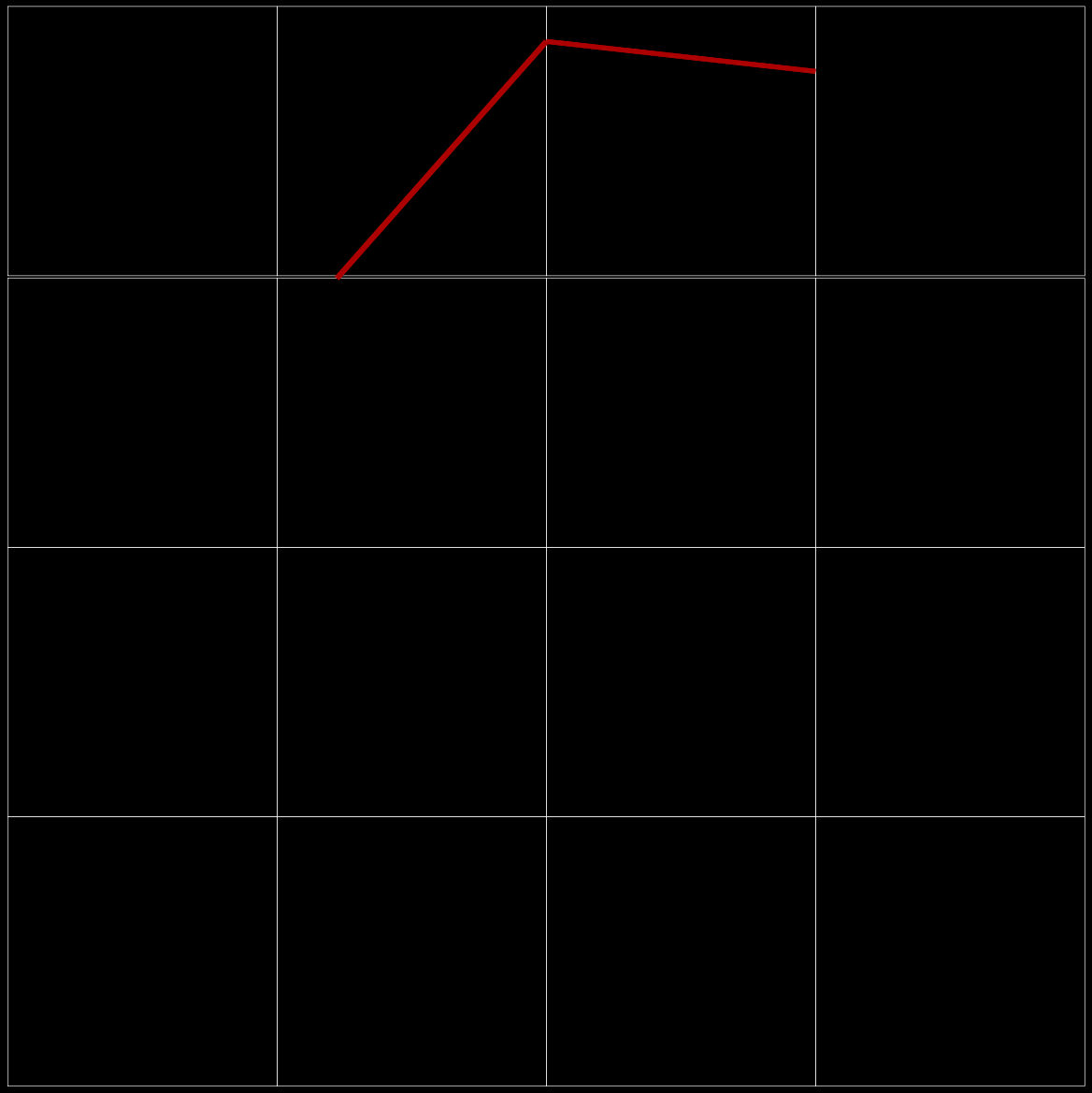

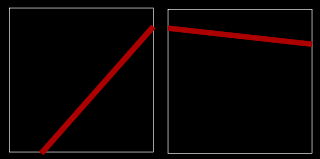

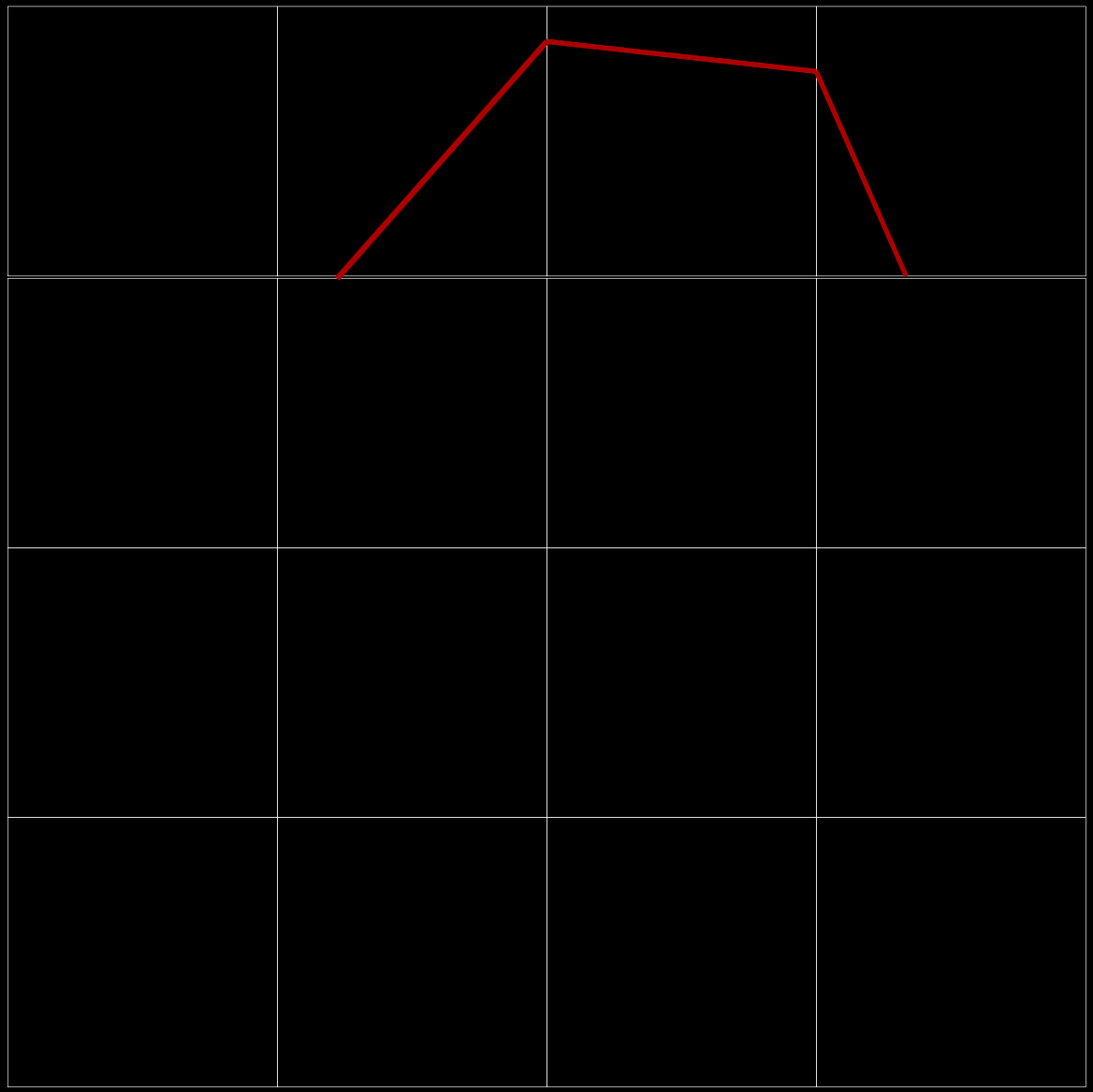

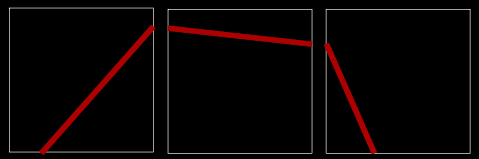

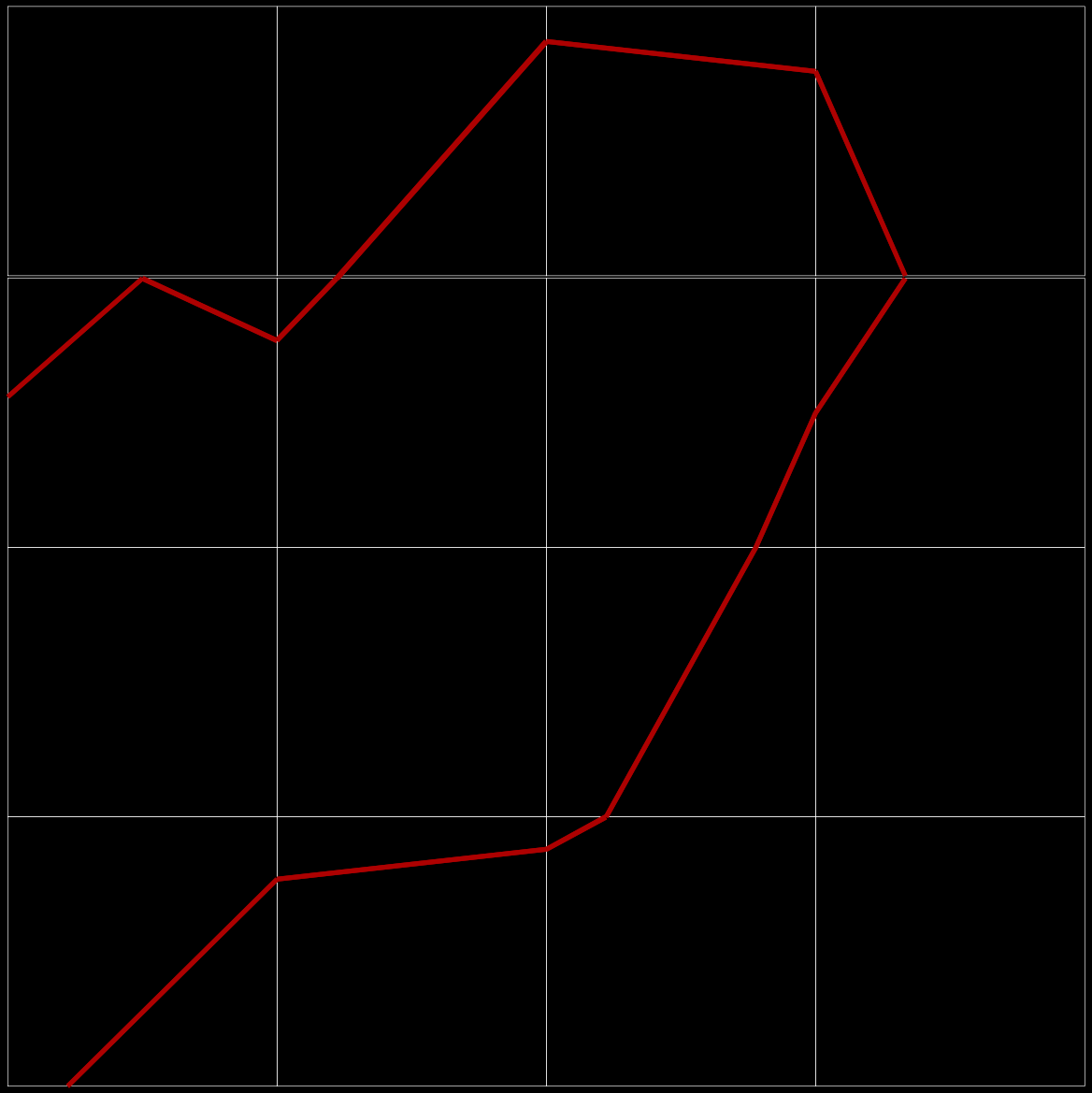

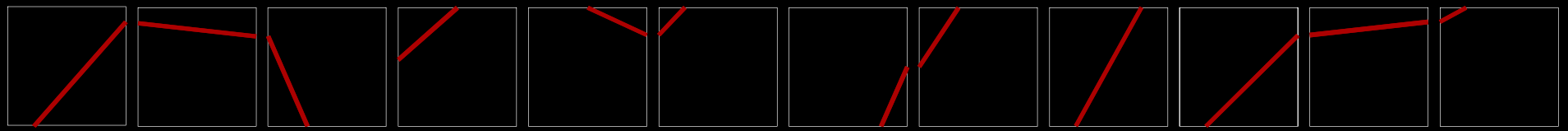

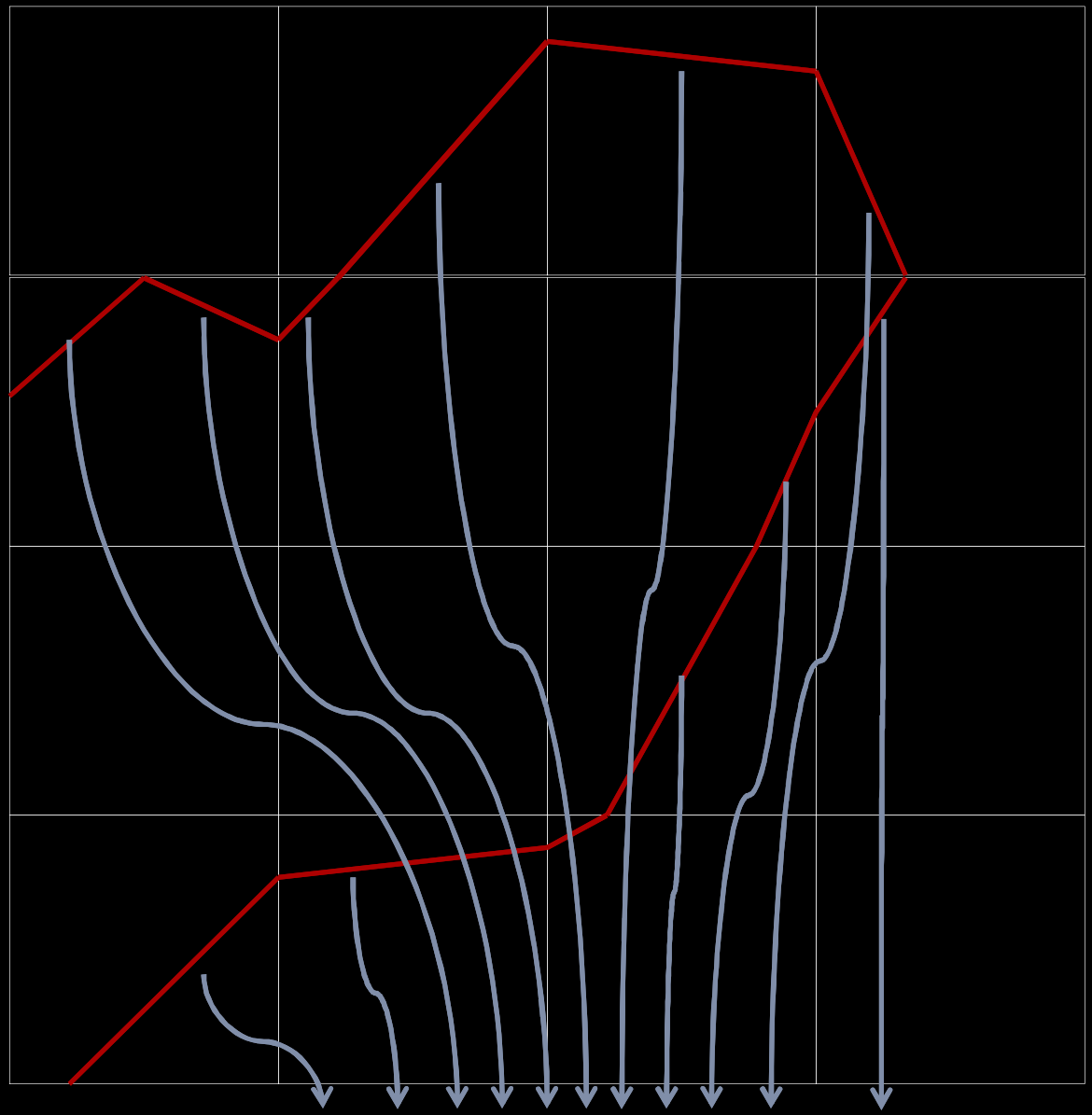

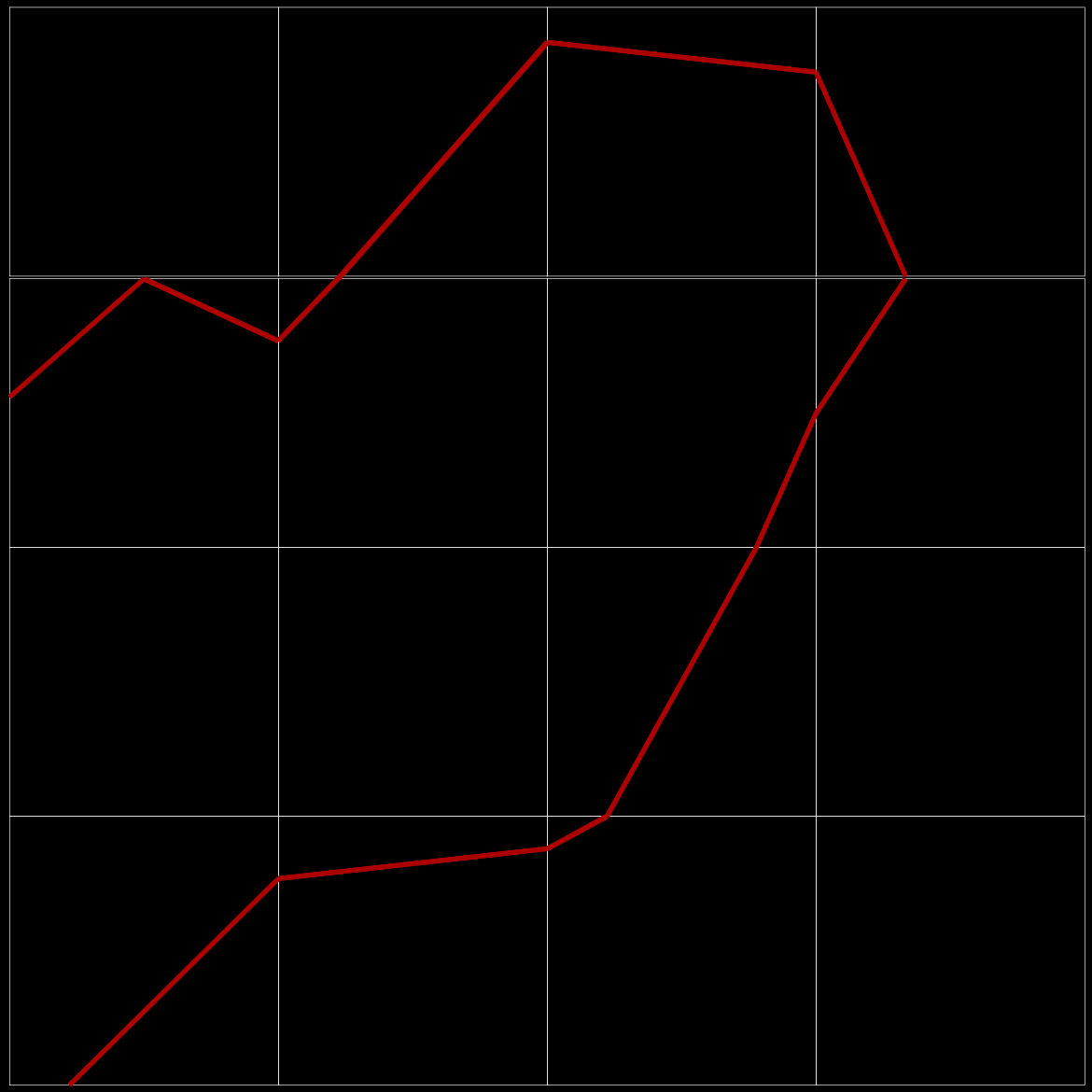

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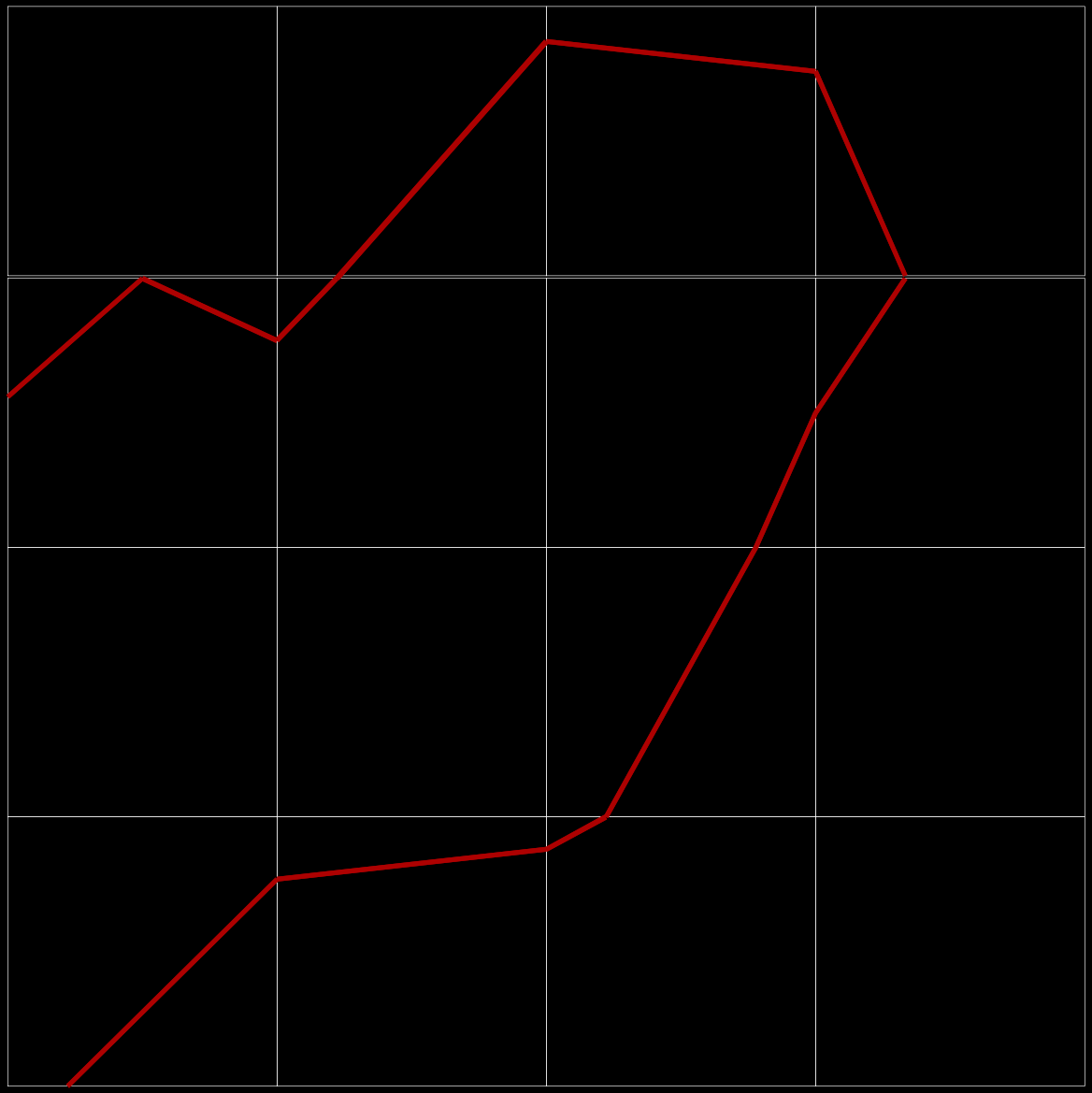

+0	+1	+1	+1	+2	+1	+1	+1	+0	+0	+1	+0	+1	+1	+1	+0
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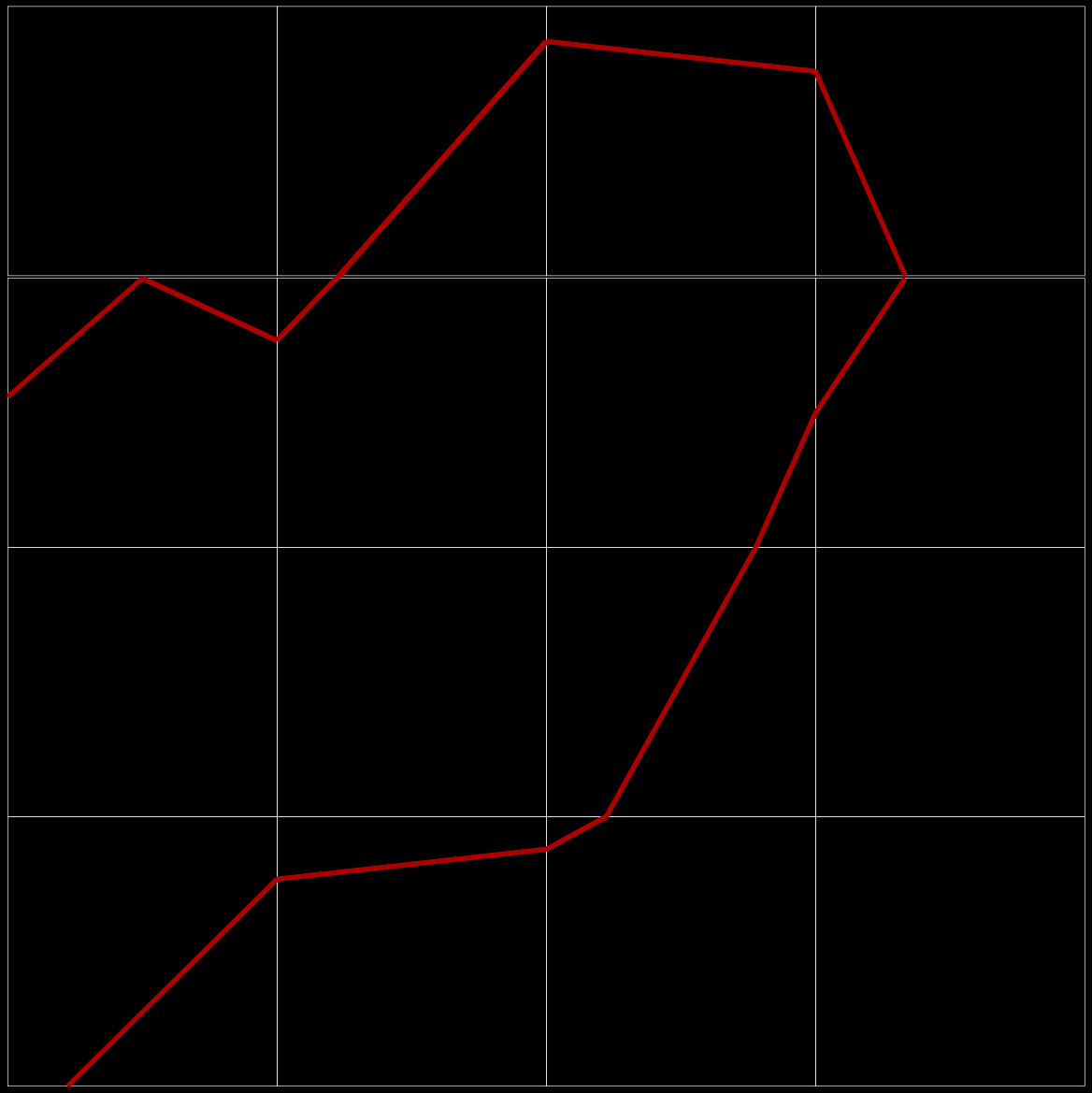
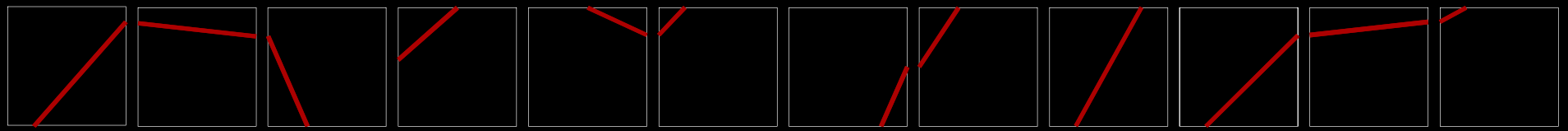
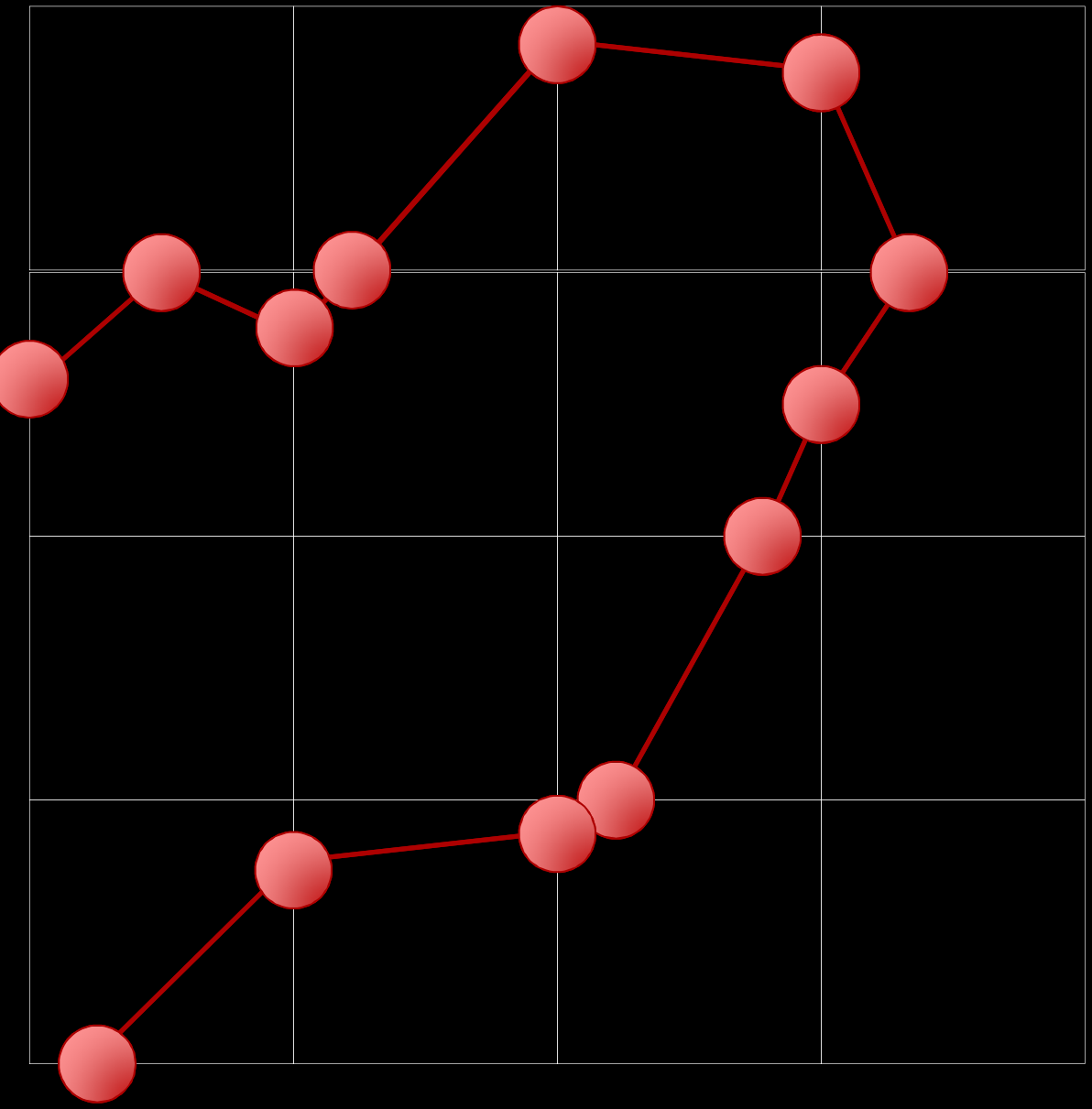
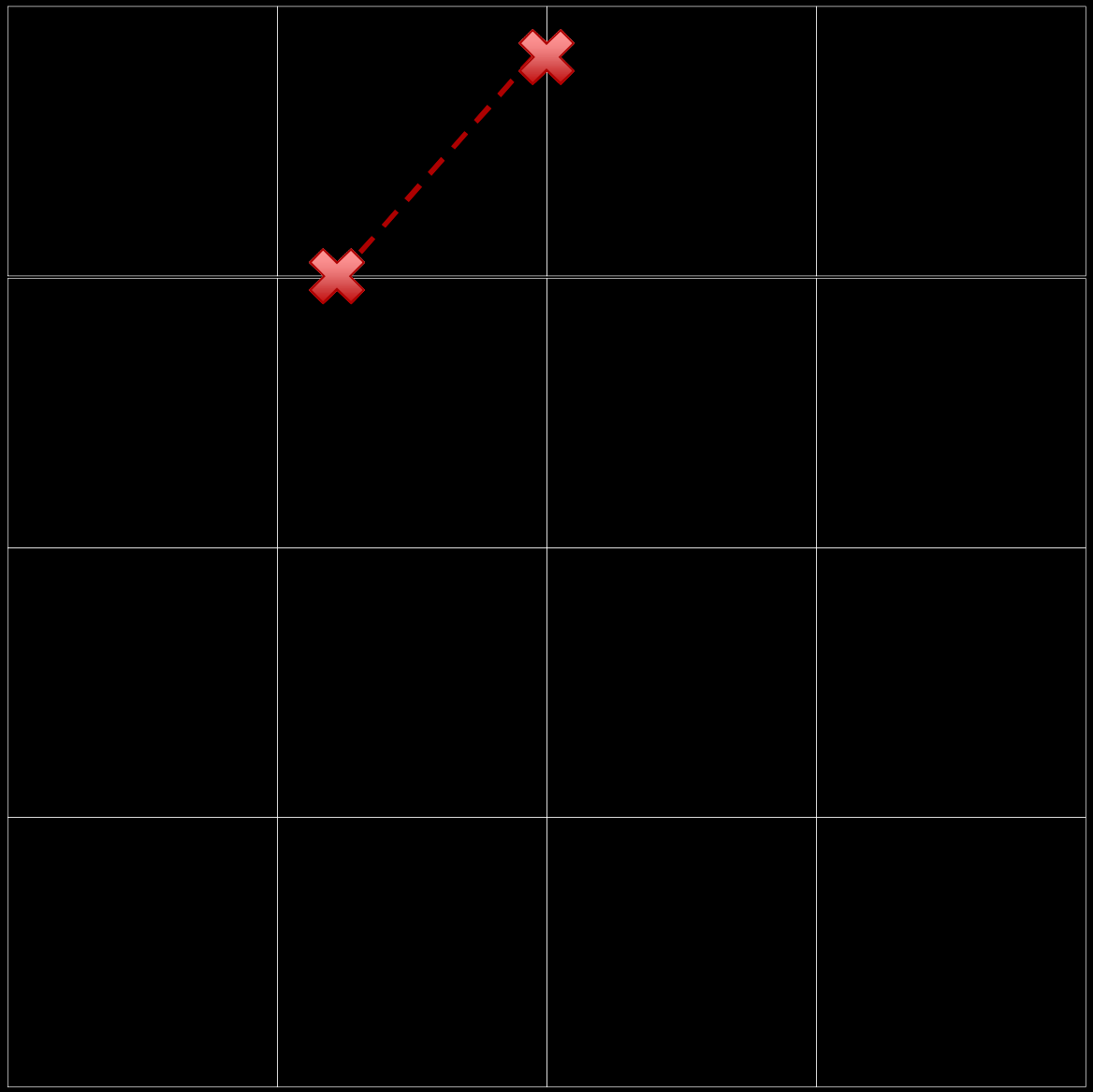
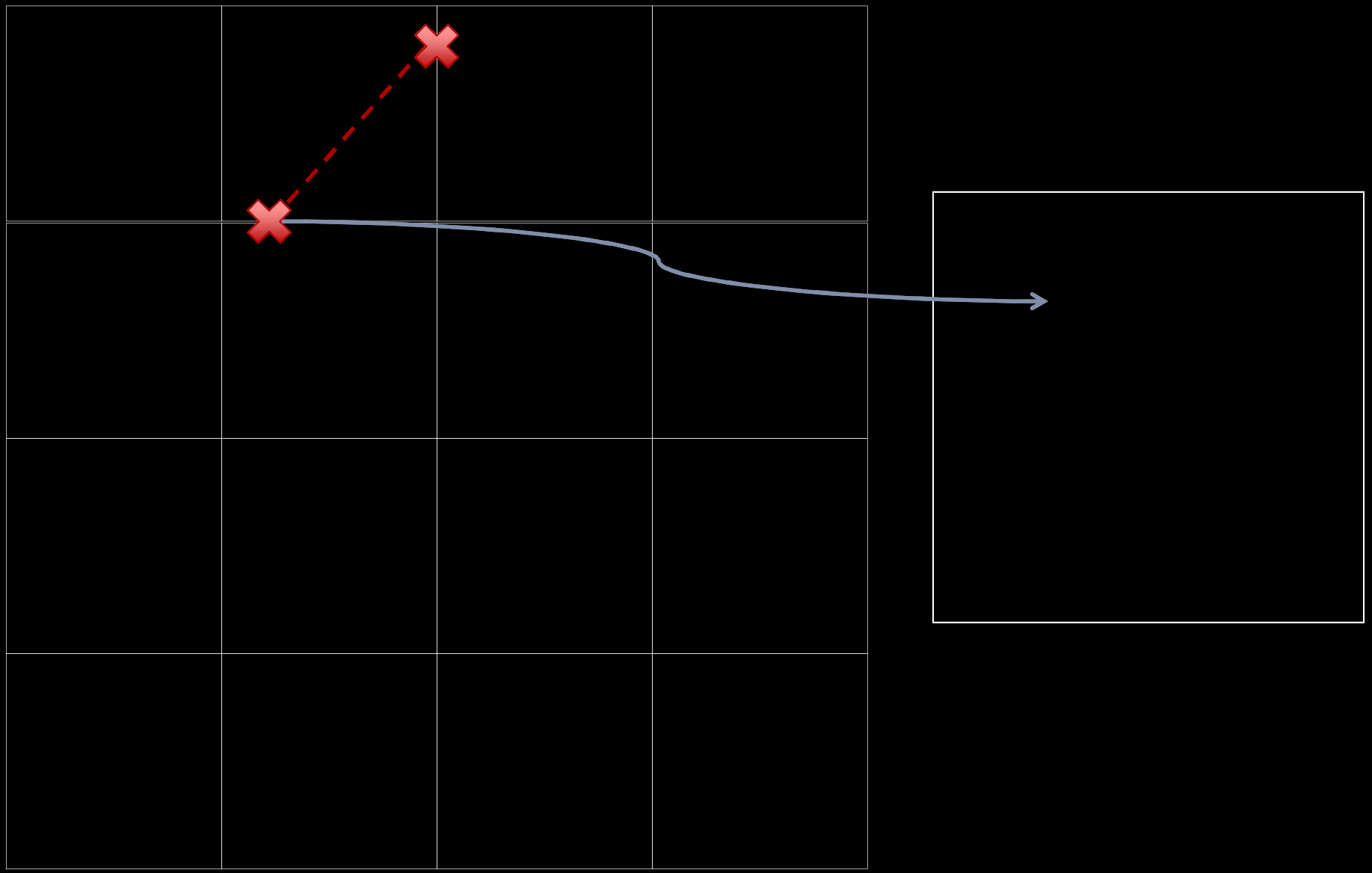
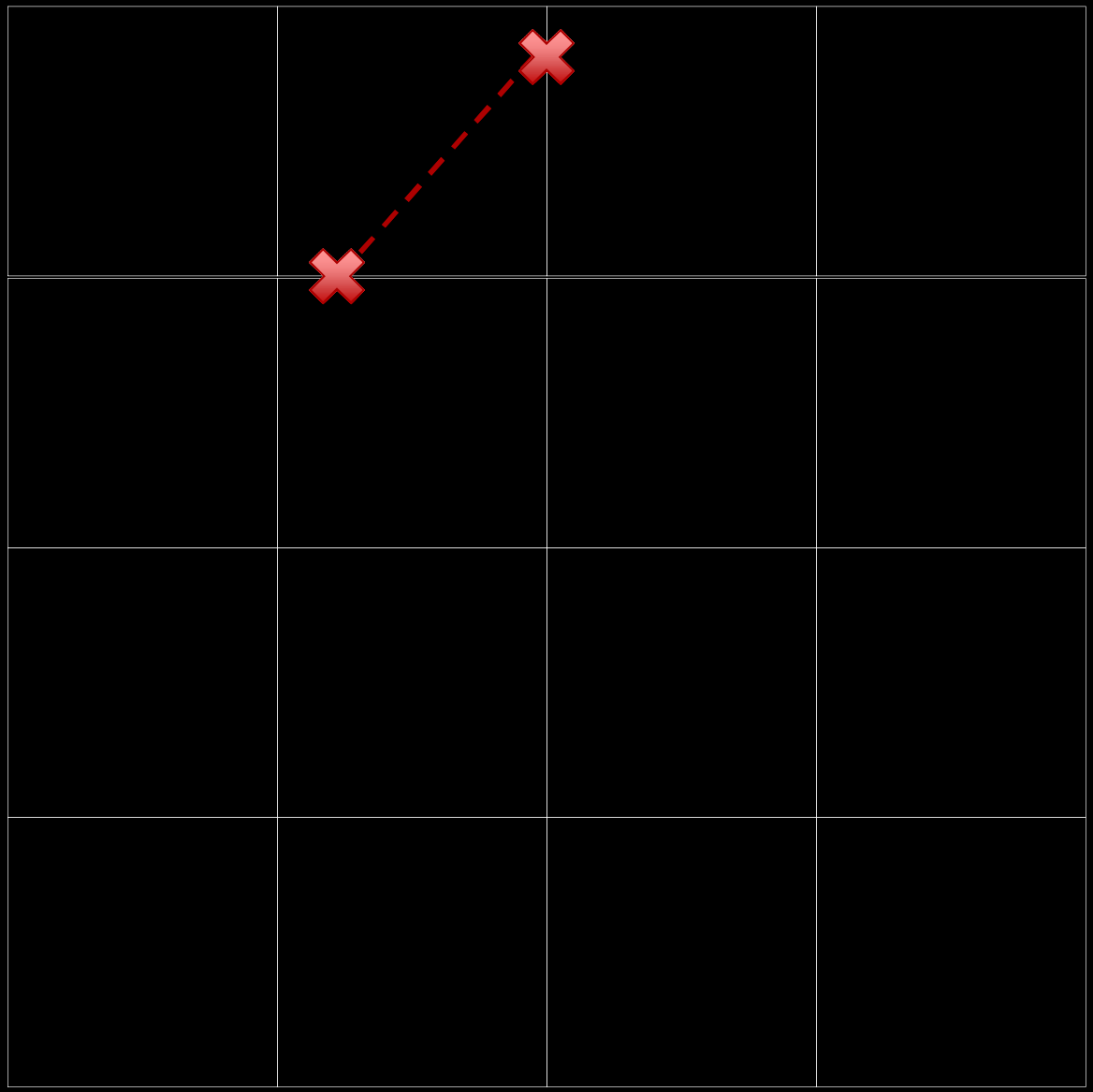


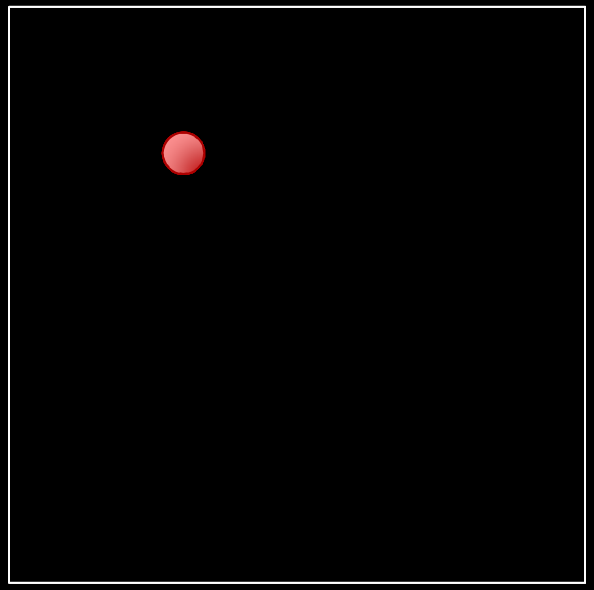


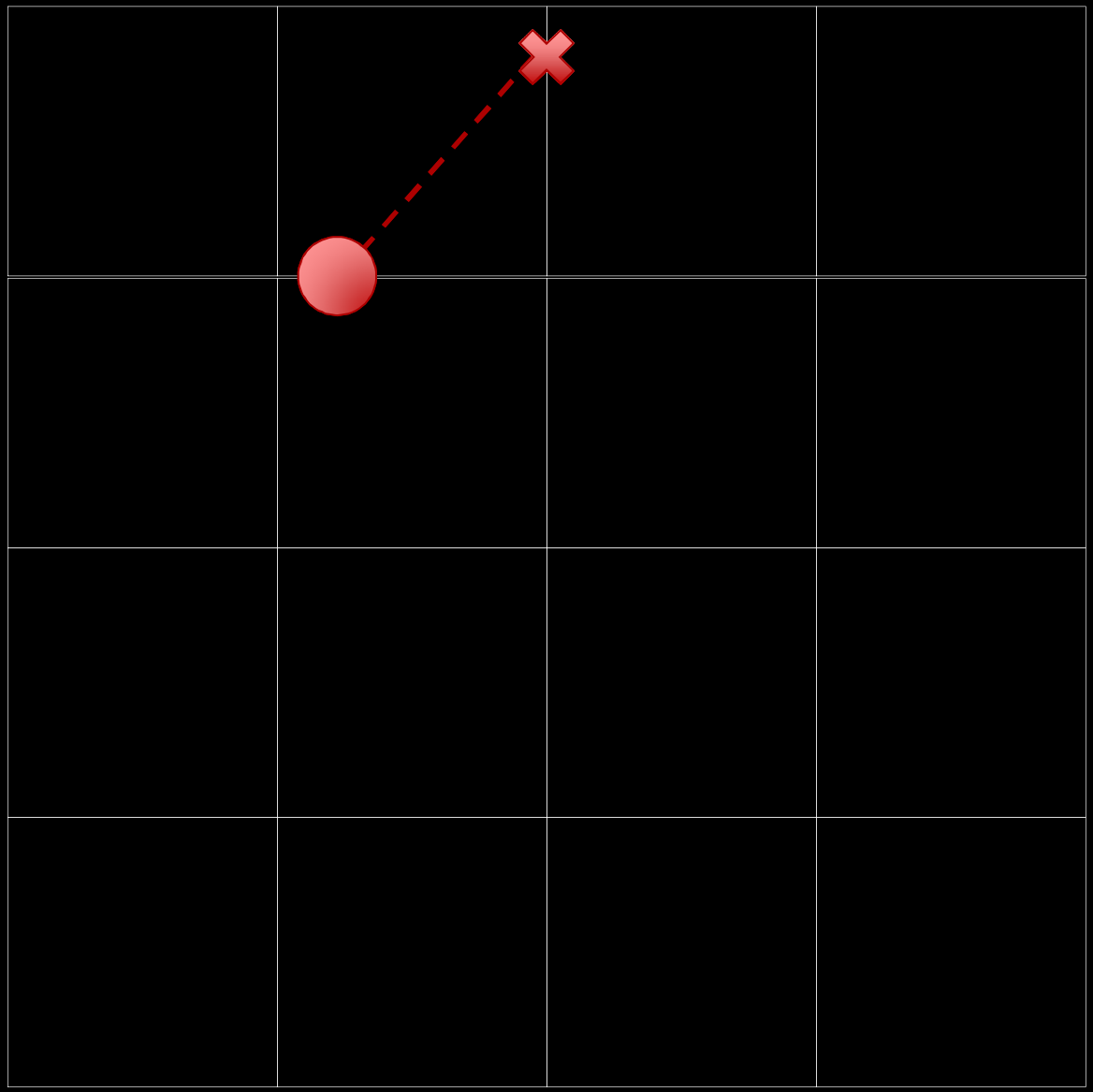


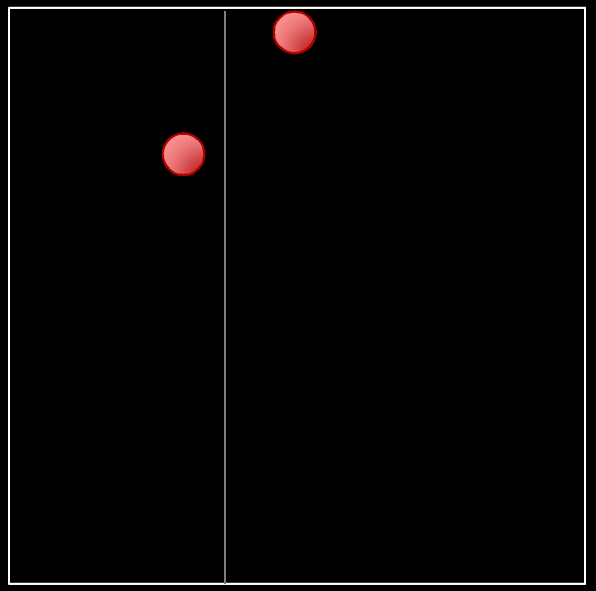


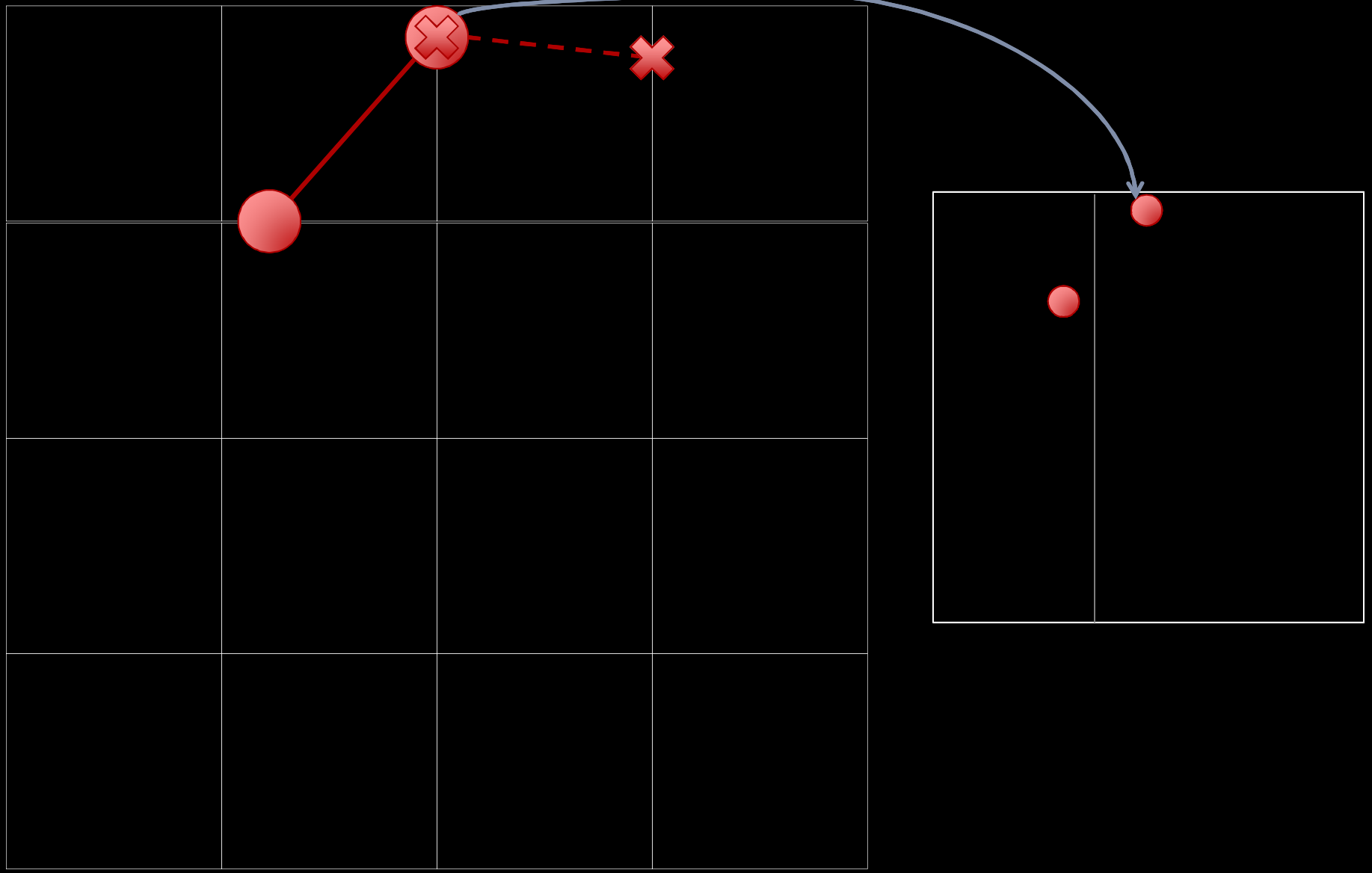


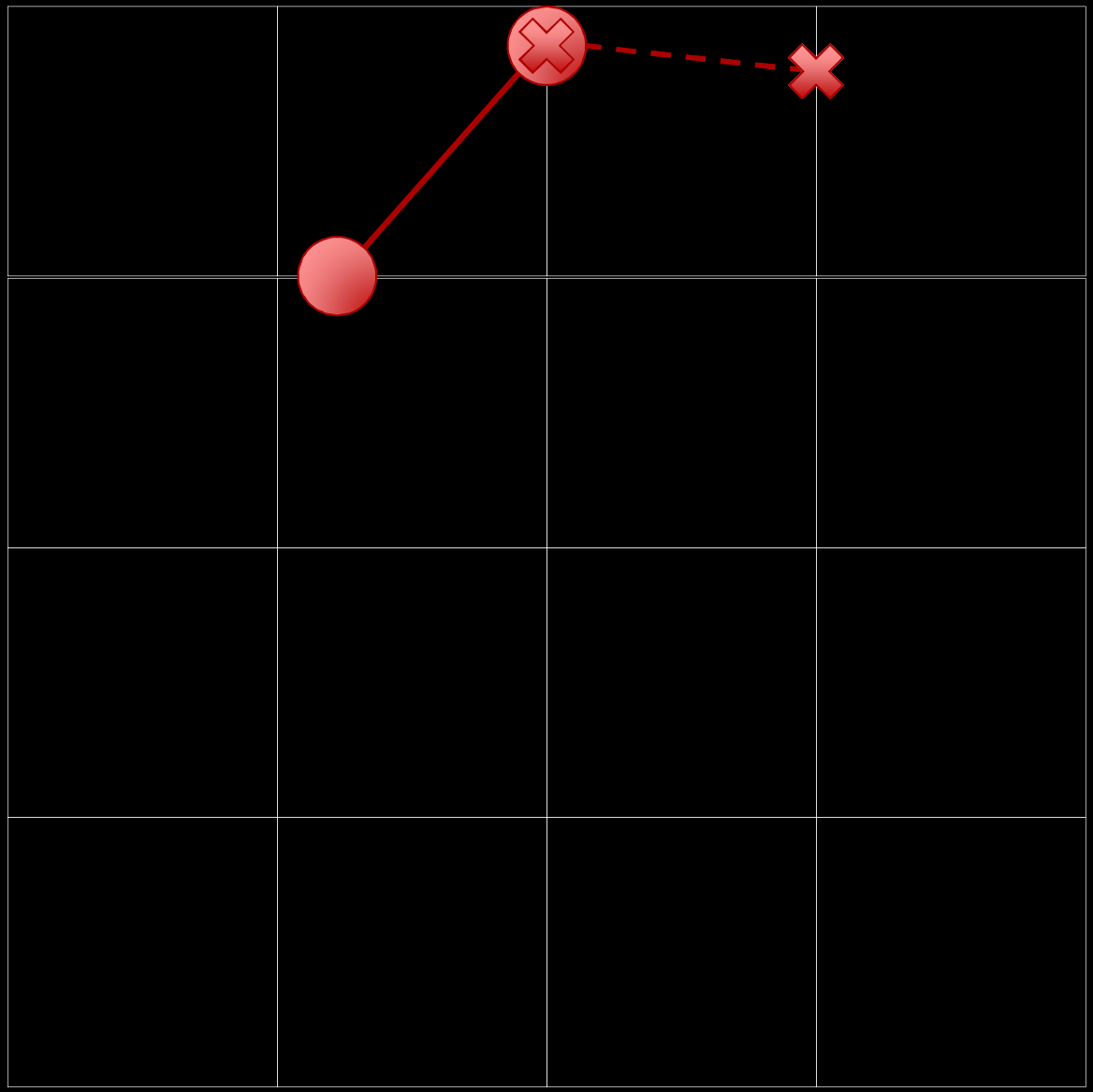


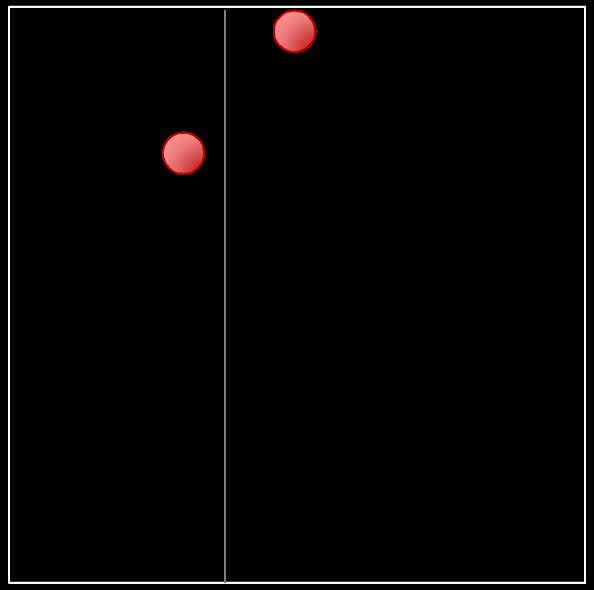


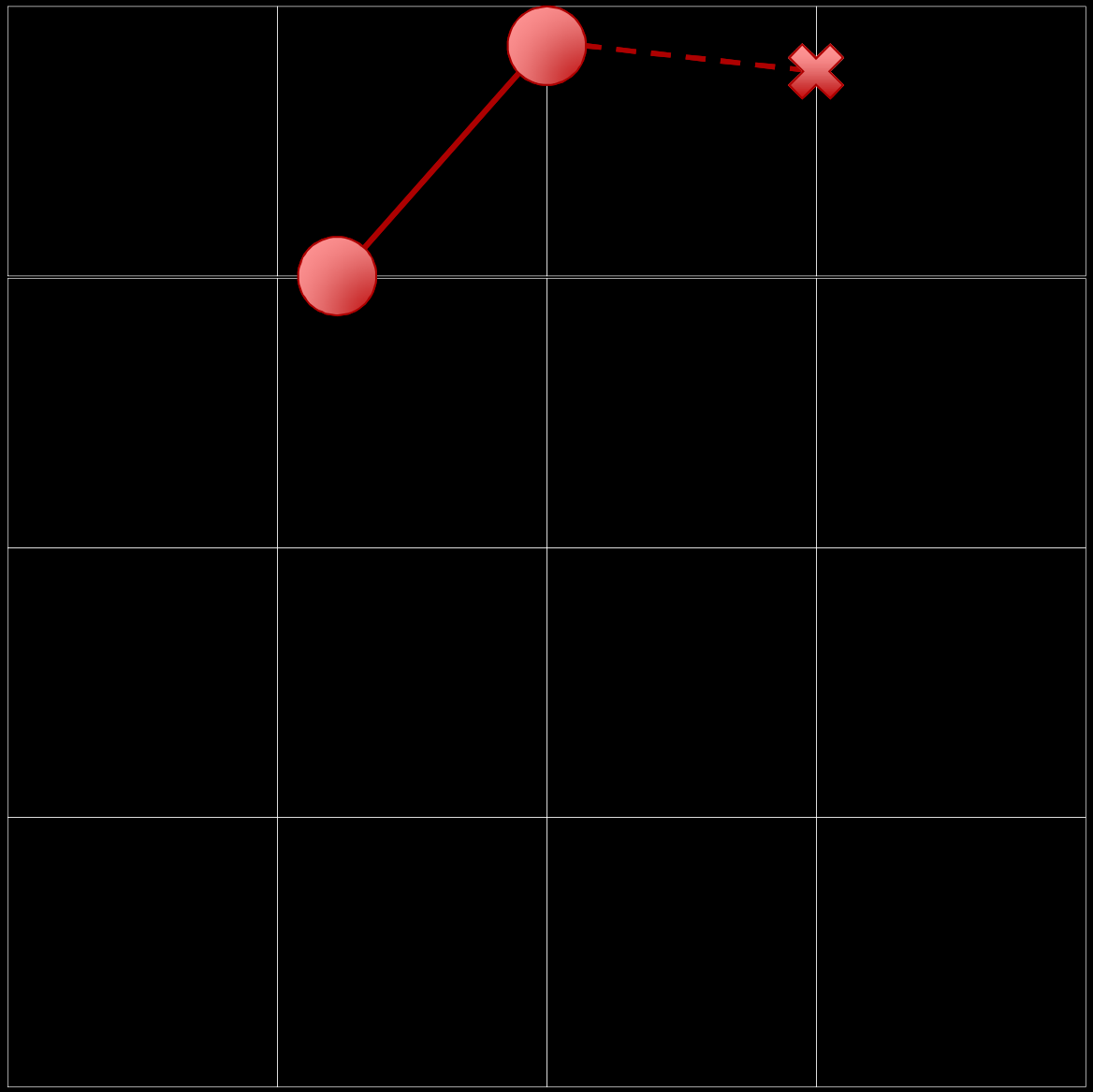


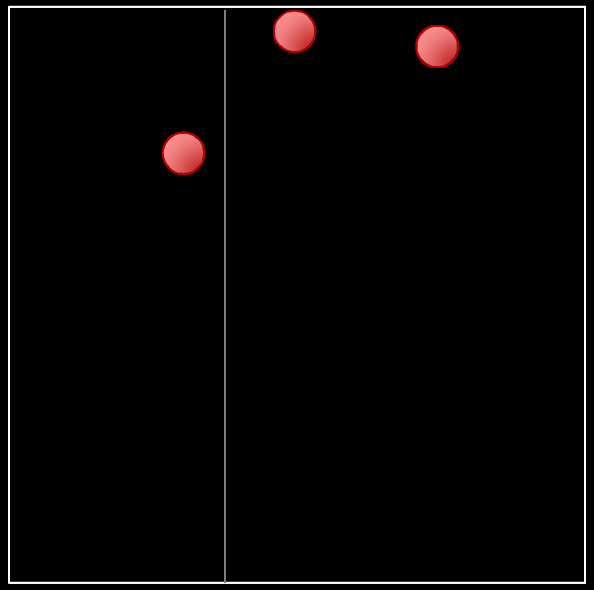


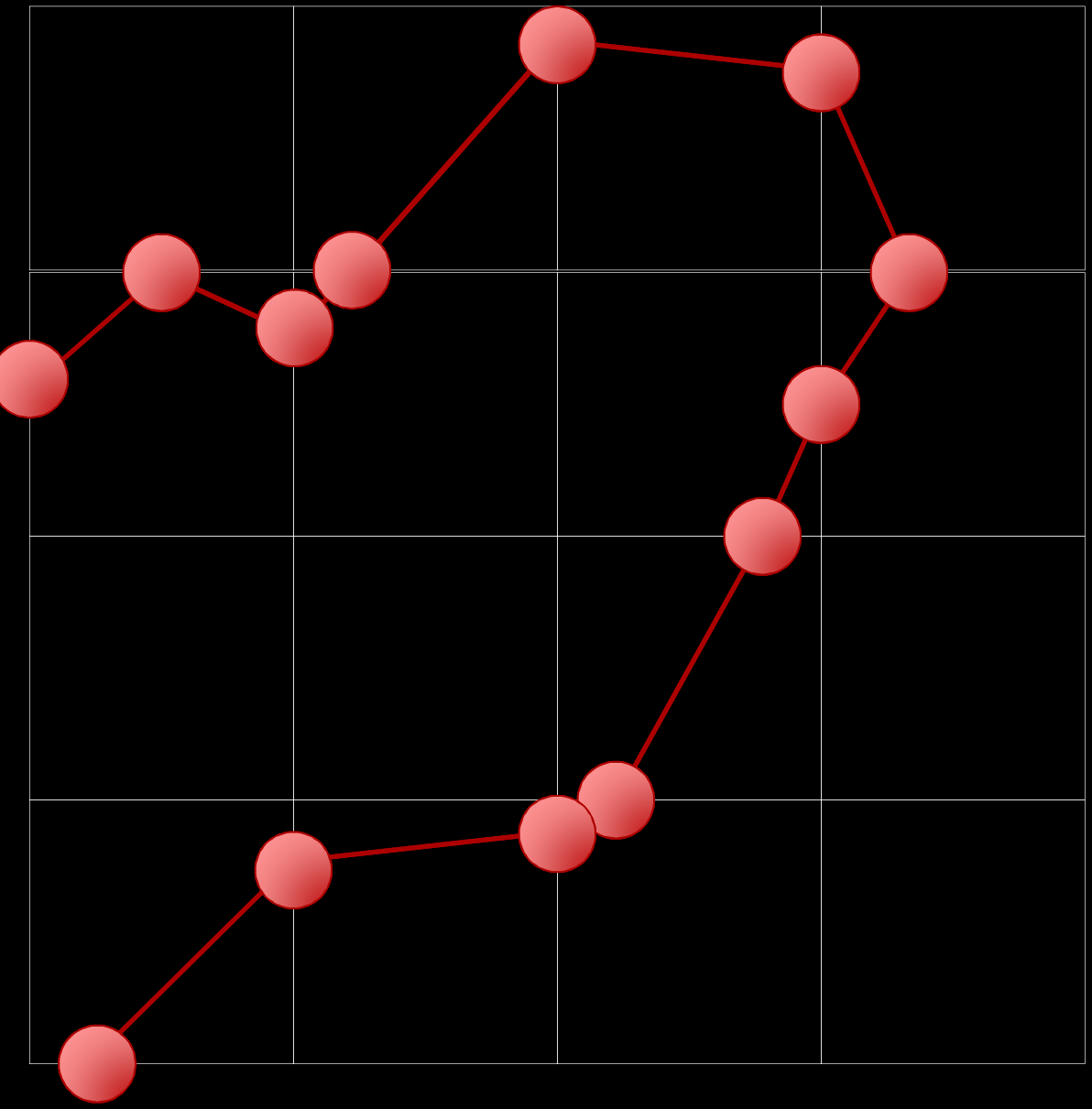


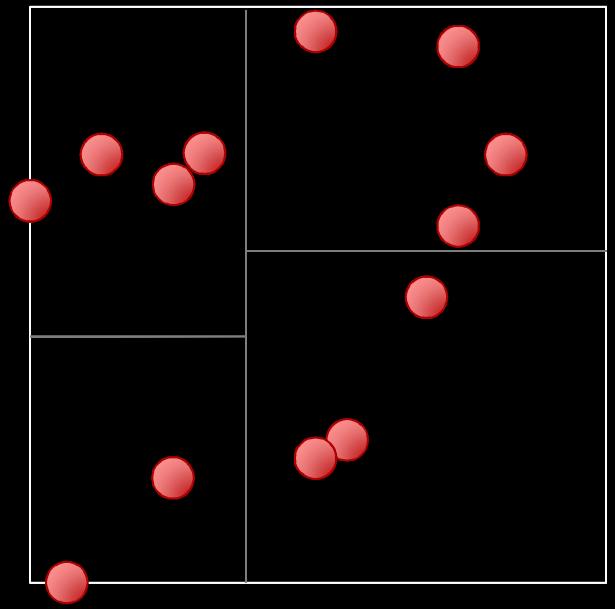


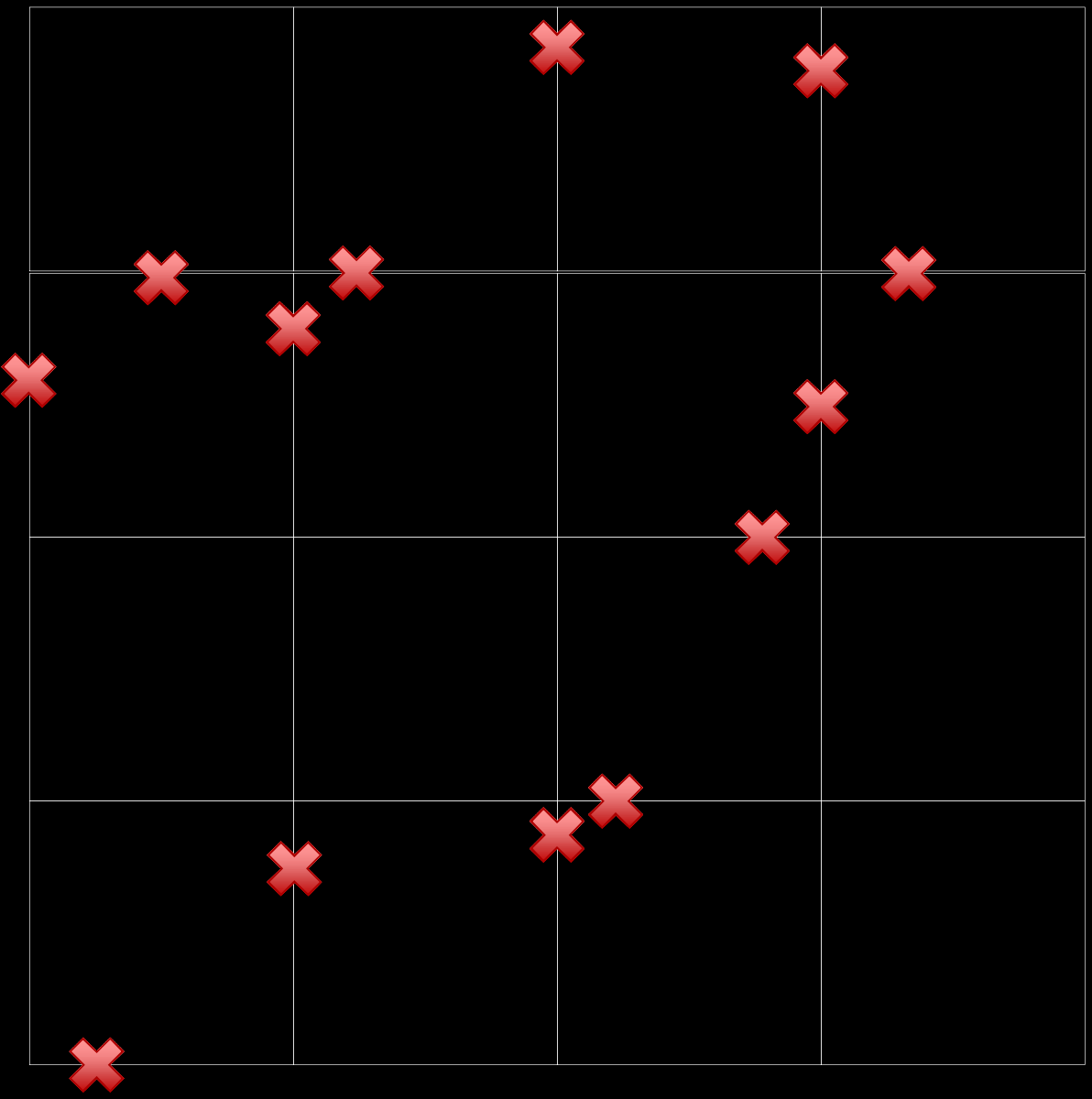


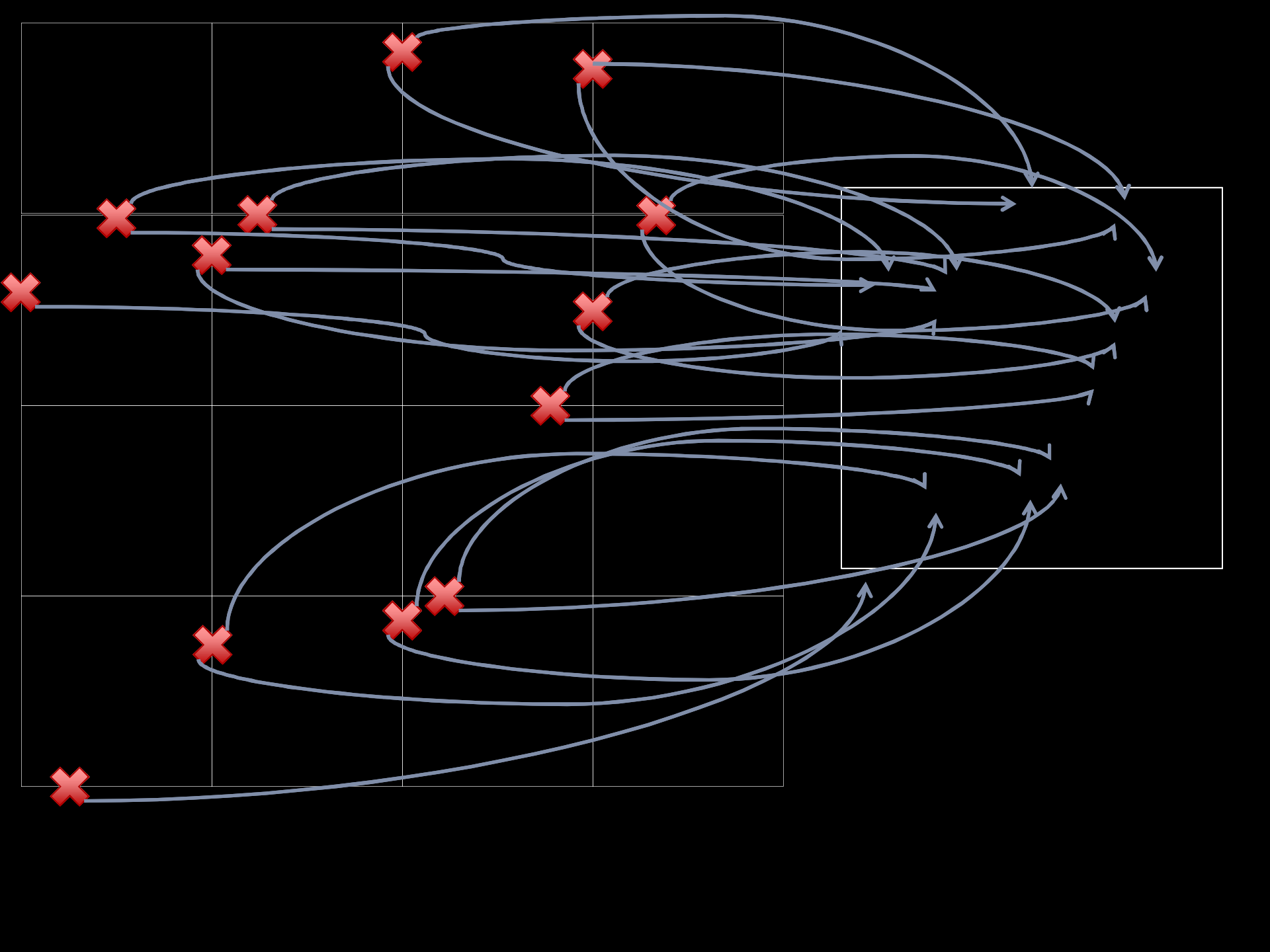


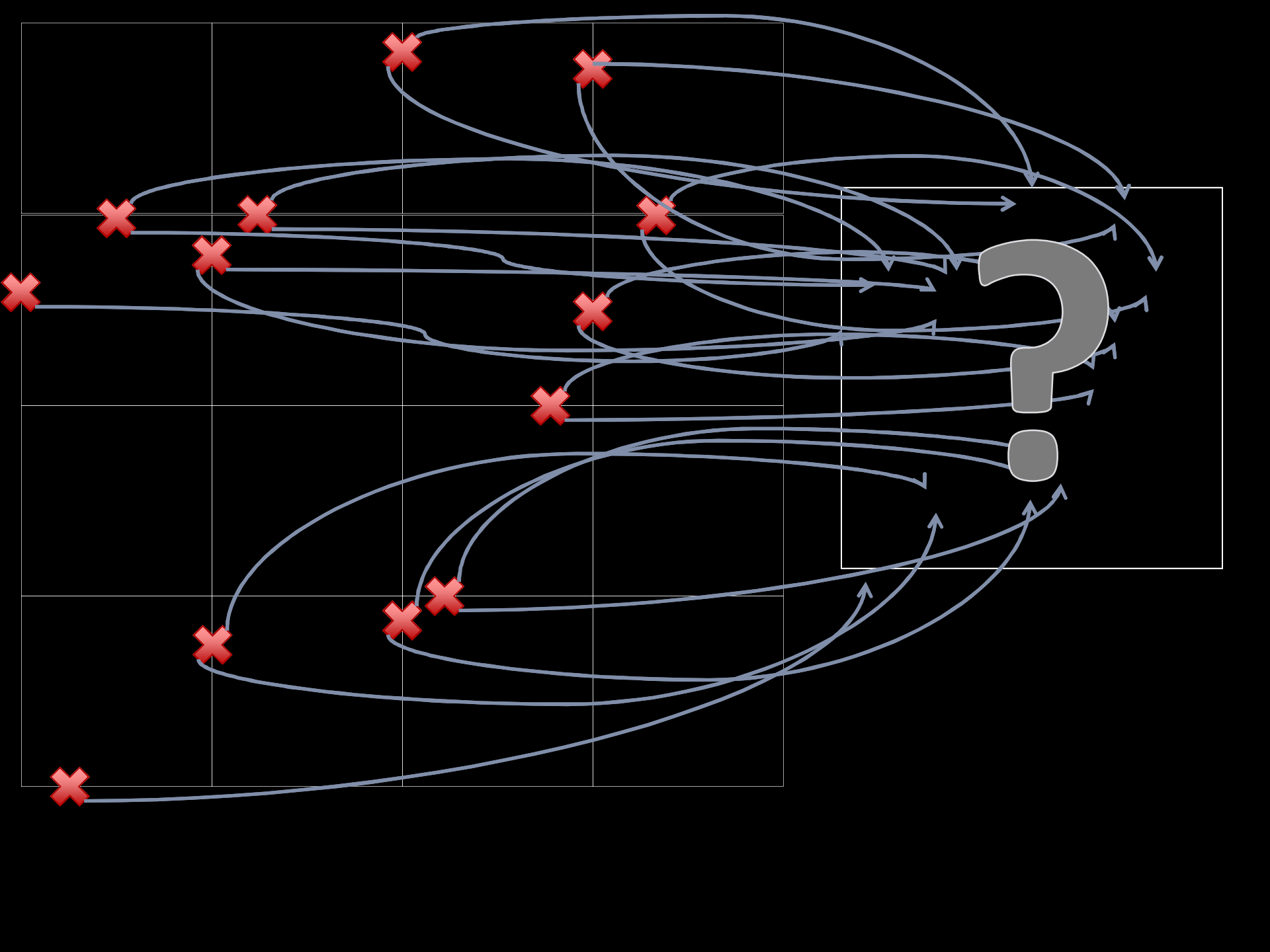


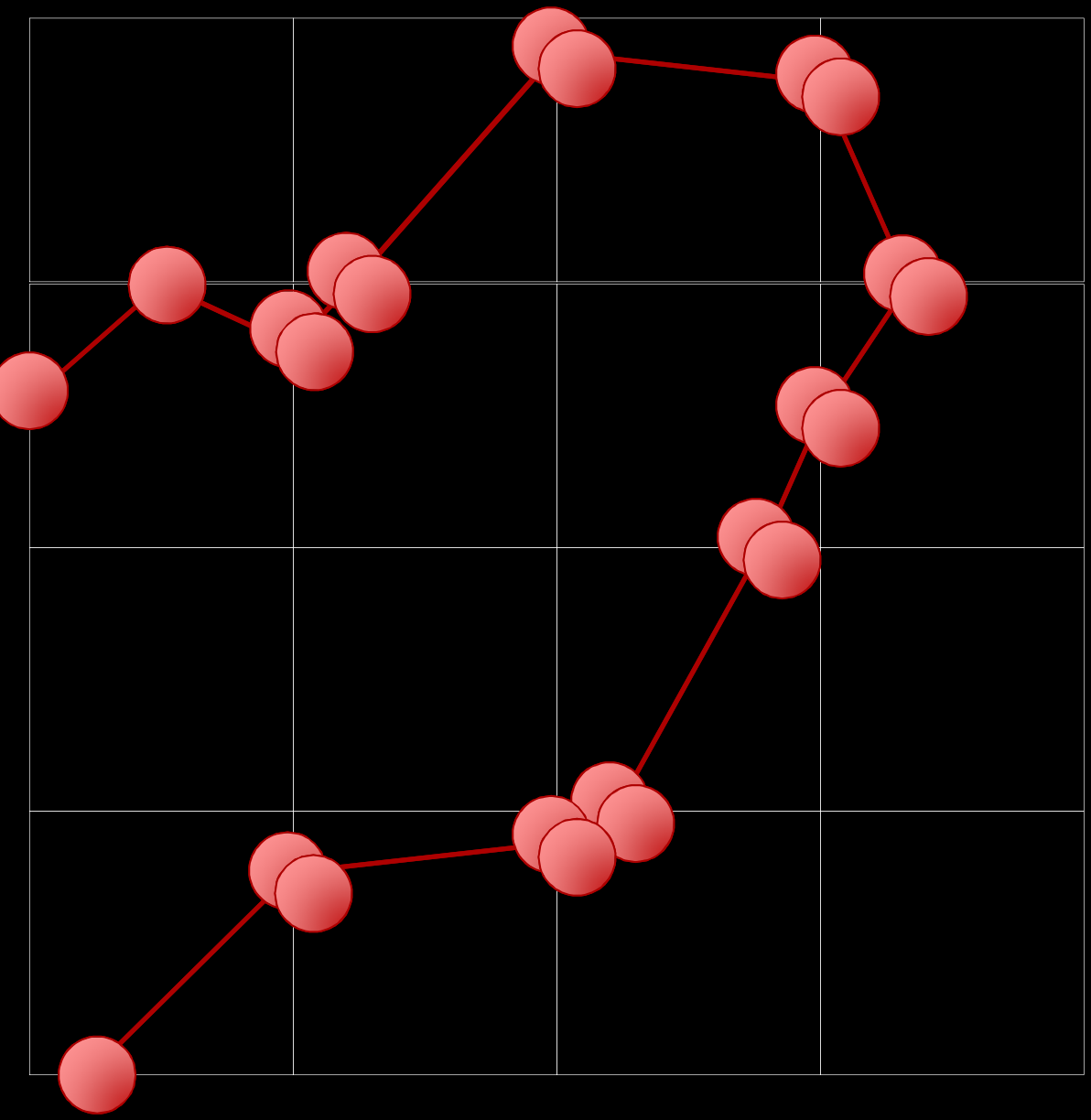






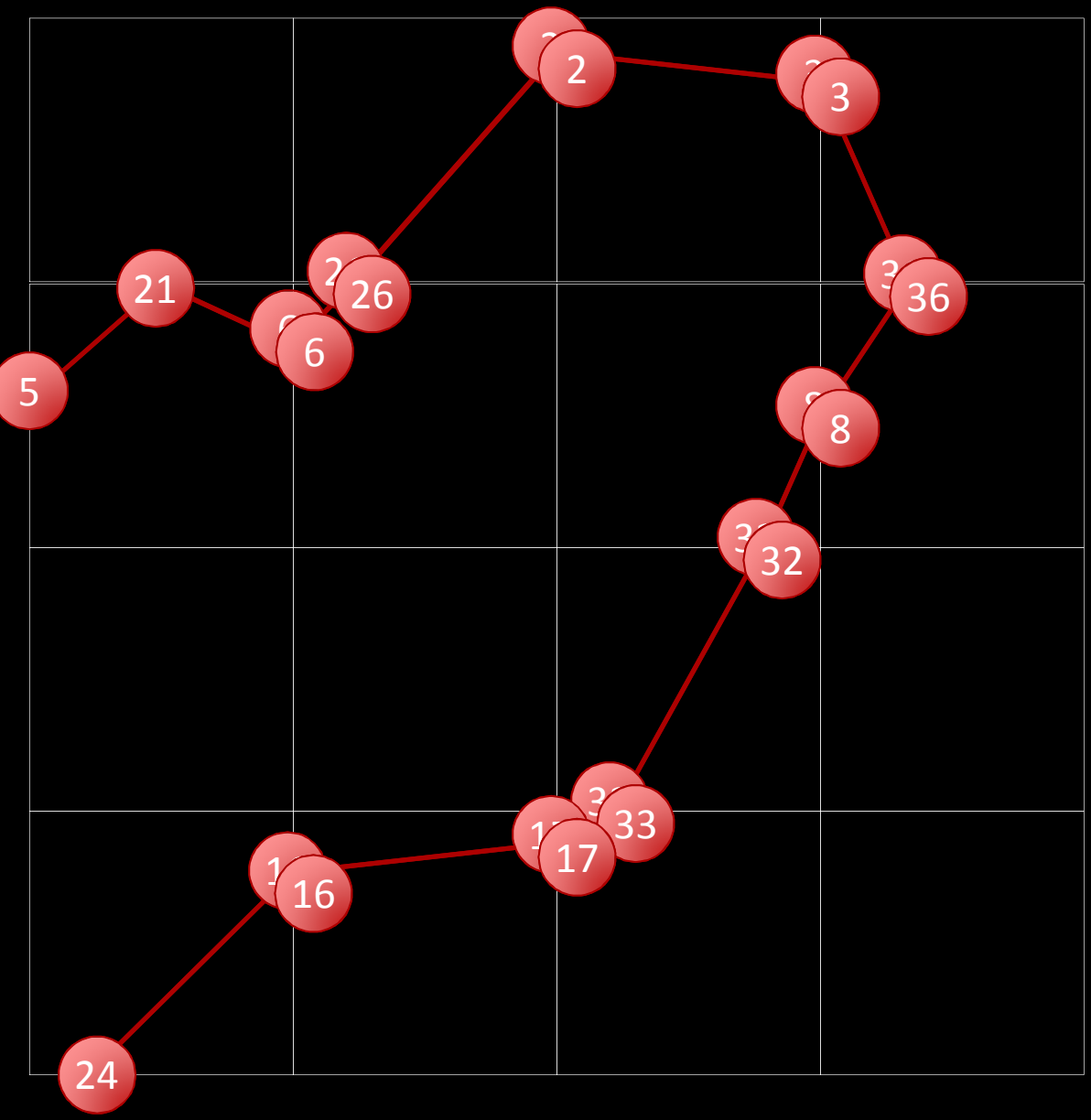






Faceted Normals

Smoothed Normals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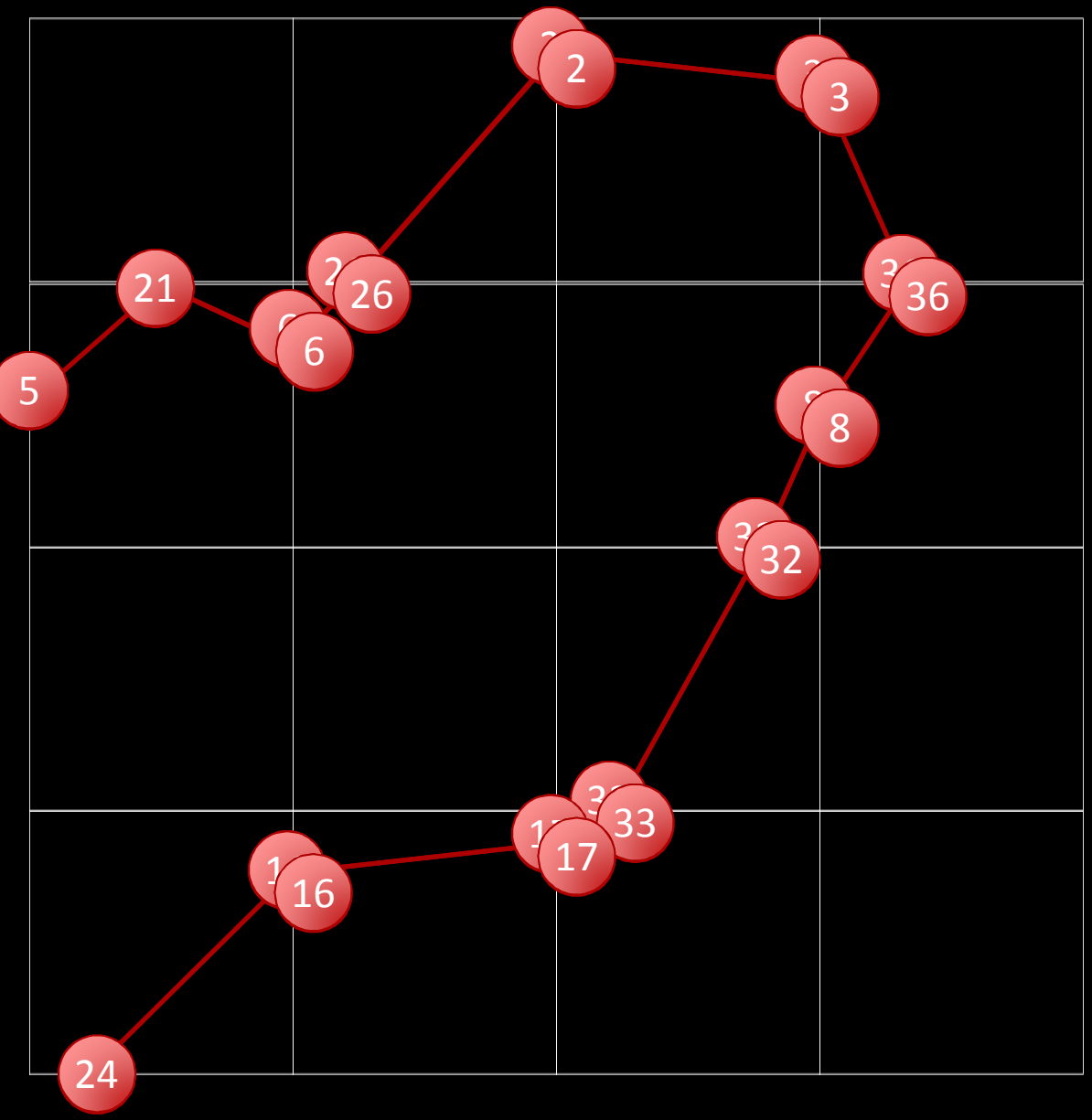
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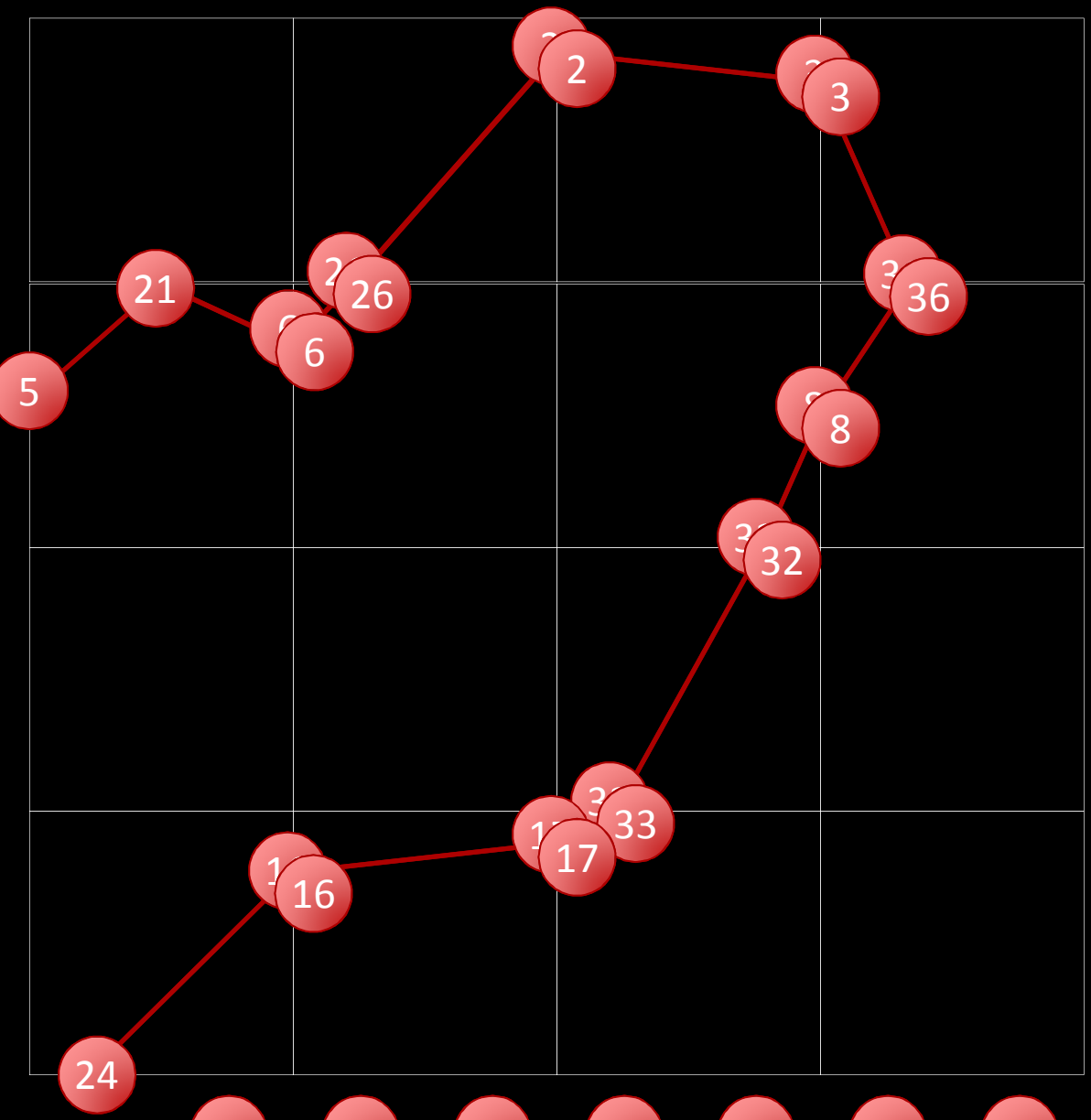

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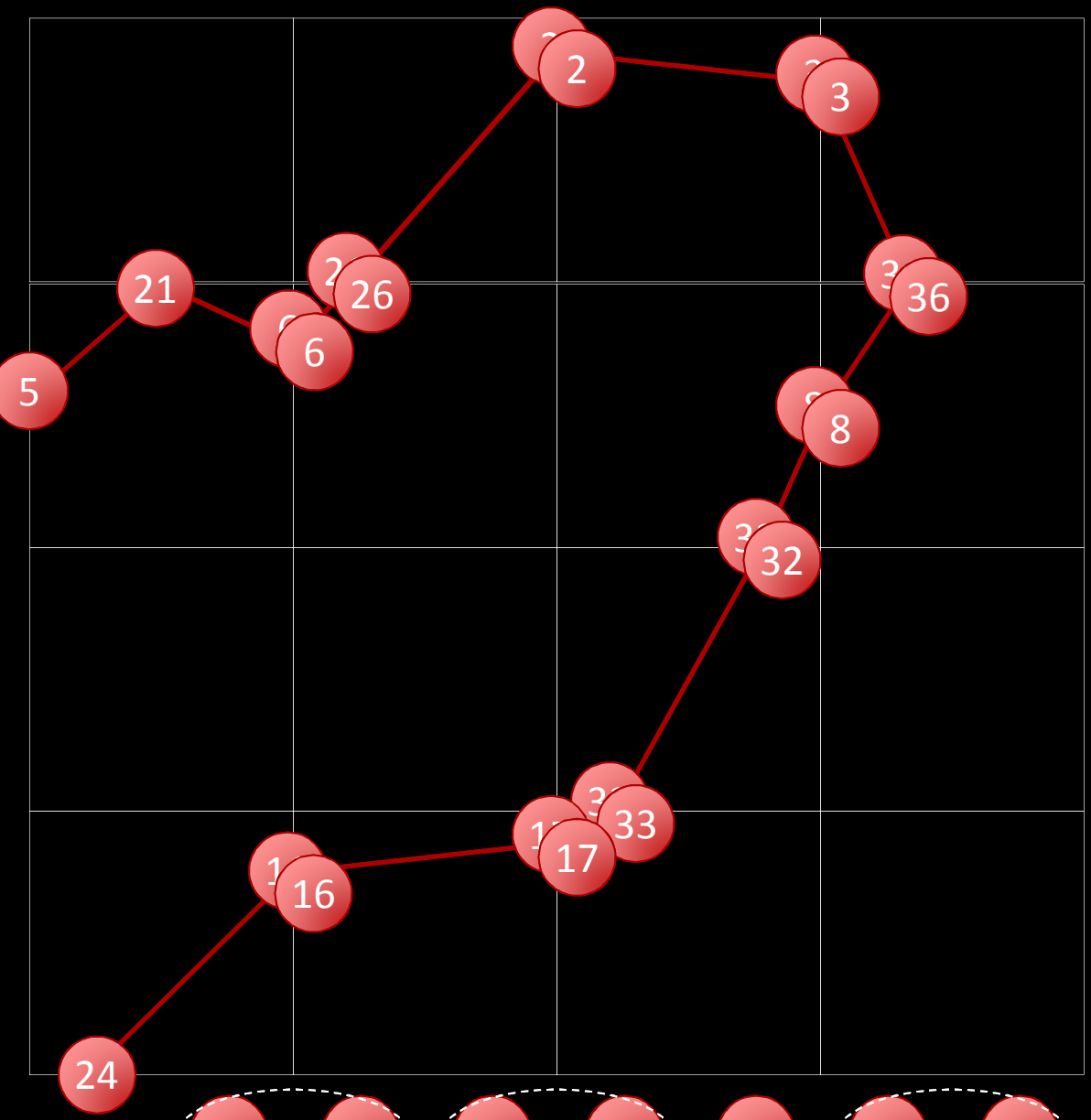

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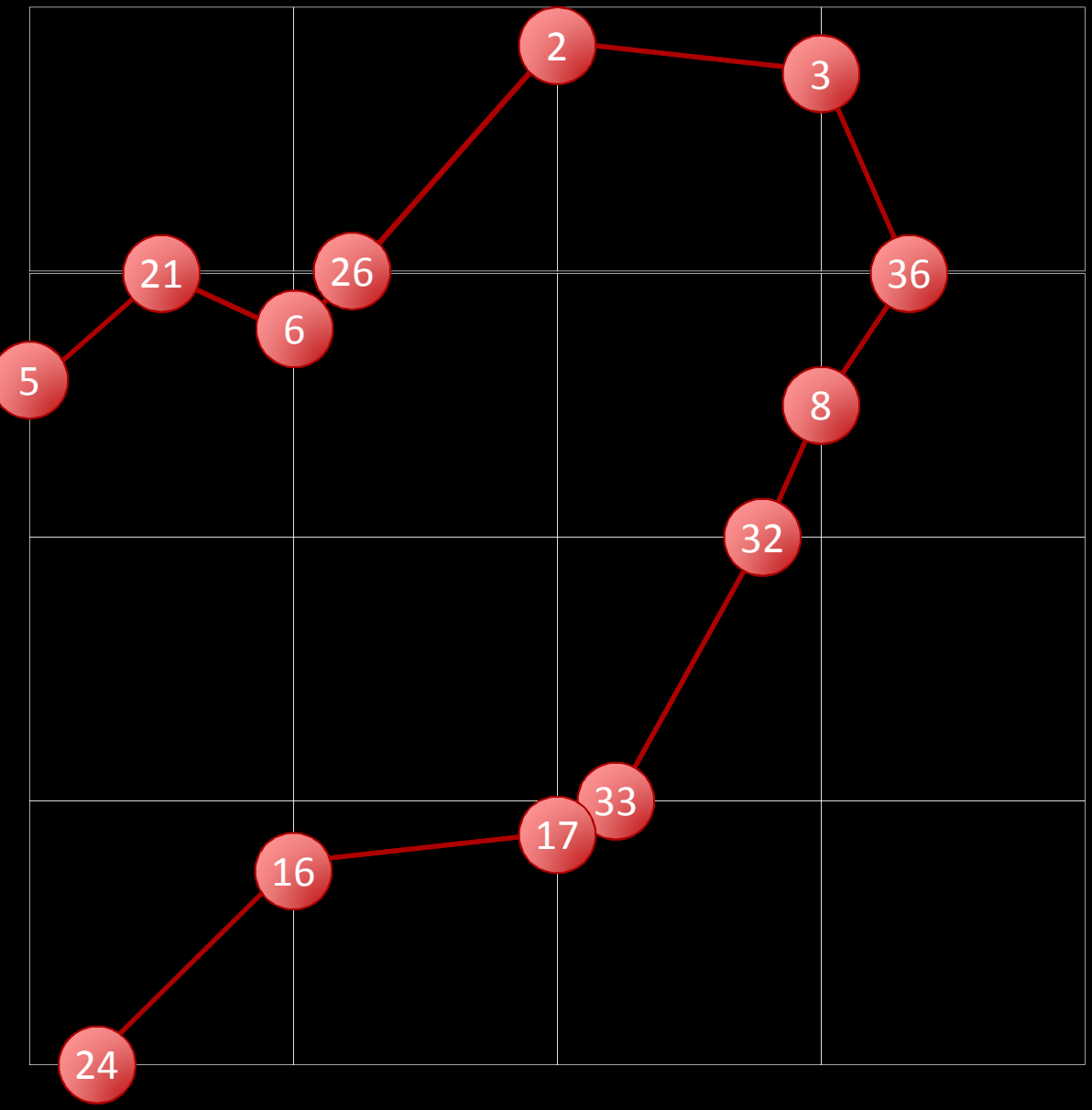
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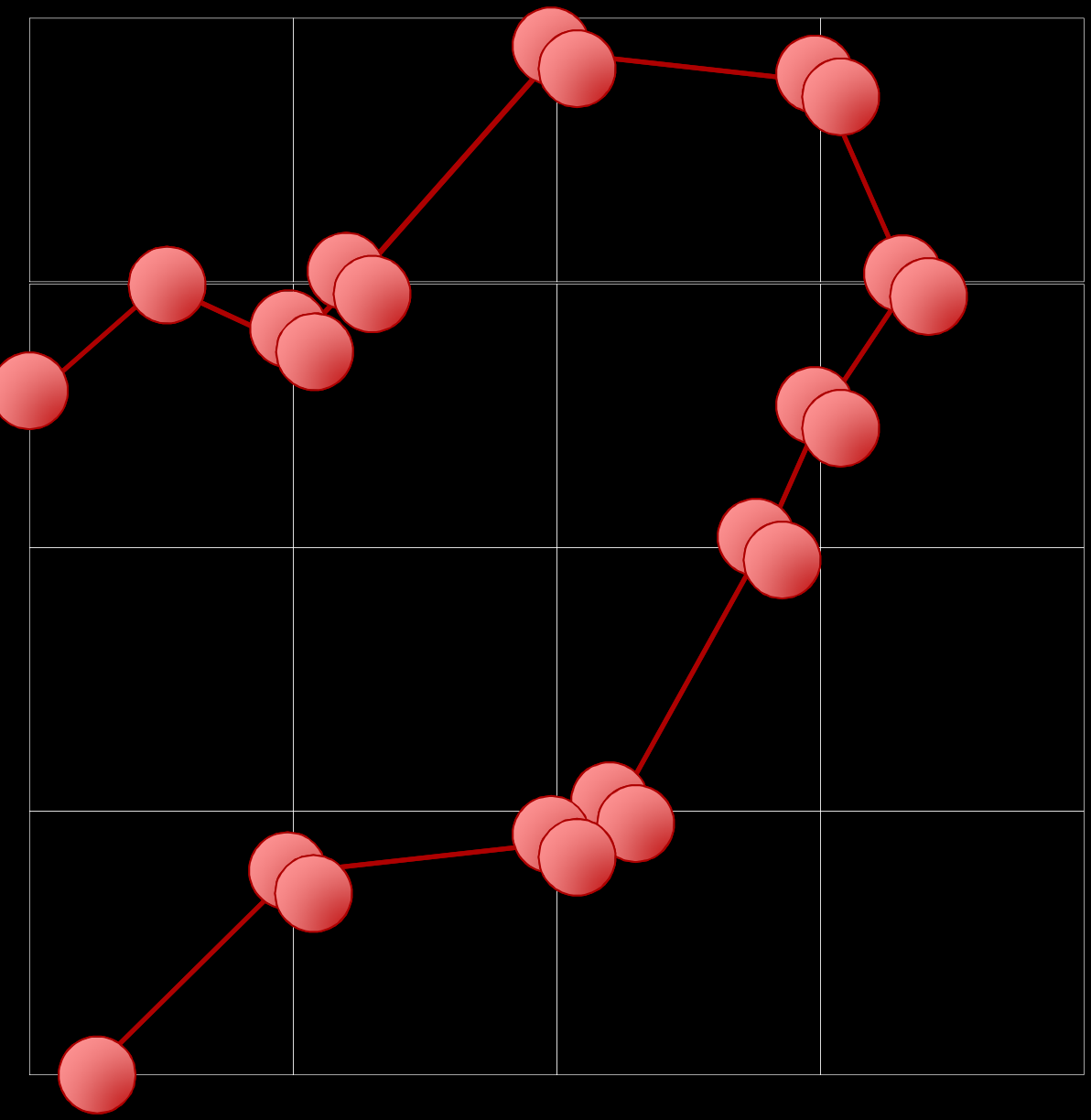
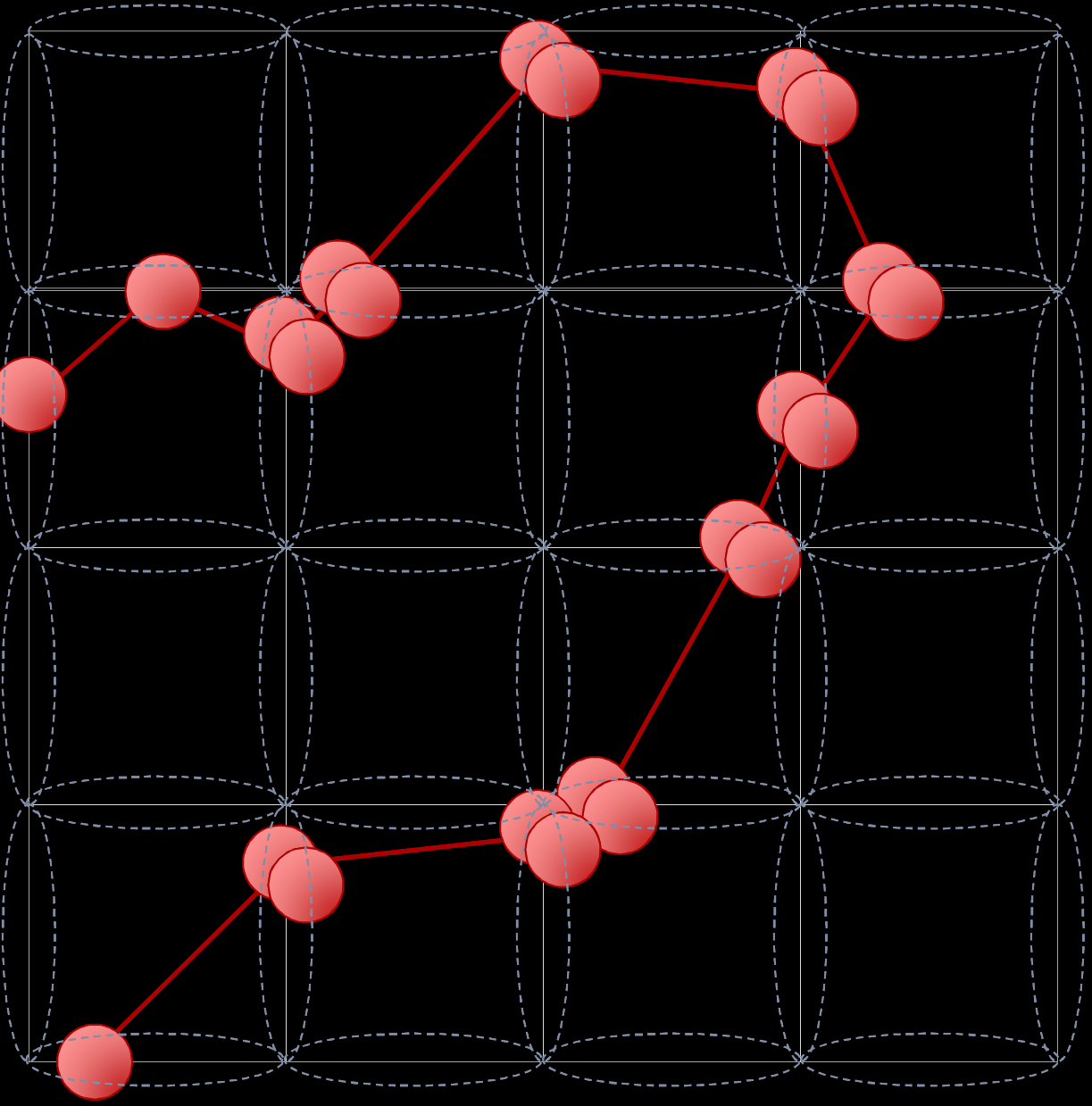
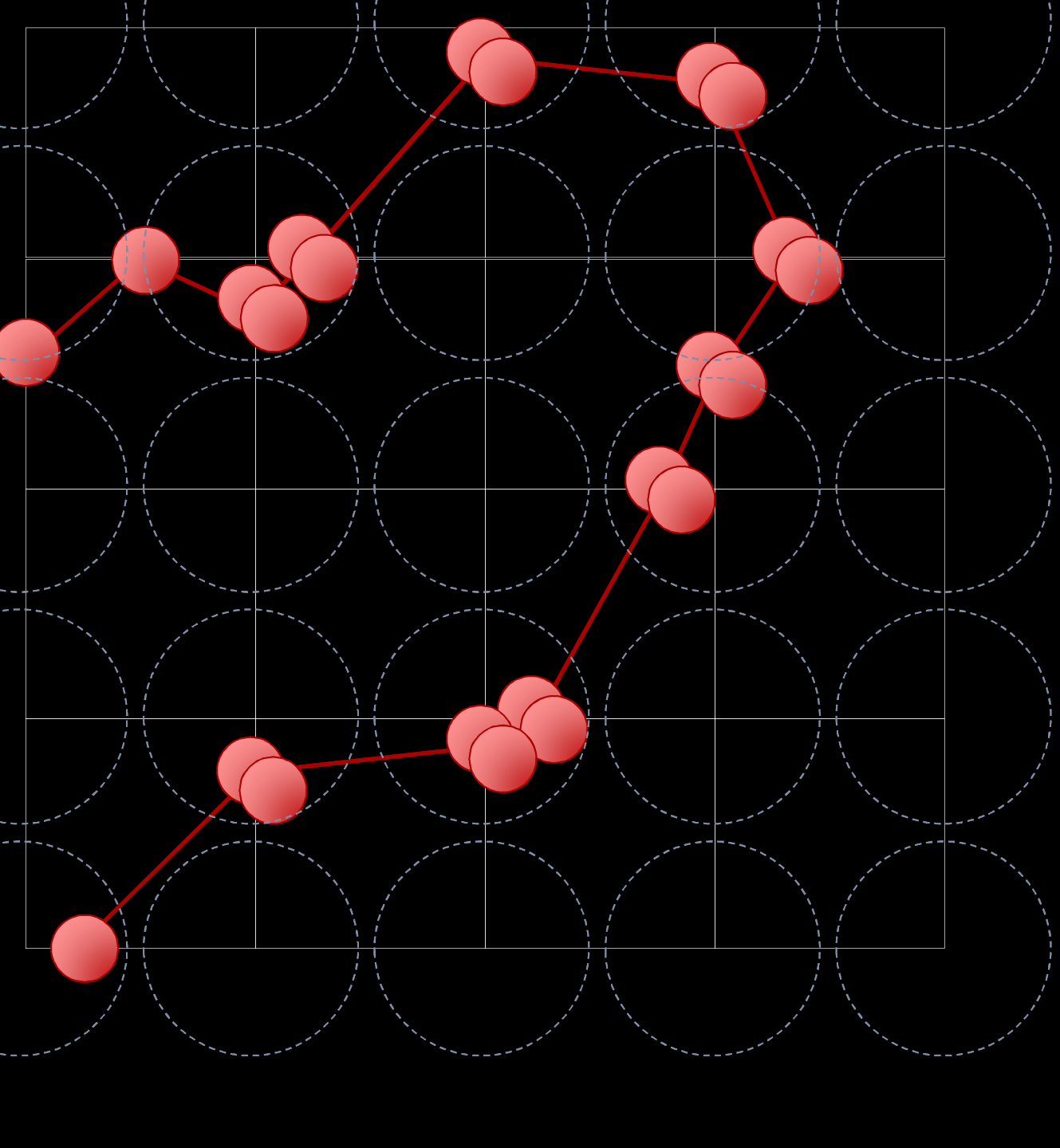


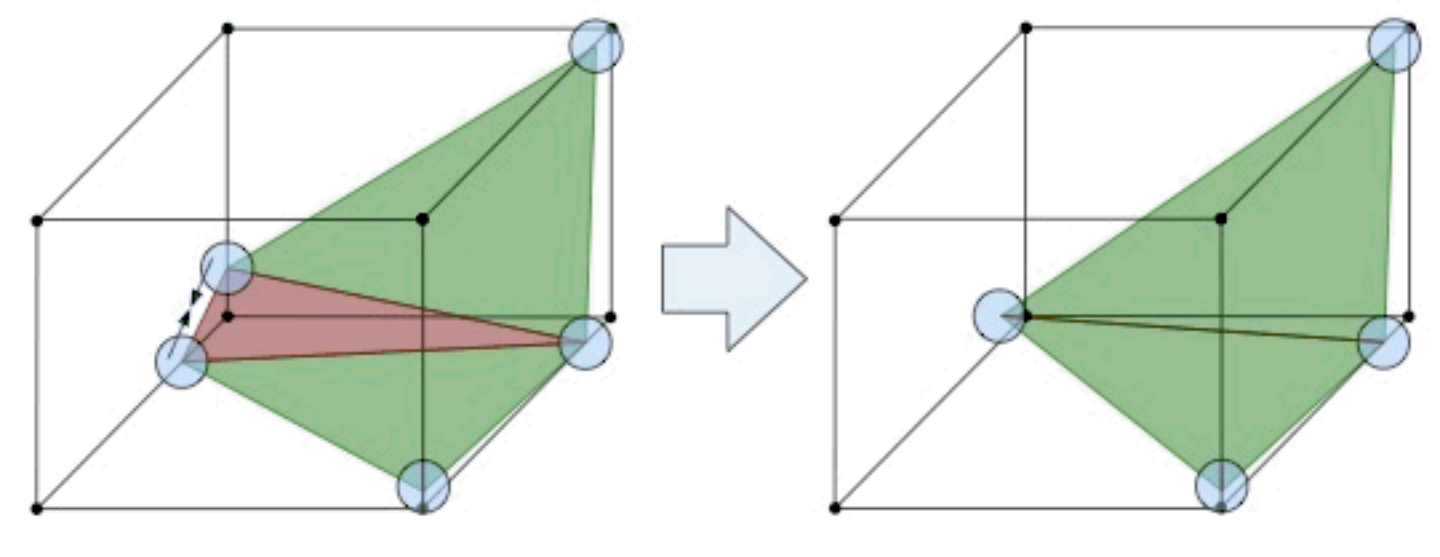


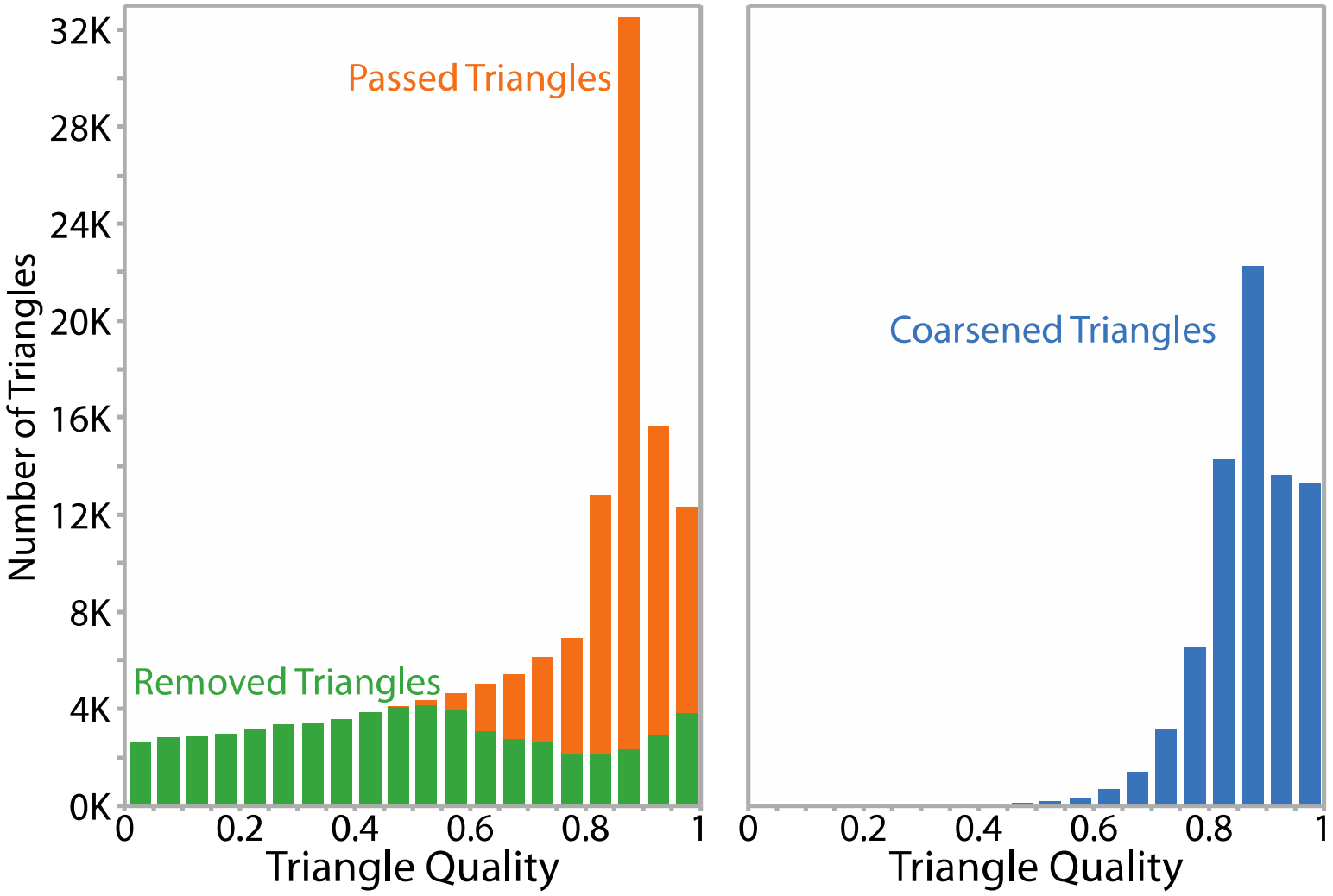


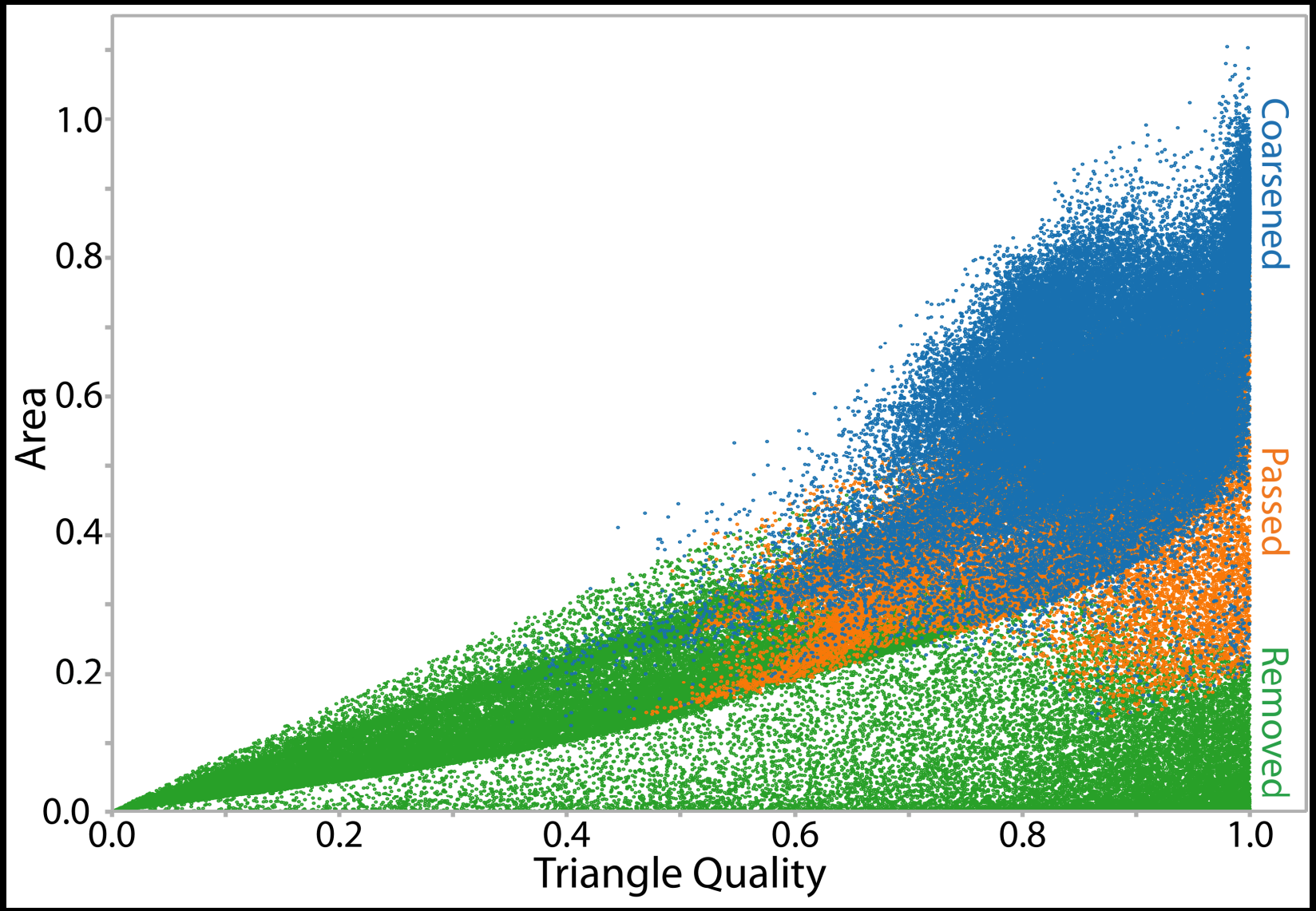
Faceted Normals

Smoothed Normals

Simplified Mesh




Number of Triangles
32K
28K
24K
20K
16K
12K
8K
4K
0K
Passed Triangles
Removed Triangles
0
0.2
0.4
0.6
0.8
1
Triangle Quality
Coarsened Triangles
0
0.2
0.4
0.6
0.8
1
Triangle Quality


Area
1.0
0.8
0.6
0.4
0.2
0.0
0.0
0.2
0.4
0.6
0.8
1.0
Triangle Quality
Coarsened
Passed
Removed

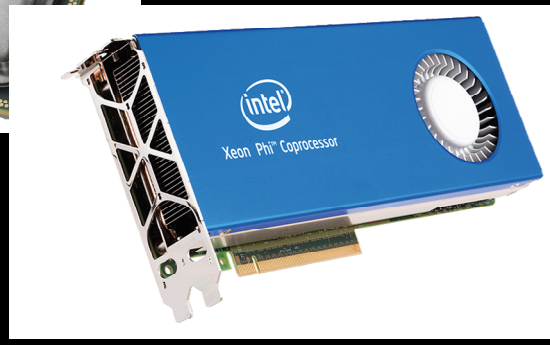
Like a washbasin knocking on your door…

we’re gonna let that sink in.

How Many Architectures To Support?

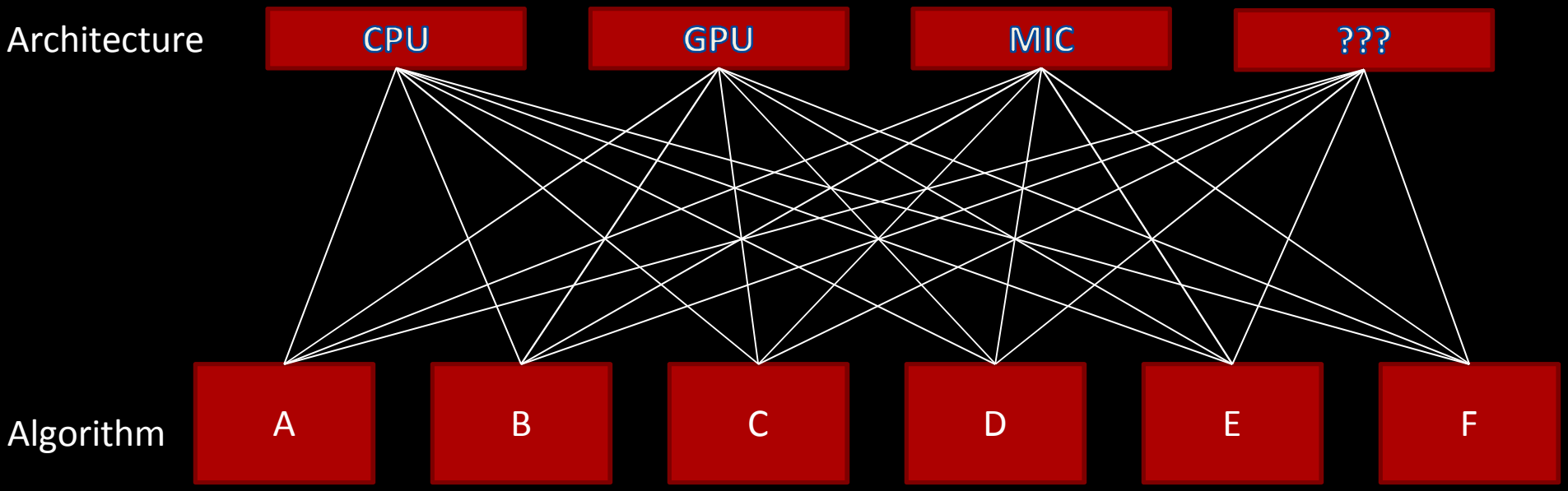
- GPU (NVIDIA)
  - Sub-architectures :
    - Fermi, Kepler, Maxwell
  - Multiple Memory Types:
    - Global, shared, constant, texture
  - Memory Amount:
    - Up to 12 GB
  - 1000s of threads
    - Grids, Blocks, and Warps

- CPU/MIC
  - Multiple ISAs:
    - Vector Unit Widths:
      - » 2,4,8 / 16
  - Single Memory Type
  - Larger Memory Size (CPU)
  - Up to 20/60 threads
    - No explicit organization



Performance Portability

- Visualization developers faced with a decision:
  - Pick a target architecture
  - Add additional implementations of the same algorithm:



Data Parallel Primitives

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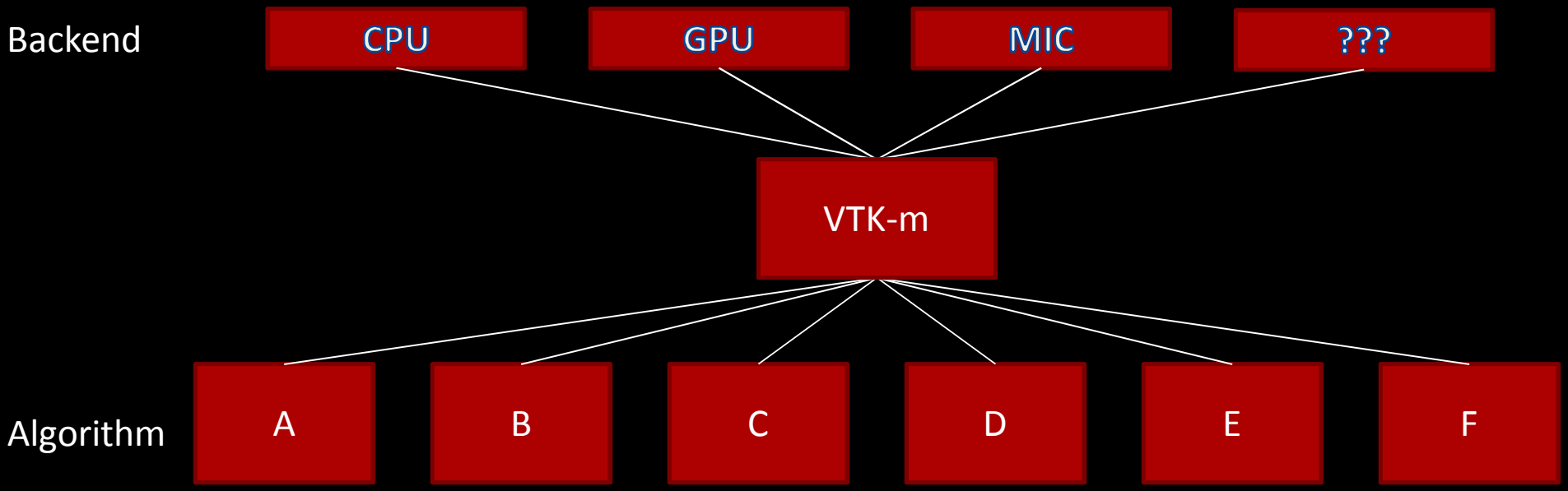
- What are they?
  - Provide a level of abstraction based on Blelloch's parallel primitive operators
    - Examples: Map, Reduce, Scan, Gather, Scatter, Sort
    - Provides node-level parallelism
- Benefits
  - Portable performance
  - Future-proofed implementations
  - Higher productivity

Data Parallel Primitives Benefit

- Backend: Implement fast parallel primitive operators for each new architecture
- Frontend: Re-think current algorithms in terms of the primitives



1. input

transform(classify_cell)

2. caseNums

3. numVertices

transform_inclusive_scan(is_valid_cell)

4. validCellEnum

5. CountingIterator

upper_bound

6. validCellIndices

make_permutation_iterator

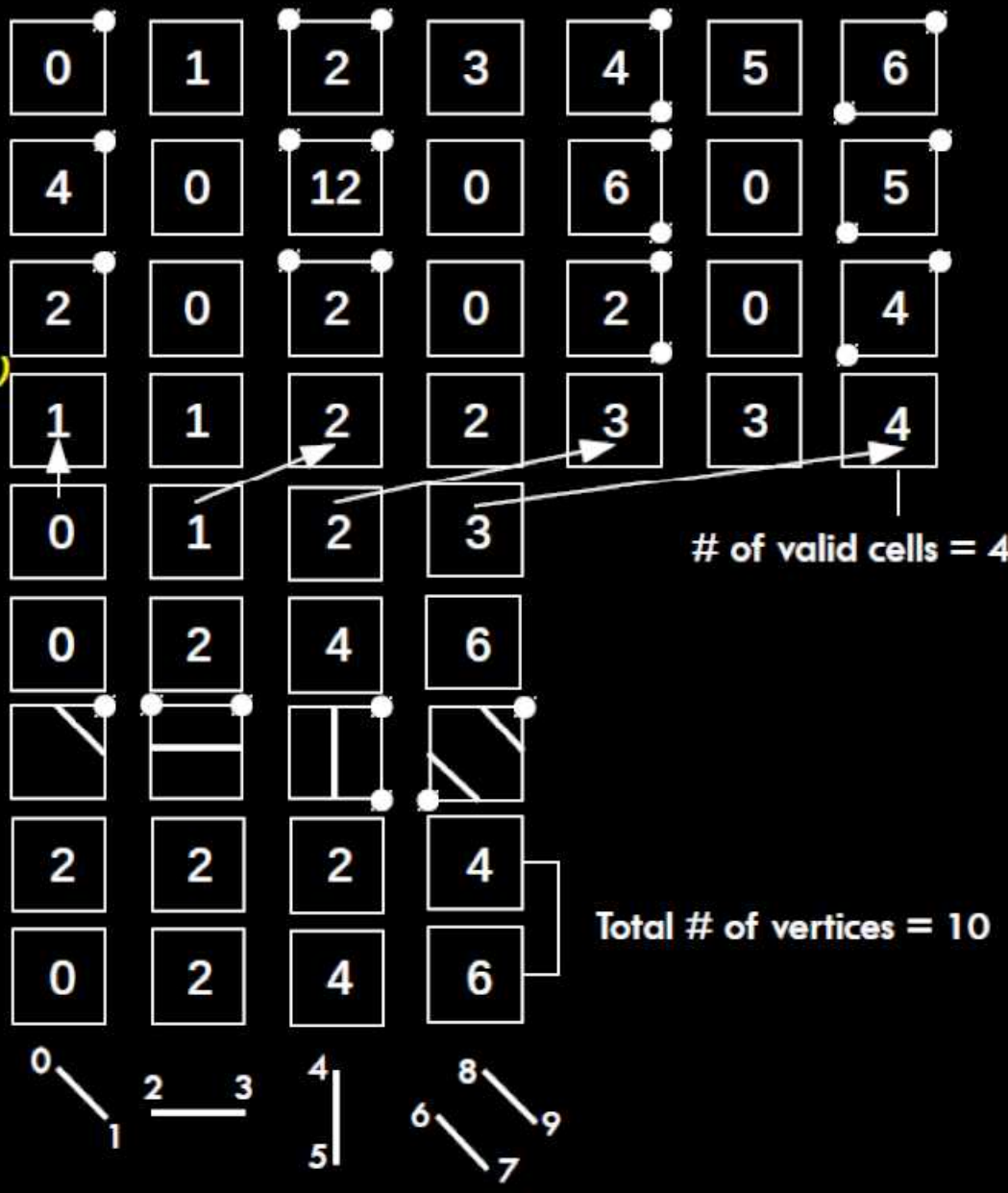
7. numVerticesCompacted

exclusive_scan

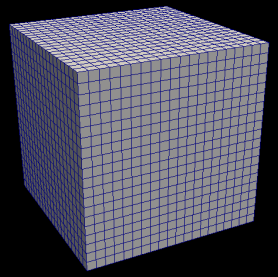
8. numVerticesEnum

for_each(isosurface_functor)

9. outputVertices



VTK-m Framework



Control Environment

Grid Topology
Array Handle
Invoke

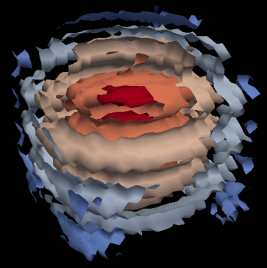
Device Adapter

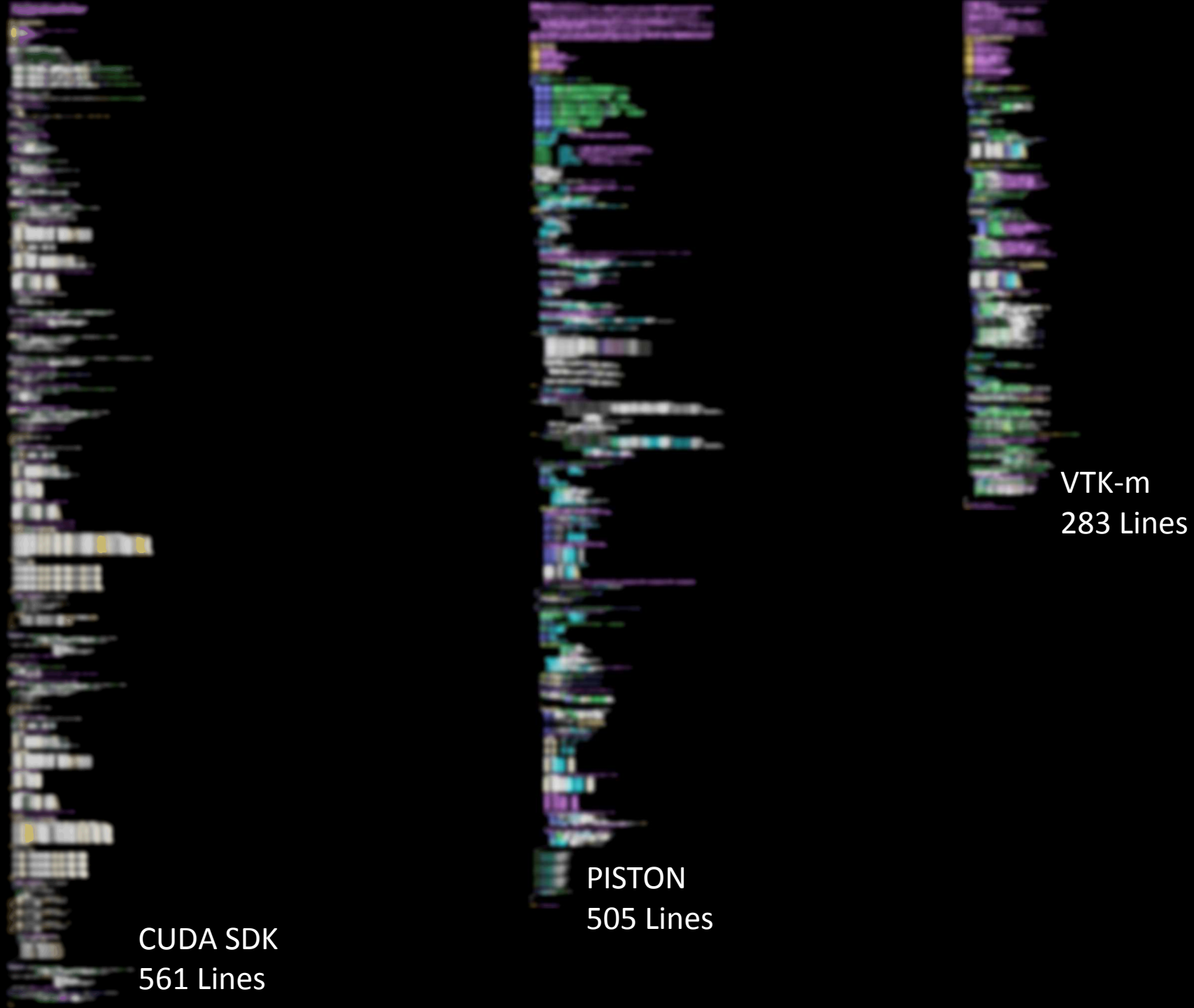
Allocate
Transfer
Schedule
Sort
…

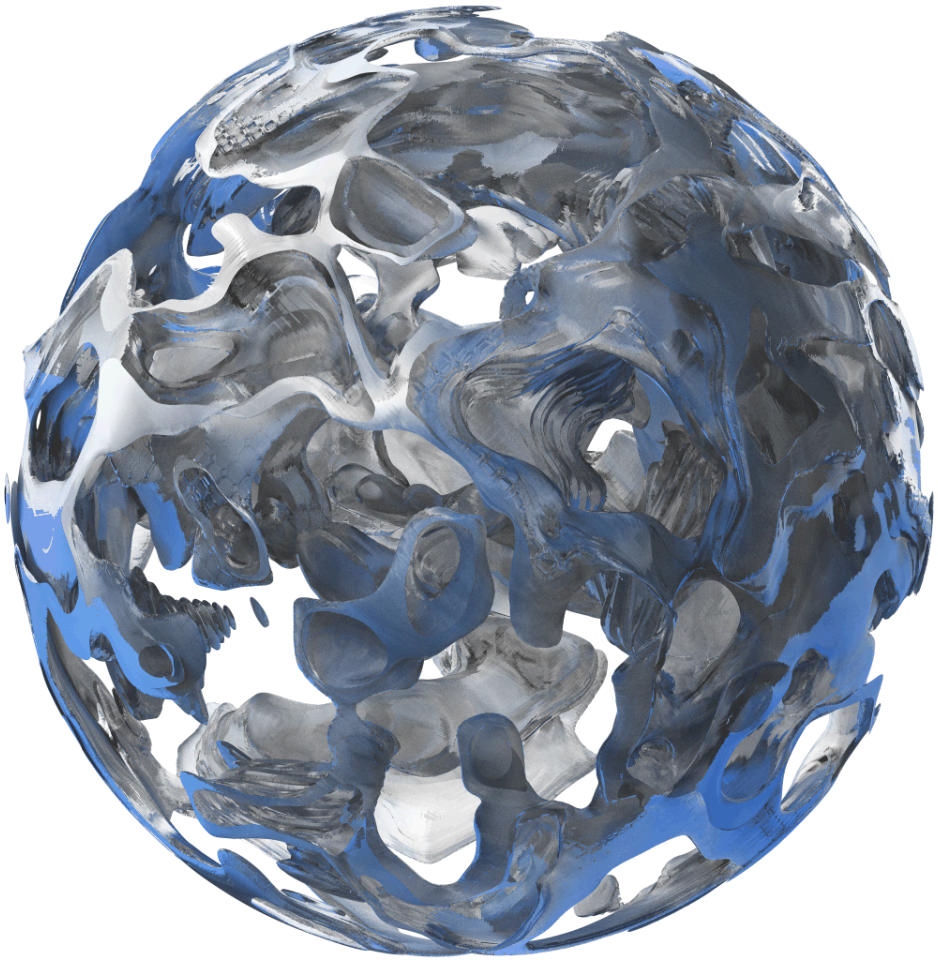
Execution Environment

Cell Operations
Field Operations
Basic Math
Make Cells

Worklet



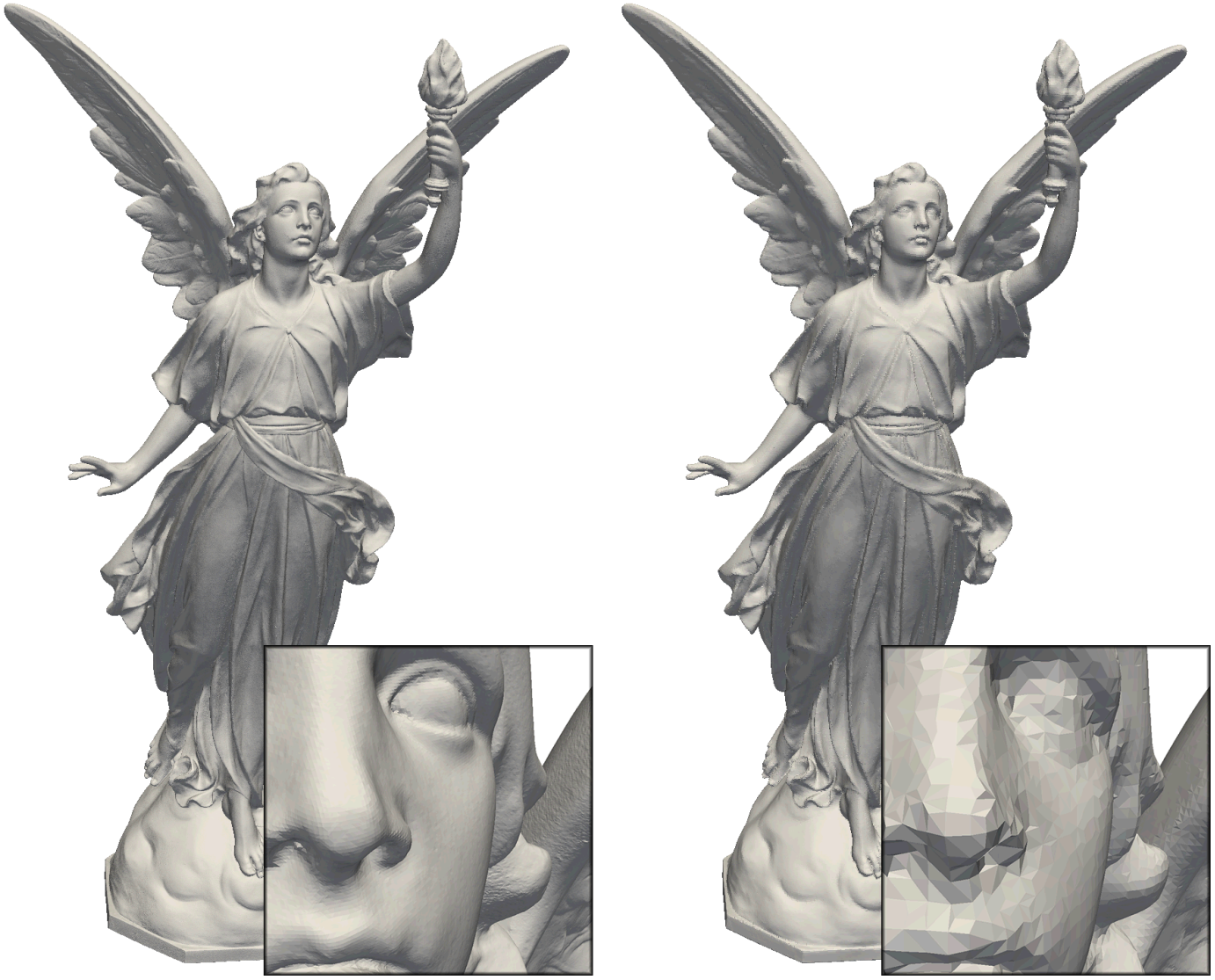

CUDA SDK
561 Lines
PISTON
505 Lines
VTK-m
283 Lines



Rendering

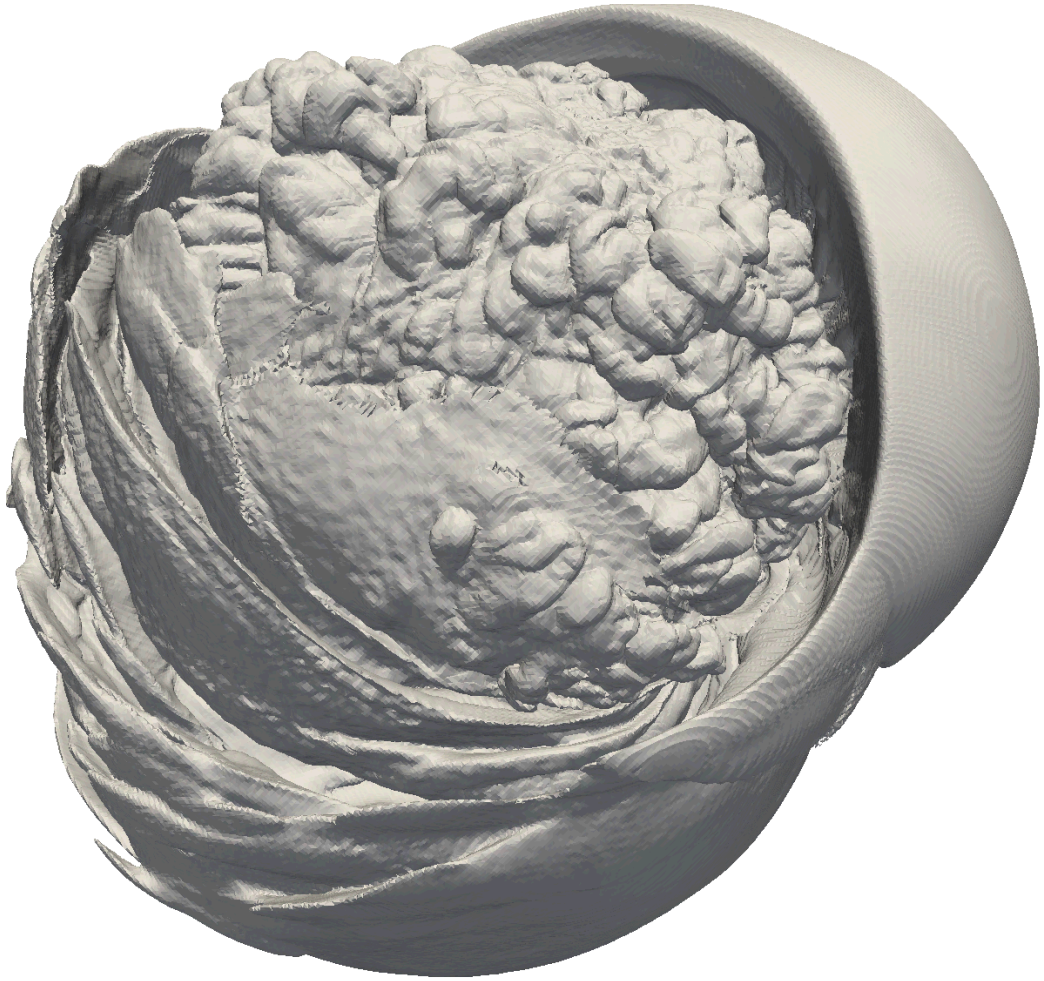
Data Set	Algorithm	Millions of Rays Per Second
LT_350K	OptiX Prime	357.6
	EAVL	150.8
	VTK-m	164.5
LT_372K	OptiX Prime	322.4
	EAVL	124.7
	VTK-m	140.8
RM_350K	OptiX Prime	436.5
	EAVL	197.5
	VTK-m	200.8
RM_650K	OptiX Prime	420.4
	EAVL	172.9
	VTK-m	166.0
RM_970K	OptiX Prime	347.1
	EAVL	152.8
	VTK-m	163.5
RM_1.7M	OptiX Prime	266.8
	EAVL	136.6
	VTK-m	148.8
RM_3.2M	OptiX Prime	264.5
	EAVL	124.8
	VTK-m	134.5
Seismic	OptiX Prime	267.8
	EAVL	106.3
	VTK-m	119.4

Data Set	Algorithm	Millions of Rays Per Second
LT_350K	Embree	51.9
	EAVL	27.7
	VTK-m	38.5
LT_372K	Embree	56.5
	EAVL	26.1
	VTK-m	36.0
RM_350K	Embree	64.8
	EAVL	33.3
	VTK-m	47.8
RM_650K	Embree	65.9
	EAVL	35.6
	VTK-m	49.1
RM_970K	Embree	59.1
	EAVL	29.3
	VTK-m	41.0
RM_1.7M	Embree	52.4
	EAVL	27.0
	VTK-m	37.8
RM_3.2M	Embree	48.4
	EAVL	28.3
	VTK-m	33.9
Seismic	Embree	43.2
	EAVL	25.2
	VTK-m	34.5



Surface Simplification

Algorithm	Device	512^3	1024^3	2048^3
VTK	Serial	3.65 s	11.40 s	
VTK-m	Serial	2.73 s	2.93 s	5.22 s
VTK-m	TBB 36 threads	0.36 s	0.45 s	0.72 s
VTK-m	TBB 72 threads	0.41 s	0.49 s	0.74 s
VTK-m	CUDA	0.18 s	0.19 s	0.20 s



Algorithm	Device	Time
vtkMarchingCubes	Serial	11.917 s
vtkMarchingCubes	32 MPI Ranks	1.352 s
vtkMarchingCubes	64 MPI Ranks	1.922 s
PISTON	Serial	19.895 s
PISTON	CUDA	0.514 s
PISTON	TBB	0.955 s
VTK-m	Serial	20.784 s
VTK-m	CUDA	0.560 s
VTK-m	TBB	1.161 s

Summary

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- Processing in HPC has rapidly evolved
  - Visualization (as with the rest of HPC computing) needs to adjust
- There is lots of parallelism available for visualization
  - But taking advantage of it is not always straightforward
- Updating algorithms is a lengthy process
  - There are lots of distinct algorithms (more than 400 in VTK)
- Data parallel primitives simplify the implementation and provide performance portability
- VTK-m is collecting and implementing these algorithms

http://m.vtk.org

Acknowledgements

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