SAND2017-1698C

ADVANCED ARCHITECTURE TEST BEDS

Quantum Testbeds Stakeholder Workshop

Sandia's ASC NNSA Testbed Project

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U.S. DEPARTMENT OF ENERGY

NNSA National Nuclear Security Administration

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Advanced Architecture Testbed Project

Goals

- Reduce impact on mission labs in a rapidly changing technology environment
  - Significant PRODUCTION code rewrite or modification may be required
- Go through all the pain up front so the transition for full codes is made easier
- Eliminate or reduce missteps

… to be a scout for future computer architectu

Philosophy

- Hardware and Software intended (and has proven) to be highly dynamic
- INTENTIONALLY closer to prototypes than production
- Systems are NOT for production capability/capacity cycles

riority is to explore a wide and diverse set of merging architectural alternatives

Current state of technology REQUIRES exploratory R&D of:

- Alternative Programming Models
- Architecture-aware algorithms
- Advanced memory sub-system development
- Energy-efficient hardware, runtime, systems software and APPLICATIONS

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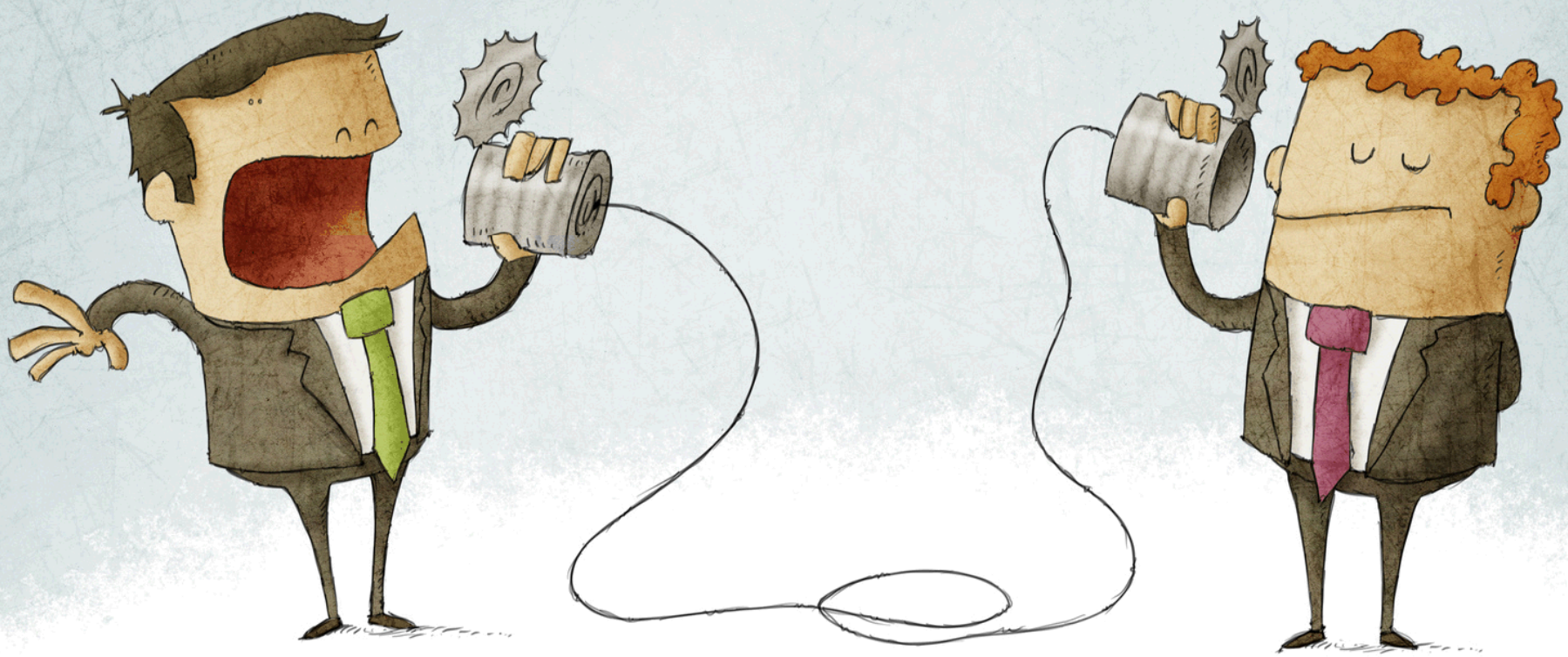
gnificantly impacted the vendor offerings procurements

- Significantly improved *performance-portability*
- Dramatically increased the maturity of the vendor software stack (especially compilers) - more efficient use of delivered hardware
- Provides environment for accelerated development of next-generation algorithms and programming models

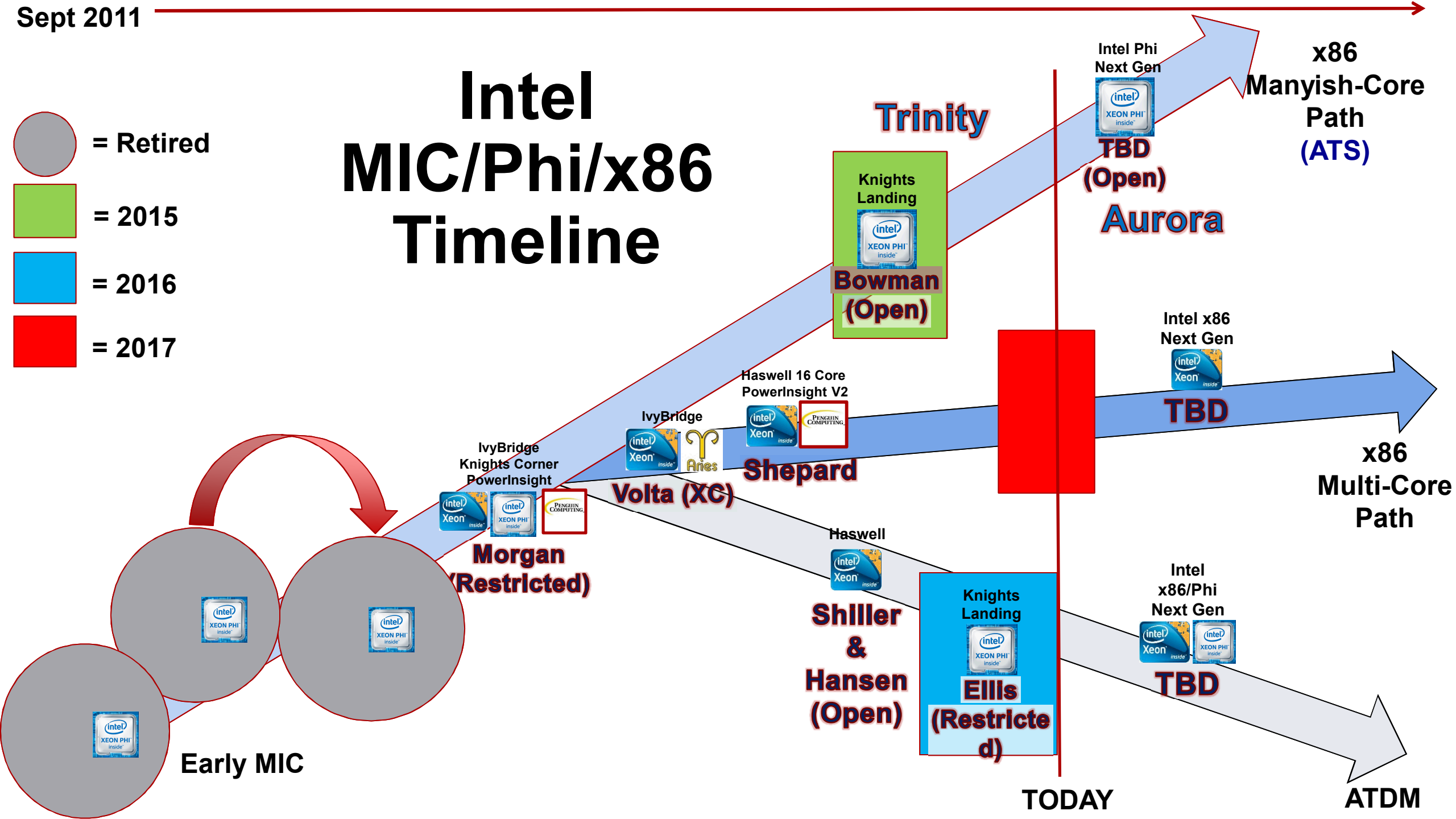
Communication

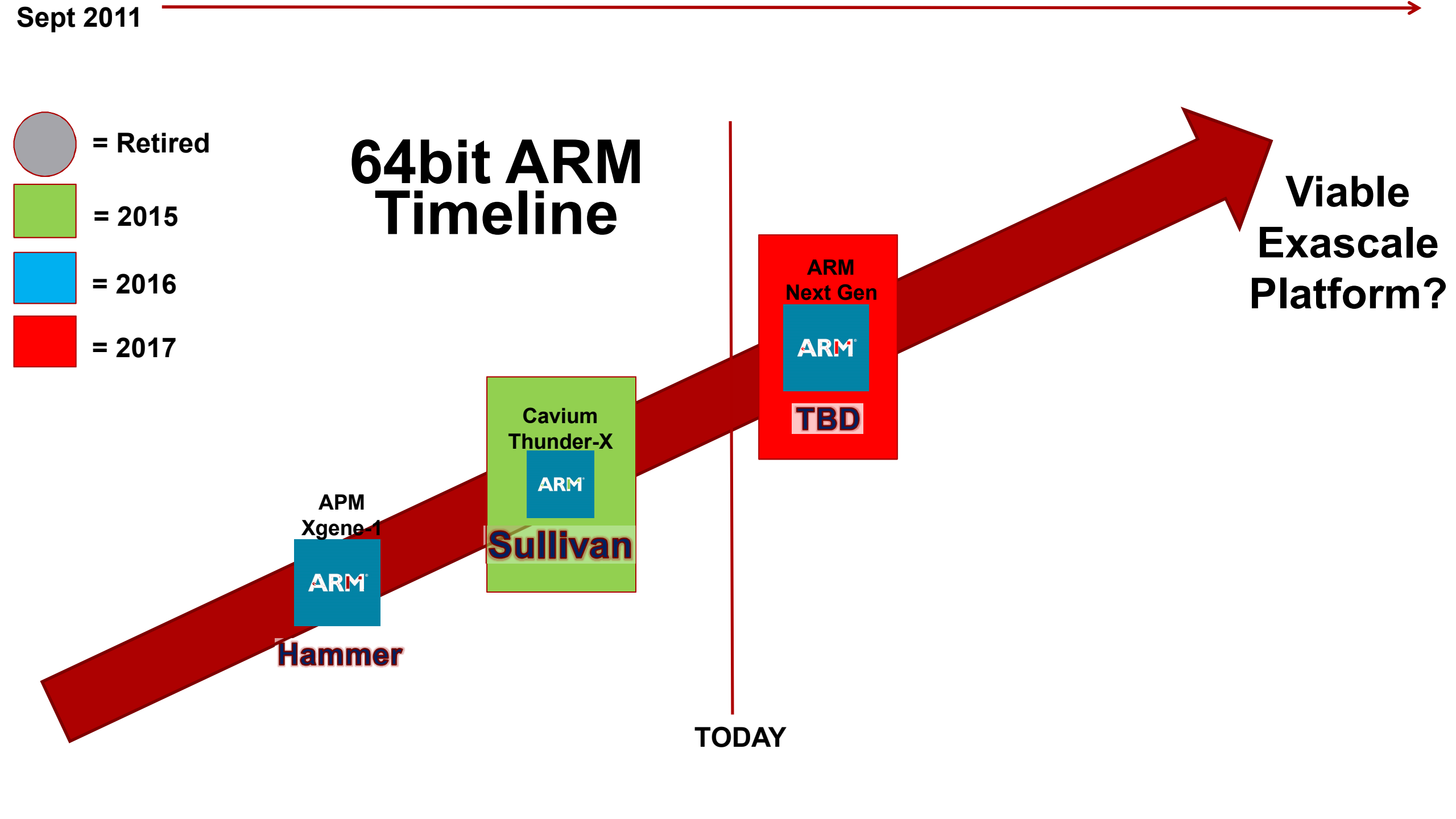
- The Test Bed program leveraged Sandia's existing reputation as **THE** Engineering/Architecture laboratory
  - ASCI Red
  - Cplant
  - Red Storm
- Developed extremely close collaborative relationships beneficial to all participants

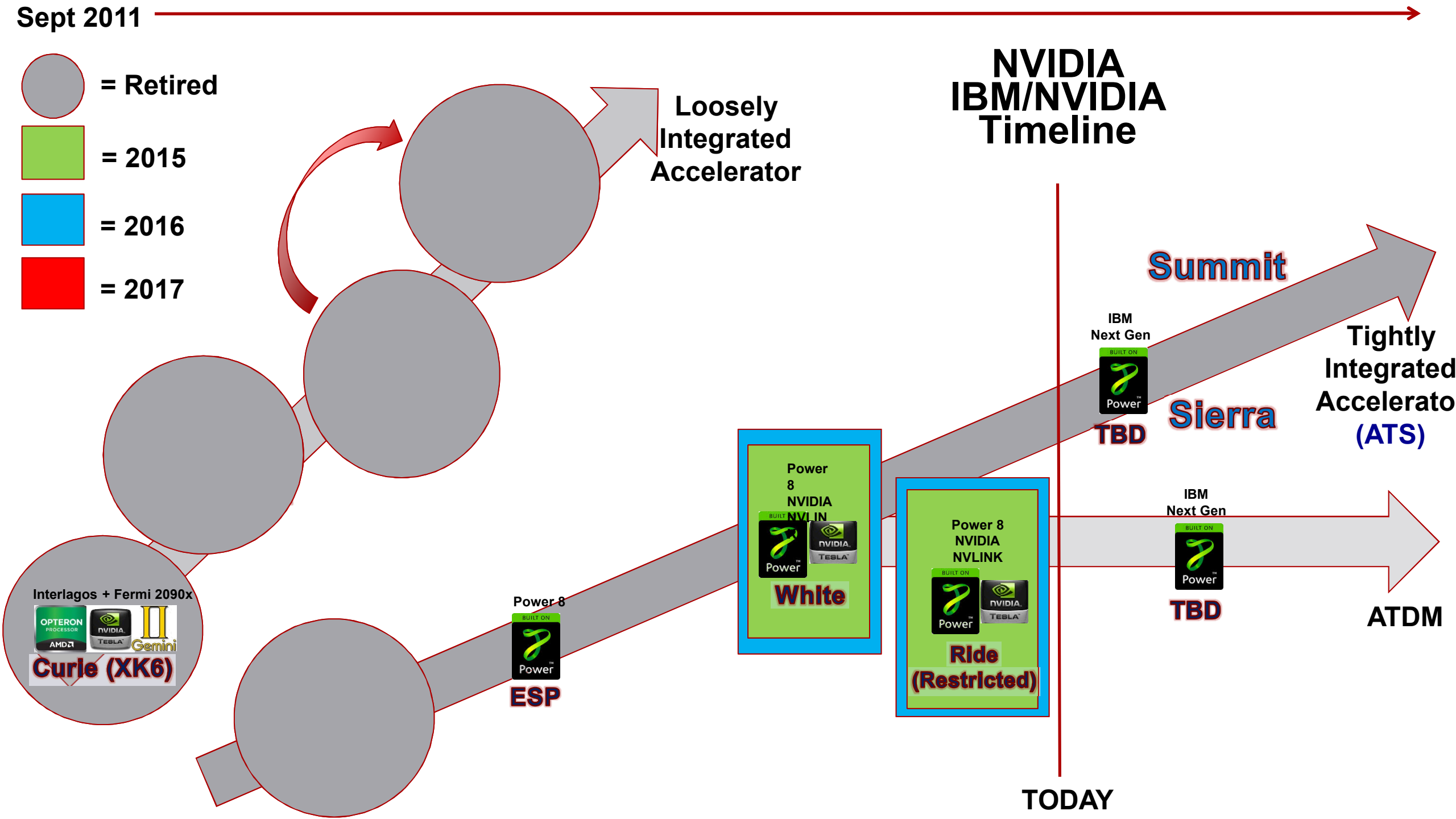
- **Most important lesson, testbeds act as a conduit for MEANINGFUL conversation and co-design**
  - In our case, labs, technology providers and universities
- Conversation not limited by duration of single procurement
- Identify your stakeholders and ensure goals, philosophy and your implementation facilitate the conversation

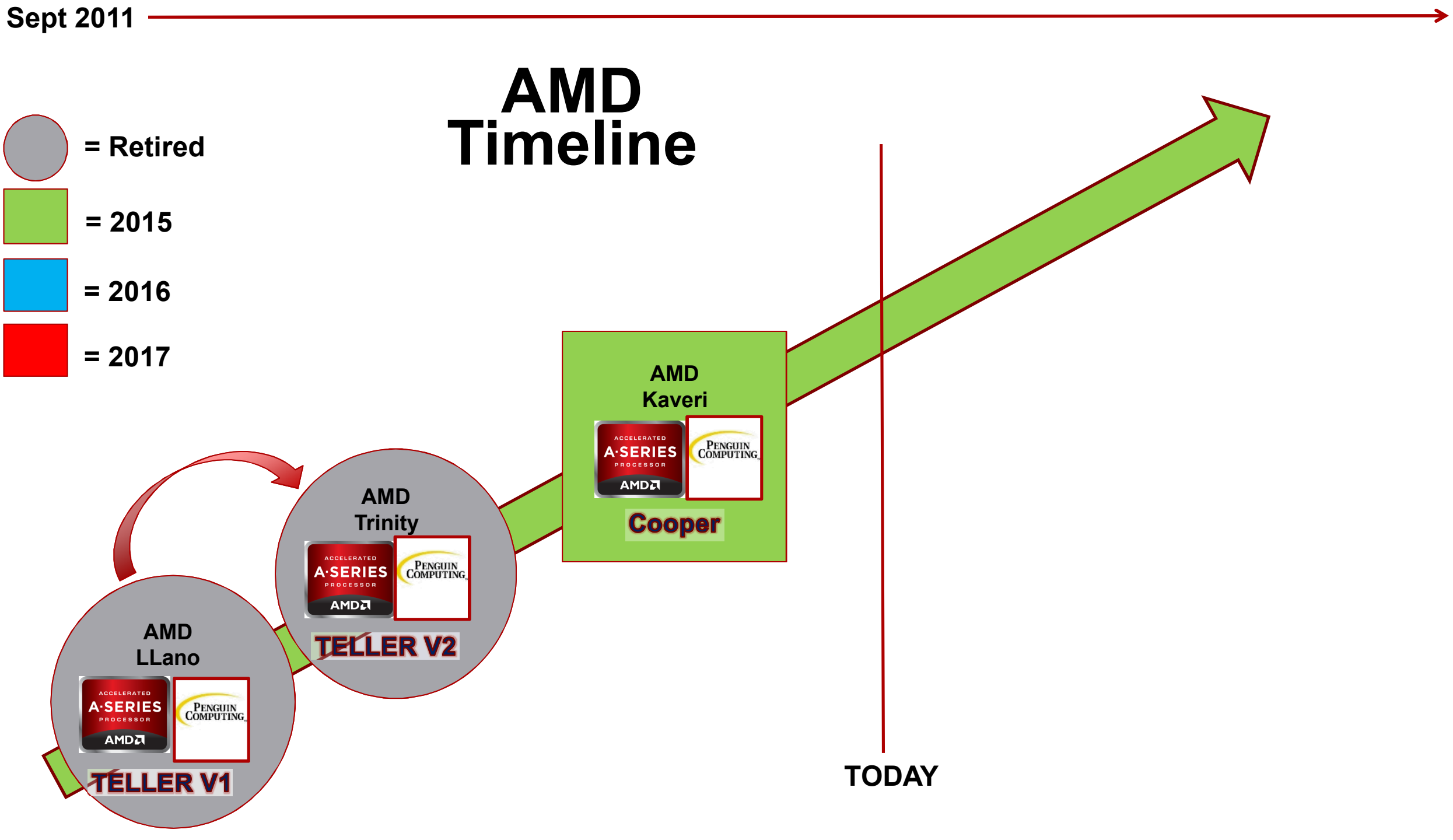


TECHNOLOGY TIMELINES


Sept 2011
Intel MIC/Phi/x86 Timeline
= Retired
= 2015
= 2016
= 2017
Early MIC
IvyBridge
Knights Corner
PowerInsight
Morgan
(Restricted)
IvyBridge
Volta (XC)
Haswell 16 Core
PowerInsight V2
Shepard
Haswell
Shiller
&
Hansen
(Open)
Trinity
Knights
Landing
Bowman
(Open)
Knights
Landing
Ellis
(Restricte
d)
Intel Phi
Next Gen
TBD
(Open)
Aurora
x86
Manyish-Core
Path
(ATS)
Intel x86
Next Gen
TBD
x86
Multi-Core
Path
Intel
x86/Phi
Next Gen
TBD
TODAY
ATDM


Sept 2011
= Retired
= 2015
= 2016
= 2017
64bit ARM Timeline
APM Xgene-1
ARM
Hammer
Cavium Thunder-X
ARM
Sullivan
ARM Next Gen
ARM
TBD
TODAY
Viable Exascale Platform?


Sept 2011
= Retired
= 2015
= 2016
= 2017
NVIDIA
IBM/NVIDIA
Timeline
Loosely
Integrated
Accelerator
Summit
IBM
Next Gen
TBD
Sierra
Tightly
Integrated
Accelerato
(ATS)
Power
8
NVIDIA
NVLIN
White
Power 8
NVIDIA
NVLINK
Ride
(Restricted)
IBM
Next Gen
TBD
ATDM
Interlagos + Fermi 2090x
Curie (XK6)
Power 8
ESP
TODAY


Sept 2011
AMD Timeline
= Retired
= 2015
= 2016
= 2017
AMD LLano
TELLER V1
AMD Trinity
TELLER V2
AMD Kaveri
Cooper
TODAY