SAND2017-5998C

Efficient layout for silicon quantum dot spin qubits

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June 7th 2017
12th Canadian Quantum Information Student's Conference
Orford, Québec, Canada

1 INSTITUT QUANTIQUE
2 UNIVERSITÉ DE SHERBROOKE
3 Sandia National Laboratories
4 THE UNIVERSITY of NEW MEXICO
5 CCR Center for Computing Research
7 CIFAR CANADIAN INSTITUTE FOR ADVANCED RESEARCH
6 Center for Integrated Nanotechnologies (CINT)

Fonds de recherche sur la nature et les technologies Québec
CRSNG NSERC

State of the art for Si quantum dot spin qubits

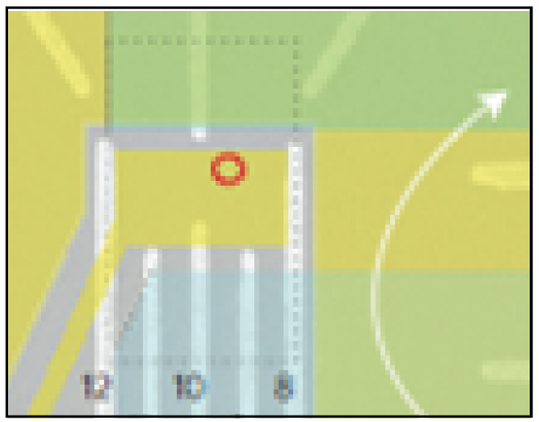
Single qubit gates

Kawakami *et al*., 2014

Si/SiGe (natural)

Fidelity: 99 %

Micro-magnet (EDSR)

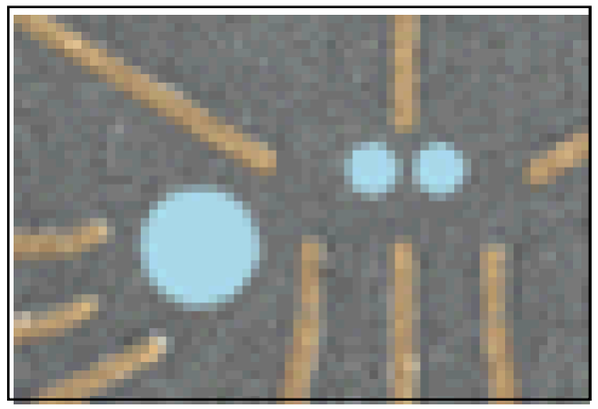


Takeda *et al*., 2016

Si/SiGe (natural)

Fidelity: 99.6 %

Micro-magnet (EDSR)

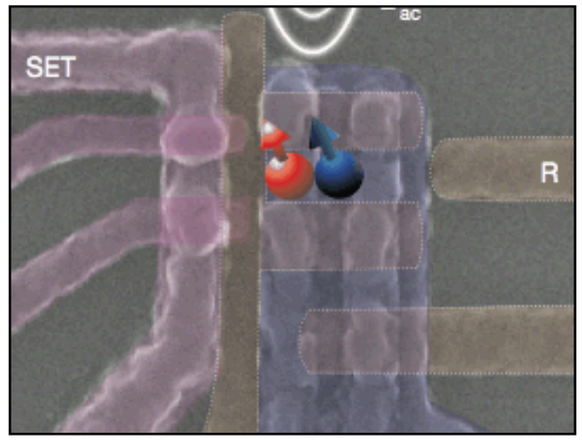


Veldhorst *et al*., 2014

MOS (Al), Si 28

Fidelity: 99.6 %

Transmission line (ESR)



Large QDs array

Zajac *et al*., 2016

Si/SiGe

9 QDs

Good reproducibility for charging energies and orbital energies

Two-qubit gates

also

Veldhorst *et al*., 2015

MOS (Al), Si 28

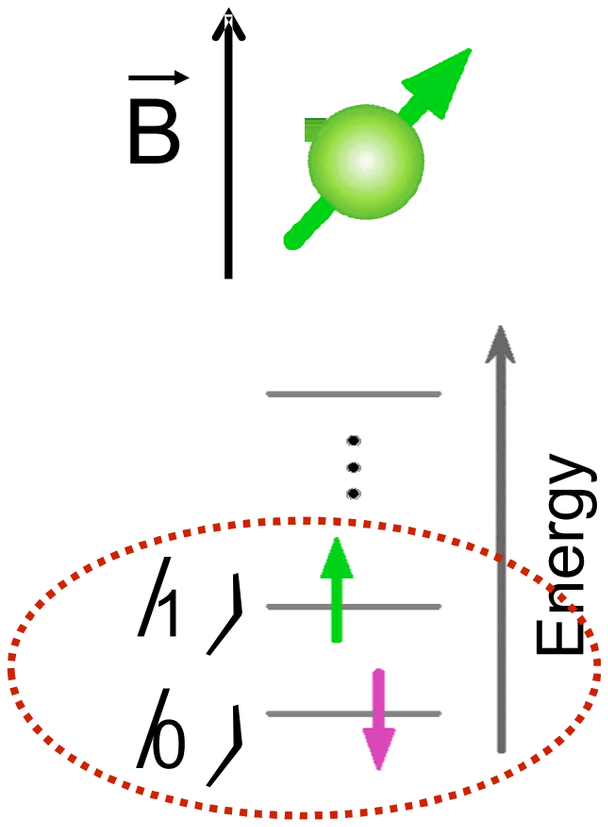
Fidelity: < 90 %

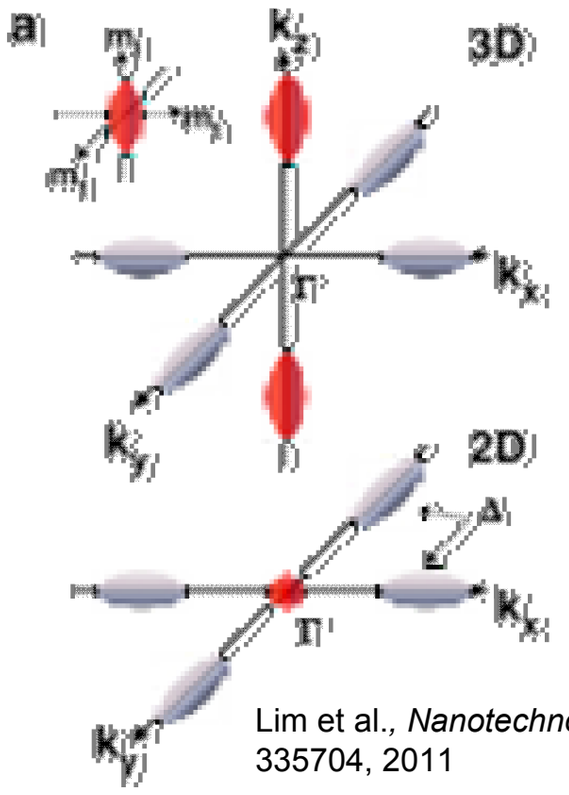
Presentation structure

- A reliable Si QD platform
  - Well-isolated two-level system
  - Dot-reservoir tunnel barrier tunability
  - Extensible fabrication
- Our approach
  - Split accumulation gate architecture
  - Prototypes and fabrication process
- Results
  - Single electron regime
  - Dot-reservoir tunnel rate control
  - Valley splitting tuning
- Conclusion

A reliable platform for scaling up QD arrays

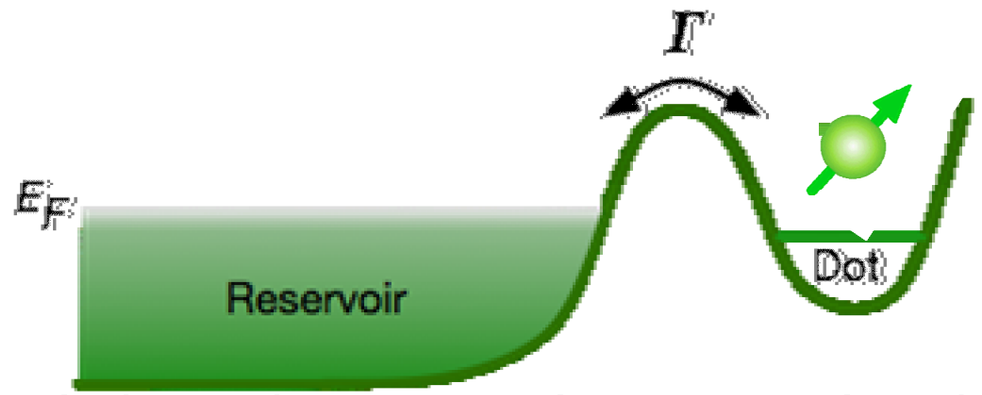
(1) Well-isolated two-level system





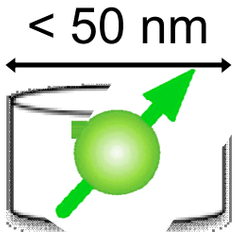
Lim et al., *Nanotechnology* 22, 335704, 2011

(2) Dot-reservoir tunnel rate control



-« Independant » tunnel rate control vs dot occupation

(3) Extensible fabrication



-Strong confinement

-Large and tunable valley splitting

- CMOS compatibility

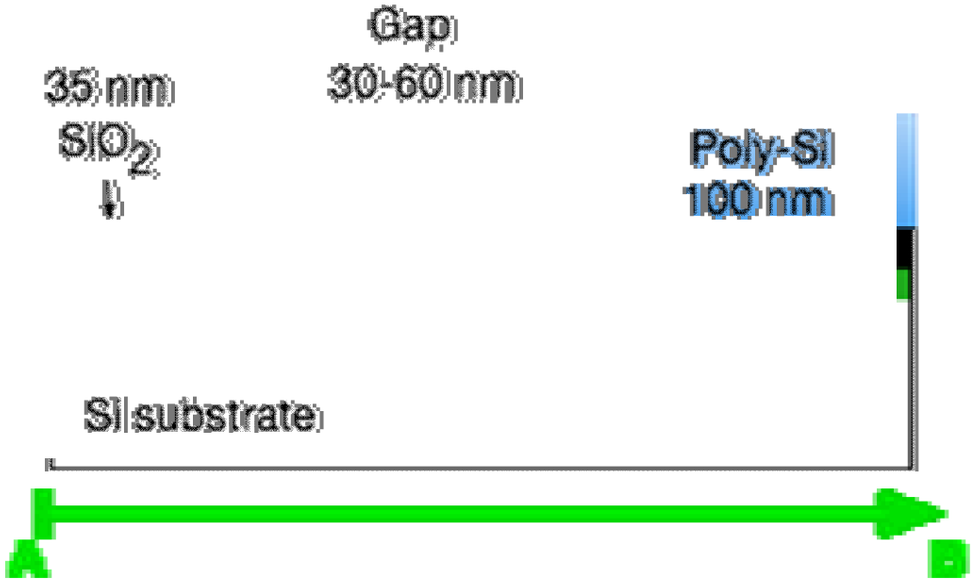
-Reproductibility and yield

-Simplified operation

Our approach

Split accumulation gate architecture

- Poly-silicon gates: CMOS compatible, less stress and noise than Al gates.
- Single gate stack subtractive fabrication process (no lift-off), CMOS compatible and better yield.
  Sandia National Laboratories fabrication process
- Minimalist planar architecture: we have to make it work with one less gate.
- Fabrication: check. Do we fulfill the other criterias?



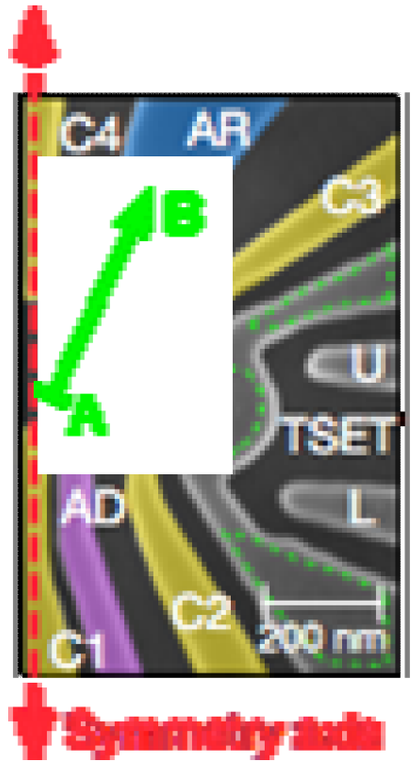
Single-lead device

Tested in

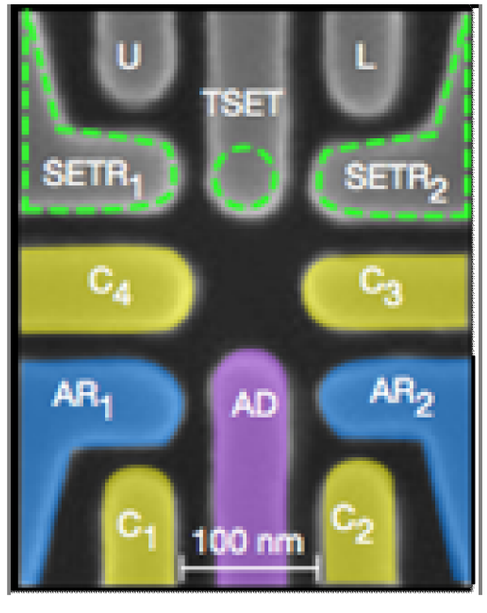
UNIVERSITÉ DE SHERBROOI

T_e =125 m

Charge detecti only



Double-lead device



Tested in

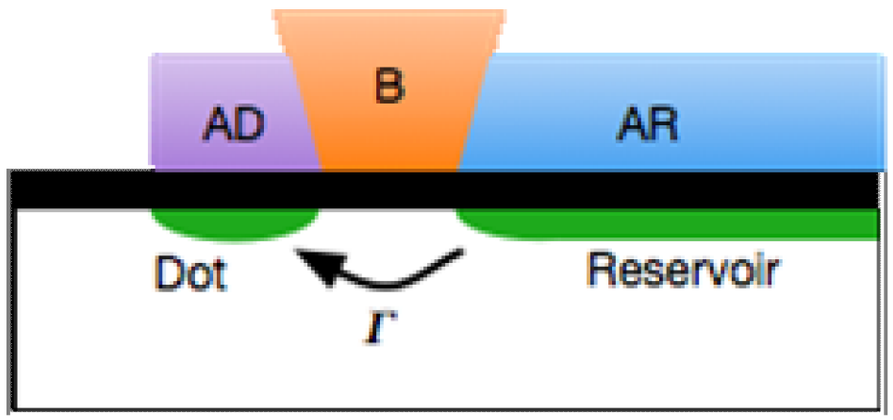
Sandia National Laboratories

T_e =160 mK

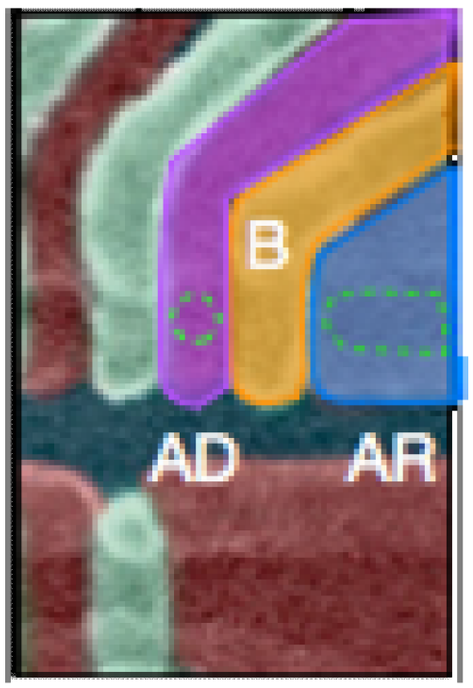
Charge detection + transport

Dot-reservoir tunnel barrier control methods

Local accumulation devices



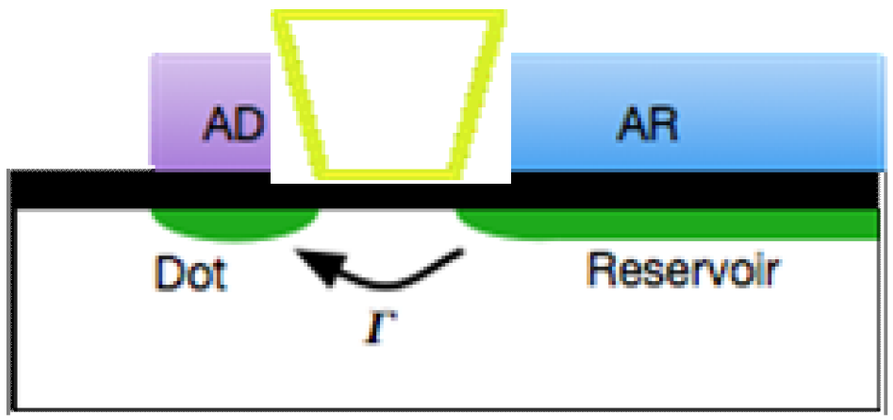
Dedicated barrier gate



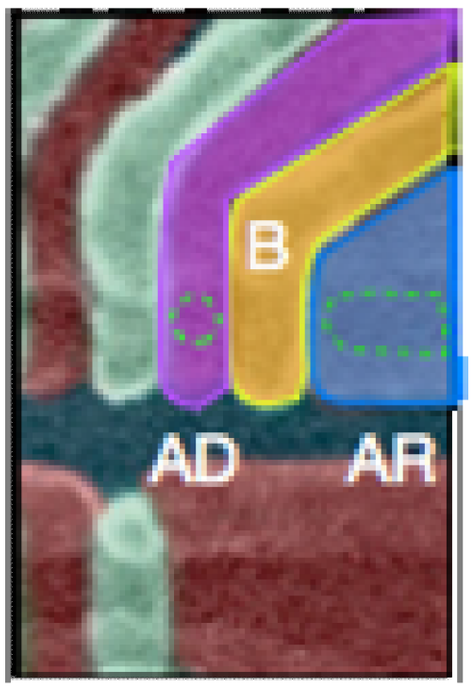
Zajac *et al*., 2016

Dot-reservoir tunnel barrier control methods

Local accumulation devices



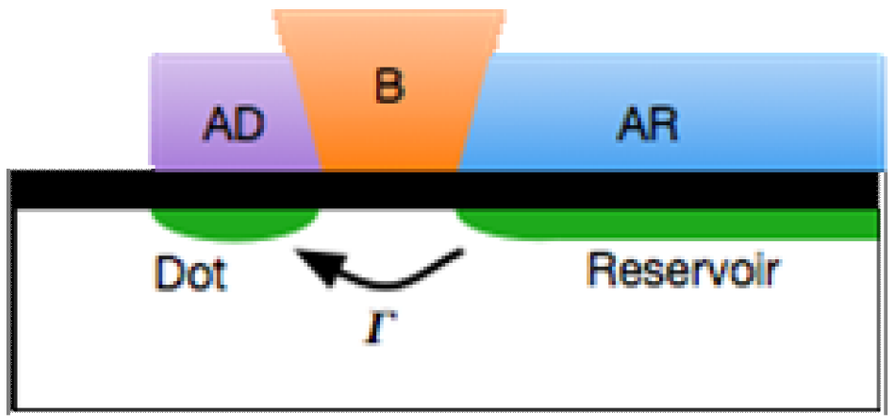
Dedicated barrier gate

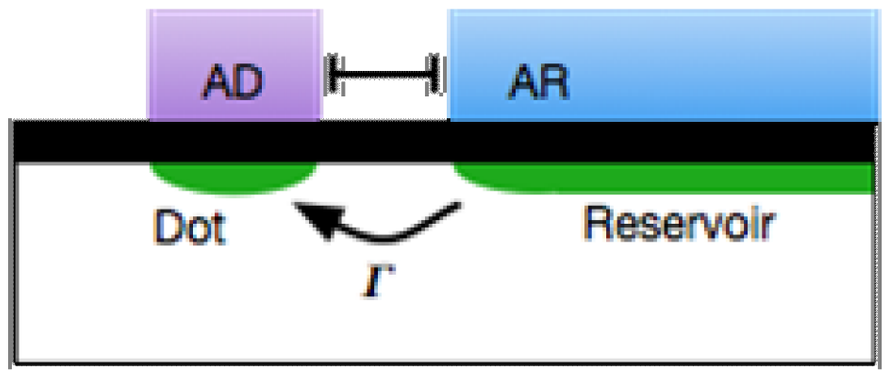


Zajac *et al*., 2016

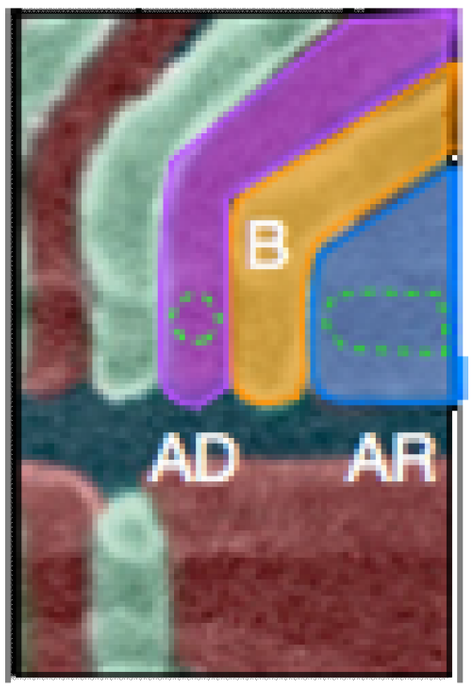
Dot-reservoir tunnel barrier control methods

Local accumulation devices



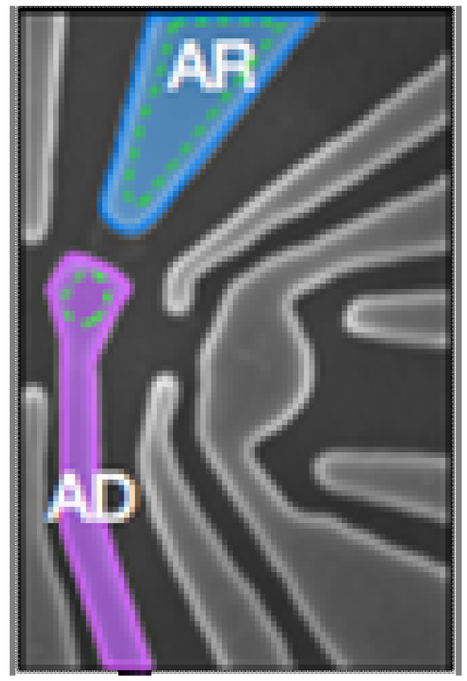


Dedicated barrier gate



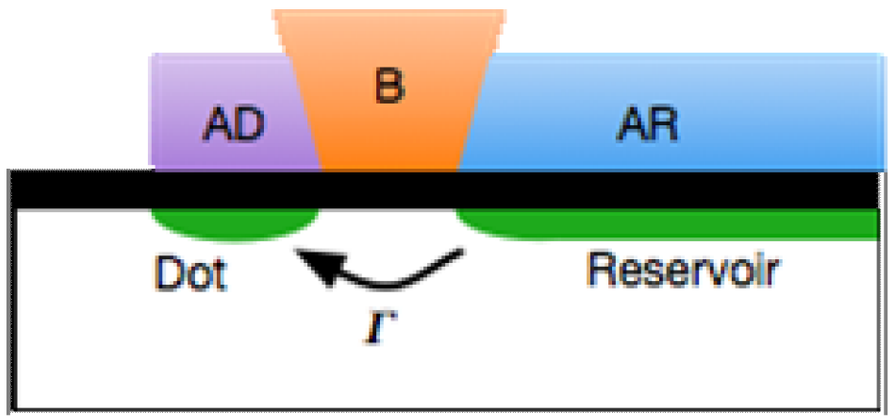
Zajac *et al*., 2016

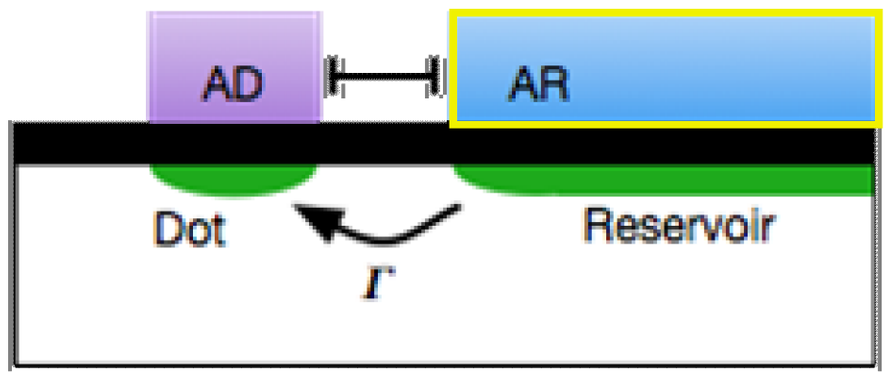
Minimalist architecture



Dot-reservoir tunnel barrier control methods

Local accumulation devices





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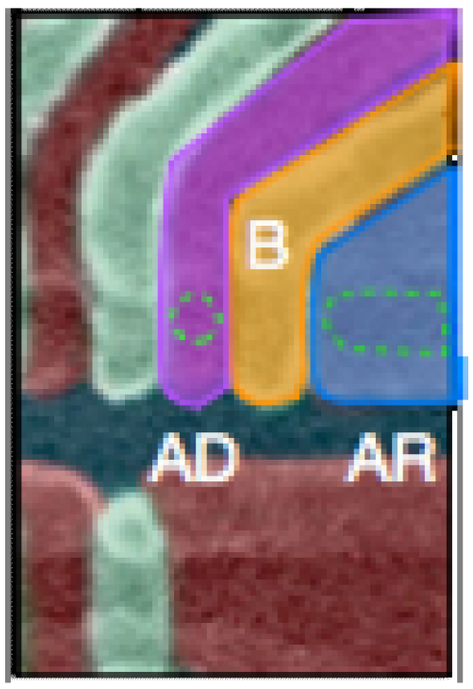

Zajac *et al*., 2016

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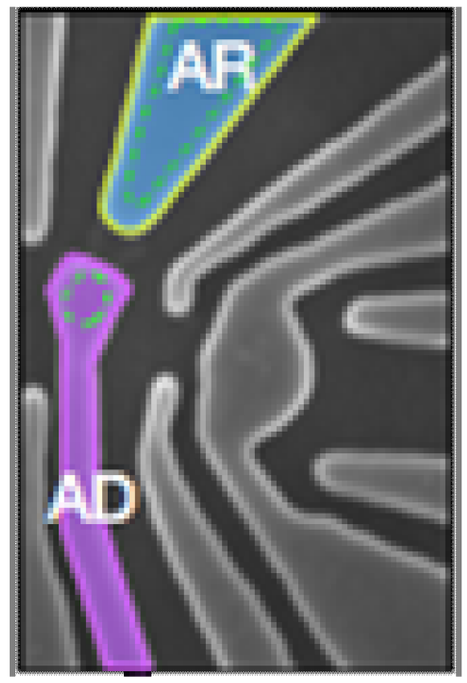
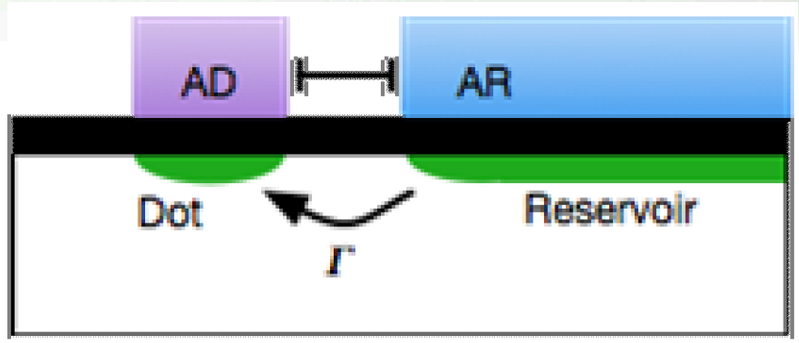
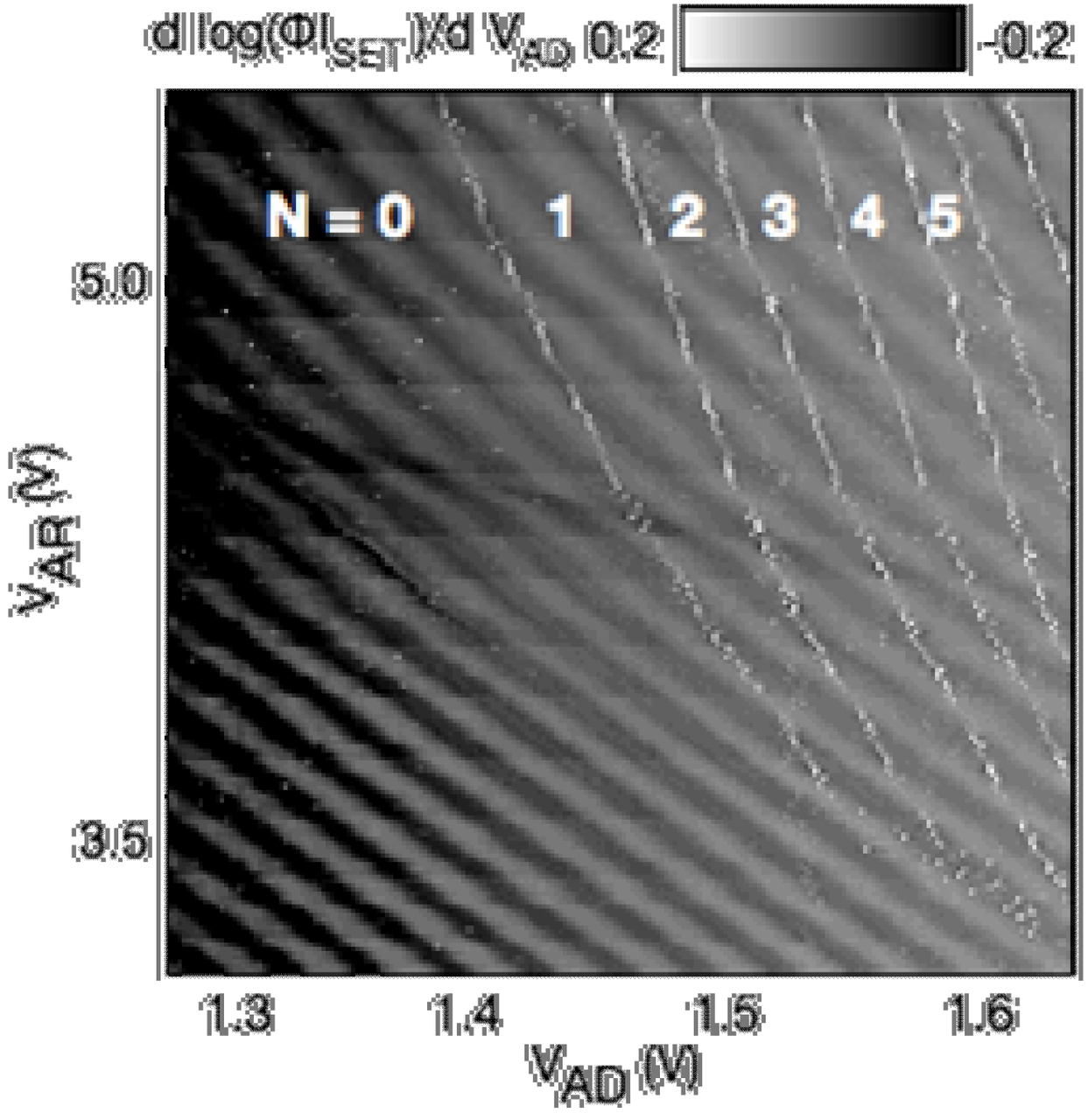


Single-electron regime

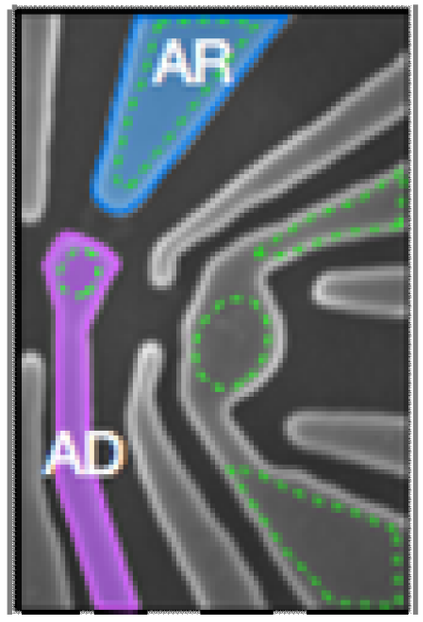


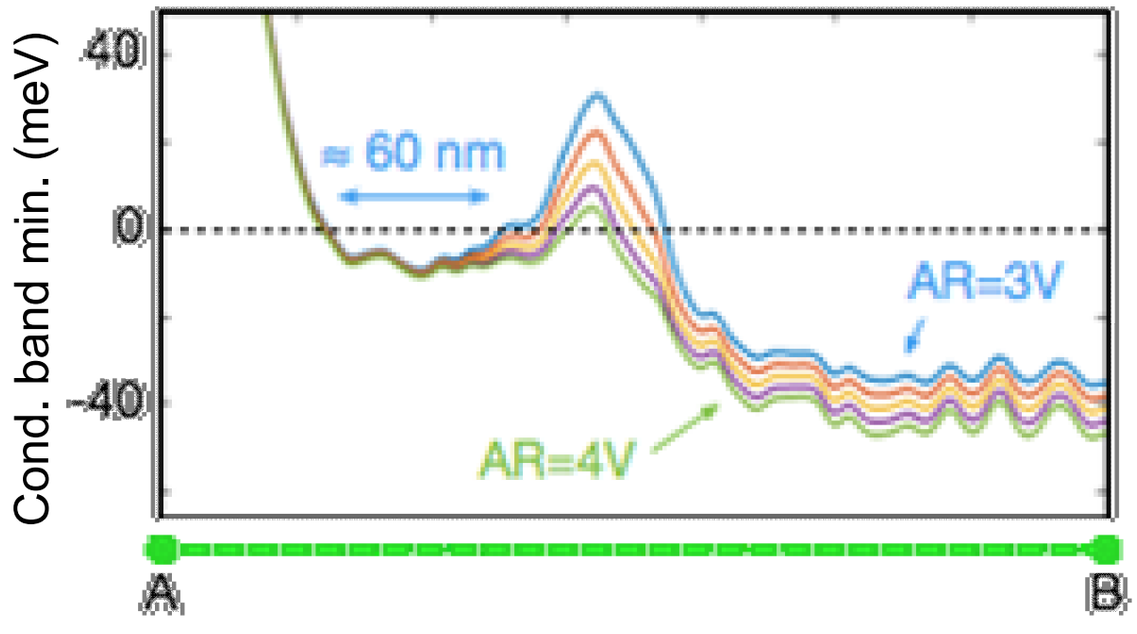
Single-lead device



Background:
SET oscillations

Effect of AR on
the tunnel rate Γ





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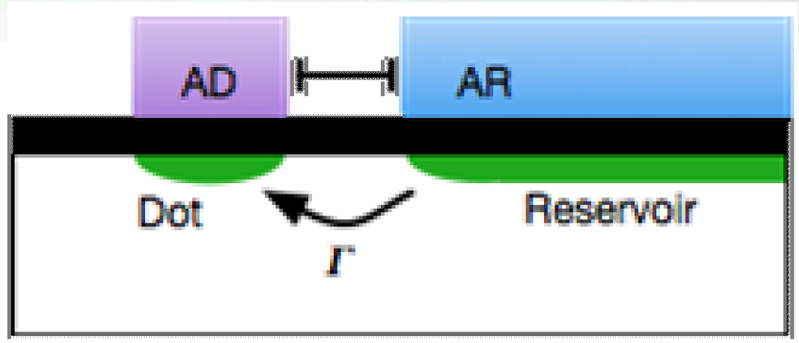
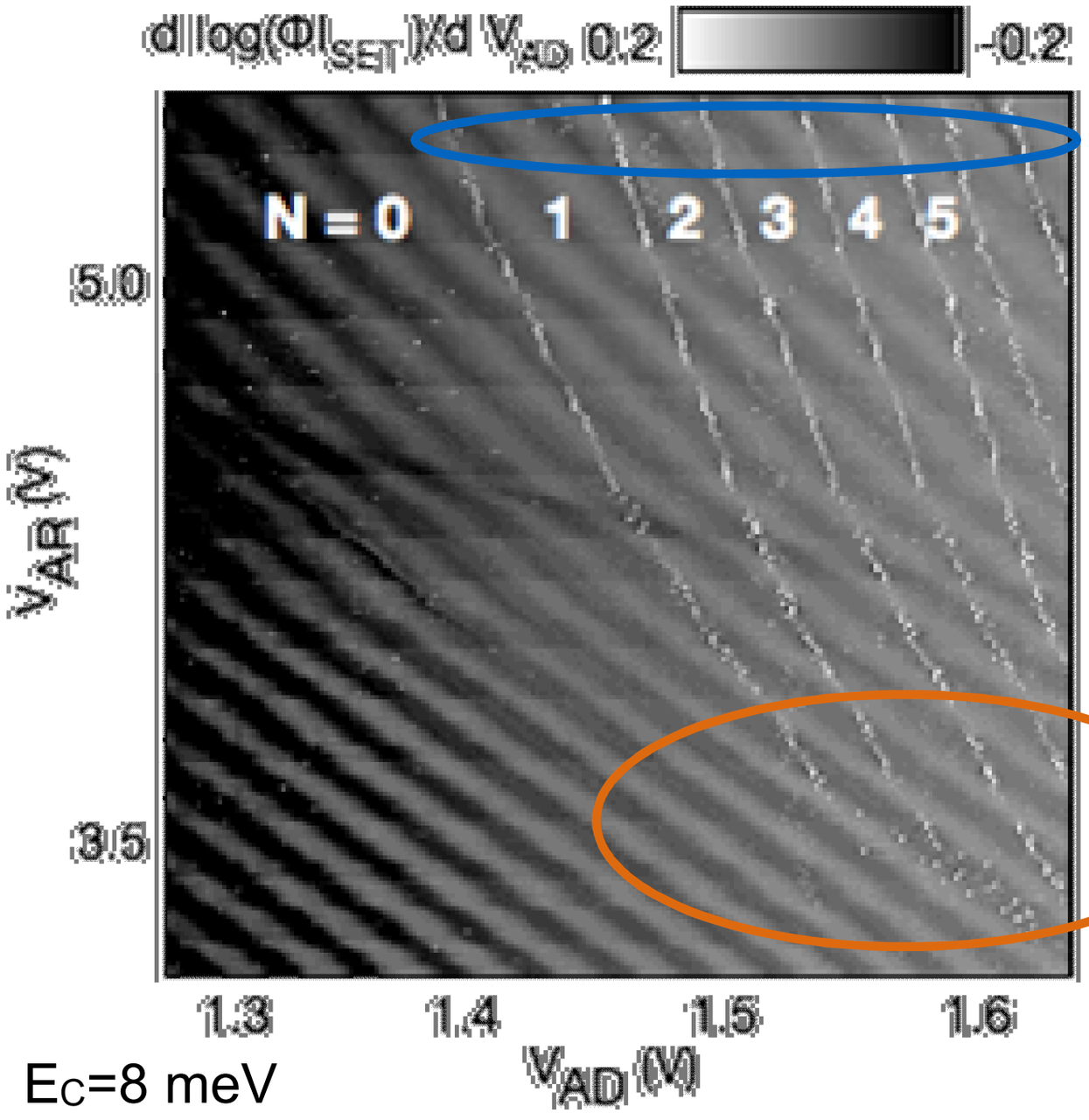


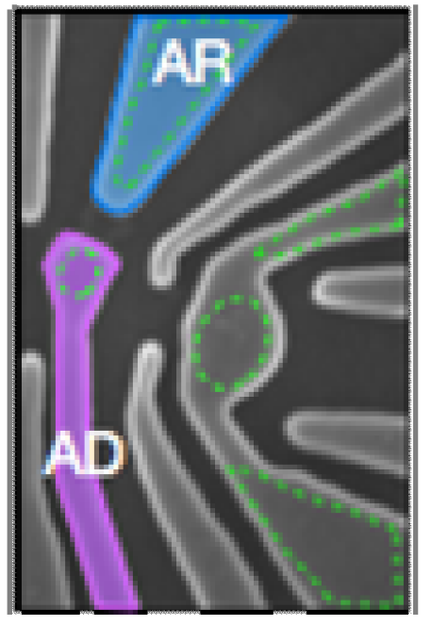


E_C=8 meV

Fast Γ compared to measurement time

Slow Γ compared to measurement time

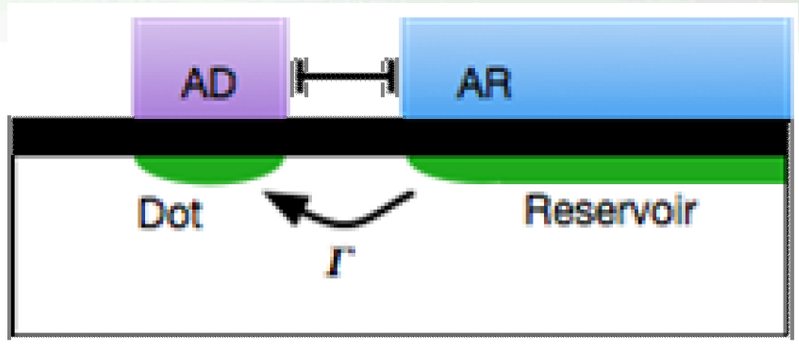
Single-lead device

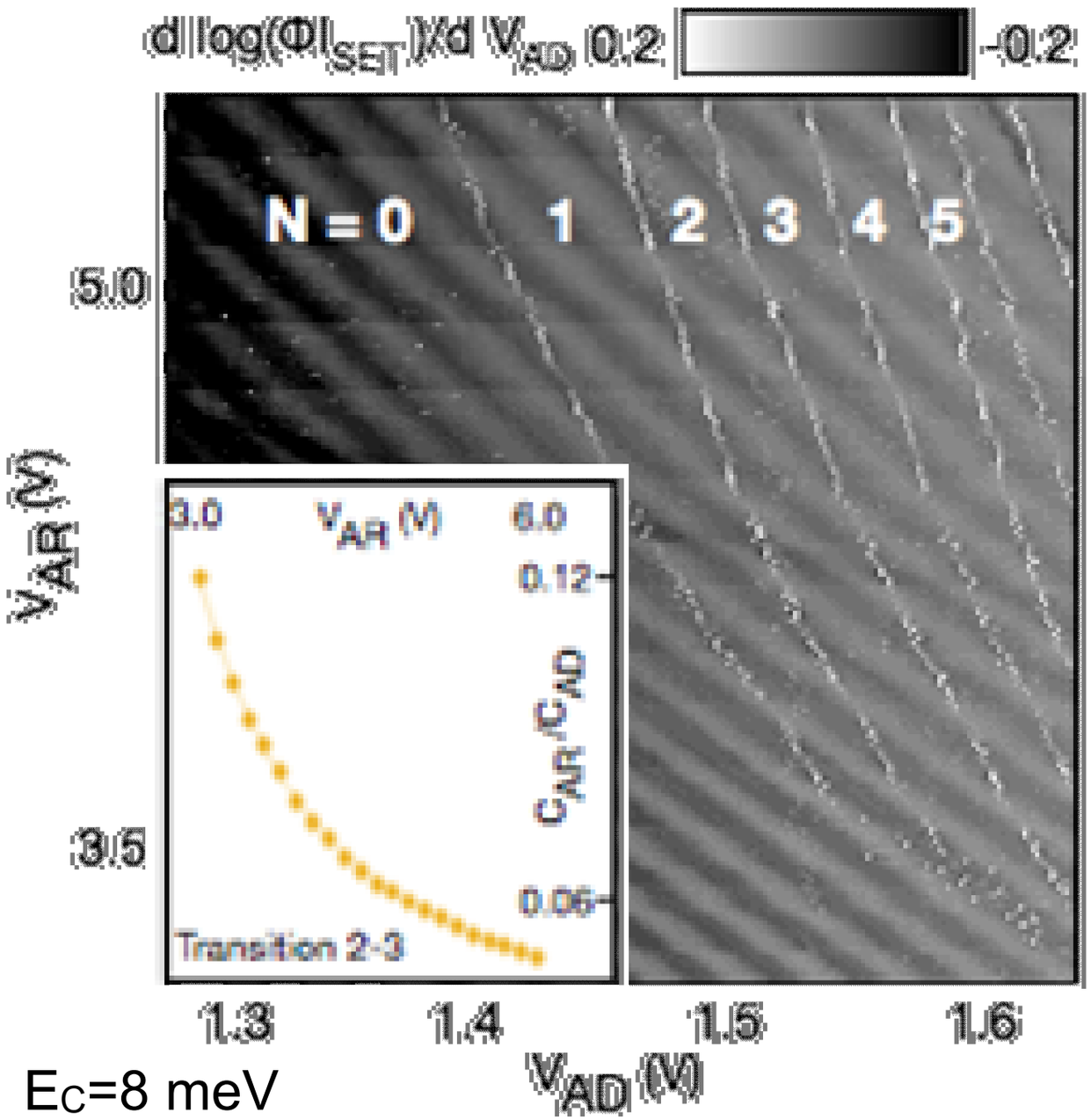


Effect of AR on the tunnel rate Γ

Thalakulam et al., APL 96, 183104 (2010).

Single-electron regime



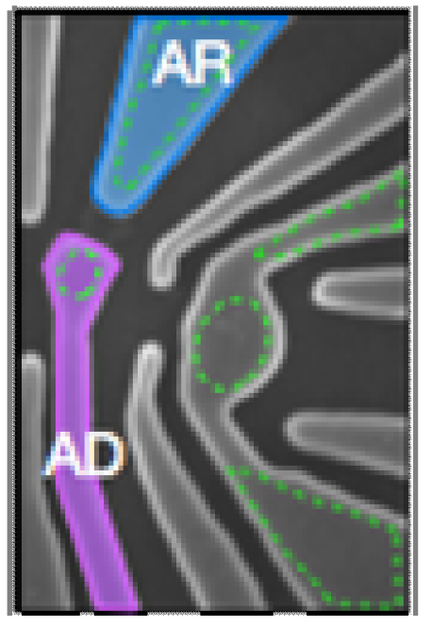


E_C=8 meV

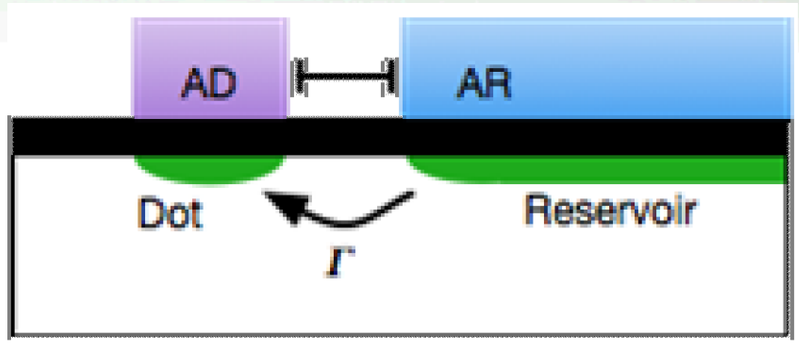
Gradual decrease of $C_{AR\text{-}dot}/C_{AD\text{-}dot}$

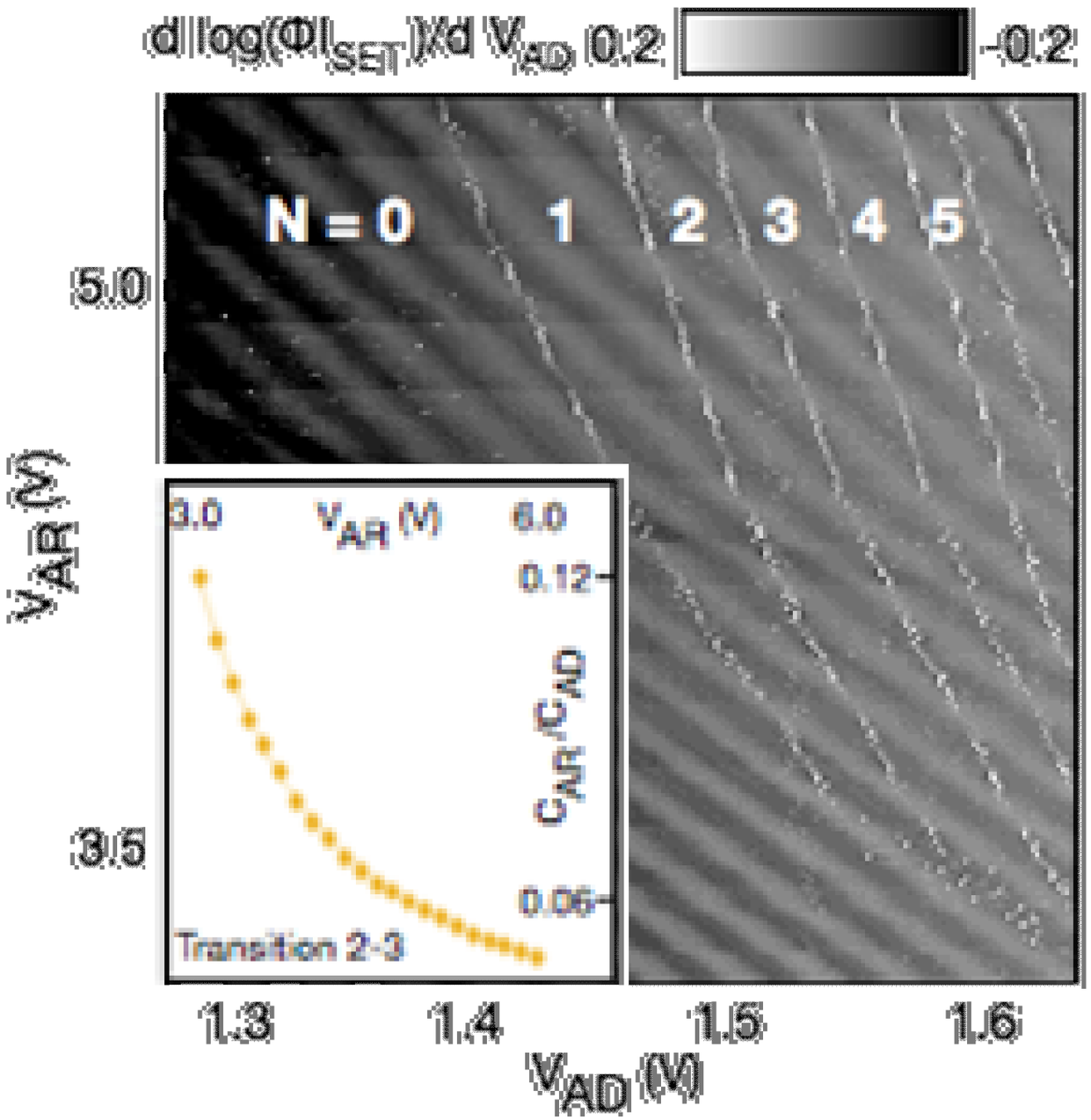
Filling of the reservoir

Single-lead device



Single-electron regime





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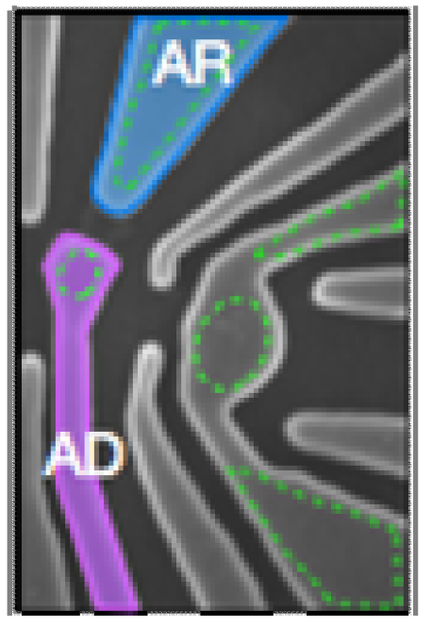
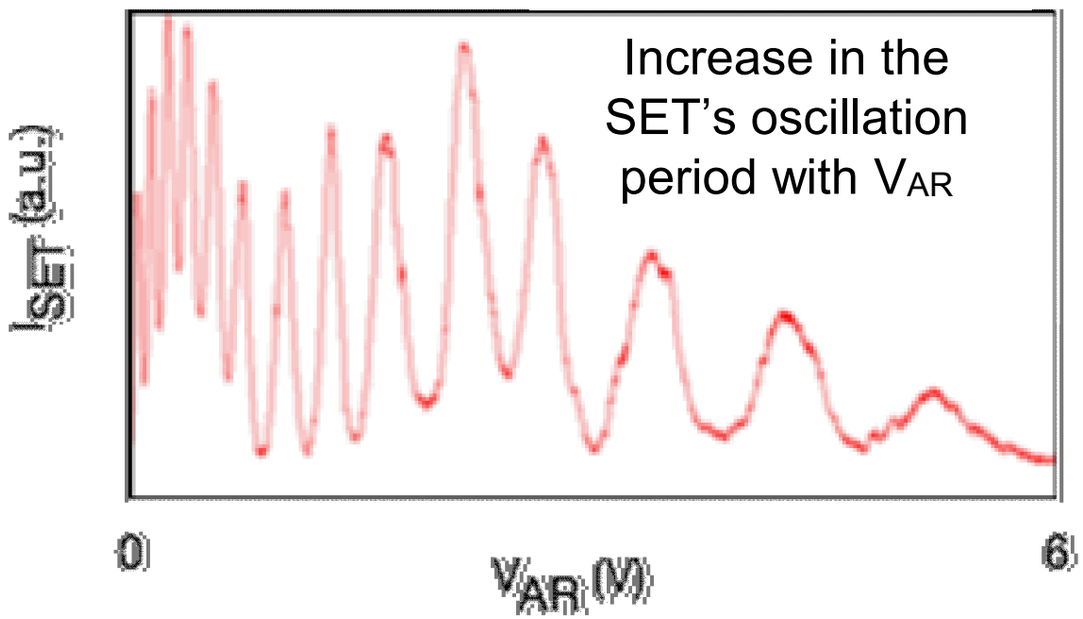
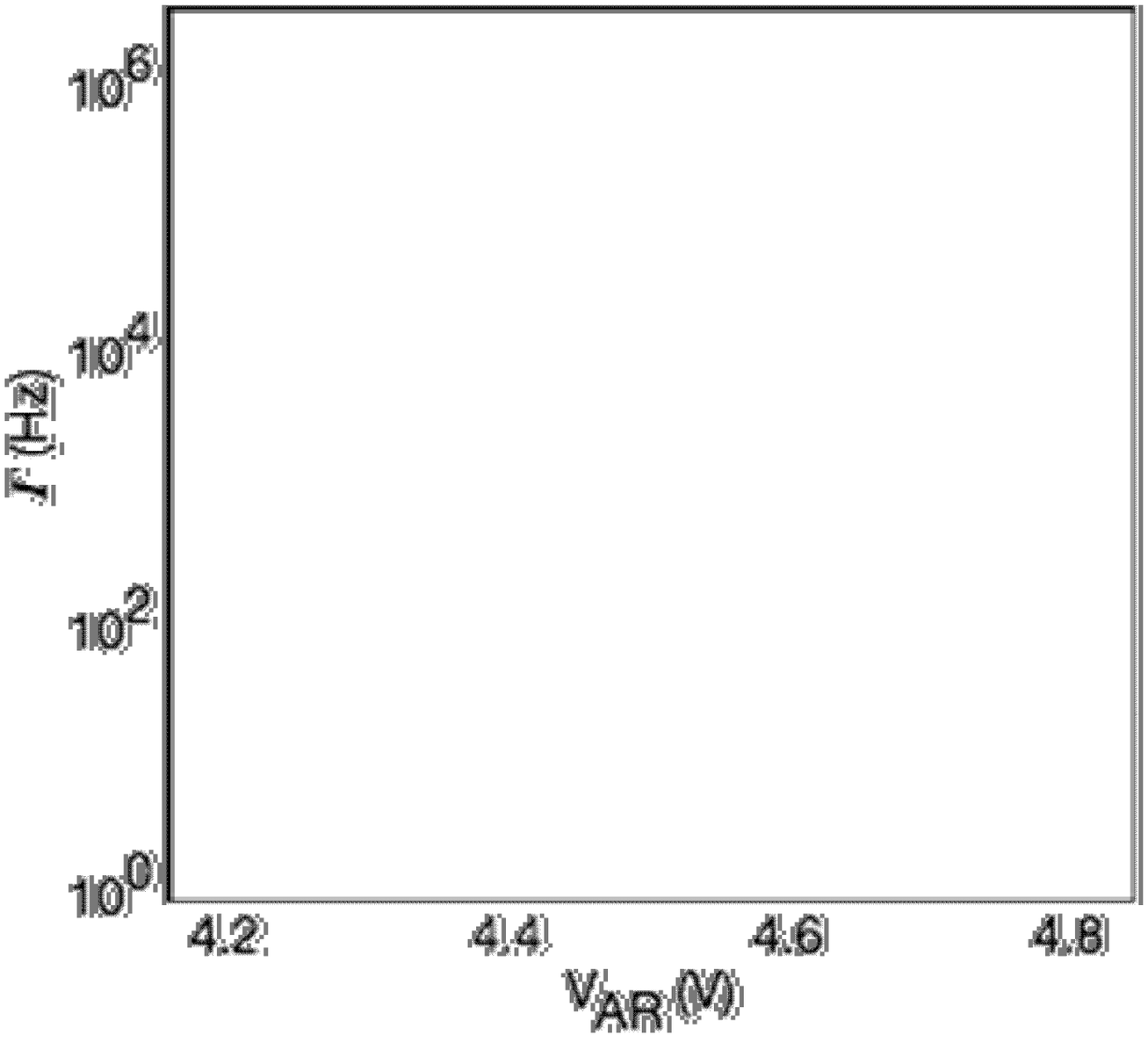
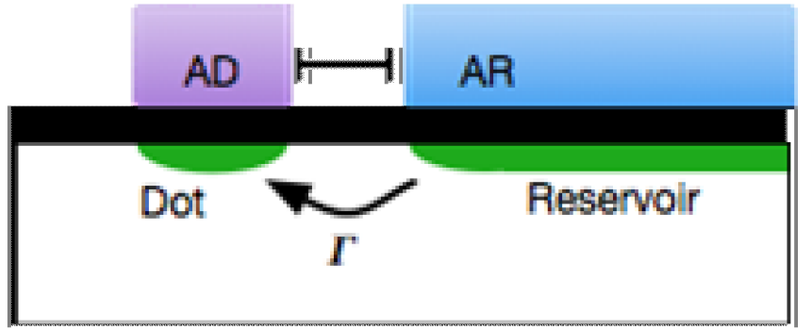




Tuning orthogonality: tunnel rate and dot occupation





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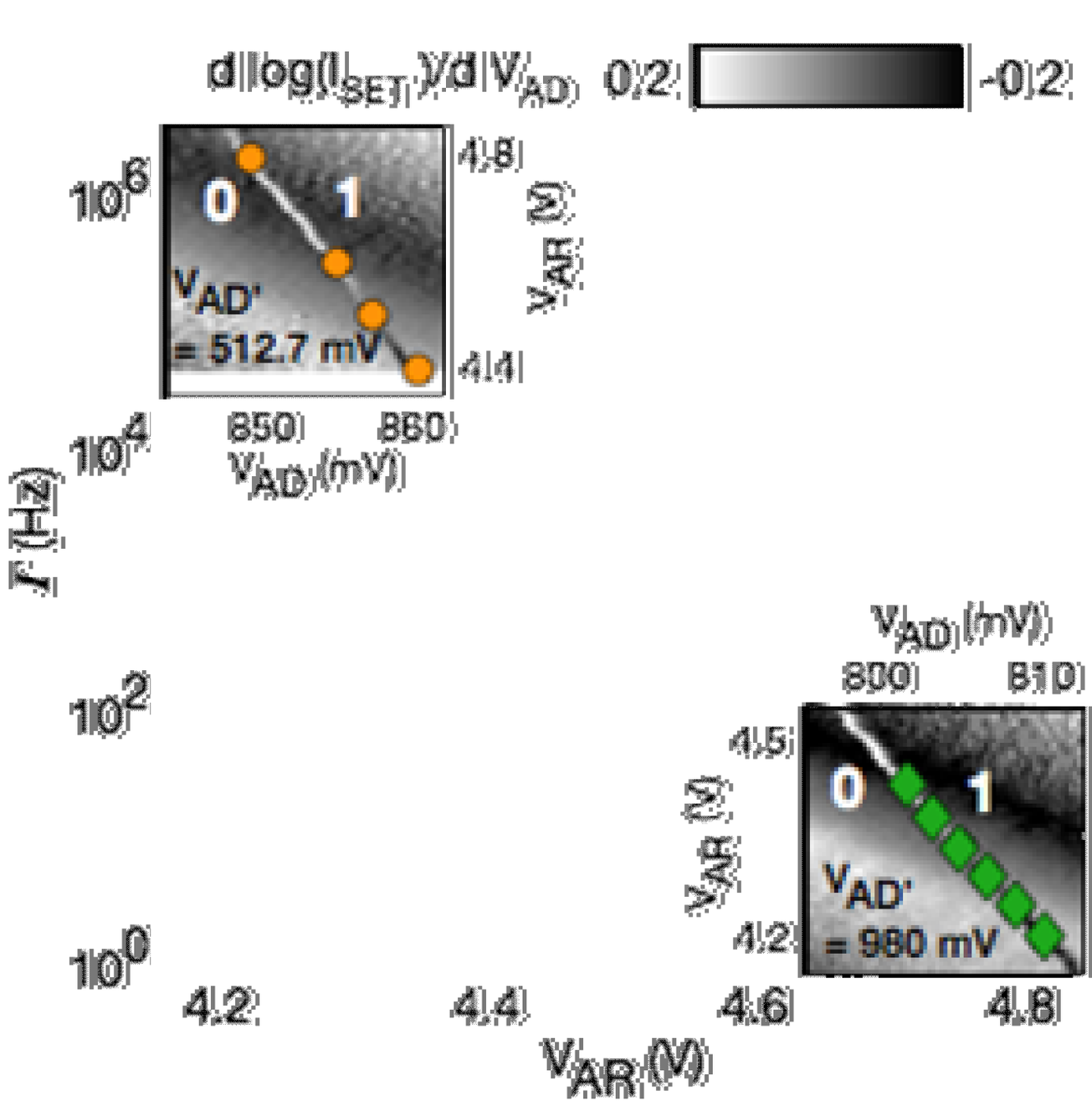
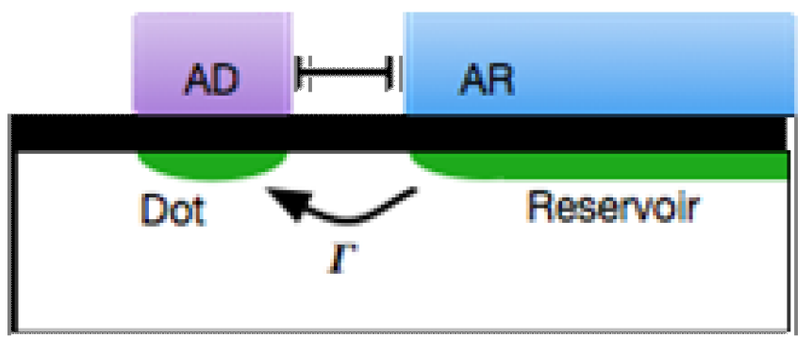
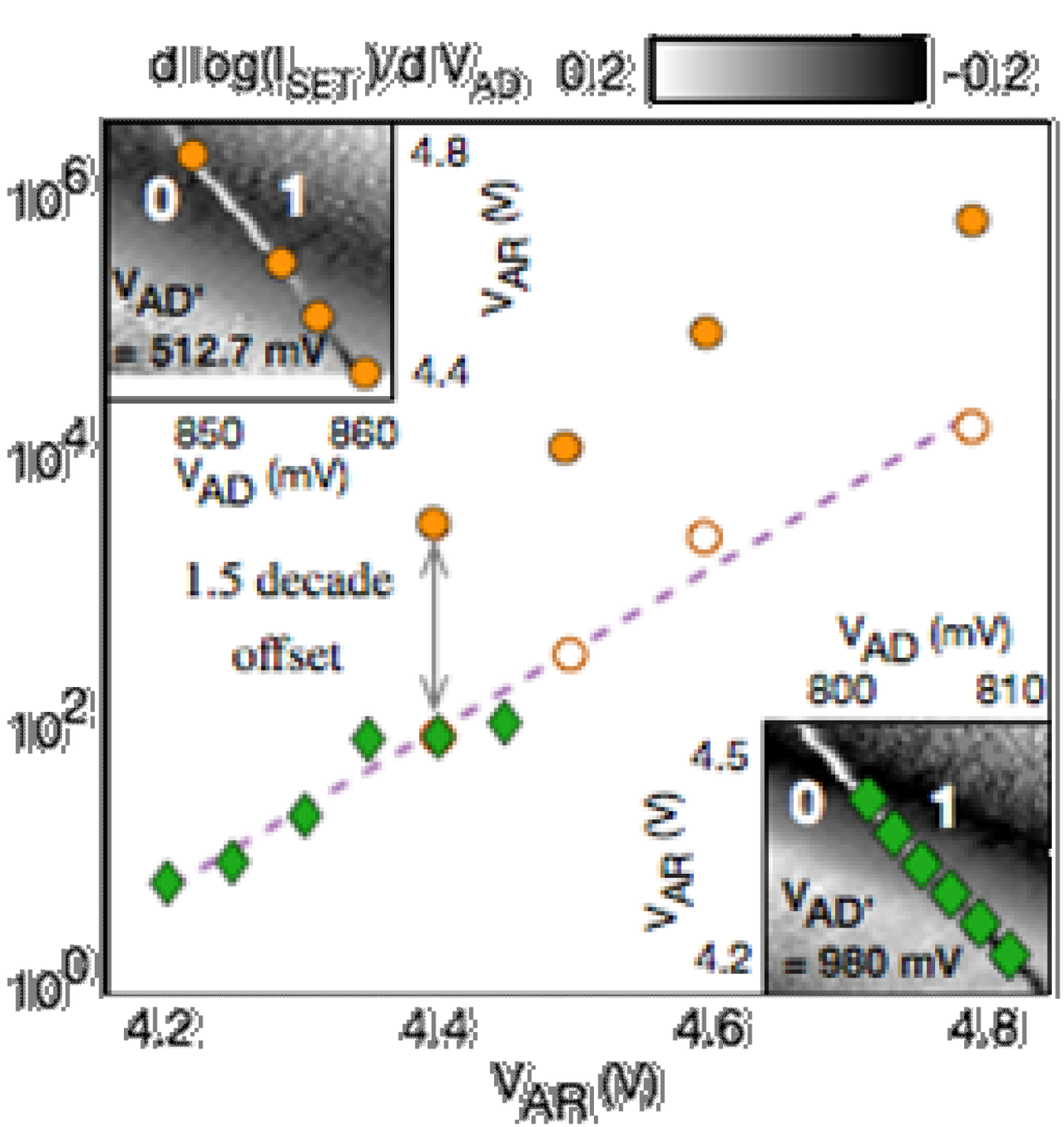
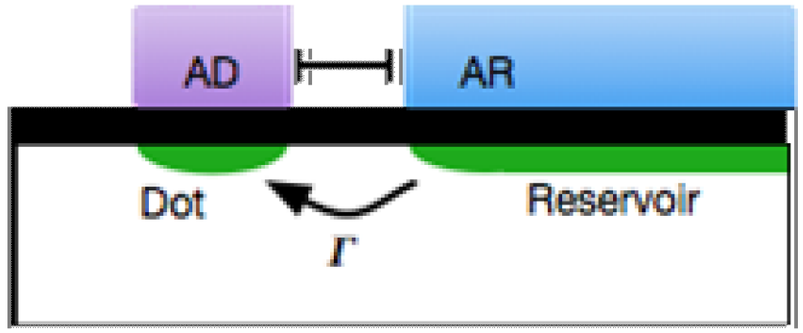




Tuning orthogonality: tunnel rate and dot occupation

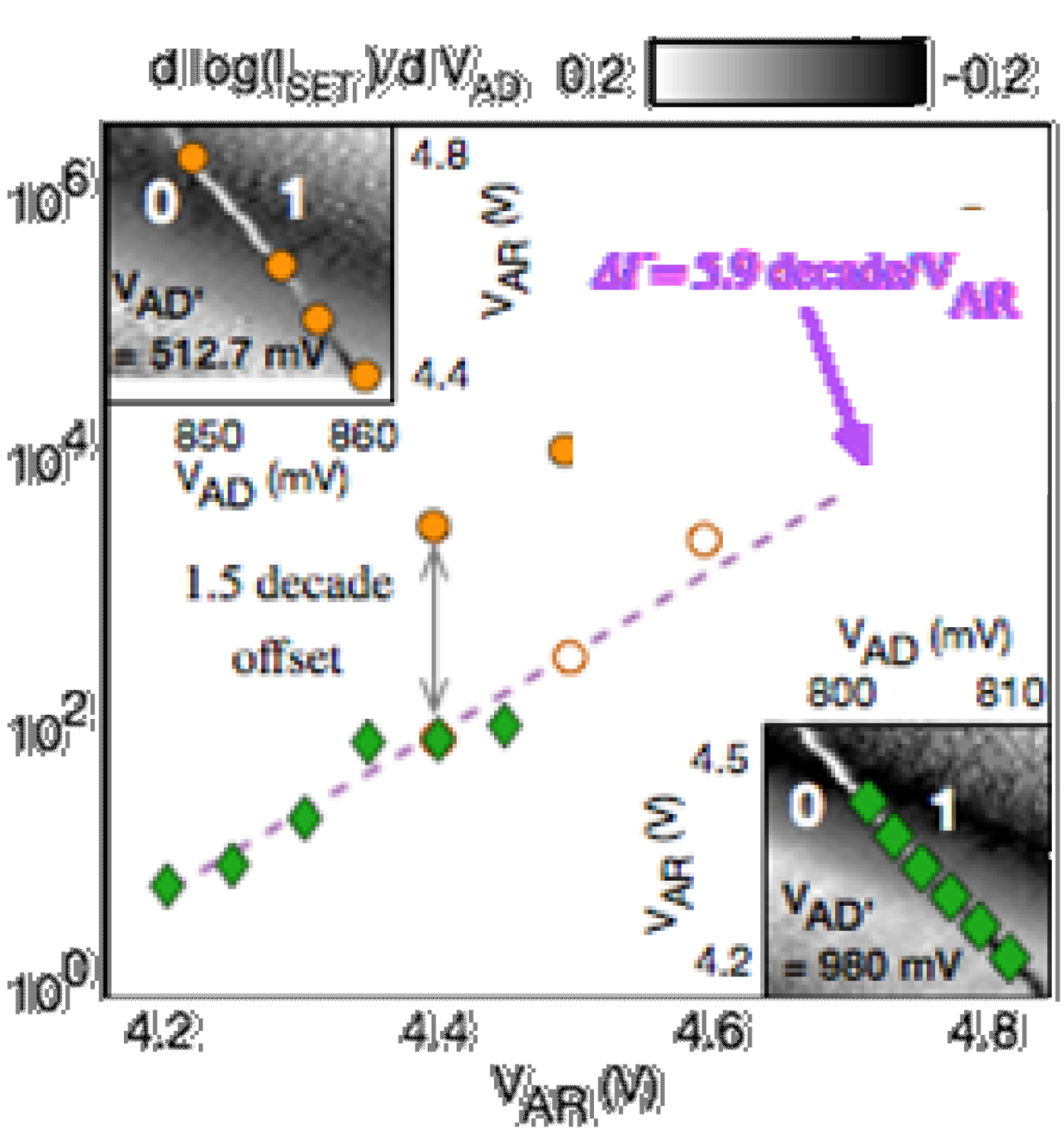


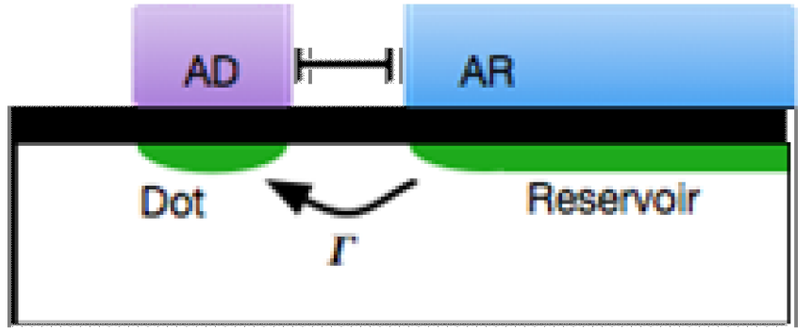


Gustavsson et al., Surf. Science Rep. 64, 191 (2009).

Elzerman et al., APL 84, 234617 (2004).

Tuning orthogonality: tunnel rate and dot occupation





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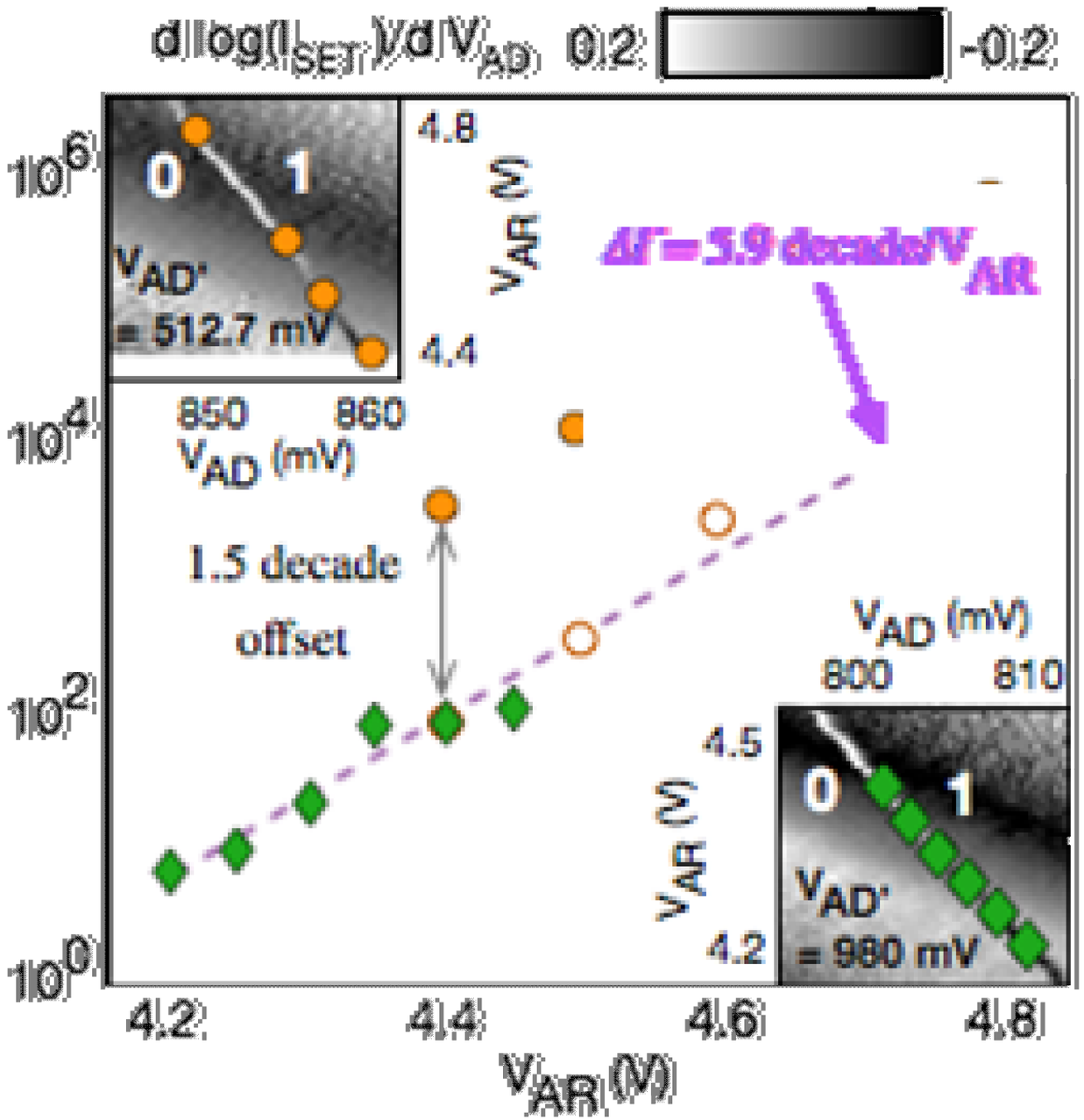
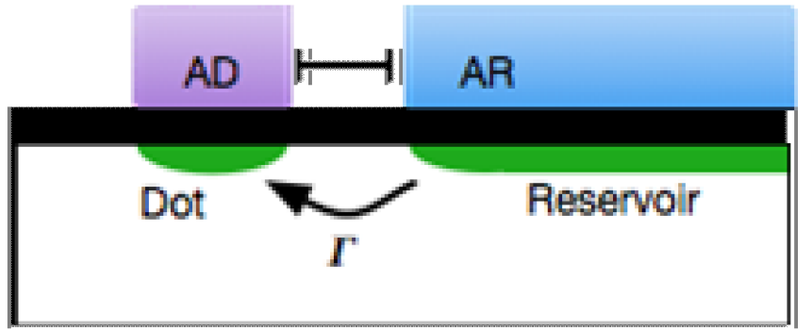
Tuning orthogonality: tunnel rate and dot occupation





Tuning orthogonality

$\beta_{AR,\,AD} = \Delta\Gamma_{AR} / \Delta\mu_{AR}$

$\beta_{AR,\,AD} \approx 0.9 \pm 0.3$ decade/mV

Dedicated barrier gate:

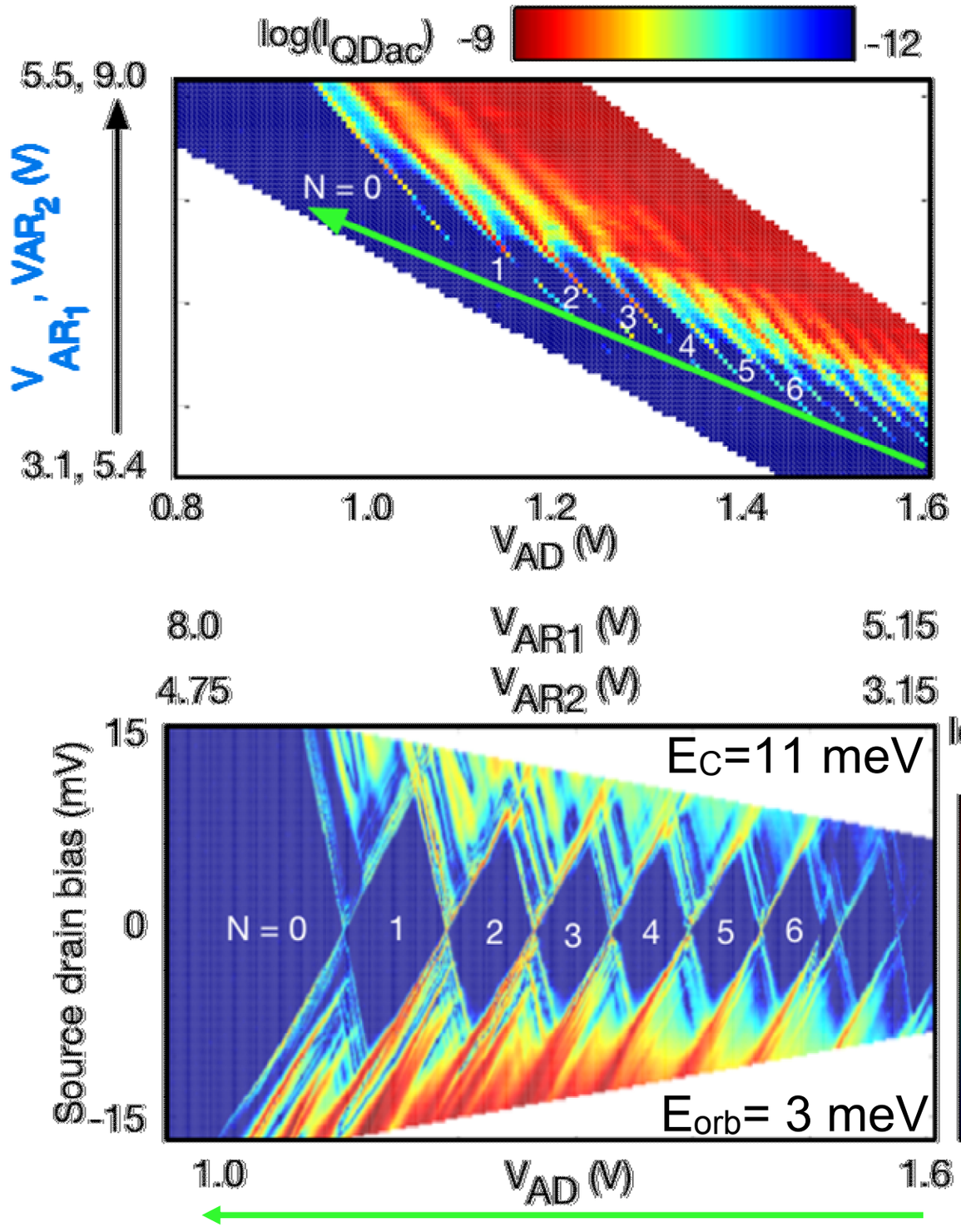
Zajac et al., APL 106, 223507 (2015).

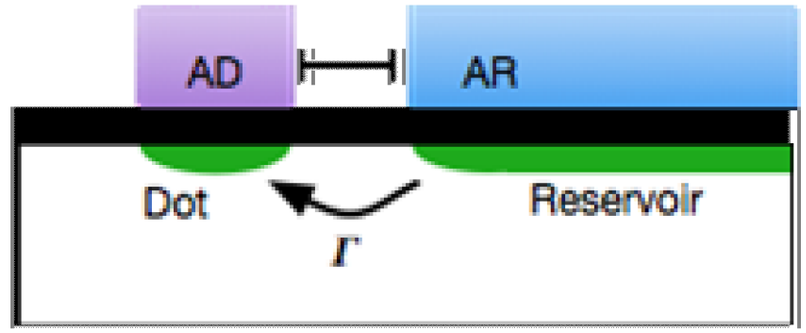
$\beta_{B,\,AD} \approx 1.1 \pm 0.3$ decade/mV

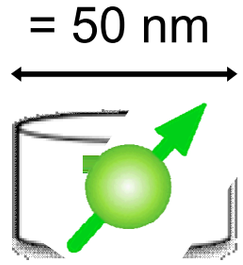
Gustavsson et al., Surf. Science Rep. 64, 191 (2009).
Elzerman et al., APL 84, 234617 (2004).

S. Rochette et al., in preparation

Quantum dot confinement in the split gate devices







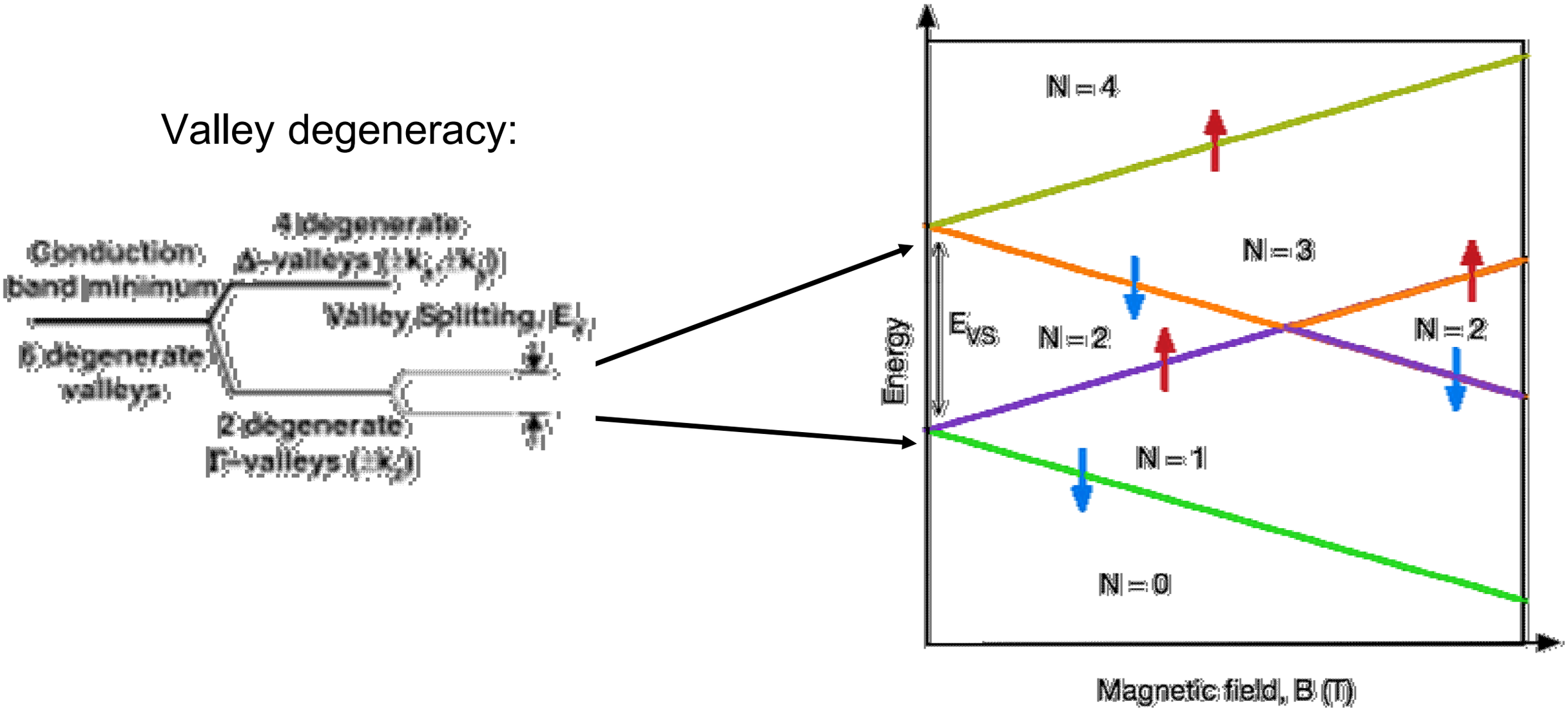
Strong confinement

Double-lead device

Data by Martin Rudolph, SNL

Magnetospectroscopy: Spin states in silicon

Valley degeneracy:



Electronic states in silicon quantum dots: Multivalley artificial atoms,
Y. Hada and M.Eto, PRB 68, 155322, 2003

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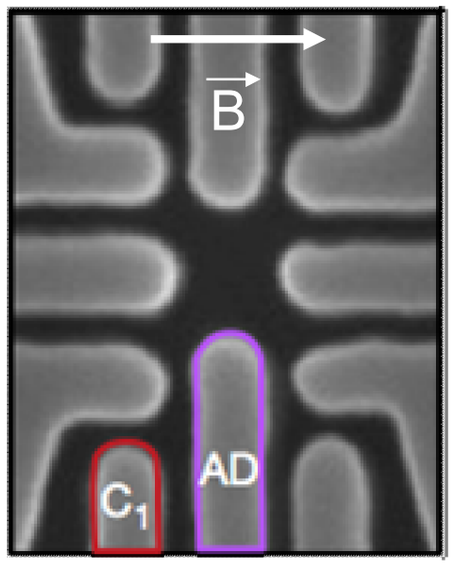

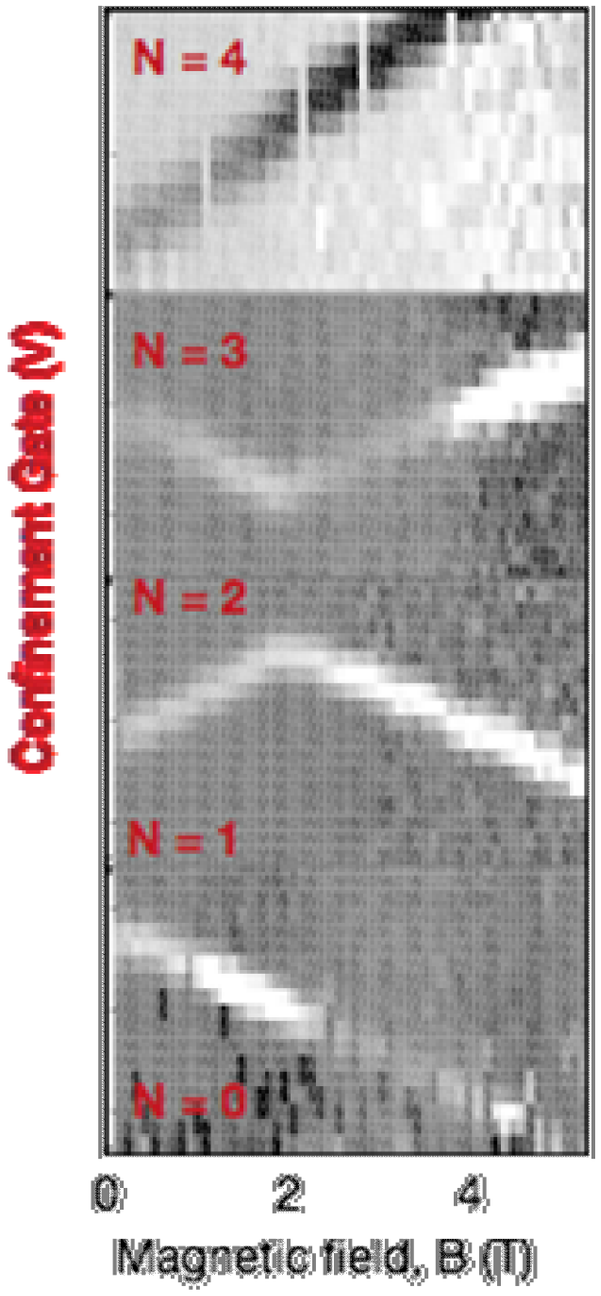

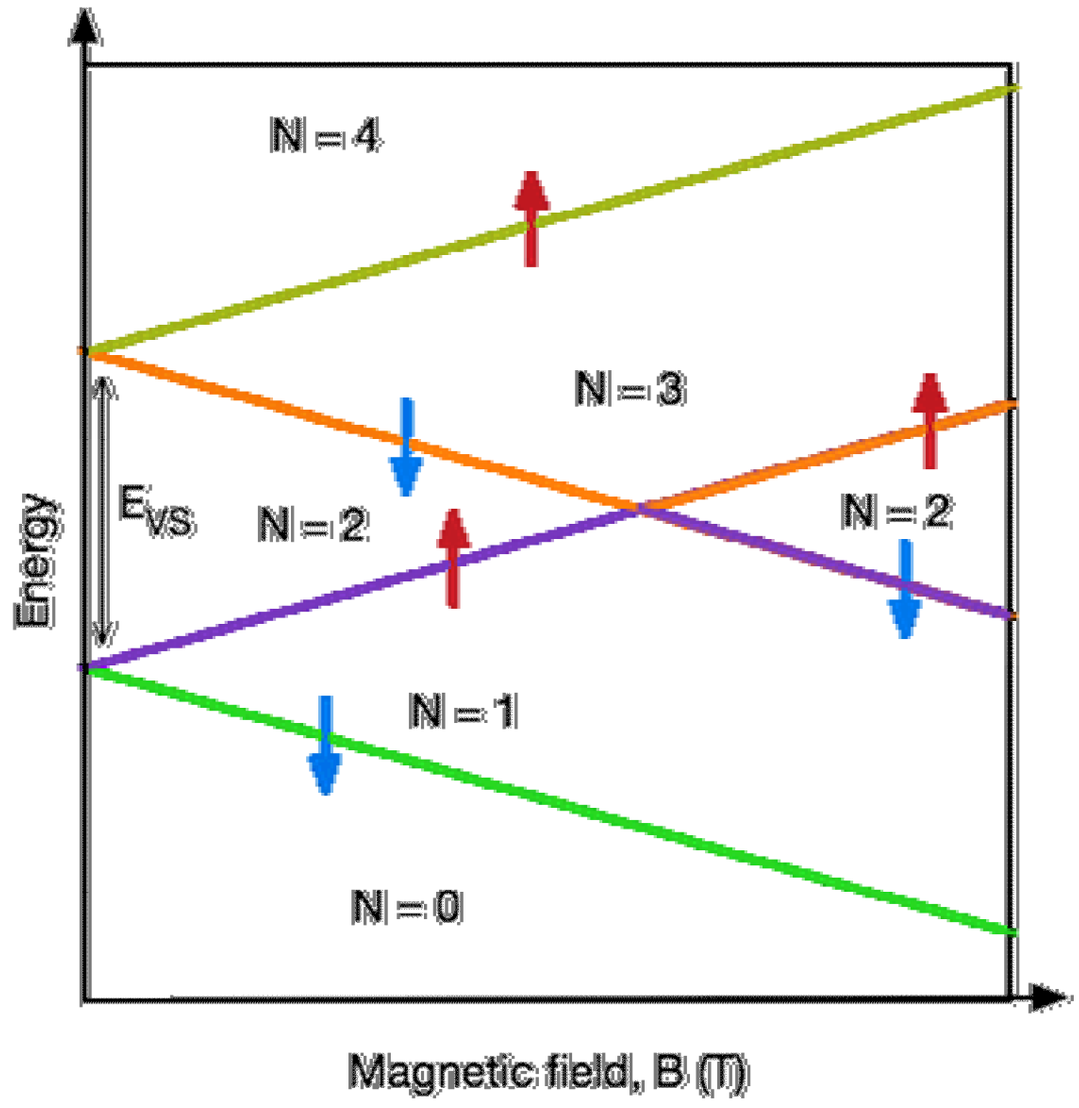

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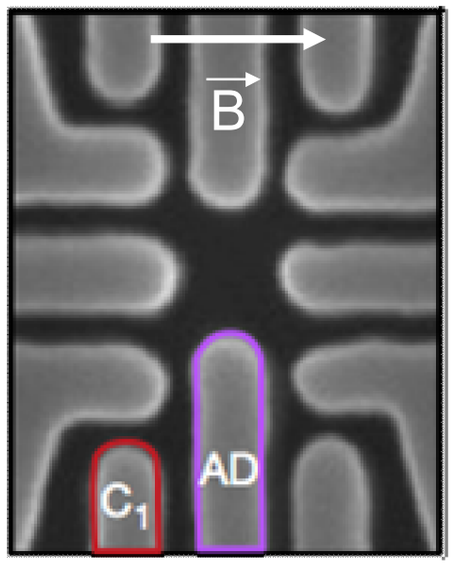

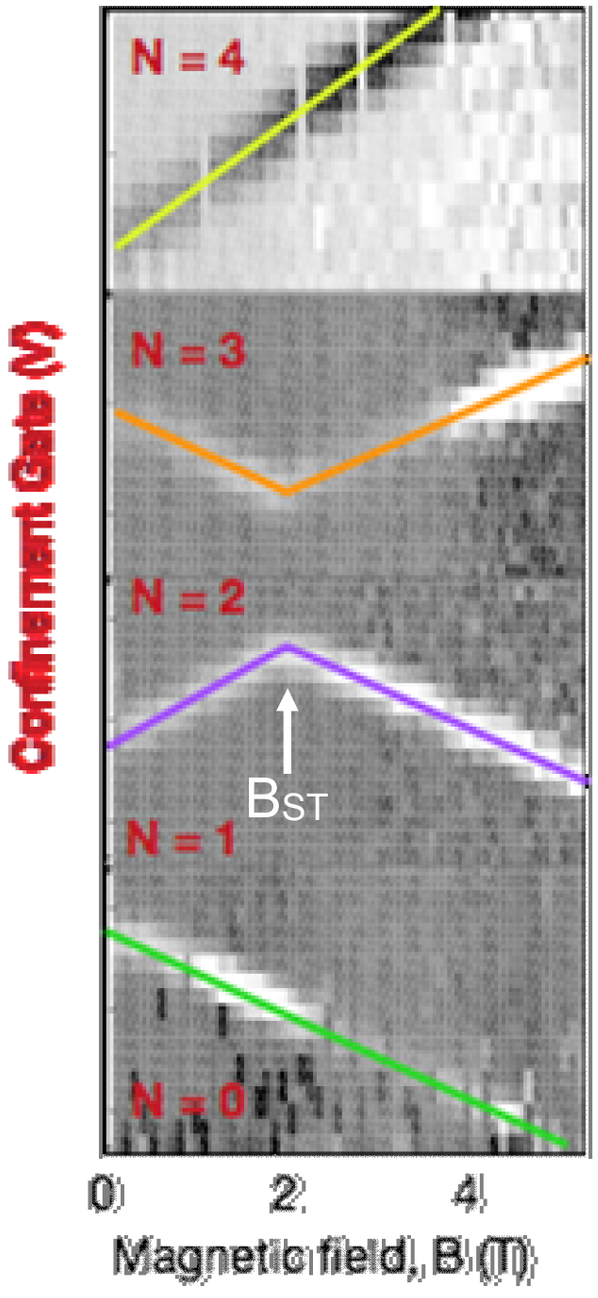

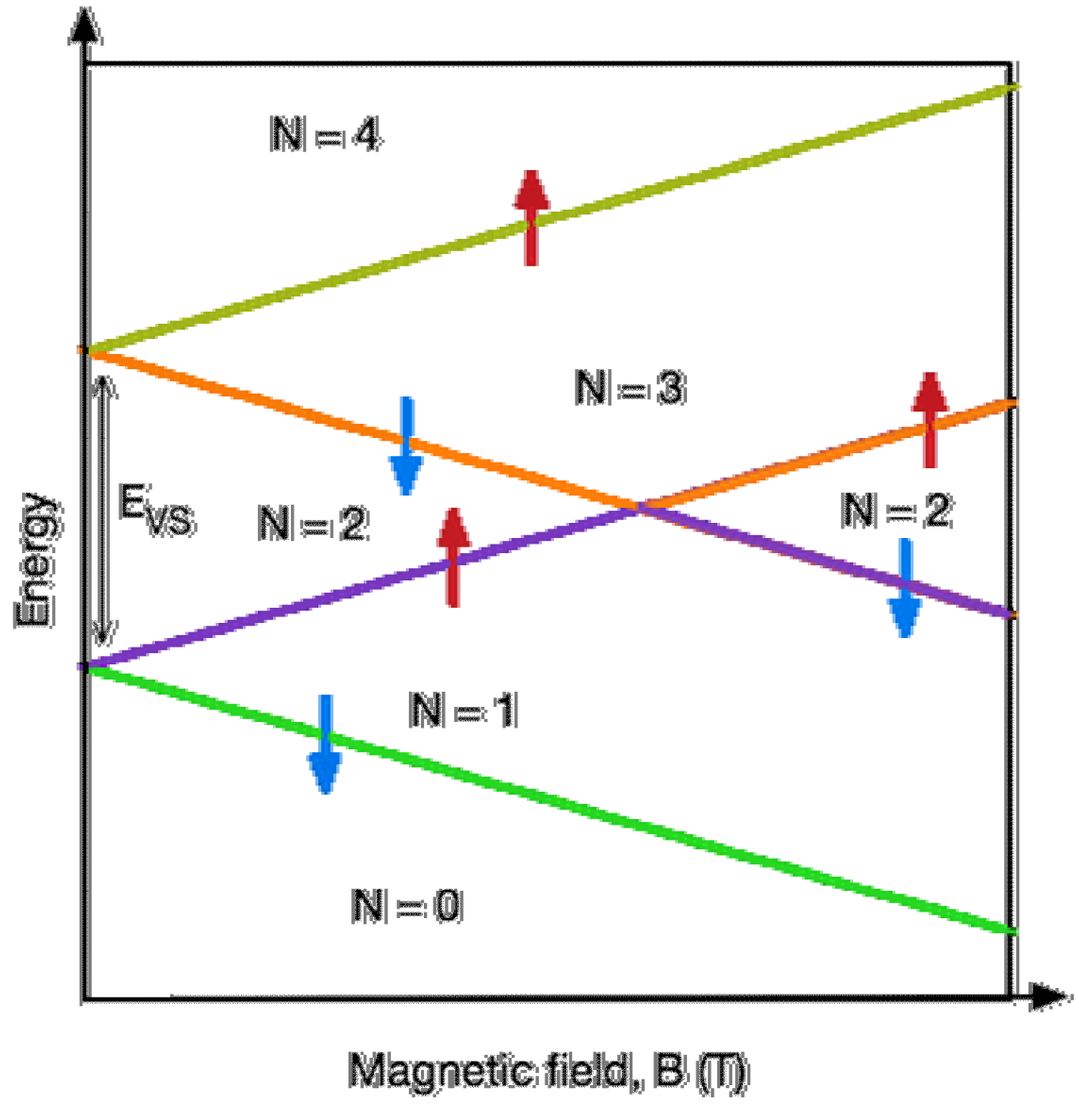

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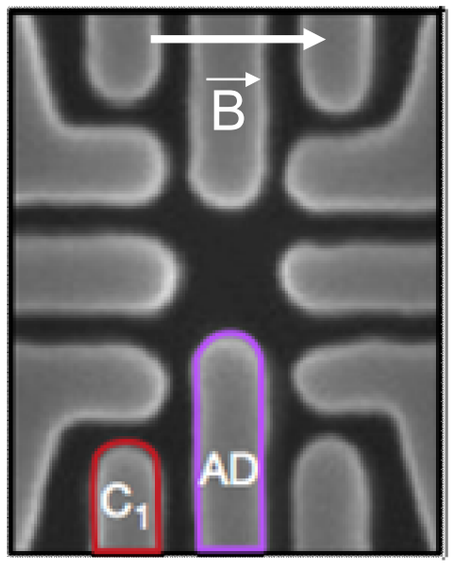
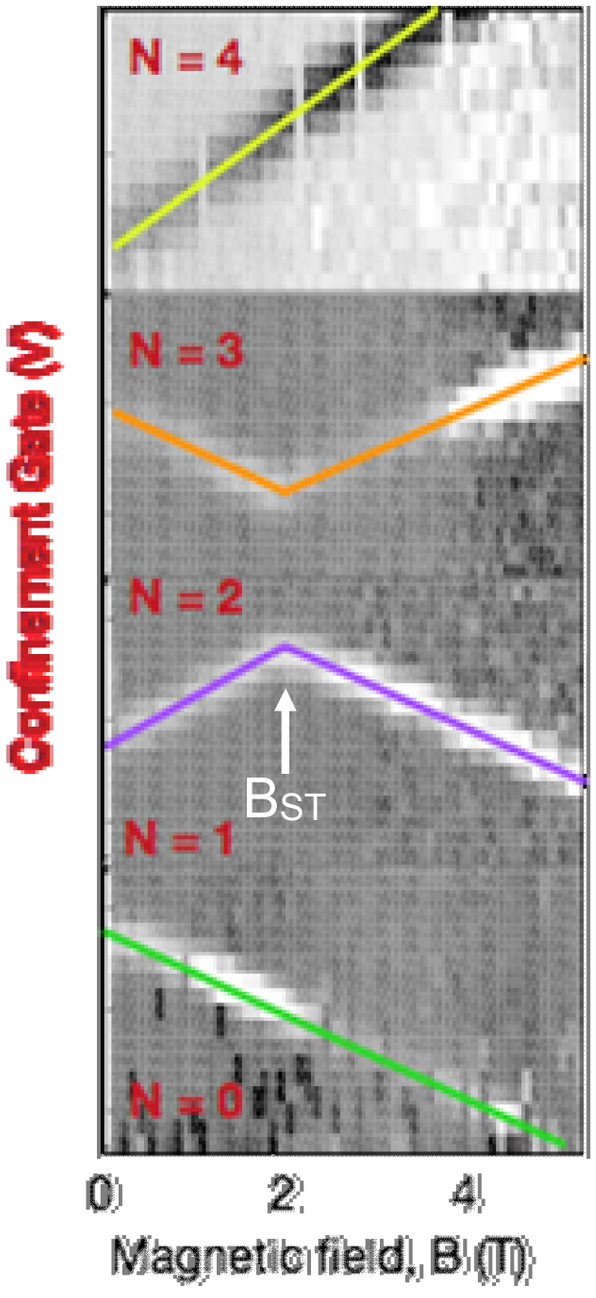
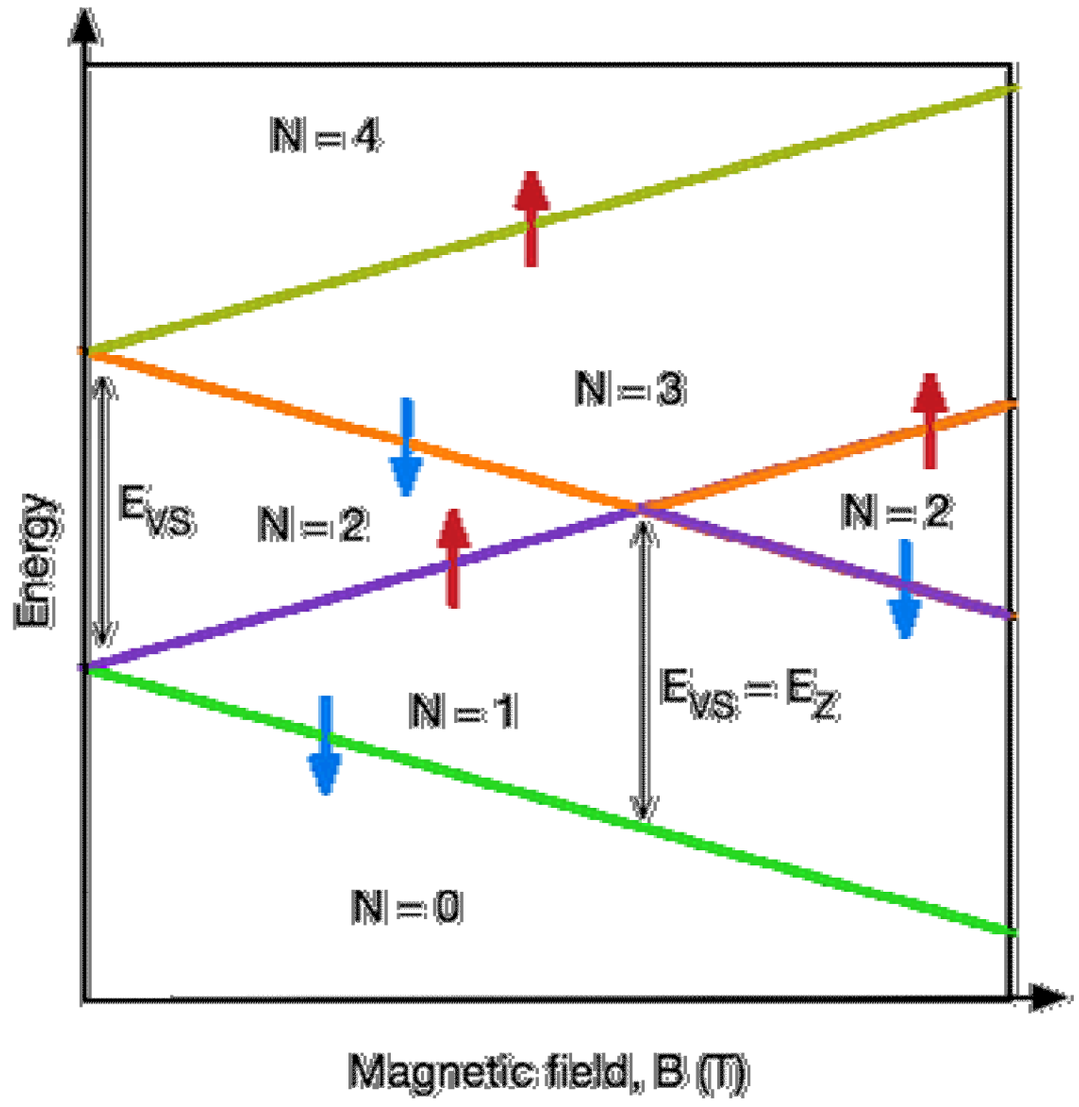


$$E_{VS} = g\mu_B B_{ST}$$

$$\approx 220\ \mu\text{eV}$$





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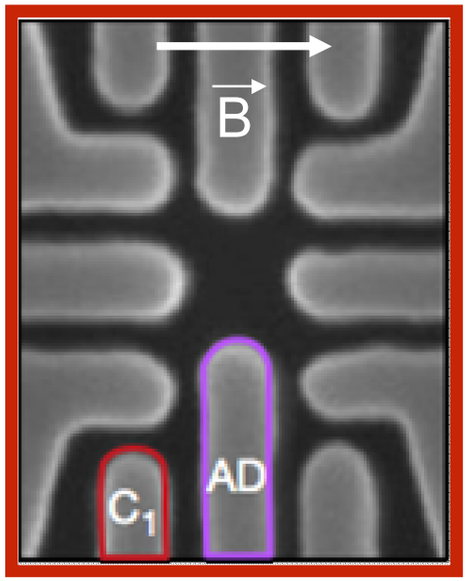
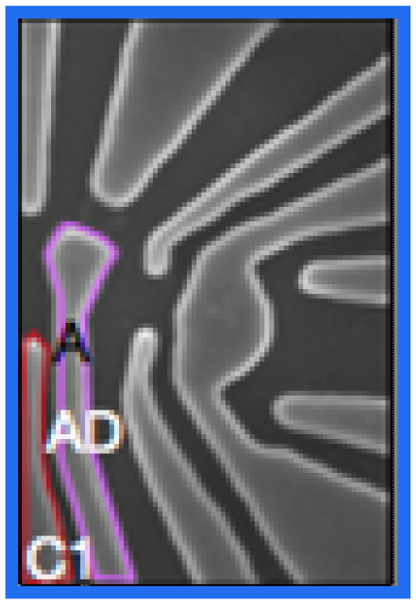
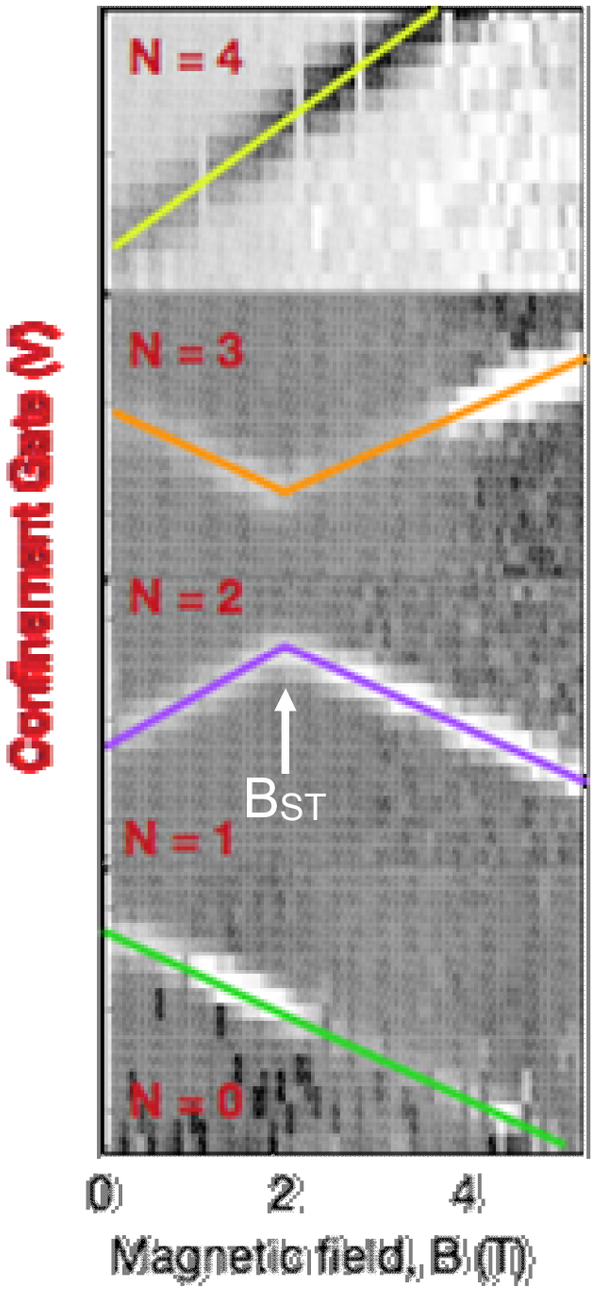
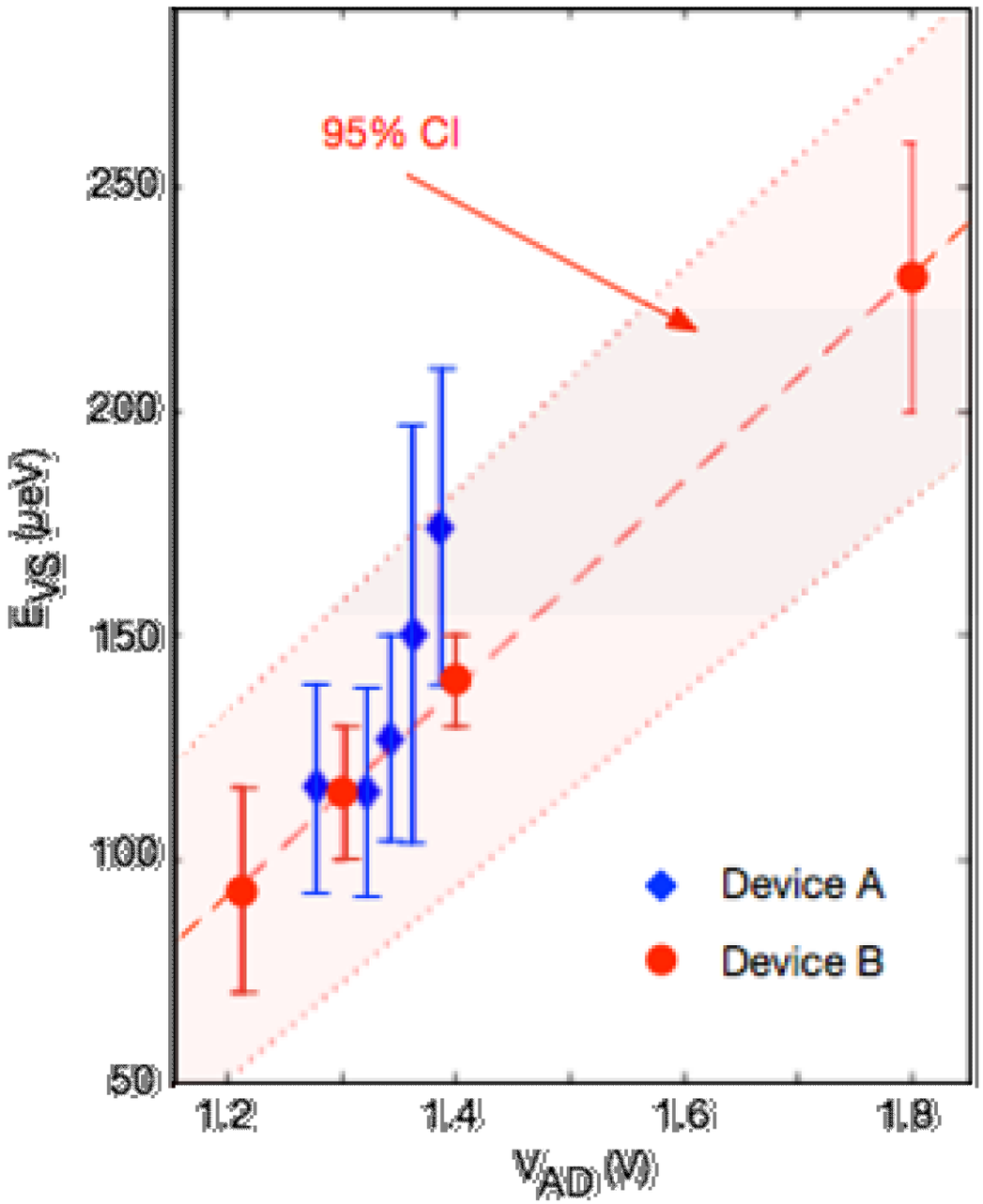
Valley splitting tuning







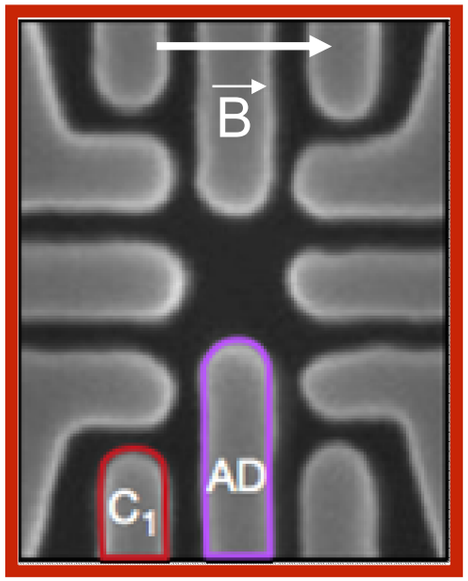
Separation ST increases with the vertical electric field (V_{AD})

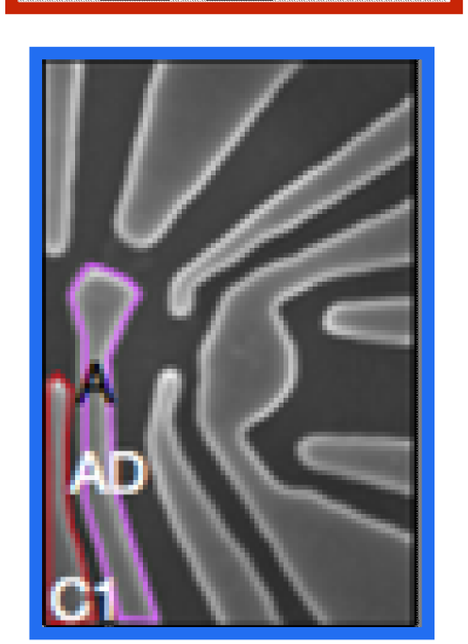


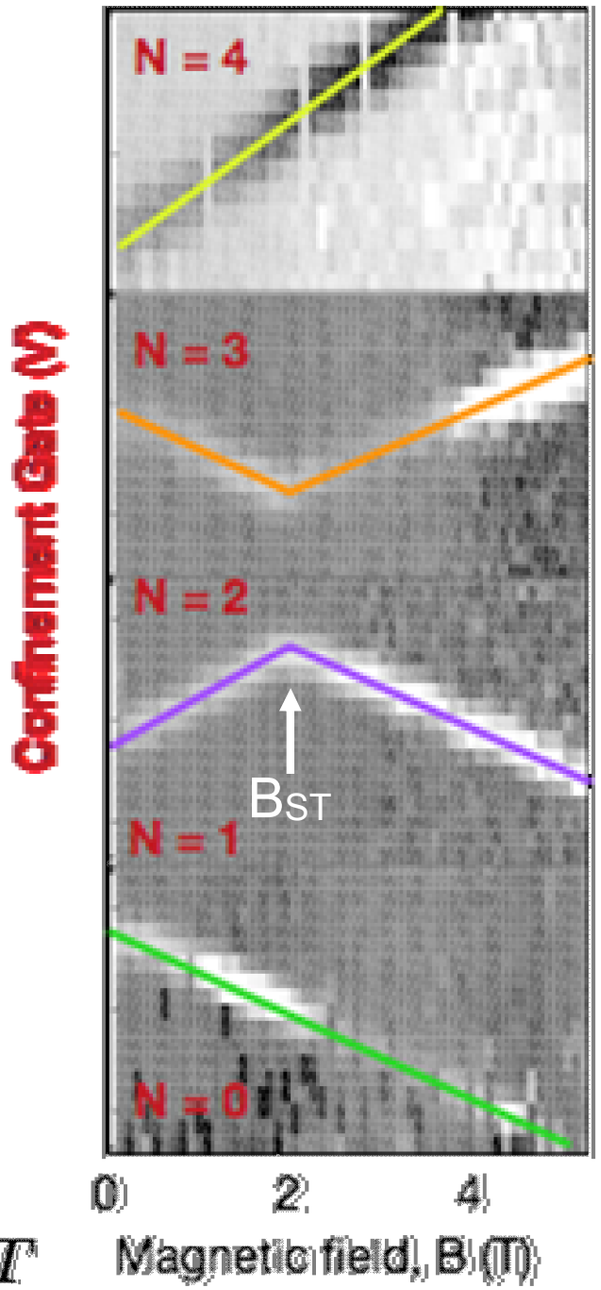
Yang 2013's results, after division by 3.5 to take in account differences in the gate oxide thickness: **182 µeV/V**

Spin valley lifetimes in a silicon quantum dot with a tunable valley splitting, C. H. Yang et al, *Nat. Comm.*, 2013

Valley splitting tuning







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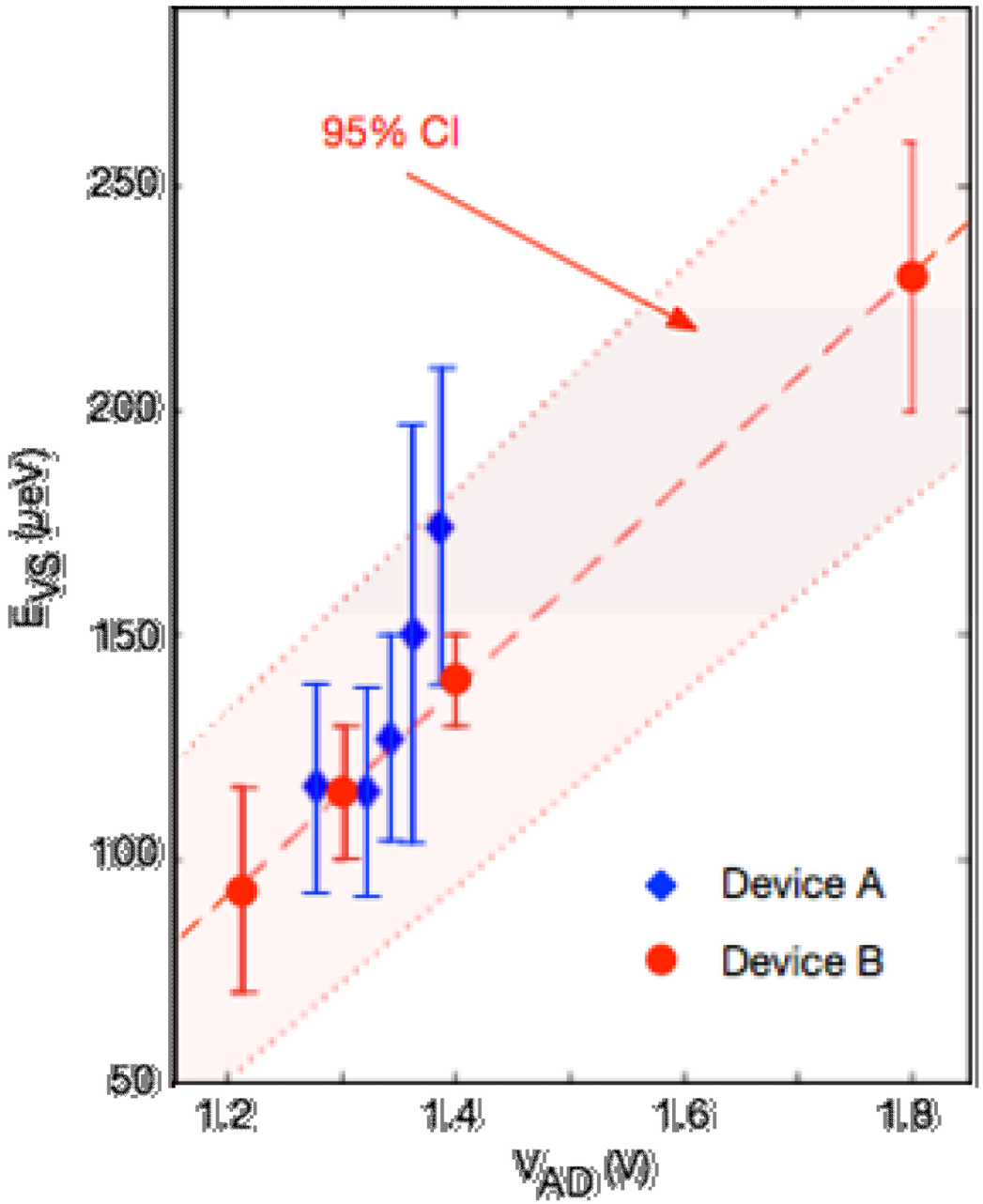
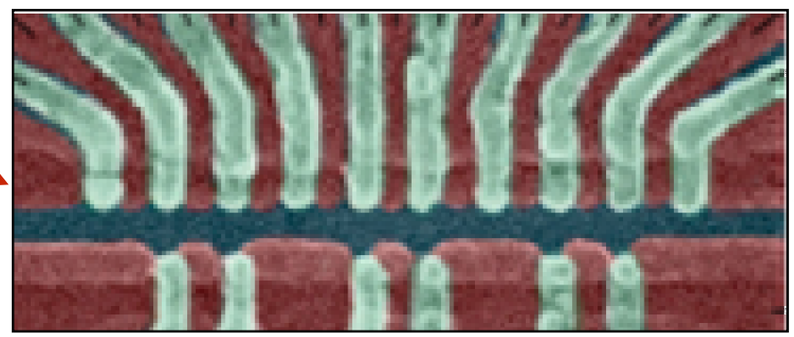


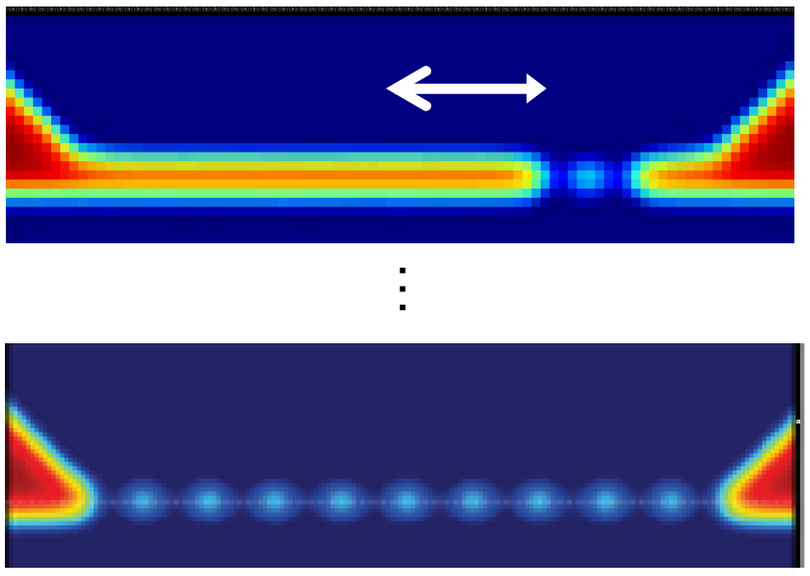
Yang 2013's results, after division by 3.5 to take in account differences in the gate oxide thickness: **182 µeV/V**

Multiple quantum dots initialization and readout

One reservoir per extremity

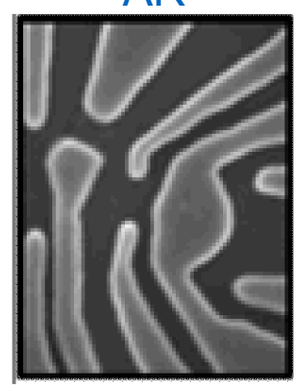


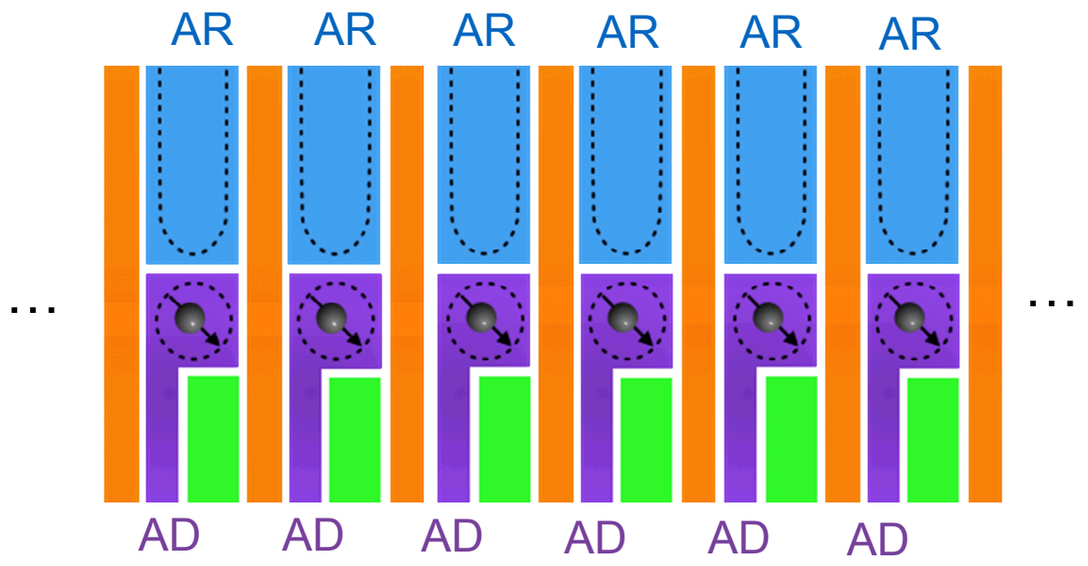
Initialization of a 1D array



Readout: SWAP until reservoir reached (or PSB)

One reservoir per QD?



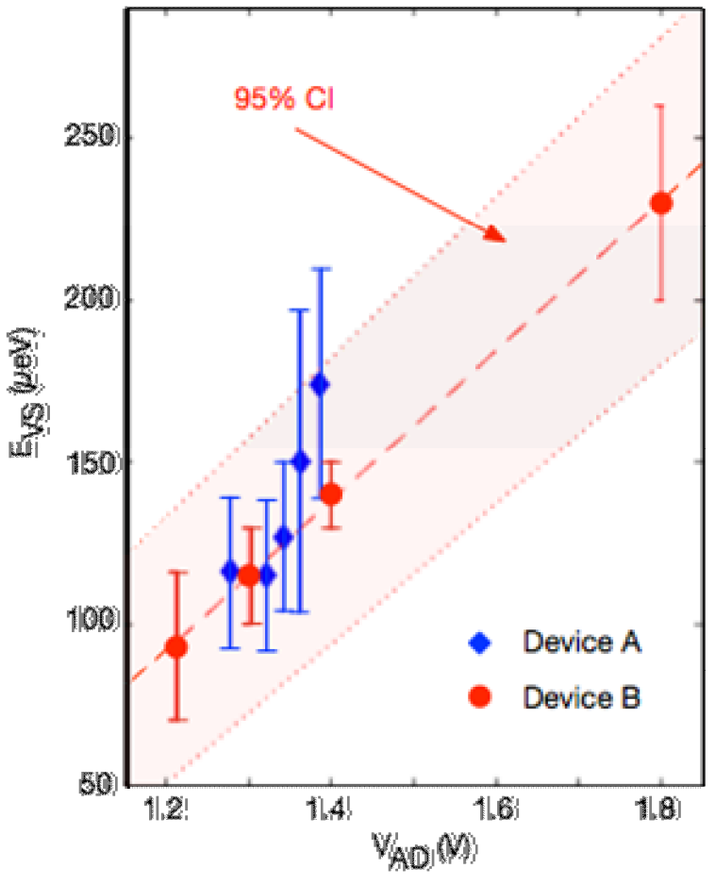


Initialization and readout accessible for each quantum dot

Zajac *et al.*, 2016

A reliable platform for scaling up QD arrays

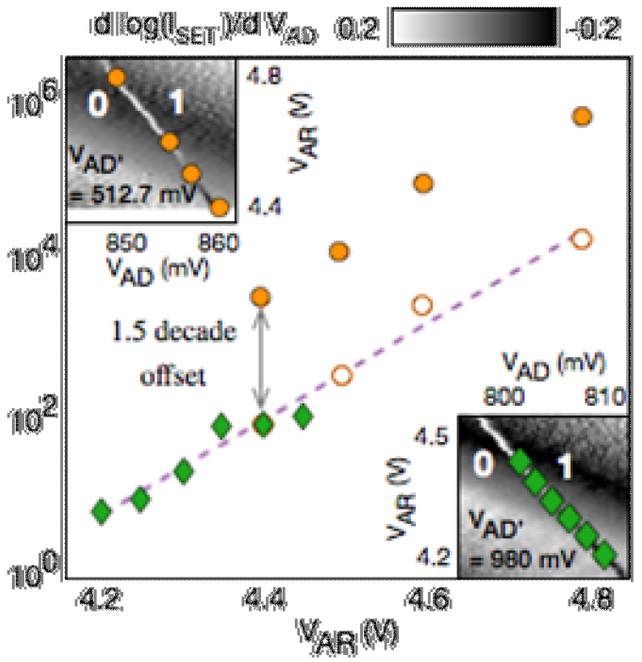
(1) Well-isolated two-level system

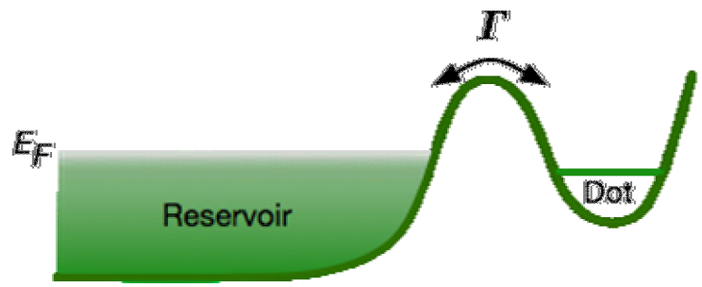


-Strong confinement, d < 50 nm

-Large and tunable valley splitting, 75 to 225 μeV and +

(2) Dot-reservoir tunnel rate control



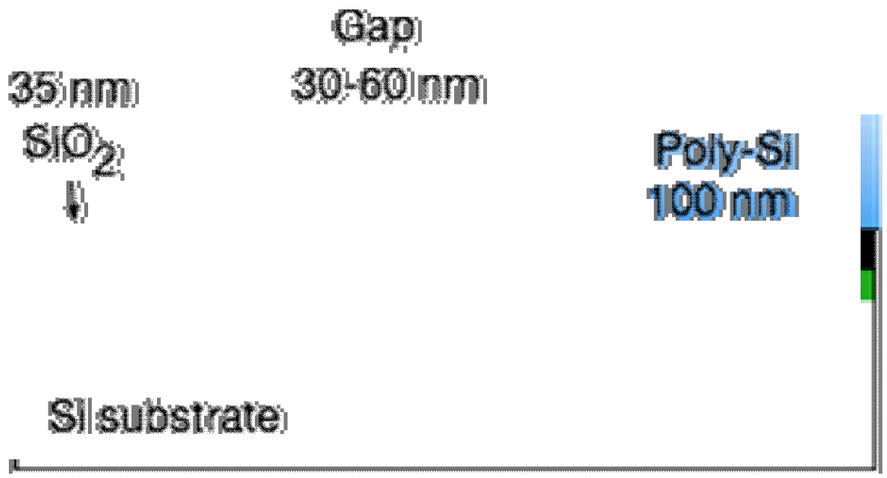


Tuning orthogonality tunnel rate vs dot occupation:

$\beta_{AR,\,AD} \approx 0.9 \pm 0.3$ decade/mV

Comparable to dedicated barrier gate devices

(3) Extensible fabrication



- Single poly-si gate stack process entirely CMOS compatible and high yield

-One reservoir per dot: Could simplify initialization and readout for large arrays

Acknowledgements

Project supervision

M. Pioro-Ladrière
M. S. Carroll

Data and analysis

M. Rudolph
M. J. Curry
A.-M. Roy

Sandia National Laboratories

G. A. Ten Eyck
J. Dominguez
R. P. Manginell
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J. K. Gamble
M. P. Lilly
C. Bureau-Oxton

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