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Time Delay Definitions and Characterization in the Pacific DC Intertie Wide Area Damping Controller

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***Abstract*—When large generation and load centers are separated by long transmission lines, the propensity for complex inter-area oscillations increases. These oscillations are deleterious to utility systems since they may cause damage to equipment or restrictions on power flows. To improve small-signal stability in the utility grid, new methods of control have been introduced that utilize local and remote feedback of phasor measurement unit signals to compute a control action. A key consideration in the implementation of these controls is thus the network and control delays associated with these signals since excessive control delay may degrade performance. This work focuses on the recently installed Pacific DC Intertie wide area damping controller prototype system located at the Celilo Converter Station. Network and control delays are defined and quantified through experiments done to commission the system, and the results are discussed in the context of the controller's expected performance.**

***Index Terms*—HVDC modulation, time delay, communication latency, Pacific DC Intertie, smart grid, synchrophasors, wide area control**

I. Introduction

Large power systems with long transmission corridors often have small signal stability problems that are characterized by a low-damping condition and are thus prone to inter-area oscillations. The small signal stability problem is mitigated by adding power system stabilizers (PSSs) to specific conventional generators throughout the system. The PSS works by adding a control signal to the excitation system of the generator, but the PSS control signal is based on only local measurements and typically needs to be tuned. Despite these controls, however, small signal stability issues all too often result in limits to power transfer between areas.

It has recently been shown that control action based on feedback from local and remote locations in the grid can help improve the stability of the system [1]. This is the concept of wide area control, wherein controllers throughout the power system receive real-time information over a network and compute a control signal based on local and remote feedback. This idea has been facilitated with the recent introduction of phasor measurement units (PMUs) into the grid. PMUs measure and transmit (over a network) important system variables such as voltage and current magnitudes and angles as well as real and reactive power flows. In addition, the PMU data is GPS time stamped, allowing data from different locations to be synchronized.

For controls that depend on transmitted data from remote locations, the control performance will invariably depend on the network latency. Delays associated with message handling, processing, and control actuation must also be accounted for. Excessive time delays have been shown to degrade the performance of wide area control systems [2], [3]. Modeling and quantifying the different components of this time delay is hence of critical importance to predict and enhance performance of wide area controllers [4], [5].

In this work, the network and control delays associated with the Pacific DC Intertie (PDCI) wide area damping controller [1], [6] prototype are characterized in detail and quantified through extensive experimental work. The paper starts by systematically defining the different types of delays associated with this application of PMU-based real time control. The delays account for the lags in the information flow from the time a PMU measurement is captured to the moment that information is translated into a PDCI action. The paper then presents a detailed characterization of the defined delays which are quantified using actual data obtained from PDCI damping controller tests conducted in September 2016.

This paper is organized as follows, Section II presents an overview of the PDCI damping controller, Section III defines the delays related with this controller. Section IV presents actual measurements of the defined delays. Finally, Section V outlines the conclusions and future work for better handling time delays in wide area control systems.

II. Overview of the PDCI Damping Controller

The sparse nature of the western North American Power System (wNAPS) with generation and loads separated by large distances and loosely connected by long transmission lines makes it particularly vulnerable to inter-area oscillations. Low damping conditions often limit the transfer capabilities of long transmission corridors; providing supplemental damping may increase the power transfer capacity of these corridors. In 1996 inter-area oscillations were part of the root cause of a breakup of the wNAPS in which nearly 7.5 million people lost power [7]. As a precautionary measure to avoid a repeat of this event, the power export from the northern part of the system (rich in hydro electricity) to the southern part of the system (having large load centers) was curtailed.

A collaborative effort by Sandia National Laboratories (SNL), Montana Tech University (MTU) and Bonneville

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Power Administration (BPA) to provide damping to these oscillations is currently underway with focus on the North-South B mode [1]. This project aims at designing and implementing a damping controller prototype to modulate the power transfer of the PDCI. The PDCI is the longest HVDC link in the United States linking the Washington-Oregon border with the Southern California region (Los Angeles). The controller is located at the Celilo Converter Station which is the northern terminus of the PDCI. The PMU data is streamed to this location in accordance with the C37.118 standard using a UDP protocol in multicast configuration through a dedicated fiber network.

The controller prototype utilizes the difference between a northern and a southern synchrophasor frequency measurement [1] to construct the modulation signal command for the PDCI [1]. However, to improve controller resiliency, four different measurements in the north and four different measurements in the south are monitored and made available for redundancy. Availability of these signals allow the controller to select the best pair of signals from 16 possible options [6]. In the subsequent section, delays are characterized for each of these eight PMUs.

III. Characterization of System Time Delays

This section outlines definitions of time delays related with the progression of information in the PDCI wide area damping controller. Fig. 1 illustrates the progression of information from the moment a measurement is captured in the grid, to the time this information is reflected in a PDCI adjustment as a result of a control command. The time delays associated with the different stages underwent by the flow of information in the controller, presented in Fig. 1, are defined as follows:

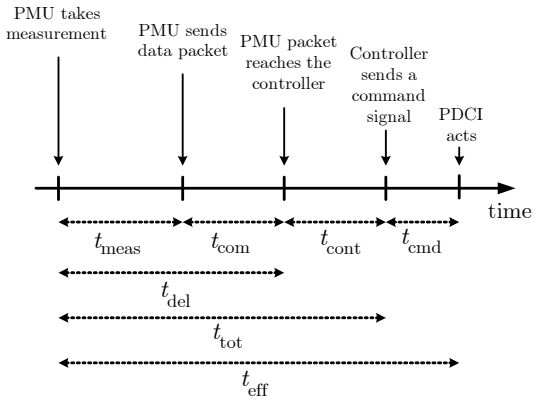

Fig. 1. Different time delays associated in the controller, from the time of measurement to the time this information is reflected in a PDCI action. This time frame of delays corresponds to a single PMU.

PMU Delay (t_{meas}) – the time for a PMU to take a measurement from the grid, construct a data packet, and send it to the network.

Communications delay (t_{com}) – the amount of time for a PMU data packet to reach its destination (the controller) from the moment it is sent by the PMU.

[1]The controller actually uses voltage angle measurements to obtain frequency measurements using a derivative filter.

Signal delay (t_{del}) – the total time taken for a measurement to reach the controller. It is the addition of the communications delay and the PMU measurement delay.

Controller processing delay (t_{cont}) – it is the time elapsed between the moment a PMU data packet arrives at the controller and the moment the controller sends a power command based on the information of that data packet.

Total controller delay (t_{tot}) – it is the time elapsed between the PMU measurement and the moment the power command is sent by the controller. It consist of the addition of the signal delay and the controller processing delay.

Command delay (t_{cmd}) – it is the time elapsed from the moment the controller sends a power command to the moment the PDCI responds.

Effective delay (t_{eff}) – the time between the moment the PMU takes a measurement and the moment when the PDCI acts on the information from that measurement.

Interpacket delay (Δt) – it is the time difference between the time of arrival of two consecutive PMU data packets (for the same PMU).

Interpacket delay of time stamps (Δt_{TS}) – it is the time difference between the time stamps of two consecutive PMU data packets.

IV. System Latency Measurements

A. Interpacket Delays

The interpacket delay is the interval of time from the arrival at the controller of one data packet to the next. Because the PMUs have a uniform sampling rate of 60 samples per second (sps) the interpacket delays measured at arrival are expected to cluster at around $16.66\overline{6}$ms.

1) Network Characterization: The interpacket delay for the 8 PMUs used by the controller are shown in Figs. 2 (a)-(b). These results show that interpacket delays have the following behavior: (i) on average they approach the expected $16.66\overline{6}$ms, (ii) however, sometimes they experience cyclical behaviors of the type shown in closer detail in Fig. 2 (b); during this behavior the time between data packets is sometimes high around 24ms and sometimes low around 10 ms. In fact, three interpacket delays add up to 50ms for an average of $16.66\overline{6}$ ms among those three (three interpacket delays are obtained from four packets sent). The lower interpacket delay value is prompted by the higher one as the PMU has to catch up and sends two packets spaced within less than $16.66\overline{6}$ms, and (iii) at the top of every minute the interpacket delay increases to above 34 ms and is followed by delays of around 4 ms again to make an average of $16.66\overline{6}$ms among 3 data packets. This particularity is due to a configuration (config) data packet that the PMU has to send according to the C37.118 standard (at the top of every minute). Fig. 2 (c) show the distribution of one of the interpacket delays, this results are representative of the data for the other PMUs. Results in Fig. 2 (c) show a distribution highly concentrated on the anticipated mean of $16.66\overline{6}$ms with a tail that do not monotonically decrease but has small clusters around 10, 14, 19 and 24 ms which are due to the cyclical behavior in Figs. 2 (a)-(b).

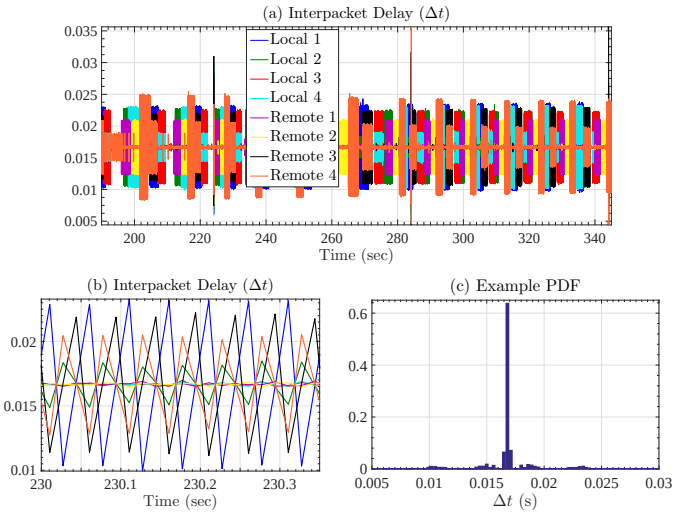

Fig. 2. Interpacket delay (Δt), from network analyzer data capture.

2) Data captured from the controller: This section presents results on how the interpacket delays are interpreted by the damping controller. The controller has a communication interface that is listening continuously for PMU data packets and storing them in a queue of data. In addition, the prototype has a control loop with an update rate 60 sps, this implies a window of time of $16.66\overline{6}$. As shown in Fig. 3, during this time interval the controller: pulls packets off of a queue of data from the 8 PMUs, time-aligns them (in pairs) according to their GPS time stamps, construct the power command action for all the 16 parallel controller instances, selects the most appropriate power command, performs all the supervisory checks [6], and prepares the data for saving it in an appropriate format for future retrieval.

Because the first action in the processing activity of the controller is fetching for data packets it is understood that if data packets arrive at the very end of one cycle they will be immediately used (at the beginning of the next cycle). However if the packets arrive after this fetching occurs they are stored in the queue and retrieved in the next cycle. If somehow more than one packet arrives during a time window, in the next iteration the controller uses all data packets (by flushing the queue) but stores only the latest one. If there are no packets in the queue (case where the interpacket delay is greater than 16.6ms) the controller repeats the previous data packet and stores this repetition.

As such the interpacket delays (of time of arrivals) as interpreted for the controller action are different than the actual interpacket delay. When the time between data packets is larger than a controller cycle (which is over $16.66\overline{6}$), the controller will repeat the previous data which implies a interpacket delay of zero. And because only the most recent data packet is stored when two data packets arrive within a 16.6ms window this implies a large time jump in the stored data. This oscillatory behavior transforms from typical values of 24, 16, and 10 ms to values of 0, 34 and 16 ms.

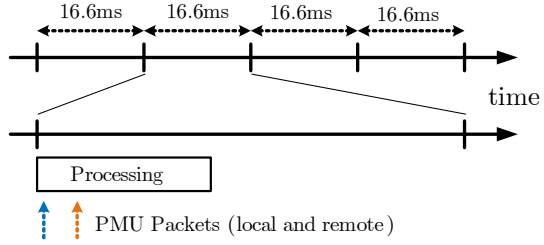

Fig. 3. Controller processing action time window.

Figs. 4 (a), (b) show the interpacket delays (of time of arrivals) (Δt_{TOA}) in the controller, where the cyclical nature of the data packets in which four of them are sent in 50ms as explained in Section IV-A1 is maintained. Fig. 4 (b) shows the interpacket delay of time of arrivals of all the 8 PMUs used in the PDCI damping controller for a period of 400 ms. During this time interval the Local 1 PMU stops sending packets for two controller loops (or more than $33.33\overline{3}$ ms) and that is reflected in the flat (dark) blue line between 1919.95 and 1920 in Fig. 4 (b). After this "mute" period this PMU catches up and this is presented as the 35 ms blue spike around the 1920 s. During the time period of interest the PMUs corresponding to: Local 2, Local 3, Remote 1, Remote 2, Remote 3, and Remote 4 all have the same behavior which is a "mute" time (reflected as 0 ms delay) of only one sample followed by a spikes of different magnitudes in the interpacket delay (but all less than 50 ms). During this same time interval the PMU correponding to Local 4 is sending packets in an erratic fashion. This is reflected by an "oscillatory" shape in the interpacket delay between 0 ms and $\sim$ 27 ms as shown in Figs. 4 (b). Fig. 4 (c) shows respectively the distribution of interpacket delays of time of arrivals for one of the PMUs which is representative of the data for the all the other PMUs. This result show the interpacket delay clustered around 16.666 and with a similar tail to those in Fig. 2 (c) only showing a higher concentration around 0 and 16.666. The maximum value of Δt_{TOA} for all the PMUs was recorded at around 45 ms with the minimum found at 0 (the moment the values are repeated).

Fig. 5 shows the interpacket delays of timestamps for the

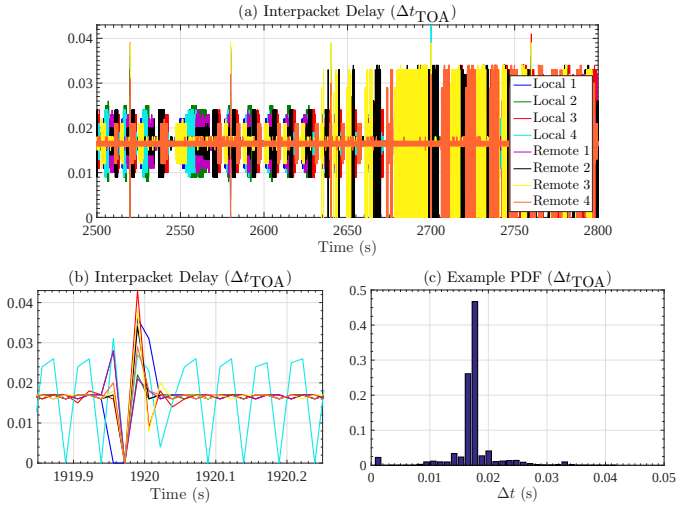

Fig. 4. Interpacket delays (Δt_{TOA}) of the system as captured by the controller.

same case as Fig. 4. In this case because the PMU time stamps are quantized with a step of 16.666 the only values allowed are multiple of this time step (0, 16.666, 33.333, 50.0). In this case after a repetition of a data packet a jump of 33 ms will follow and after a "mute" period of two interpacket latencies a jump of 50 ms will follow. The distributions in Figs. 5 show this fact by having small values at 0 and at 33 ms [2].

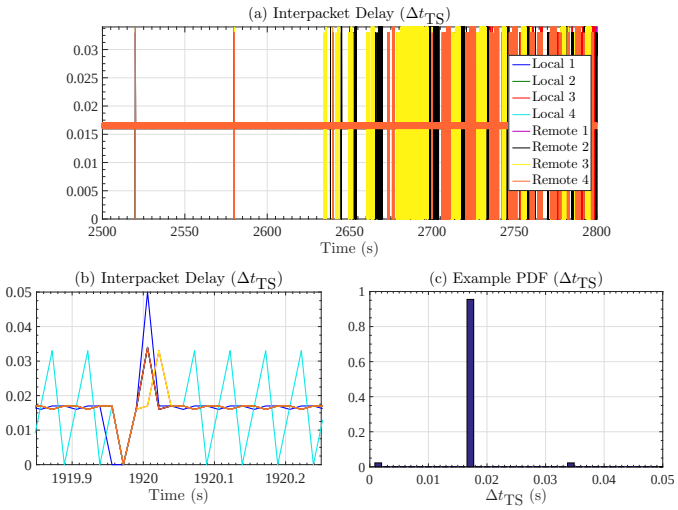

Fig. 5. Interpacket delays of time stamps (Δt_{TS}) of the system.

B. Signal Delay

The PMU used in this project need 6 sample measurements to determine an accurate phasor measurement. Because the sampling rate is 60 Hz the oldest measurement has 100 ms of delay with respect to the most recent one. Measurements taken at different times, and hence with different delays, are then involved in the construction of the phasor data packet. Even though measurements obtained at different times are used, the constructed data packet is time stamped at the middle of those 6 measurements and has at least 50 ms of delay before being sent out through the network. This time between the time stamp of the data packet and the moment the packet leaves the PMU device is named measurement delay and is not measured in this application. The communications delay is the time the data packet takes to travel the network from a PMU device to the controller. The sum of both the measurement delay and communications delay t_{del} is named the signal delay.

The damping controller is continuously listening for PMU packets in the network. As soon as a packet arrives at the controller a time stamp, named the time of arrival (TOA) is added to its phasor information. The difference between the time stamp of a data packet and the time stamp at the time of arrival given by the damping controller is t_{del}.

Figs. 6 (a), (b) shows measurements from real data of the signal delay for the damping controller system. They show that t_{del} is concentrated between 55 and 65 ms with peaks reaching the high 80 ms when there is config frame at the top of every minute. Fig. 6 (c) shows the distribution for the signal delay. The maximum value of signal delay recorded was ~ 88 ms, the minimum ~ 55 ms, with an average of around ~ 60 ms.

[2]there are some values at 50 but they are not visible at this scale

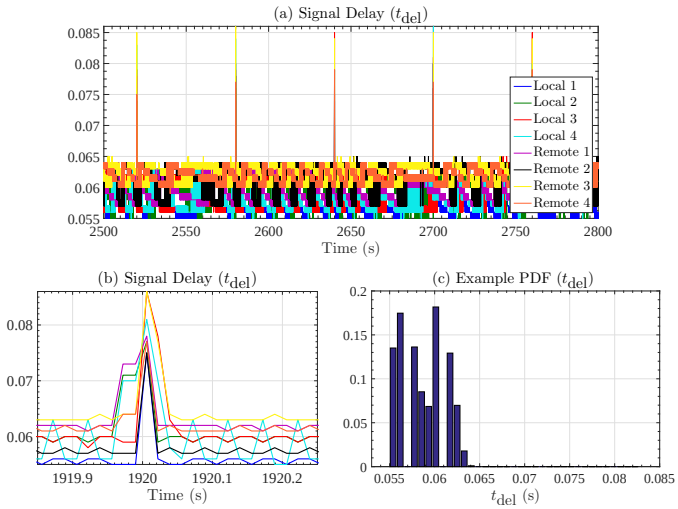

Fig. 6. Signal delay (t_{del}) in the damping controller system.

C. Controller Delay

The time taken from the time a data packet arrives at the controller to the time it emits a command action to the PDCI based on that data is named controller delay (t_{cont}). Both the controller update rate and the PMU packet emission rate are 60 sps, however these two rates are not synchronized with each other. The PMU packet emission rate is determined by a GPS clock while the controller update rate is determined by a very precise internal clock (which can be adjusted according to design specifications). But because the clocks are not the same they are drifting with one another. This means that data packets do not arrive at a constant time within the controller time window depicted in Fig. 3. There is a slight drift in the arrival of data packets with respect to the controller update rate. This difference in rates is translated in the controller delay as the periodic behavior shown in Fig. 7 (a). Results in this figure show the controller update rate is slightly faster than the PMU packet rate. The cases data packets arrive at the edges of the controller time window (the beginning of one is right next to the end of another) mark the periodicity of the shape seen Fig. 7 (a). At these moments the stochasticity of the network makes that sometimes the packet is at the beginning of one time window and sometimes it has to wait until the next controller loop, this is named the "rough zone" and is observed in Fig. 7 (a) at around 3000 s. Fig. 7 (b) show the distribution of t_{cont} which has a bimodal behavior with peaks at around 8 and 15 ms. This characteristic is product of the periodic behavior caused by the drift and its modeling is beyond the scope of this paper and matter of future research.

The periodicity of controller delay is around 14 mins. Note that within that period, the controller performs one more update cycle than the PMUs send data. Assuming a perfect PMU rate of 60 hz, the frequency of the controller loop is estimated at 60.0007507 Hz.

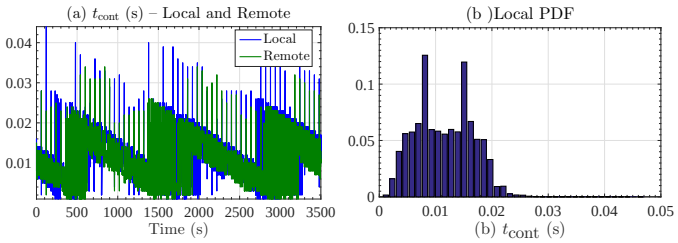

Fig. 7. Controller delay (t_{cont}) in the damping controller.

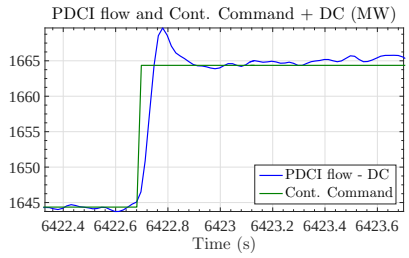

Fig. 9. Command send to the PDCI and its response.

D. Total Controller Delay

The time taken from a network measurement to a command signal sent to the PDCI is named as total delay (t_{tot}). Fig. 8 (a) shows t_{tot} for the system. The periodic behavior in these results stems for the reasons described in Section IV-C. The recurrent spikes in Fig. 8 (a) are due to config frames at the top of every minute. It should be noted that thanks to time alignment t_{tot} is the same for both local and remote PMUs. Fig. 8 (b) show the distribution of t_{tot} which also presents a bimodal shape because of the periodicity of the signal. The maximum, minimum and average total delay are estimated at ~ 102 ms, ~ 58 ms and ~ 71 ms respectively.

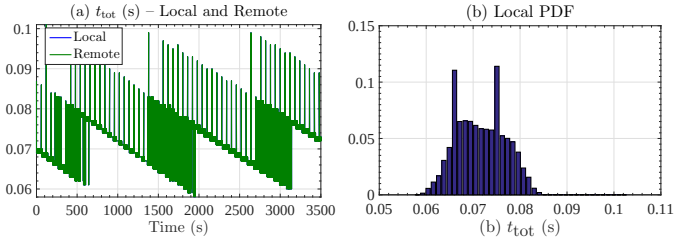

Fig. 8. Local and remote total controller delay in the system.

E. Command Delay and Effective Delay

The time elapsed from the moment the controller sends a command signal to the moment the PDCI responds to it is named the command delay (t_{cmd}). The delay was estimated from data obtained during open loop testing where the damping controller sent probing signals to the PDCI. In these tests the damping controller recorded the probing signal commanded to the PDCI as well as the estimated PDCI flow. These two signals were time stamped using GPS clock and were sampled at a rate of 60 Hz. By overlapping the signal sent with the PDCI response t_{cmd} can be then estimated. Fig 9 shows the overlap of a step probing signal and the PDCI response which is almost immediate. The estimation of the command delay is then somewhere in between 0 and $16.66\overline{6}$ ms but the sampling of the time does not allow for a perfect characterization. Frequency response methods estimated this delay to be around 11 ms [8]. The effective delay which is the addition of the total controller delay and the command delay is then estimated to have an average of 82 ms.

V. Conclusions and Future Work

This paper defines and describe all the time delays associated with the PDCI damping controller; a wide area control system that uses real-time PMU feedback. The delays are defined from the moment the PMU takes a measurement to the moment that information causes a response from the PDCI. The *total delay* which is defined from the moment a measurement is taken to the moment the controller sends a power command is around 71 ms on average; more than half of this value, 50 ms, coming from the PMU itself. The time it takes for the PDCI to react to the command signal, named *command delay*, is estimated at 11 ms. The overall *effective delay*, which is sum of the *total delay* plus the *command delay*, of the PDCI damping controller is on average 81 ms with the worst case value recorded at 113 ms.

Future work will include detailed statistical analysis in the data for each individual delay and finding corresponding models for them. Additionally making use of this information to enhance the performance of the controller is also part of the path to come.

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