Charge-Induced Damage on SOI Wafers: A Case Study

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Abstract

This work outlines a case study of charge-induced damage to SOI wafers that caused gate leakage in discrete transistors and static leakage in packaged integrated circuits (ICs). The consequential yield fallout occurred primarily at wafer center. Electrical, optical and laser-based failure analysis techniques were used to characterize the damage and determine root cause of electrical failure. The failure mechanism was localized to a rinse step during chemical mechanical planarization. Further this type of charge-induced damage to ICs on the SOI wafers was captured in trends in current-voltage sweeps and spatial patterns by thermally-induced voltage alteration (TIVA) mapping. This led to quick identification of another source of charge-induced damage that affected yield post-fab.

Case Study

The electrical failure described in this work first manifested as transistor gate leakage evident only in the center of the wafer. The structures would consistently fail at this parametric test site over multiple lots. Die yield did not indicate spatial yield loss at wafer probe, but began to indicate failures once the center dice were packaged. Both wafer-level discrete transistors and packaged ICs were delivered for failure analysis. Transistors which typically measured less than nAs of current measured greater than 1mA at 3.3V. Figure 1 shows current-voltage (I-V) sweeps typical of good and bad sites. For packaged parts, values were dependent on the type of packaged IC but all exhibited leakage-type failures.

A significant number of packaged failures originating from die that surround the center of wafer were examined. Although optically they indicated no obvious visible damage, a trend emerged in the electrical behavior of the I-V sweep. Figure 2 shows a sampling of a few of the packaged parts. The shape of the curve was very consistent for this type of failure. When compared to other leakage-type failures from the same IC-type, running IV sweeps became an easy screening method to filter out this failure mechanism prior to more destructive analysis of packaged parts (e.g. jet-etch).

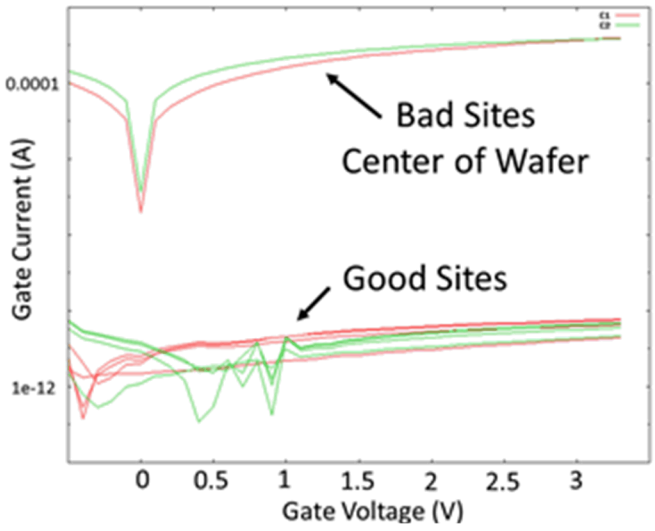

Figure 1: Comparison of level of gate current on both good and bad discrete transistors. Both bad sites shown are located at the wafer center.

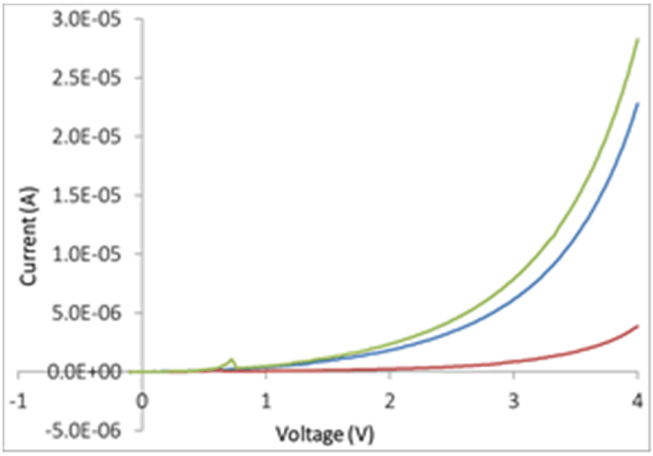

Figure 2: Characteristic I-V shape of packaged ICs that failed due to charge-induced damage

Optical inspection was also carried out on the discrete transistors where damage was observed in some structures. An example is shown in Figure 3. Although the visible damage occurred within the transistor wiring, focused ion beam (FIB) cross-sectional analysis found macroscopic damage also in the transistor itself. At the optical damage site, catastrophic melting of the metal line and cracking was observed but nothing indicating cause of failure. Within the transistor, however, a silicon filament electrically shorting the island through the buried oxide layer to the Si substrate was observed. For this work, this type of defect is referred to as a Box defect and an example is shown in Figure 4.

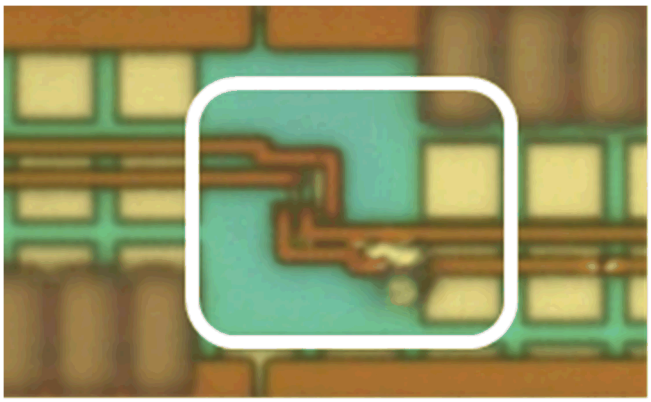

Figure 3: Optical image of cracking and melting around one of the wires leading to the discrete transistor

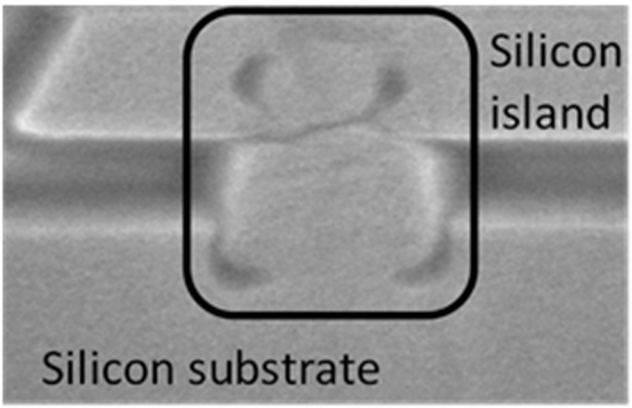

Figure 4: FIB / scanning electron microscopy (SEM) image showing a Si filament extending from the island to the silicon substrate

Although it was not yet determined whether the Box defect was causal or symptomatic of catastrophic charge-induced damage, it was necessary to determine spatial extent of damage. Individual FIB cross-sections were time consuming and only provide information on a small area of the wafer. It was understood that the center dice were not yielding and the center test structures were failing, but the step size of the die and the test structures were such that that affected area could not be accurately determined. To better understand scope of the affected area, the Si substrate was lapped and chemically etched (XeF_2) away. Optical analysis could then be performed from the backside over a large area of a wafer. The Box defects provided a Si pathway through the Box layer such that the chemical etch attacked the islands where Box defects were present. Subsequently the images shown in Figure 5 are not the Box defects themselves but rather chemically-highlighted islands where the Box defects once were. The large-scale affected zone of the wafer could be mapped out in this way.

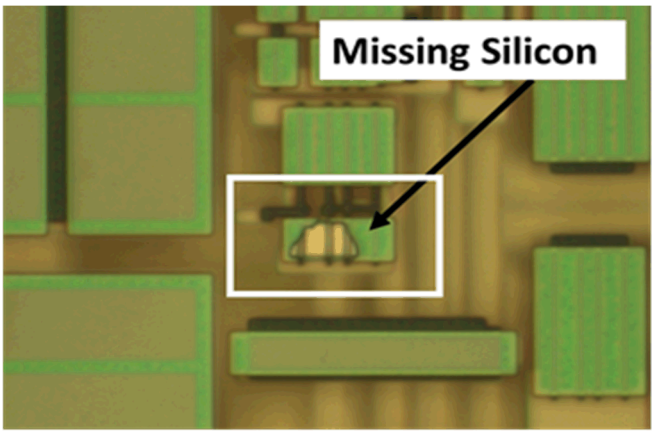

Figure 5: Optical image through the backside of the wafer with the substrate silicon chemically removed. The missing silicon within the island indicates that this structure had a Box defect that provided a physical pathway through which the XeF_2 penetrated the Box layer and attacked the island silicon.

This process was applied to both the wafers to understand affected area as well as the packaged parts to understand whether the Box defects themselves proved to be the cause of the electrical leakage. However, in the packaged parts, the Box defects showed up primarily in no connect circuitry, dummies and in areas that wouldn't necessarily lead to leakage of the device. They were not present in the array of the device. It was determined that the Box defects were symptomatic of this type of failure mechanism but not causal.

Packaged parts were also examined extensively with thermally-induced voltage alteration (TIVA) to pinpoint cause of leakage. Multiple dark diffuse defect signals were apparent in the TIVA images. Figure 6 shows an optical image of the IC and four stitched images that make up the TIVA mapping of the part. Under high magnification, the TIVA signals maintained a soft, diffuse edge, not necessarily indicating a particular transistor or similar structure. The signals also had a directionality to them. In Figure 6, white dashed guide lines indicate the directionality of the signals. This direction was consistent for the die location. Figure 7 shows how the direction of the defect signals changes with die location. The die shown in Figure 6 was positioned in the bottom right corner of the graphic. This type of TIVA signal, both in pattern and direction, proved to be very characteristic of IC charge-induced damage on the SOI wafers.

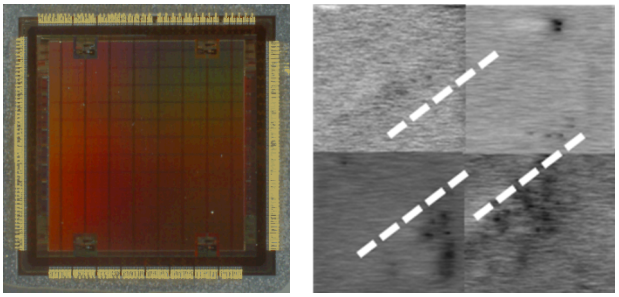

Figure 6: Characteristic TIVA map (1340nm) of packaged IC indicating a dark, diffuse, directional pattern to the TIVA signals.

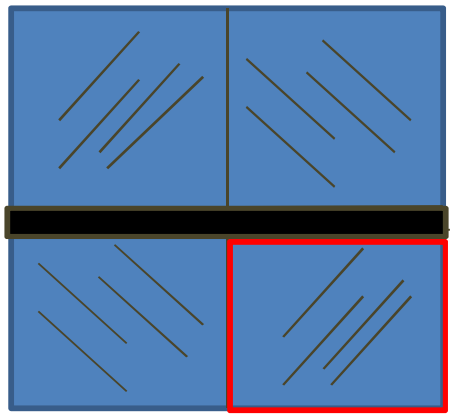

Figure 7: Schematic showing the direction of the dark, diffuse TIVA signals with respect to die location around the center of the wafer. The die shown in Fig. 6 is indicated by the red box.

More than one FIB cross section of the diffuse dark TIVA signals did not reveal any macroscopic physical defects at any of the sites. It is suspected that gate oxide failures were the cause of the signals. Gate oxide failures are not easily imaged with FIB/SEM resolution.

Conclusions

Through iterative empirical analysis and failure analysis support, the cause of the leakage in both test structures and packaged parts was found to be charge-induced damage from a high-velocity DI water spray within the chemical mechanical planarization tool. During this step, the spray is positioned at the wafer center during a high-speed rotational rinse. The charge-induced damage to the wafer manifested itself as breakdown behaviors (Box defects and gate oxide failure) between the high potential surface of the wafer and the grounded backside. Subsequently we believe with catastrophic breakdown damage to the Box layer there was also large-scale gate oxide breakdown characterized by the dark defect signals in the TIVA maps. Although the strict role the Box defects play in the ultimate leakage is not yet fully understood, they provided a symptomatic physical defect by which charge-induced damage could be identified for structures on the SOI wafers. Further, this work categorized the TIVA pattern and IV shape characteristic of this type of charge-induced damage. Thus when another submitted failure indicated these trends, we were able to quickly identify a post-fab process which delivered similar charge-induced damage and was significantly affecting package yield.

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