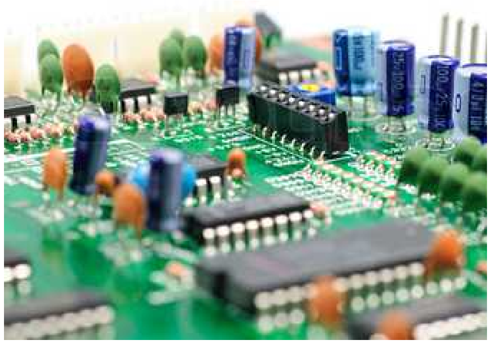
SAND2017-4433PE

SAND2017-



CHARON

Xyce™
PARALLEL ELECTRONIC SIMULATOR

Charon and Xyce Update

Overview at HEART for JPL

Larry Musson & Joe Castro

U.S. DEPARTMENT OF ENERGY

NNSA National Nuclear Security Administration

Sandia National Laboratories is a multi-mission laboratory managed and operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Corporation, for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000. SAND NO. 2011-XXXXP

Outline

- Charon
  - Staffing
  - Governing Equations
  - Modeling Capability
  - Simulation Capability
    - QASPR
    - Calibration, Validation, UQ
  - Capability Progression
  - Availability

- Xyce
  - Staffing
  - Modeling Capability & Challenges
  - Simulation Flow
  - Model Translation
  - Availability

Staffing

- Personnel
  - 1355
    - Larry Musson
    - Gary Hennigan
    - Suzey Gao
    - Mihai Negoita
    - Andy Huang
    - Joe Castro
  - 1344 & 1356
    - Dolores Black
    - Ian Wilcox
  - 1400
    - Jason Gates
    - Kara Peterson

- 1355 – code developers (except the fellow in red)
- 1344 & 1356 – analysts
- 1400 – code development support for next gen

What is Charon?

- Semiconductor *TCAD* code with support for modeling displacement damage due to neutron radiation as well as effects from other sources of radiation (e.g. ionization)
- Finite-volume and finite-element discretizations of governing PDEs
  - Drift-Diffusion
  - Drift-Diffusion + Energy (Lattice Heating)

Electric Potential

$$\begin{cases} \nabla \cdot \left(\epsilon \vec{\mathbf{E}}\right) = q\,(p - n + C) \\ \vec{\mathbf{E}} = -\nabla V \end{cases}$$

Constitutive Relations

$$\vec{\mathbf{J}}_n = q\left(n\mu_n \vec{\mathbf{E}} + D_n \nabla n\right)$$
$$\vec{\mathbf{J}}_p = q\left(p\mu_p \vec{\mathbf{E}} - D_p \nabla p\right)$$

Conservation

$$\nabla \cdot \vec{\mathbf{J}}_n - qR = q\frac{\partial n}{\partial t}$$
$$-\nabla \cdot \vec{\mathbf{J}}_p - qR = q\frac{\partial p}{\partial t}$$

Lattice Heating

$$\nabla \cdot (\kappa \nabla T_L) + H = \rho c \frac{\partial T_L}{\partial T}$$

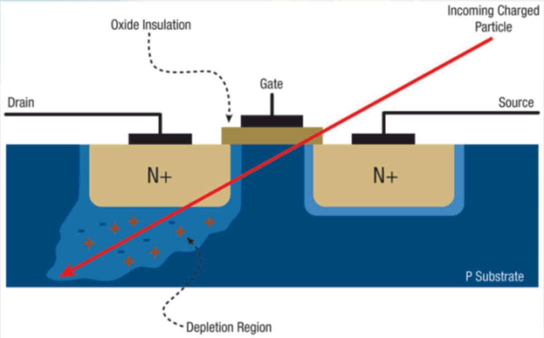
NNSA ASC Sandia National Laboratories

Environments & Device Modeling Capability

- Environments
  - Normal
  - Dose Rate – reactor environments
  - *SEE* –REHEDs FY17 LDRD
  - Total Dose – possibly in the future
- Devices
  - Diodes
  - BJT (Si)
  - HBT (III-V)
  - FETs
  - Memristor
  - Ultra-Wide Band Gap Diodes (new models)

Ongoing/Future Charon Development

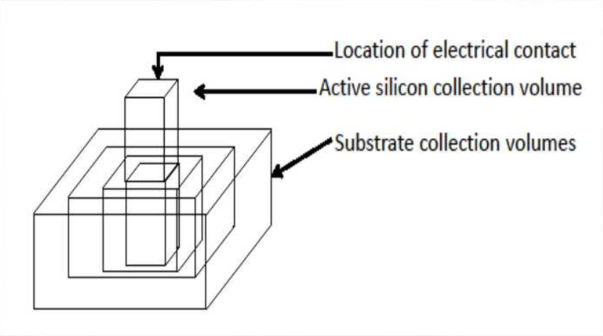
- Expanding Physics Capability
  - SEE/SEU
    - Collaboration with Vanderbilt - Monte Carlo Radiative Energy Deposition (MRED)
    - MRED training @Vanderbilt in April
    - Supporting a Vanderbilt student
  - Si HVD Analysis
  - GaN development
    - High Voltage Diodes
    - HEMTs
  - Frequency Domain Modeling (HB)
  - Improved coupled electrical & thermal
  - Dose Rate model development will begin this FY
- Next Generation Development
  - In preparation of next gen computational hardware



Single-Event Effects

SEE High Altitude View

- **We anticipate a union of tools & activities to satisfy the goals of what we intend in the LDRD**
- **Charon**
  - Device physics
    - Drift-Diffusion Model
    - Finite Element / Finite Volume
    - Recombination / Charge generation
  - *How to inform secondary effects due to parasitic bipolar enhancement



- **Monte-Carlo Radiative Energy Deposition (MRED)**
  - Particle physics (Geant 4)
  - Nested Sensitive Volumes
    - Provides approximation for device physics at reduced cost
  - *How are nested sensitive volumes defined for silicon-on-insulator (SOI) devices
- **Xyce**
  - Circuit simulation
    - Charon/ MRED SEE informed netlists
  - *Explain current anomalies in existing CMOS7 data
- **Experiments**
  - Design of experiments
  - *Validation data for research and publication

*Overall integrated, validated workflow from TCAD to IC evaluation

*Research Aspects

Progression of Charon Capabilities

III-V Work

Normal Environment GaN HVD

Single Event Effect Modeling

Normal Environment PnP HBT

Cluster Damage Model for Si

2D Modeling of HBTs

Cluster Damage Model for GaAs in HBTs

Empirical Damage Model for HBTs

Normal Environment Npn HBT

FET models with multi-region support

Time

QASPR Circuit Prototype
(Silicon BJTs, Mixed-mode)

QASPR Device Prototype
(Silicon NPN BJTs)

PN Diodes

Research Code (CSRF & LDRD)

Silicon Work

Charon Has Been Approved for Open-Source Release!

- Official release of the code will occur later in FY17
  - Need to refine user documentation
  - Have not yet decided on type of open-source license
  - Will not include the cluster damage model
- Internal version of Charon is categorized as an ITAR/Export Control Simulator
  - We have a Government Use Notice (GUN) in place with AWE
  - GUN provides a U.S. government agency or contractor access to software limited to government use

Xyce Staffing

Xyce team

xyce.sandia.gov

- Jason Verley (PI)
- Eric Keiter (Research Lead)
- Tom Russo
- Heidi Thornquist
- Rich Schiek
- Ting Mei
- Aadithya Karthik
- Sivasankaran Rajamanickam

Trilinos team

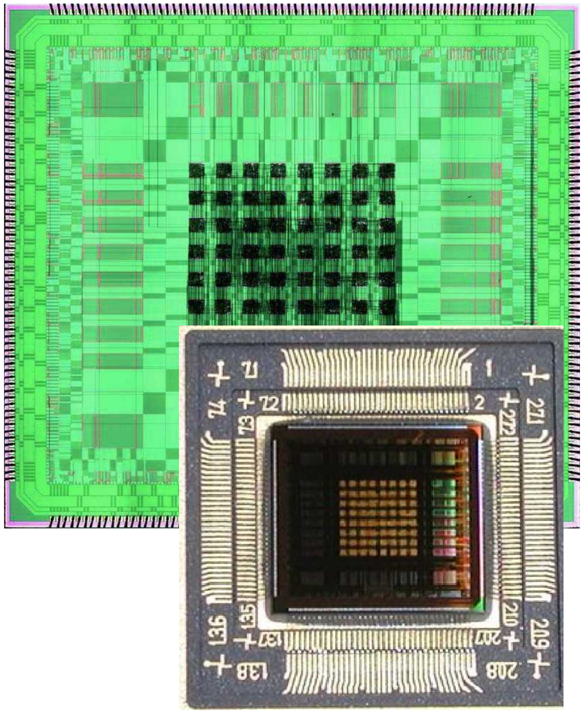
trilinos.sandia.gov

Dakota team

dakota.sandia.gov

Xyce Parallel Circuit Simulator

- Xyce: Massively Parallel circuit simulator:
  - Distributed Memory Parallel (MPI-based)
  - Unique solver algorithms
  - SPICE "Compatible"
  - Industry standard models (BSIM, PSP, EKV, VBIC, etc)
  - ADMS model compiler
- Analysis types
  - DC, TRAN, AC
  - Harmonic Balance (HB)
  - Multi-time PDE (MPDE)
  - Model order reduction (MOR)
  - Direct and Adjoint sensitivity analysis
- Sandia-specific models
  - Prompt Photocurrent
  - Prompt Neutron
  - Thermal
- Other, non-traditional models
  - Neuron/synapse
  - Reaction network
  - TCAD (PDE-based)
- Xyce Release 6.7 pending
  - Open Source!
  - GPL v3 license



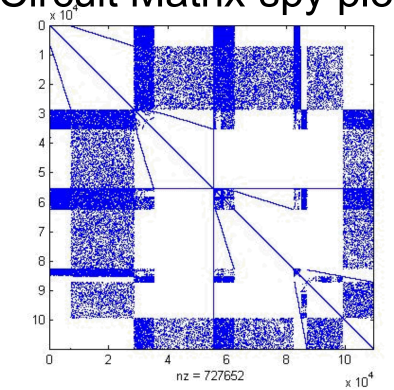
http://xyce.sandia.gov

Open Source Releases (starting in 2013):
Versions 6.0, 6.1, 6.2, 6.3, 6.4, 6.5, 6.6
>1000 unique external downloads since 6.0.
Next release (v6.7) ~May 2017

What Xyce Is, and Is Not

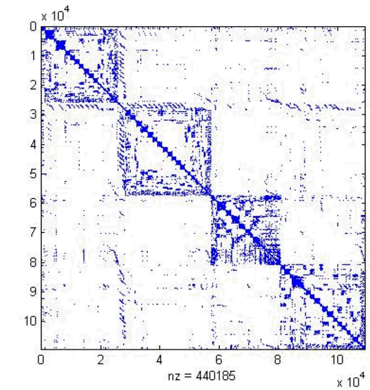
- **Xyce is: "True Spice"**
  - Large, monolithic, single Jacobian matrix.
  - Accurate.
  - Known parallel linear solvers don't scale perfectly.

Circuit Matrix spy plot



- **Xyce is not (currently): "Fast Spice"**
  - Loosely coupled separate blocks
    - Implicit solver methods within blocks
    - Explicit methods used to couple blocks
  - Table models
  - Model order reduction
  - Exploits circuit hierarchy
  - Effective primarily for digital circuits
  - less accurate than "true spice"

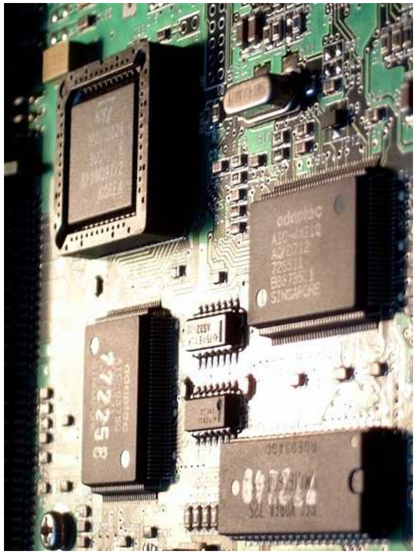
BTF+Hypergraph



4 processors

"True Spice" Xyce Circuit Simulation Challenges

- Need to efficiently and seamlessly simulate circuits that have a wide range of devices ($10\text{-}10^6$) and complexity
  - Advanced preconditioning techniques for iterative solvers
  - Must support direct solvers for smaller circuits
- Internal Customer simulation efforts inspired many of the past and current advancements for circuit simulation

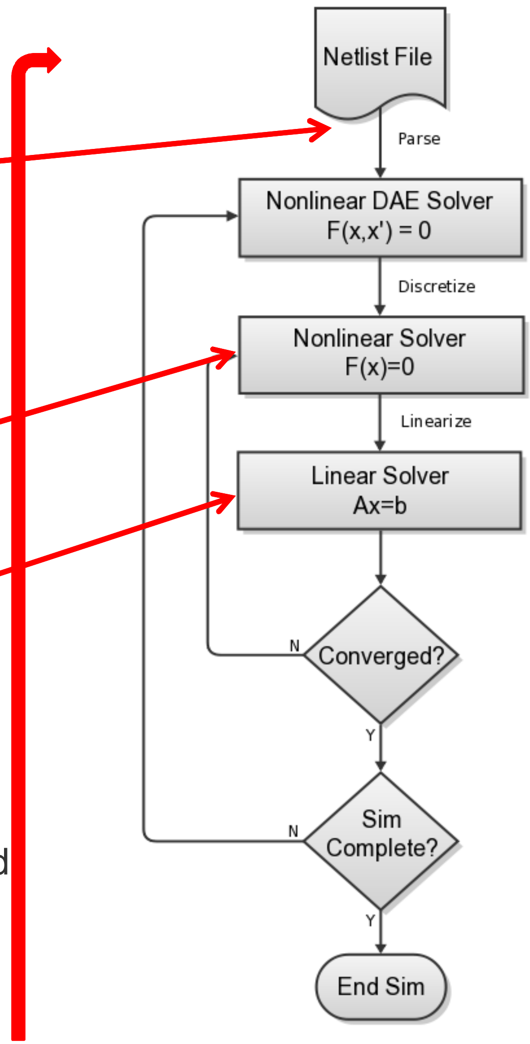


Circuit 1 (2000) → Circuit 2 (2003) → Circuit 3 (2006) → Circuit 4 (2008) → Circuit 5 (2011)

~25K unknowns | ~600K unknowns* | ~680K unknowns | ~430K unknowns | ~2M unknowns

Xyce Simulation Flow

- Parsing
  - Convert netlist file syntax to equivalent devices and network/circuit connectivity
  - Distribute devices over multiple processors
  - Determine global ordering and communication
- Device Evaluation
  - Loop through all devices for state evaluation and matrix loading
- Linear Solve
  - Sparse linear algebra and solvers used to solve linearized system
- Advanced Analysis Methods
  - Sampling: Monte Carlo, LHS (DAKOTA)



Eric Keiter, Sandia National Laboratories
2017 DARPA IDEA Workshop, Arlington, VA

Xyce Model Support with ADMS

ADMS = *Automatic Device Model Synthesizer*

Verilog-A: industry standard format for new models:e.g. VBIC, Mextram, EKV, HiCUM, etc

ADMS translates Verilog-A to Xyce-compliant C/C++ code;

API automatically handles data structures, matrices, tedious details.

itivities via Sacado automatic differentiation

nd to include Stocahstic Expansions via Stokhos.

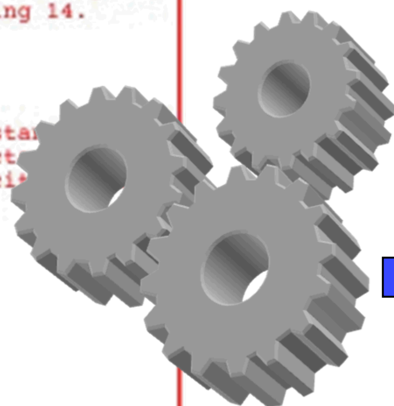
```
// Series RLC
// Version 1a, 1 June 04
// Ken Kundert
//
// Downloaded from The Designer's Guide Community
// (www.designers-guide.org).
// Taken from "The Designer's Guide to Verilog-AMS"
// by Kundert & Zinke. Chapter 3, Listing 14.

`include "disciplines.vams"

module series_rlc2 (p, n);
    parameter real r=1000;     // resista
    parameter real l=1e-9;     // induct
    parameter real c=1e-6;     // capaci
    inout p, n;
    electrical p, n, i;
    branch (p, i) rl, (i, n) cap;

    analog begin
        V(rl) <+ r*I(rl);
        V(rl) <+ ddt(l*I(rl));
        I(cap) <+ ddt(c*V(cap));
    end
endmodule
```

Verilog-A



Run admsXyce

```
// -- code converted from analog/code block// I(
((V(p,internal1)/R))staticContributions[admsNodeI
((probeVars[admsProbeID_V_p_internal1])/instanceP
deID_internal1] -=
((probeVars[admsProbeID_V_p_internal1])/instanceP
((probeVars[admsProbeID_V_internal1_internal2])*i
I(internal1,internal2) <+
((C*(CapacitorCharge))dynamicContributions[admsNo
(CapacitorCharge);dynamicContributions[admsNodeID
(CapacitorCharge);InductorCurrent = (probeVars[ad
V(internal2,n) <+
((L*ddt(InductorCurrent)))dynamicContributions[ad
(instancePar_L*(InductorCurrent));
```

C++ code snippet

(actual Xyce file is 1500 lines)

ADMS-Xyce

Development Status and Plans

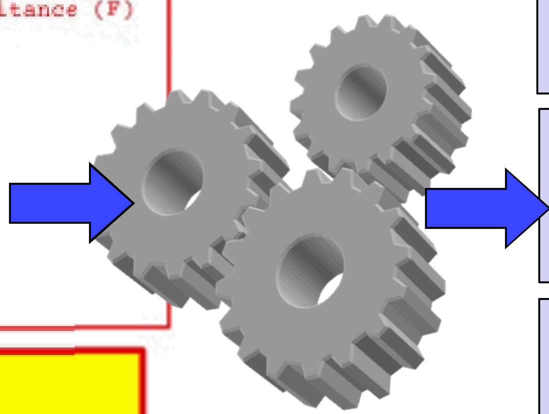
```
// Series RLC
// Version 1a, 1 June 04
// Ken Kundert
//
// Downloaded from The Designer's Guide Community
// (www.designers-guide.org).
// Taken from "The Designer's Guide to Verilog-AMS"
// by Kundert & Zinke. Chapter 3, Listing 14.

`include "disciplines.vams"

module series_rlc2 (p, n);
    parameter real r=1000;      // resistance (Ohms)
    parameter real l=1e-9;      // inductance (H)
    parameter real c=1e-6;      // capacitance (F)
    inout p, n;
    electrical p, n, i;
    branch (p, i) rl, (i, n) cap;

    analog begin
    V(rl) <+ r*I(rl);
    V(rl) <+ ddt(l*I(rl));
    I(cap) <+ ddt(c*V(cap));
    end
endmodule
```

Verilog-A



NextGen (ATDM)
Kokkos

Embedded UQ
Stokhos
$$f(\theta) = \sum_{k=0}^{\infty} F_{pk}\Phi_k(\epsilon)$$

Planned

Dynamic Linking
`*.so` files

Param Sensitivities
Sacado
$$\frac{d\vec{f}(\vec{x})}{dp}, \frac{d\vec{q}(\vec{x})}{dp}$$

DAE support
***Sacado* (Jacobian)**
$$\frac{d}{dt}\vec{q}(\vec{x}(t)) + \vec{f}(\vec{x}(t), \vec{u}(t)) = \vec{0}$$

Implemented

Verilog-A (high level modeling language) Input

Run admsXyce

Ready-to-compile C++ code

Xyce Accessibility

Open Source

- First open source release, v6.0 (2013)
- GPL license v3.0
- Source and binary downloads available
- Foster external collaboration
- Feedback from wider community
- Taxpayer funded; encouraged to open src.

OUO Version

- Xyce has been licensed to gov. labs
- Requires Government-Use (GUN) License.
- This version of Xyce includes rad models

Training

- Training classes available on case-by-case basis.
- Training videos online at the website.

xyce.sandia.gov