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Center of Wafer Gate Leakage Resulting in Product Yield Loss: A Failure Analysis Perspective

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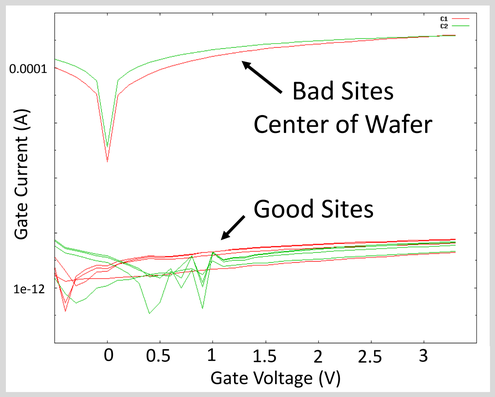
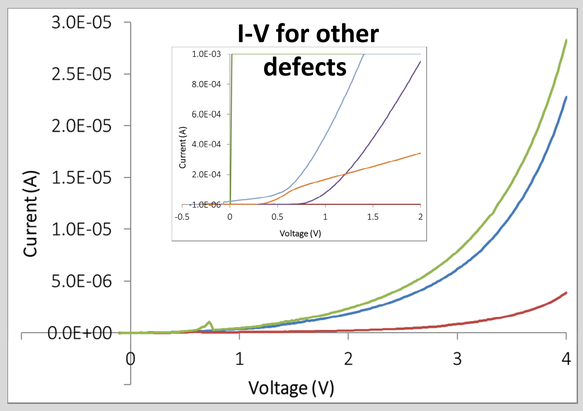
Research Problem

- Look for historic trending in data or in previous work
- Look for similar electrical signals in chronologically relevant lots
- Understand scope of problem: wafer and/or package-level
- Problem was limited to center of wafer evidenced by product lot spatial yield loss

Electrical Analysis

- Confirm failure type on both on wafer level and on packaged device



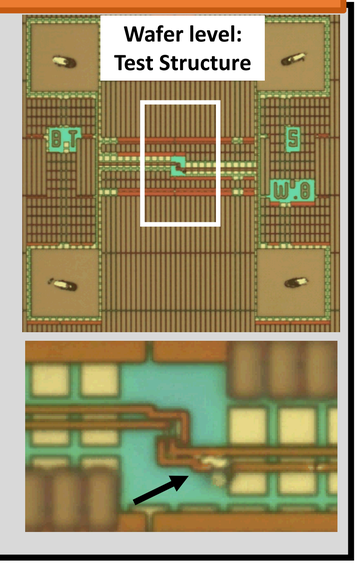


Wafer-level: Discrete Transistor
Data indicates high current at center site (~10^{-4} A at 3V) and at good die sites (~10^{-10} A at 3V).

Packaged Eiger Device
Determined characteristic shape of current-voltage sweep: Bad site (>10^{-6} A @ 3V). Good site (~10^{-7} A @ 3V).

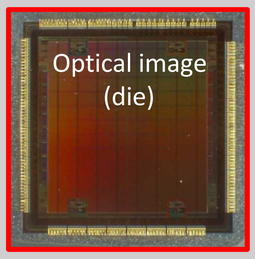
Optical inspection

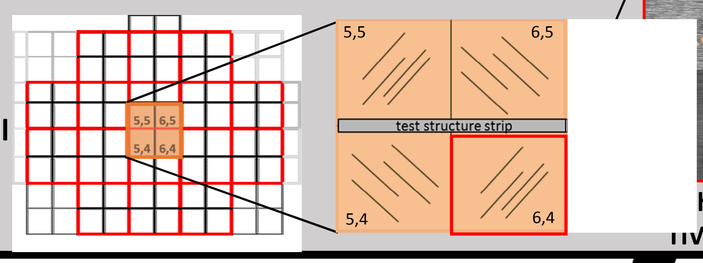
- Optical inspection of area of interest
- May require jet-etch to expose die on packaged parts
- Some but not all of the test structures indicated damage
- Packaged parts did not show visible evidence of damage

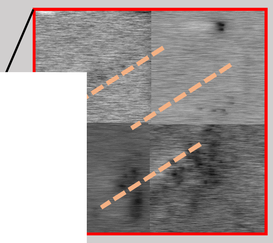


Laser-based Technique

- Laser technique used to localize failure sites (thermally-induced voltage alteration, TIVA)
- In packaged parts, we determined a characteristic pattern for this failure mode
  - Directional with respect to the center of the wafer
  - Diffuse dark signals



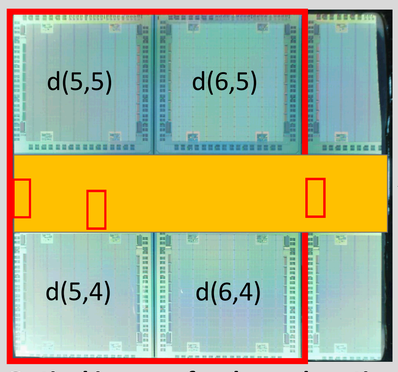




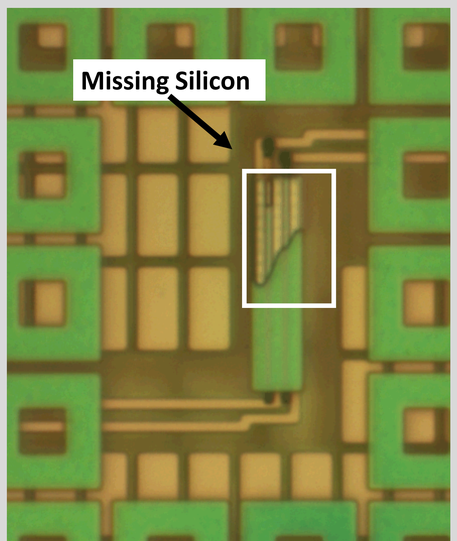
Backside Thinning and Analysis

- Determine large area density of box defects and extent of affected area

Method:
- Cleave and isolate area of interest
- Backside lap
- Chemical etch (XeF_2) to reveal defect
- Defect provides pathway through Box to etch island
- Process can be applied to both wafers and packaged parts after the die is removed from the package.



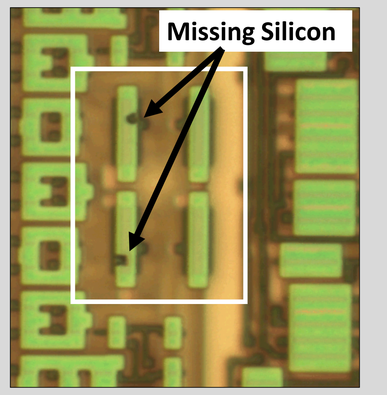
Optical image of a cleaved section from a wafer post thinning



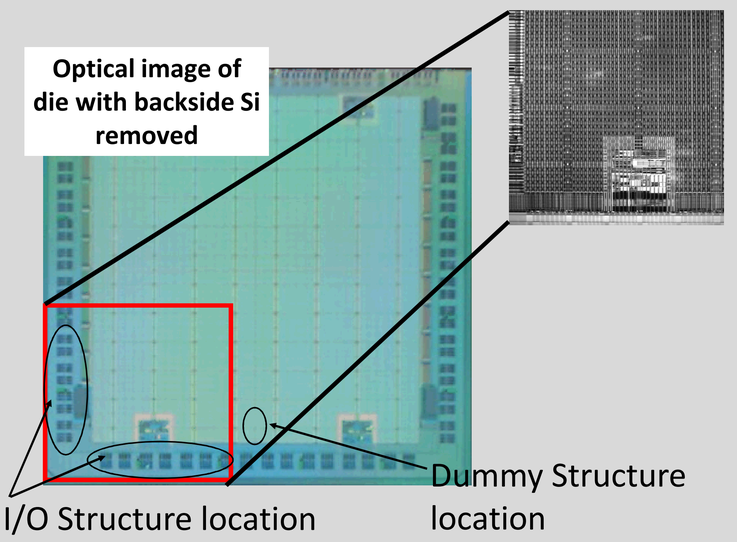
Backside optical image of a single transistor where part of the Si island has been etched away indicating the presence of a Box defect.

Box Defects were found in:
- Areas outside of the four center die
- Passing discrete transistors (confirm FIB results)
- Die I/O circuitry that does not influence device leakage
- Dummy structures

Box Defects were not found at the TIVA signal sites (confirmed FIB results) but were found in close by I/O structures and dummy structures.

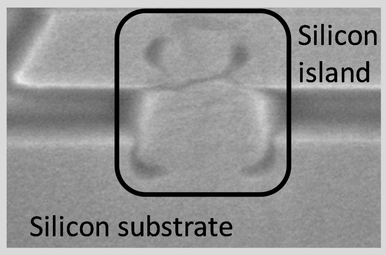


Optical image of Box defects found in dummy structures

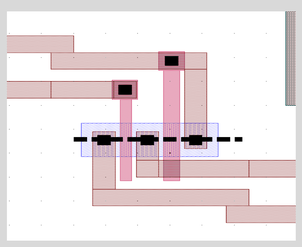


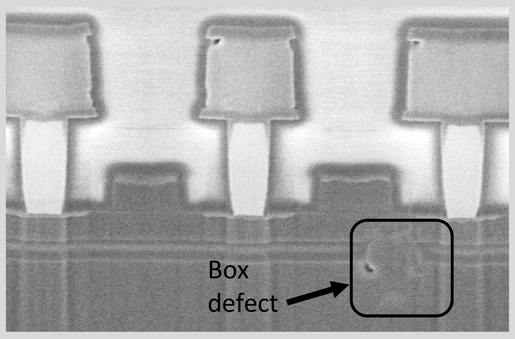
Cross-sectional Focused Ion Beam (FIB) / Scanning Electron Microscopy

- Ability to cross-section, image and provide chemical analysis at defect location
- Typically utilized after other localization FA techniques



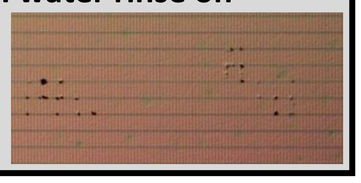
- At wafer level, the leaky transistors had leakage paths to the substrate (Box defects)
  - Transistors without gate leakage also exhibited Box defects
- At package level, we never found macroscopic physical defects





Conclusions/Further Work

- Helped identify CMP as the source of charge-induced damage
  - Determined scope of affected area (wafer real estate)
  - Characterized Box defects
  - Provided iterative and timely FA to support empirical fab experiments
- Generated a failure mode library both of TIVA imaging and I-V sweeps on packaged parts characteristic to charge-induced damage
- *This work enabled quick identification of a similar charge-induced damage issue in backend processing outside of the fab causing product yield loss*
- Similar charge-induced damage caused by atomized DI water rinse on topside of finished wafers



Optical image of 'tetris-like' defects observed on test structure dummies at the center of wafer

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