

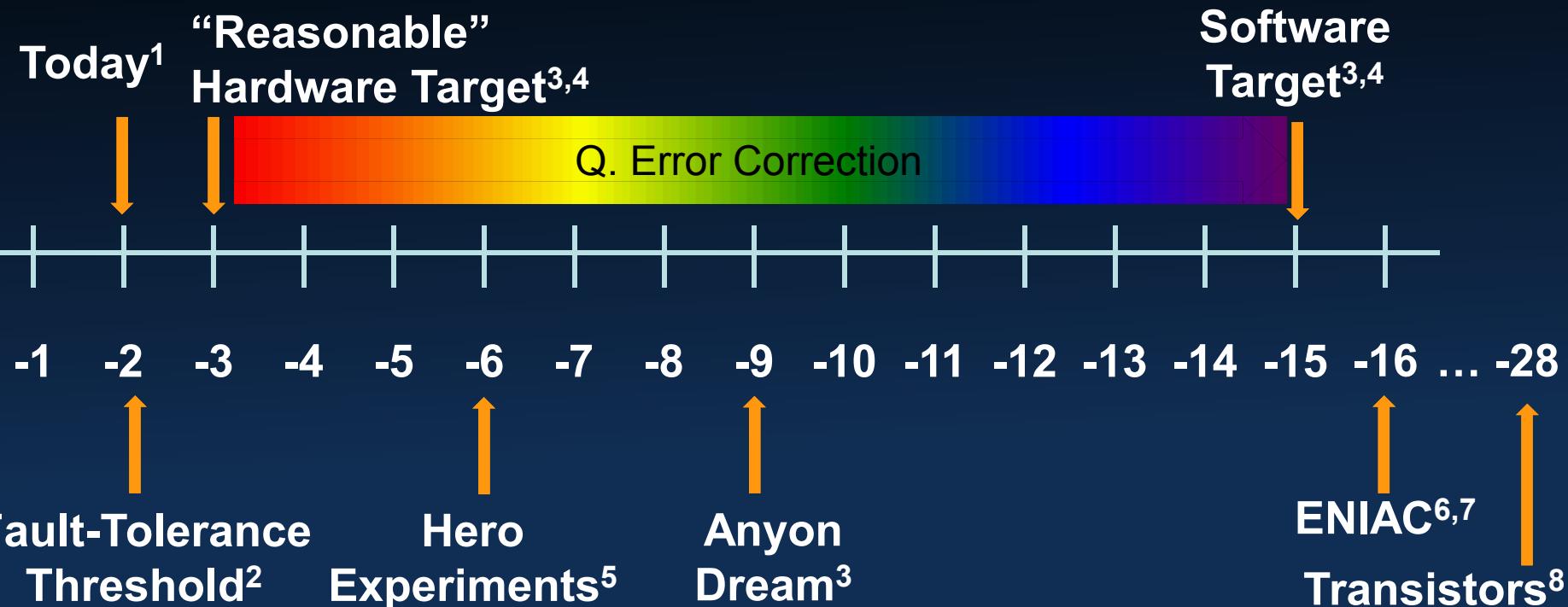
# Quantum Computing: Engineering Challenges and Underlying Technologies

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# #1 Challenge: Errors

*Chart: Quop error probabilities ( $\log_{10}$ )*



# Mantra

The logical qubit is the analogue of the electronic bit

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# Outline

**The first 10X: Hardware**

**The next  $10^{12}$ X: Architecture**

# The first 10X: Hardware

# Quantum Chips

*Each has its strengths & weaknesses*

Trapped atoms



Trapped ions



Silicon



Superconducting

UCSB

# Environmental Controls

## Cryogenic

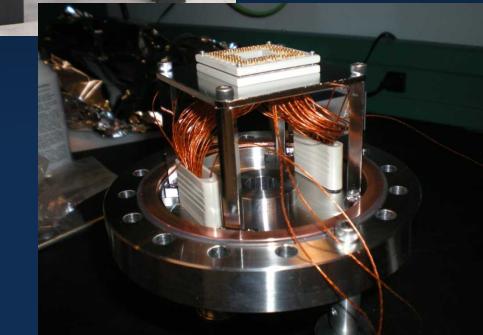
- Low-power, hi-speed signal feed-thrus
  - Analog *and* digital
- Low-power cryogenic amplifiers
- Increased cooling power (<< 4K)

## Vacuum

- UHV ( $10^{-11}$  torr) for atoms & ion qubits
- Vacuum feed-thrus (electrical and optical)
- Vacuum-compatible materials

## Electromagnetic

- Helmholtz coils
- Faraday cages
- Local low-frequency EM-field compensation
- High-powered magnets



# Devices & Signaling

## Material

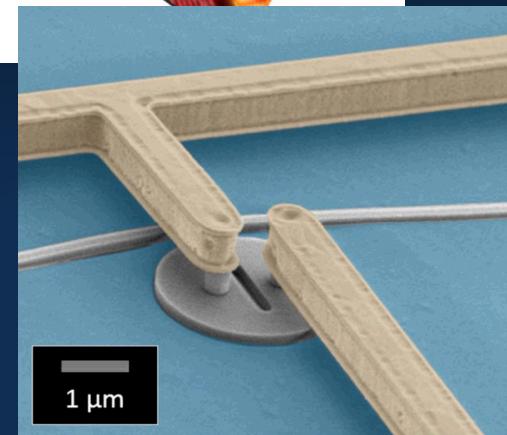
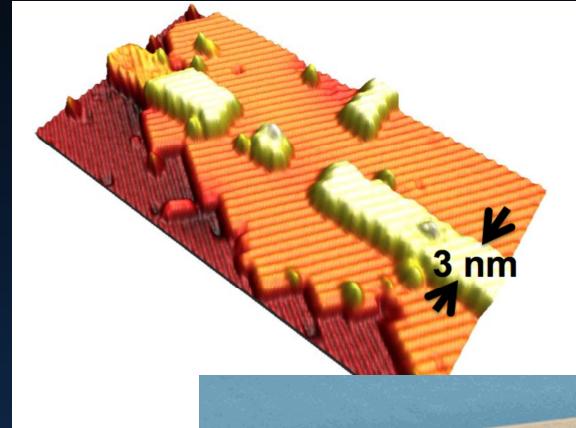
- “Quantum-grade” silicon, diamond
- Integrated nanostructures
- Engineered quantum behaviors

## Electronics

- Fast & precise low-power DACs
- Superconducting control electronics
- Error syndrome decoders

## Interconnects

- Unusually high-quality required:
  - Low power, low-loss, low-crosstalk
  - Wide-bandwidth, long-distance
  - Phase-locked, polarization-maintaining
- Holy Grail: Coherent quantum transducers



# The next $10^{12}$ X: Architecture

# Architecture

*Design in the face of constraints<sup>9,10</sup>*



Environment

Devices & Signals

System

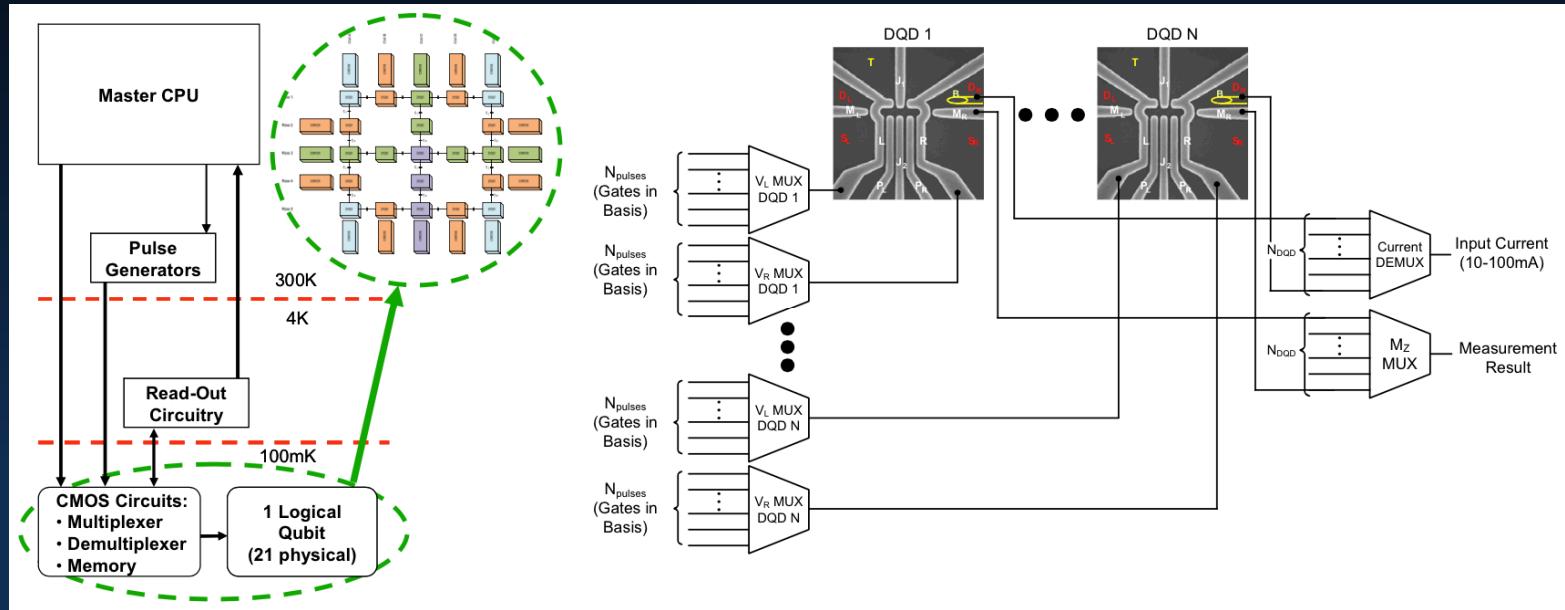
- Cooling power limits
- Vacuum limits
- EM control limits
- Yield limits
- Parallelism limits
- Latency limits
- I/O limits
- Routing limits
- Power limits
- Floor space limits
- Dollar limits

# Case Study: Bacon-Shor

*Electronics constraints radically change conclusions*<sup>9,10,11</sup>

**W/o constraints<sup>12</sup>:**  $p_{th} = 5.0 \times 10^{-4}$

**W/constraints<sup>10</sup>:**  $p_{th} = 2.0 \times 10^{-5}$



# Fault-Tolerance Cost

*Trading quality for quantity*

Factoring a 2,000-bit number<sup>4</sup>:

- $10^{12}$  quops deep, 4,000 qubits wide (error-free)
- Errors demand logical (encoded) qubits and logical (encoded) “magic states” to facilitate fault tolerance
  - $10^{-3}$  error: **1.02 Gqb (physical)**.
  - $10^{-4}$  error: **130 Mqb (physical)**.

# Fault-Tolerance Cost

*Trading quality for quantity*

Quantitatively accurate simulation of FeMoCo<sup>3</sup>:

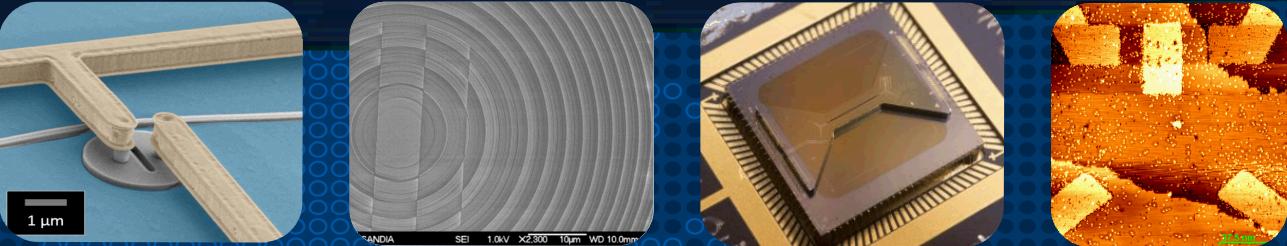
- $10^{12}$  quops deep, 135 qubits wide (error-free)
- Errors demand logical (encoded) qubits and logical (encoded) “magic states” to facilitate fault tolerance
  - $10^{-3}$  error: **5.1 Gqb (physical)**.
  - $10^{-6}$  error: **30 Mqb (physical)**.

# Architecture Challenges

- Codes well-matched to HW constraints
- Codes well-matched to SW applications
- More efficient methods for error-corrected universal QC
- Data from testbed machines on errors in QEC
  - QEC is the killer app for a testbed machine

# References

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