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INSTRUCTION AND MAINTENANCE MANUAL FOR BUFFER STORAGE UNIT 114-102

INTRODUCTION

Buffer Storage Unit 114-102 (BSU) provides eight channels of single-bit memory for accepting fast logic pulses from discriminator or coincidence circuits. Each set-input is direct-coupled to the input signal source. A single reset circuit is shared by all eight memory channels. A single output control gate is shared by the eight channels to provide a means for parallel multiplexing of the outputs for data-bus applications. The unit is packaged in a NIM #2 module as shown in Figs. 1a, 1b, and 1c. Each output channel provides a high-level signal to its load via an appropriate junction-box. A block diagram of a typical installation is shown in Fig. 2.

SPECIFICATION

Set Inputs:

Number of channels	$N = 8$
Input impedance	Z_{in} = 50 ohms nominal
Normal set pulse	V_s = -0.7 volt nominal at pulse width $\tau_s \geq 2$ nsec
Absolute maximum input	$\lvert V_s \rvert \leq (3.5/\rho_s)$ volt $\leq$ 12 volt peak where $\rho_s = (\tau_s/\text{pulse period})$
Sensitivity	Transition assured from logical zero to logical one for normal input voltage of -0.7 volts and τ_s = 2 nsec. DC triggering level equals -0.3 volt.

Reset:

Single reset serves	8 channels
Input impedance	Z_{in} = 1K nominal
Input voltage	V_r = ± 3 volts at pulse width
	$\tau_r \geq 20$ nsec
Absolute maximum input	$\lvert V_r \rvert \leq (10/\rho_r)$ volts $\leq$ 33 volts peak where
	$\rho_r = (\tau_r/\text{pulse period})$

Output Gate:

Gate signal	3 volts $\leq V_g \leq$ 33 volts peak at
	$\tau_g \geq 1\ \mu$sec
Maximum V_g	$\lvert V_g \rvert <$ 33 volts

Output gate can be permanently enabled by shorting out the output gate driver.

Output Level:

Current supplied to external load limited to 10 mA.

See text for options available.

Temperature Range:

0^{o}C to 60^{o}C

Power Requirements:

+12 VDC	150 mA maximum
-12 VDC	150 mA maximum

CIRCUIT DESCRIPTION

The eight memory and amplifier channels of the buffer storage unit are identical; therefore, only the first one will be described. The reset, output gate, and bias voltage circuits will be described after the operation of the basic memory circuit has been considered in detail.

The circuit operation is understood with the aid of the accompanying diagram of Fig. 3. Input pulses are accepted at input J-1 which is terminated to present a 50-ohm load. Transistor Q101 serves as an isolation amplifier. Since the base of Q101 is maintained at a constant voltage of approximately +0.6 volts, the emitter potential is held essentially constant at approximately 0 volts. By selecting the value of resistor R105, variability in the diode drop of CR101 can be corrected so that the drop across C101 is equal to the base-emitter drop of Q101. A current of 0.4 mA flows through resistor R103. If the voltage drop across C101 equals the base-emitter drop of Q101, then the emitter current is equal to the current through R103, and the collector current is equal to

$$i_c = \frac{\beta}{1+\beta} i_e . \qquad (1)$$

Consequently, when a negative voltage pulse appears across R101, a current change in the emitter circuit results in a corresponding current change in the collector circuit equal to

$$\Delta i_c = \frac{\beta}{1+\beta} \Delta i_e$$

$$= \frac{\beta}{1+\beta} \frac{V_{in}}{R102} \qquad (2)$$

Assuming that $\beta = 10$, for example, an input signal of -470 mV will result in a change in collector current of

$$\Delta i_c = \frac{10}{1+10} \cdot \frac{-470}{470}$$

$$= -0.90 \text{ mA} \qquad (3)$$

For a wide input pulse, the current through tunnel diode CR102 changes from 0.4 mA to 1.3 mA, neglecting the current flowing through R108. Since the input resistance of A101 is in the order of 100K, the current through R108 is indeed

negligible. The switching action that occurs for the example under consideration can be understood with the aid of Fig. 4 which shows the current versus voltage characteristic of the IN3712 diode used for CR102. When Δi_c is large enough to increase the current through CR102 well above i_p, the operating point shifts from point No. 1 to point No. 3. The voltage increases suddenly to V_3 and then decreases to V_2 when the input voltage is reduced to zero.

The change in current Δi_c need only be large enough to increase the tunnel diode current above i_p to effect a switching from operating point No. 1 to operating point No. 2. This would correspond to a nominal input voltage of $(0.6\ \text{mA})(470\ \Omega) \cong 300\ \text{mV}$ for a very wide pulse. Because of the limited gain-bandwidth product of the transistor amplifier, however, a somewhat larger input voltage is required for a narrow pulse to effect a transfer from point No. 1 to point No. 2. When a type 2N709 transistor is used for Q1, the condition for switching is given approximately by

$$(V_s + 0.3)\,\tau_s = -0.8 \times 10^{-9}\ \text{volt} \cdot \text{seconds}$$

For example, when $V_s = -0.7$ volt, a pulse duration $\tau_s = 2$ nsec is required to assure a transition.

Reset of the tunnel diode is effected by reducing the collector current in Q101 below i_v to zero. This is accomplished by raising the emitter of Q101 to approximately 450 mV when a reset pulse $|V_r| > 3$ volts is applied at J9. The action of the reset circuit is considered later. The voltage drop across the tunnel diode varies from less than 0.1 volt (corresponding to operating point No. 1) to approximately 0.5 V (corresponding to operating point No. 2). During the reset condition, the voltage at the inverting input pin No. 1 of A101 is approximately 4.5 volts. During the set condition, the voltage at pin No. 1 is approximately 4.0 volts. Since pin 6 of the differential amplifier is held at 4.4 volts, the output

at pin 10 of A101 varies from approximately 3.5 volts to +7.1 volts. This indicates that the differential amplifier has a gain of 10 or greater.

In the set condition, transistor Q102 is saturated and draws collector current through R112 and the base of Q103. Resistor R115 limits the current in the collector circuit of Q103 to approximately 10 mA. For a high resistance load in the collector circuit, the voltage at J10A can rise to approximately 10 V. For specific loads, the operating voltage levels can be adjusted by means of an appropriate junction box. For example, one could return the output from J10A to -12 volts at J10K through an external 2.2K resistor. The use of an external 2.2K resistor in such a manner would make the buffer storage unit compatible with a fast digital input channel of the IBM1800 system. The equivalent circuit would then be represented as shown in Fig. 5. For the equivalent circuit of Fig. 5 , when $i = 0$, $V = -8.8$ volts for binary "0"; when $i = 10$ mA, $V = +2.1$ volts for binary "1". For devices requiring a positive-true voltage, one could return an output resistive load of 1K or greater to ground at J10A. The output would then vary between 0 and +10 volts.

A common output gate is provided to control the flow of current in all of the output circuits. This facilitates parallel readout onto a multiplexed data-bus. Taking channel 1 as the typical circuit, it can be seen that Q4 acts as a series switch for Q103. Similarly Q4 also controls the current flowing into the emitters of Q203, Q303, ... through Q803. Transistor Q4 in turn is controlled by Q3. When a positive signal in excess of 2 volts is applied at either J10N or J11, current flows through Q3, and base current is drawn from Q4. For gate signals of 3 volts or greater, Q3 and Q4 are saturated. The collector of Q3 can be permanently connected to ground by shorting J10L and J10M. Base current sufficient to saturate Q4 is then drawn through R5. Transistor Q4 then is capable of supplying current to the emitters of Q103 through Q108 for any channel in the set condition.

Reset pulses are applied at either J9 or P1-35. The reset circuit can accept either positive or negative pulses. If positive pulses greater in magnitude than 3 volts are applied, current flows through CR1, CR2, and R1, causing diode CR5 to be back-biased. Current is then steered through resistor R2 and diode CR6 into resistor R104. The current then divides with most of the current flowing through R102 and R101 to ground; the remainder flows through R103 to the -12 volt supply. Since there are seven additional loads fed by CR6, the impedance seen by CR6 is approximately 190 Ω. Consequently, the voltages at the emitters of Q101, Q201, ... through Q801 must rise to approximately 0.45 volts. Then, in channel 1, current flow through the emitter of Q101 is interrupted and the current through CR102 decreases to zero (neglecting the small current flowing through R108). When the reset pulse is removed, the operating point is shifted from the origin to operating point No. 1. If a minus reset pulse whose magnitude exceeds 3 volts is applied, zener diode CR4 conducts so that the potential at the base of Q2 drops below 3.9 volts. Transistor Q2 then conducts and current flows through R7, CR6, and R104. The action is then similar to that which occurs when a positive reset pulse is applied.

The buffer storage unit draws currents not exceeding 150 mA from a ± 12 V supply such as the Power Designs No. AEC-320-3. Besides the ±12 volt supply potentials, additional voltages are derived internally. A 6.2 volt supply is derived using zener diode CR7. The 6.2 volt supply provides a bias voltage to R114 through R814 which draw no current in reset condition. The 6.2 volt supply is also used to derive a 5.1 volt reference source from zener diode CR8. The 5.1 volt reference is applied to the base of Q1 which functions as an emitter follower. The output of the emitter follower is approximately 4.5 volts, from which is derived a 4.4 volt supply through a voltage divider consisting of R16 and R17.

MAINTENANCE

The operation of the buffer storage unit can be checked with the assistance of the test set whose circuit diagram is shown in Fig. 6. In addition to the test set, it will be necessary to use a NIM bin and its associated power supply. A test setup for go/no-go checks is shown in Fig. 7.

The test set accepts inputs from each of the eight output channels from the buffer storage unit utilizing a standard interconnecting cable. By means of switch S1, one can select whether the 2.2K load resistor is connected to -12 volts or to ground. A 3.6K resistor shunts the input signal to ground via the base of a transistor used as a lamp driver and the cable connecting back to the unit under test. The presence of a ONE output, where $V_{out} > 2$ volts, is sufficient to turn on the indicator lamps when the buffer storage is set and when the output gate is operational. The output gate is cheated out when switch S2 is in position OUT. The test set can provide both set and reset pulses to the unit under test. A set pulse is obtained when switch S4 is depressed. A reset pulse is obtained when Switch S3 is depressed.

To use the test set, interconnect the cabling and house both the unit under test and the test set in a NIM bin. Turn on power supply and reset by depressing S3. Connect a coaxial cable between the output of J11 of the test set and input J1 of the unit under test. Depress switch S4 to set channel 1. Display lamp DS1 should now be lighted. Reconnect the cable to J2, J3, ... J8 in turn and repeat the above procedure. The corresponding display lamps should now light in turn. Depress switch S3 and note whether all display lamps extinguish as they should for proper operation.

If the unit under test fails to respond to the go/no-go check, it will be necessary to check voltage levels and wave forms. The location of the components with respect

to the etched circuit is shown in the component layout diagram of Fig. 8. The key voltages are those at the collector, base, and emitter Q101, Q201, ... etc. These should be approximately equal to the values shown in the following table:

	Collector	Base	Emitter
Set Condition	4.0 v	0.6	0
Reset Condition	4.45 v	0.6	0

Dynamic testing will require the use of a sampling scope and a nanosecond pulse generator. Defective tunnel diodes or isolation amplifiers can be detected generally by observing the waveforms at the collectors of Q101 - Q801.

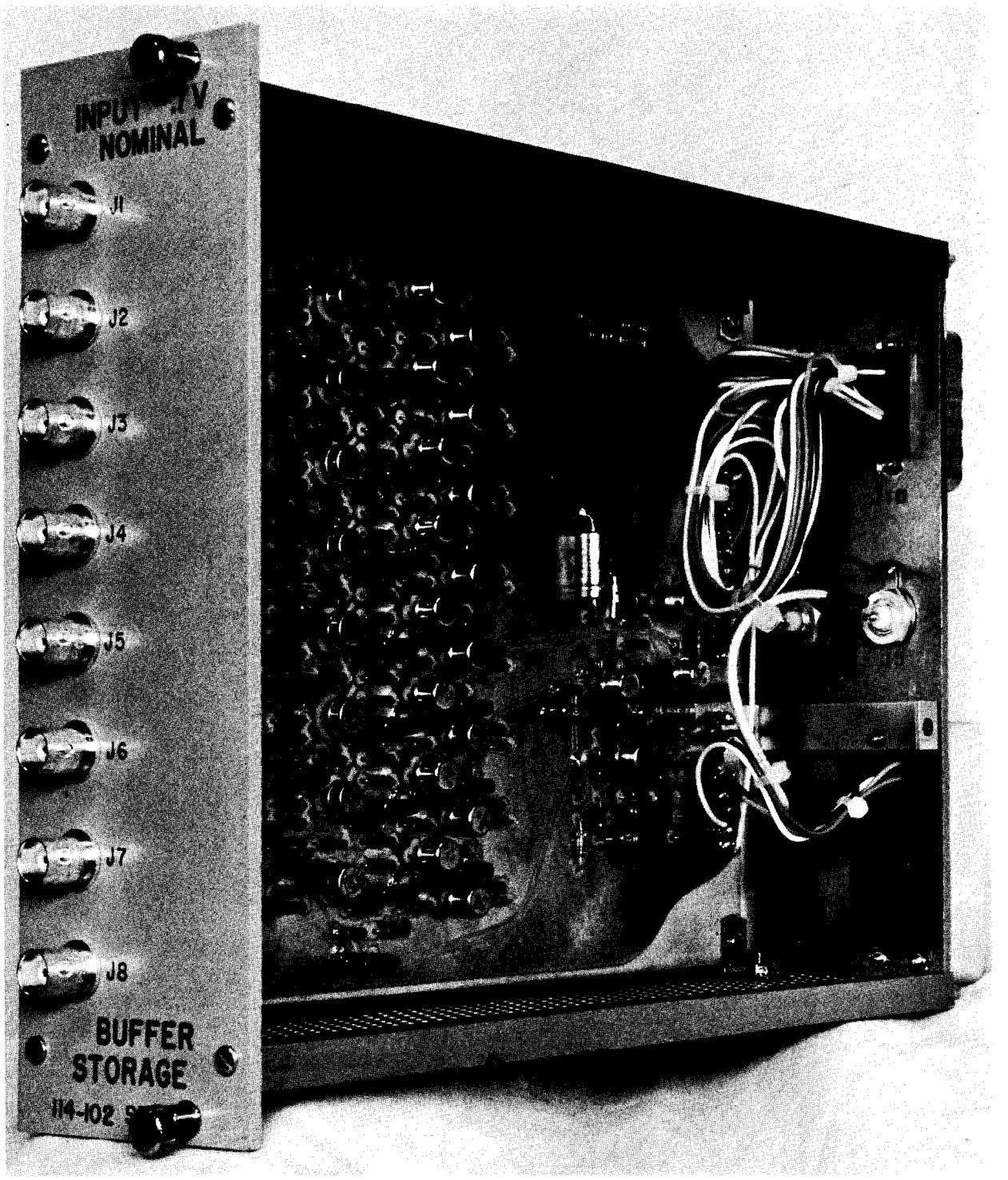


FIG. 1a--Front oblique view of buffer storage unit (cover removed) showing component side of printed circuit board.

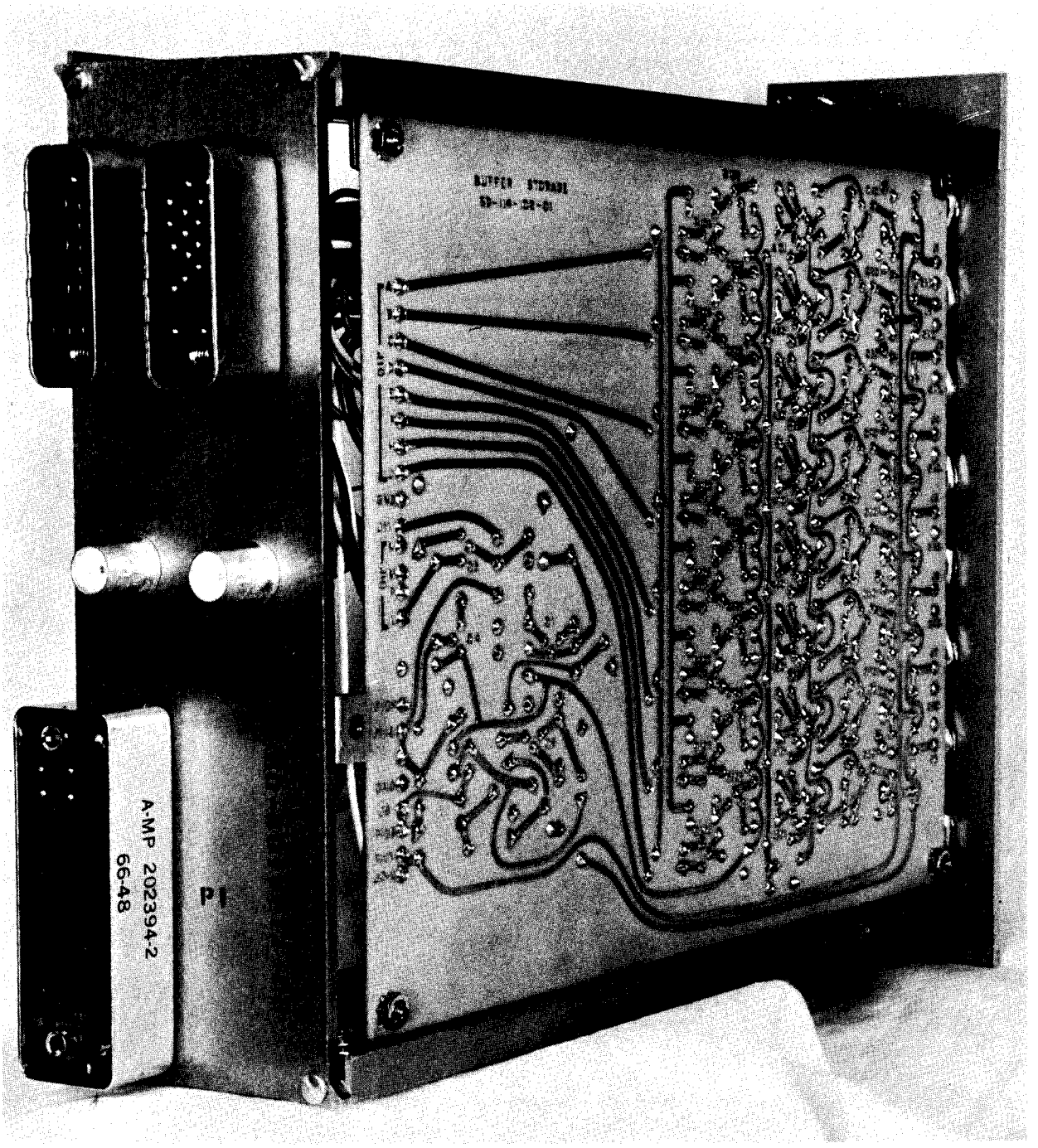


FIG. 1b--Rear oblique view of buffer storage unit (cover removed) showing etched wiring side of printed circuit board.

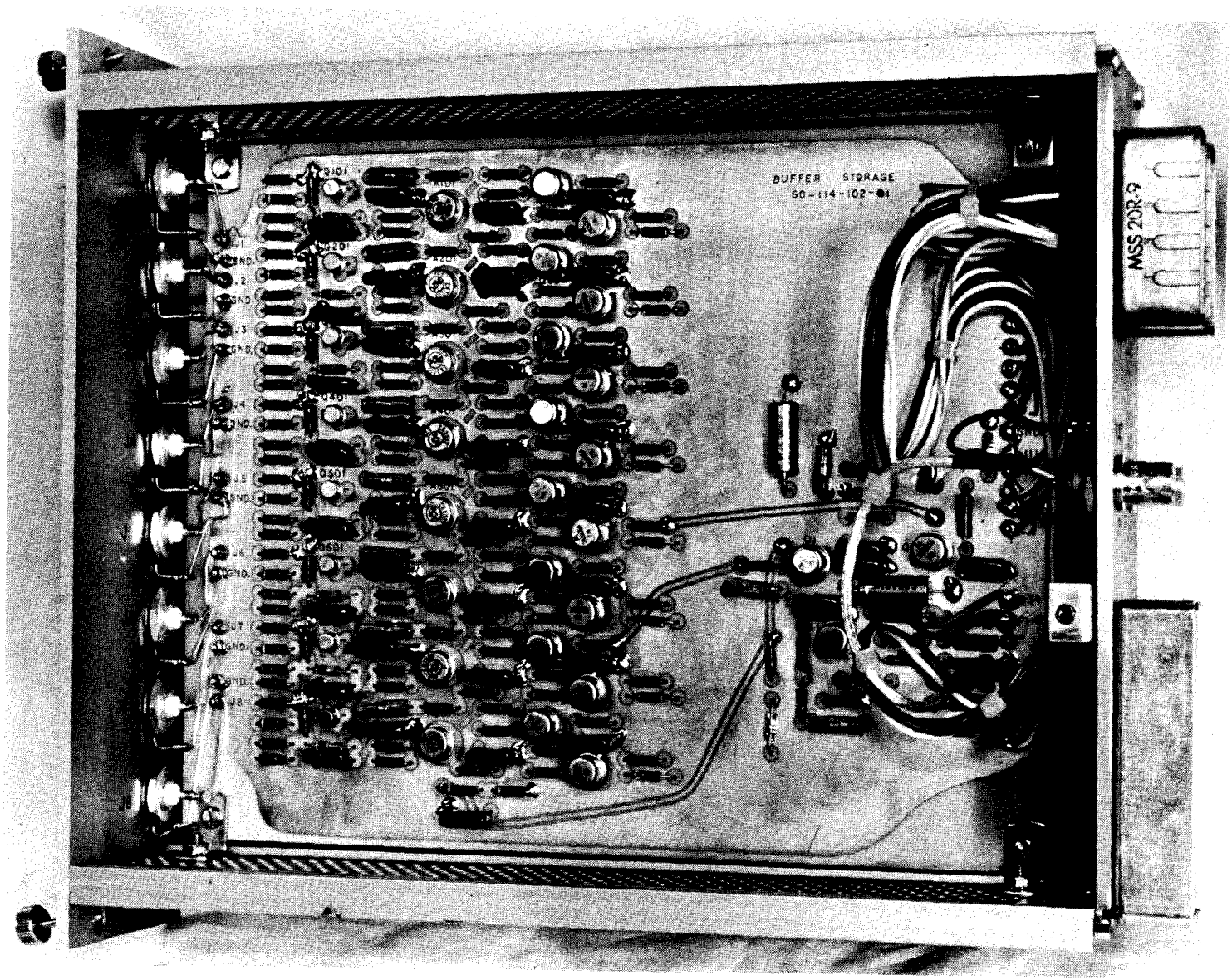


FIG. 1c--Side view of buffer storage unit (cover removed).

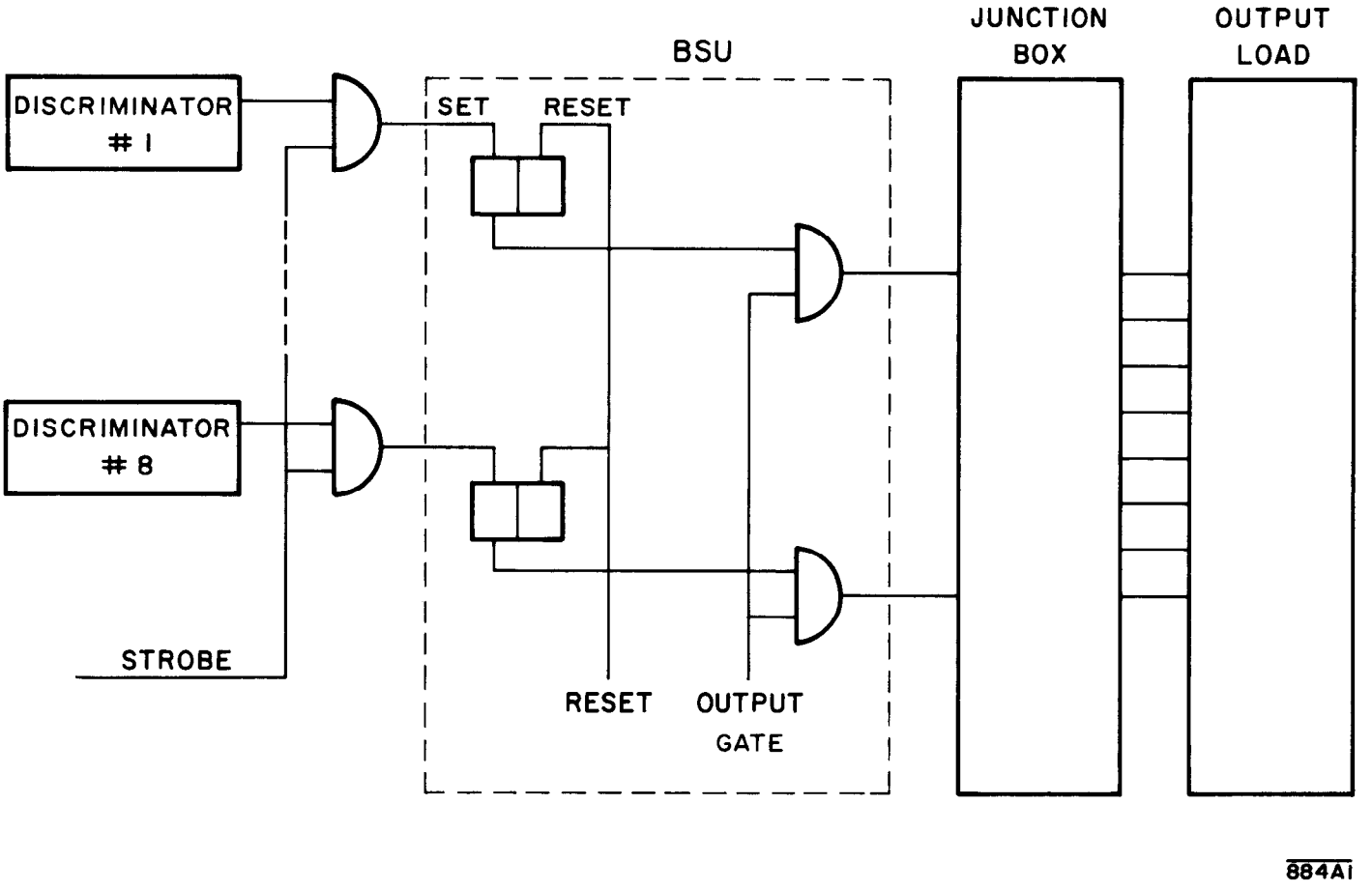
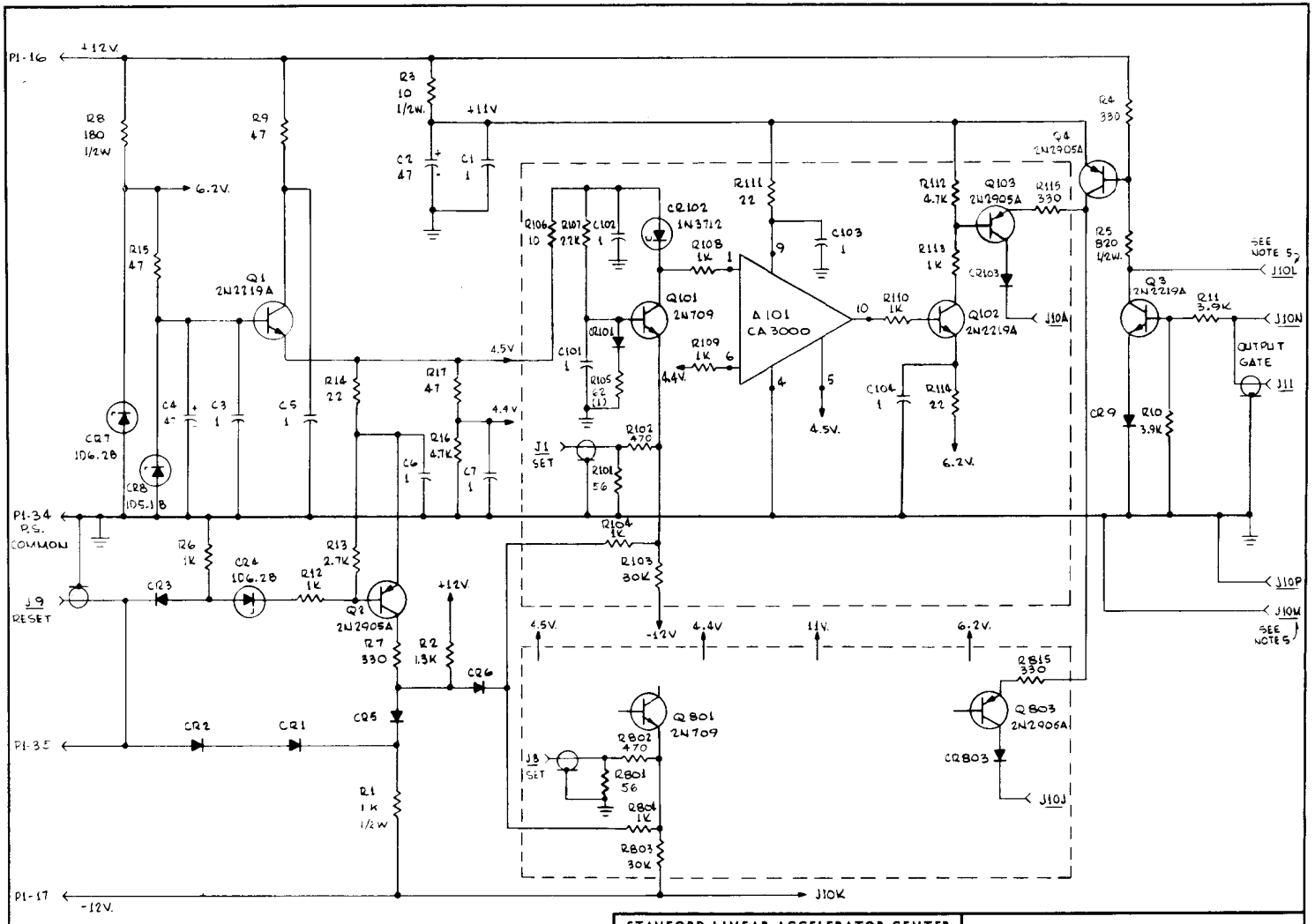


FIG. 2 -- TYPICAL INSTALLATION INCORPORATING BUFFER STORAGE UNIT



NOTES:

1. 2105 THRU R805 SELECTED IF NECESSARY. NOMINAL VALUE = 62Ω.
2. ALL RESISTORS IN OHMS AND 1/4W., UNLESS OTHERWISE SPECIFIED.
3. ALL DIODES TYPE IN3064 UNLESS OTHERWISE SPECIFIED.
4. ALL CAPACITORS IN μf UNLESS OTHERWISE SPECIFIED.
5. SHORT J10-L AND J10-M EXTERNALLY FOR PERMANENT OUTPUT ENABLE.

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APPROVALS [illegible] 8/3/67

SCHEMATIC
BUFFER STORAGE

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884A2

FIG. 3

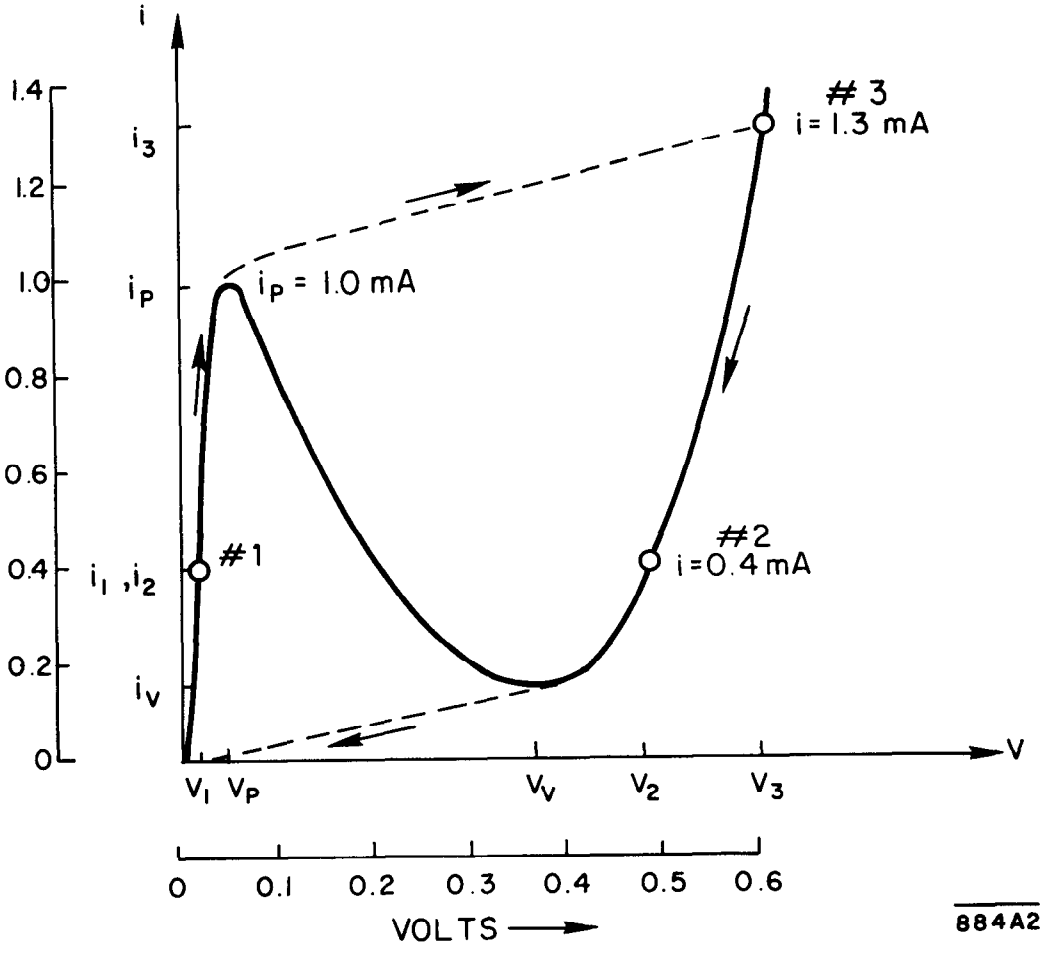

FIG. 4 ---TUNNEL DIODE CURRENT vs VOLTAGE CHARACTERISTIC.

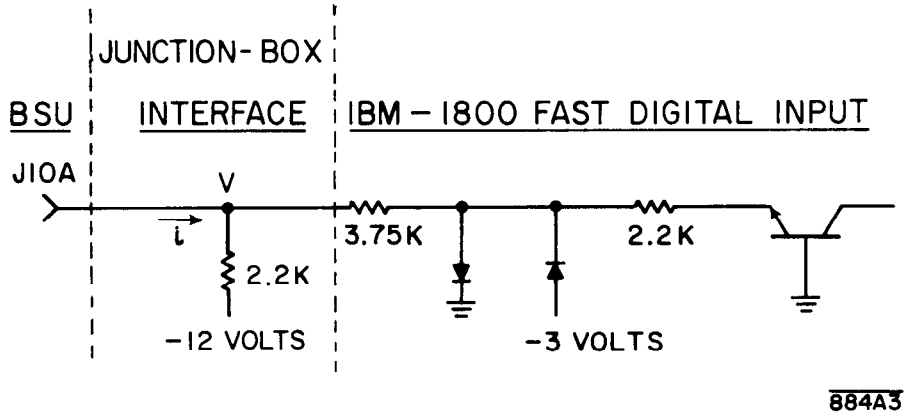

FIG. 5 -- EQUIVALENT CIRCUIT REPRESENTATION

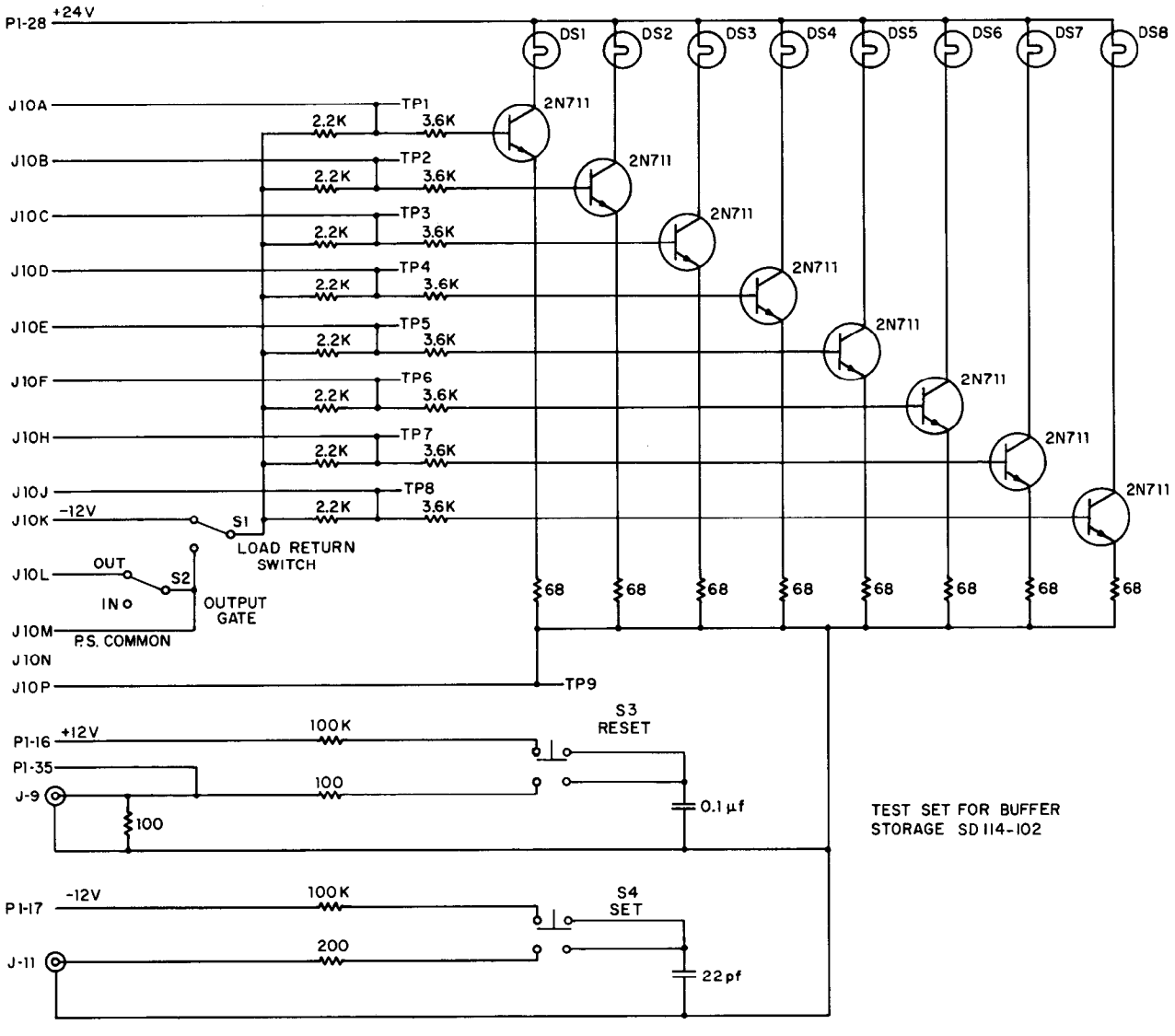
P1-28 +24V
DS1
DS2
DS3
DS4
DS5
DS6
DS7
DS8
J10A
J10B
J10C
J10D
J10E
J10F
J10H
J10J
J10K -12V
J10L
J10M
J10N
J10P
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
2.2K
3.6K
2N711
68
S1
LOAD RETURN SWITCH
OUT
S2
IN
OUTPUT GATE
P.S. COMMON
P1-16 +12V
P1-35
J-9
100K
100
0.1 µf
S3
RESET
P1-17 -12V
J-11
200
22pf
S4
SET
TEST SET FOR BUFFER STORAGE SD 114-102

FIG. 6

88484

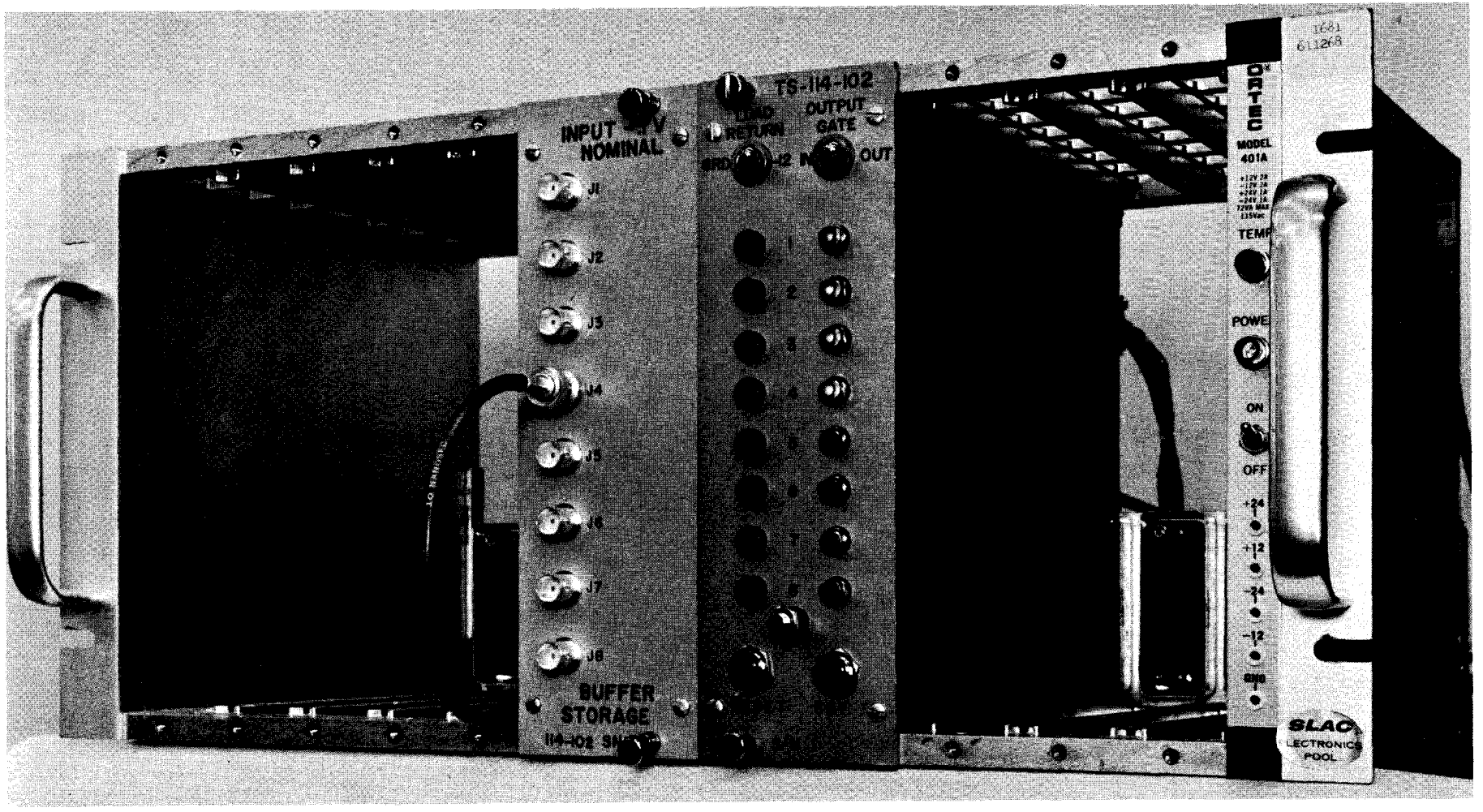

FIG. 7--Go/no-go test setup.

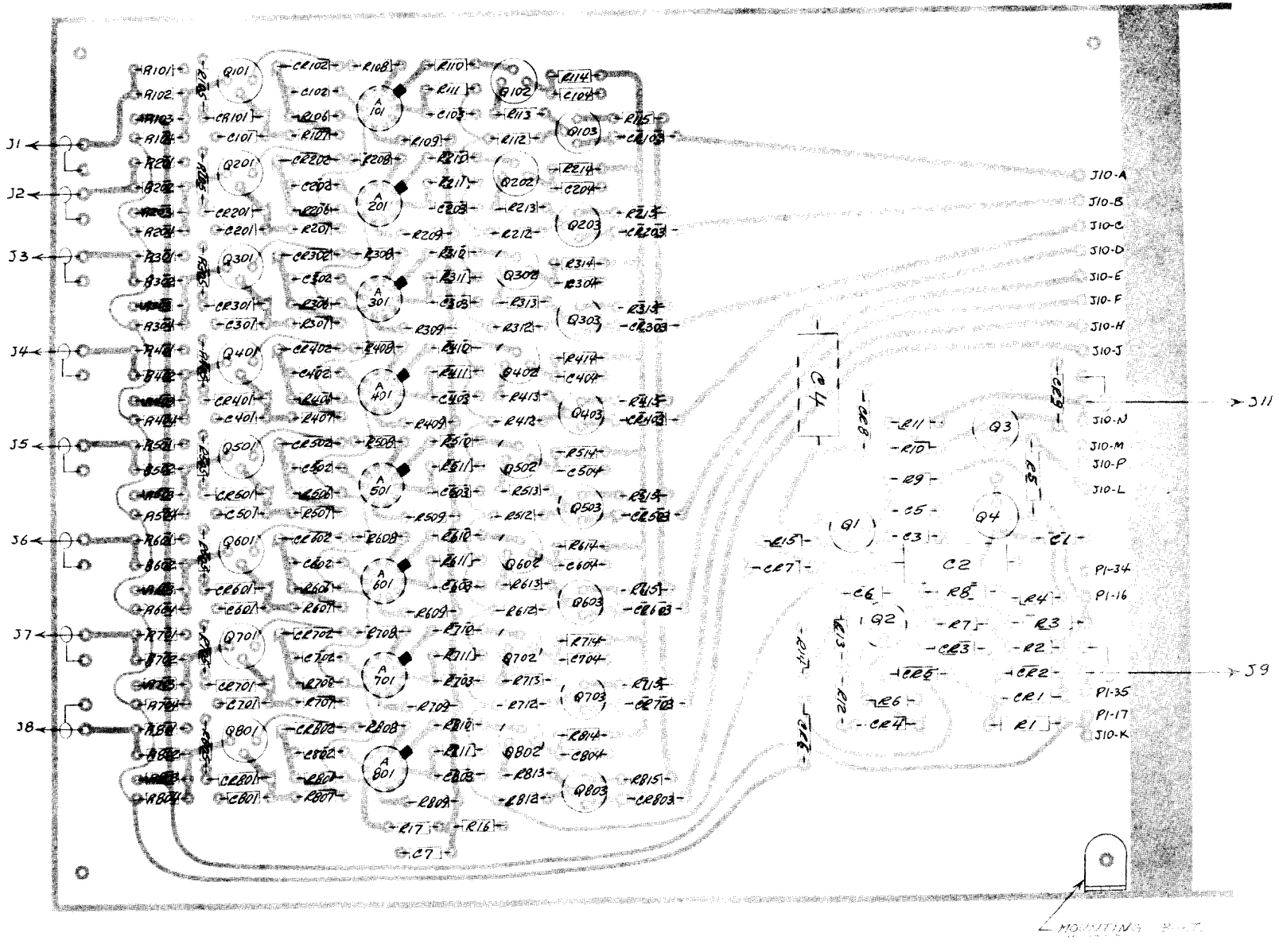

FIG. 8--Component layout.