SLAC-PUB-4758
LBL-26103
October 1988
(A/I)

GALLIUM ARSENIDE DIGITAL INTEGRATED CIRCUITS FOR CONTROLLING SLAC CW-RF SYSTEMS*

M. T. RONAN AND K. L. LEE
Lawrence Berkeley Laboratory, Berkeley, California 94720
and
P. CORREDOURA AND J. G. JUDKINS
Stanford Linear Accelerator Center, Stanford University, Stanford, California 94309

ABSTRACT

In order to fill the PEP and SPEAR storage rings with beams from the SLC linac and damping rings, precise control of the linac subharmonic buncher and the damping ring RF is required. Recently several companies have developed resettable GaAs master/slave *D*-type flip-flops which are capable of operating at frequencies of 3 GHz and higher. Using these digital devices as frequency dividers, one can phase shift the SLAC CW-RF systems to optimize the timing for filling the storage rings. We have evaluated the performance of integrated circuits from two vendors for our particular application. Using microstrip circuit techniques, we have built and operated in the accelerator several chassis to synchronize a reset signal from the storage rings to the SLAC 2.856 GHz RF and to phase shift divide-by-four and divide-by-sixteen frequency dividers to the nearest 350 psec bucket required for filling.

INTRODUCTION

In the past, the PEP and SPEAR e^+e^- storage rings at the Stanford Linear Accelerator Center have been filled using the two-mile long linac with its electron gun and an inline positron source. Each 2 nsec gun pulse would fill several linac 2856 MHz RF buckets, thus dominating the timing error in filling a storage RF bucket. A relatively low yield of positrons with large beam emittance from the inline target made e^+ filling quite a challenge.

Now, with the upgrade of the linac for operation of the Stanford Linear Collider (SLC) having been completed, the new accelerator systems—including an electron gun with a subharmonic buncher and an off-axis high-yield positron source, as well as electron and positron damping rings—are being used to fill the storage rings. The subharmonic buncher, operating at 178.5 MHz, is used to compress the electron pulse from the gun to fill only one linac RF bucket. With the high intensity beams from the electron gun and positron source, and the low emittances obtained using the damping rings, the storage rings are being filled in minutes. Several improvements to the linac timing and control systems were needed in order to allow storage ring filling with the new SLC accelerator systems. The timing system improvements included: distributing timing reference signals between the various accelerators, phase-locking the storage rings to the linac time base, upgrading the linac trigger (fiducial) generation system, and several upgrades to the linac RF system. In this paper, we will describe some of the new electronics which have been developed for the RF modifications; the complete timing system upgrade is described in another report.[1]

CONTROLLING CW-RF SYSTEMS

In order to fill the PEP and SPEAR storage rings with beams from the SLC linac and damping rings, precise control of the linac CW-RF system is required. Although the PEP and SPEAR master oscillators, operating at RF frequencies of 353.210 MHz and 358.540 MHz, respectively, have been phase-locked to the linac master oscillator operating at 476 MHz, phase shifting of the CW-RF is required to pulse the linac at a fixed phase of the 360 Hz power line.

Recently several companies have developed GaAs master/slave *D*-type flip-flops which are capable of operating at frequencies of 3 GHz and higher. We have tested integrated circuits for our particular application from two vendors, Harris Microwave Semiconductor and Nippon Electric Corporation (NEC), as described below.

*This work was supported by the Director, Office of Energy Research, Office of High Energy and Nuclear Physics, Division of High Energy Physics, of the US. Department of Energy under contracts DE-AC03-76SF00098 and DE-AC03-76SF00515.

Using these digital devices, we have built resettable frequency divider circuits operating at the linac klystron RF frequency (2.856 GHz) which divide the clock frequency by four or sixteen to generate the 714 MHz and 178.5 MHz needed for driving the damping ring RF and the subharmonic buncher, respectively. Using the reset feature and a timing reference from the storage rings, the CW-RF systems are phase-shifted to the nearest 350 psec RF bucket that matches the beam timing required for filling, while synchronous operation within the linac accelerator systems is maintained.

A separate GaAs unit synchronizes the storage ring reference signal to the 2856 MHz clock before it is distributed as a reset to the damping ring and subharmonic buncher dividers to insure synchronous resetting, as shown in the block diagram (Fig. 1). The synchronizer effectively selects the linac RF bucket to be used and then resets both GaAs dividers to the same RF bucket. When PEP and SPEAR filling has been completed, a trigger signal from the linac synchronous timing system is used to reset the RF system for normal SLC operation.

HARRIS EVALUATION AND CIRCUIT OPERATION

The data given in the manufacturer's specification sheet for the Harris GaAs digital device[2] are shown in Table 1. For our application, we specified that devices should be selected which would operate at frequencies of 3.0 GHz minimum.

Table 1. Harris HMD-11131 master/slave *D*-type flip-flop specifications.

• Propagation Delay	600 ps	typ.
• Clock Rate Max (Single Phase)	2000–2500 MHz	
• Clock Rate Max (Dual Phase)	2800 MHz	typ.
• Data Input Rate Max	1000–1250 MHz	
• Output Transition Low to High	150 ps	typ.
• Output Transition High to Low	220 ps	typ.
• Setup Time	220 ps	typ.
• Hold Time	0 ps	typ.

The power supply voltage requirements are +4.5 V dc and −3.5 V dc referenced to dc ground. These voltages produce compatible logic levels to the ECL logic family. Power supply current requirements for the IC are typically 180 mA and 150 mA for the positive and negative supplies, respectively. In addition, each output with an external pulldown resistor of 51 Ω to −3.5 V dc will add a 65 mA load.

CIRCUIT OPERATION

We have used these devices as a clock synchronizer and as adjustable modulus frequency dividers with synchronous reset. For the synchronizer, an asynchronous signal is introduced at the *D* input and the resulting *Q* output has its edges synchronized to the clock. The divider circuit design uses a conventional technique of feeding back the $\overline{Q}$ output to the data input to form a toggle flip-flop which normally functions as a divide-by-two counter. For the Harris circuit, synchronous resetting is performed by using the second *D* input to inhibit toggling with a logic high level.

Presented at the Nuclear Science Symposium, Orlando, Florida, November 9–11, 1988

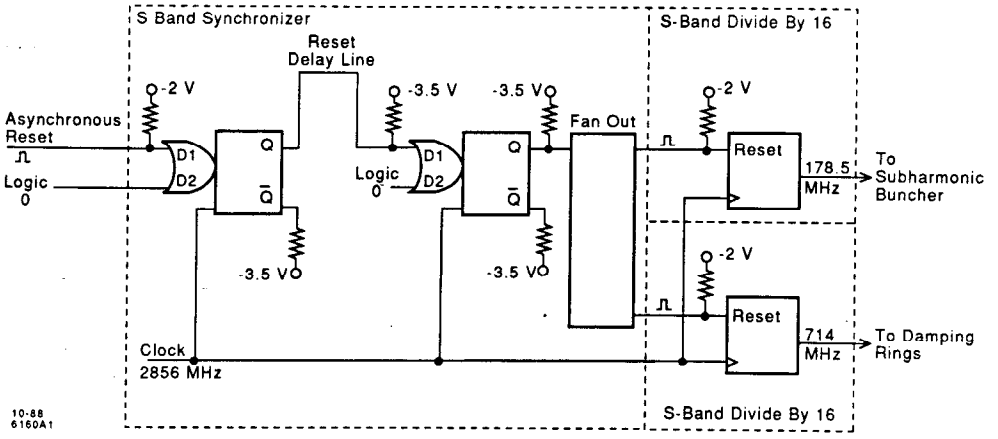

Fig. 1. Block Diagram of SLAC CW-RF Control System.

In the synchronizer circuit, two GaAs flip-flops have been used to obtain an accurately timed, synchronous reset signal. The asynchronous input signal, connected to the D input of the first flip-flop, is nearly synchronous at the output (Q). A second stage flip-flop is used to eliminate the time spread of the output edges caused by the nonsynchronous reset violating setup and hold times for the first flip-flop.

In designing a frequency divider which divides by an arbitrary number, a delay line is introduced to delay the time between a $\overline{Q}$ output transition and the change at the data input. The delay inhibits the flip-flop from changing state for a time period equal to the time of the delay plus propagation delay through the device.

The divide-by-four counter was designed simply by connecting the $\overline{Q}$ output directly to the D input, since internal propagation delay provided the two clock cycles delay needed to form a divide-by-four counter; while for the divide-by-sixteen counter, a delay cable was needed to provide a total effective delay of eight clock cycles in the feedback path. The length of this cable was estimated from a measurement of the internal propagation delay of the device; with the final length being determined empirically for each IC by requiring a stable division ratio over a wide range of threshold adjustment.

TEST RESULTS

Measurements of the propagation delays indicated values similar to those given on the manufacturer's data sheet. We have found by connecting the $\overline{Q}$ output directly back to the D-input, that the devices would operate reliably as a divide-by-four up to over 3.0 GHz; with some devices continuing to clock up to 4.0 GHz but at a division ratio greater than four. In tests of the gating, an abnormality was found which required a change in how the synchronous reset was applied. Originally, the $\overline{CLR}$ input was used as the reset input; however, the internal interruption of the clock by the "clear" signal introduced output timing jitter. After a circuit modification, the second D input was used to "reset" the counter by forcing the flip-flop into the logical-one state. Another phenomenon called the "wake-up effect" was also uncovered[2] and is described below.

To describe the "wake-up effect" assume the clock is free running and the flip-flop is toggling. A logic low applied to the $\overline{CLR}$ input (or a high applied to the second D input) will inhibit the flip-flop from toggling and hold it in a fixed state. In a typical toggling flip-flop, releasing the resetting signal will normally allow the flip-flop to begin toggling again after a short internal propagation delay. As shown in Fig. 2, for the Harris chip using the $\overline{CLR}$ reset, we see the Q output initially goes high but remains high for a period of about three output cycles before normal operation. A similar effect is also observed using the second D input. This dead time has been referred to as a wake-up time.[2]

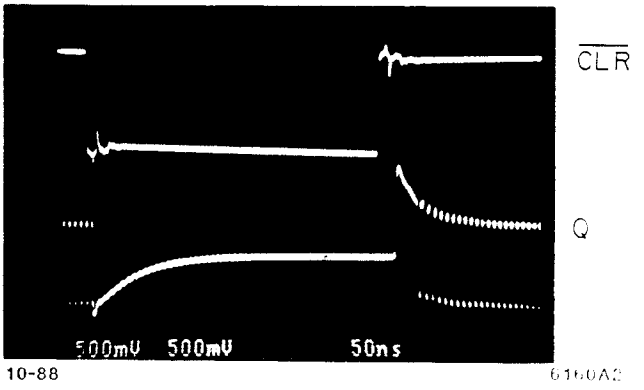

Fig. 2. Scope display of reset operation with a Harris device[2] demonstrating the "wake-up effect."

In testing the operation of the Harris chip as a synchronizer, we have been able to achieve better than 20 psec stability of the output edge with respect to the 2856 MHz clock, as shown in Fig. 3. We find the output pulse width is several nanoseconds less than the input pulse due to the "wake-up effect" for each of the two flip-flops. In addition, we have found that the propagation delay of the trailing edge changes as the width of the reset pulse is changed; in our application, we avoid this problem by using a pulse of constant width.

Since the "wake-up effect" has been relatively stable, the Harris device has been found adequate for our initial application. As in using any device near the limit of its operation, consideration to propagation delays are important and hand tailoring may be necessary to make the system functional. The circuit board and related components have been assembled using standard microwave techniques including: high quality microwave chip capacitors for bypassing and RT/6000 Duriod,[3] a substrate 10 mils thick with a dielectric constant of six to allow line widths which match the integrated circuit leads.

NEC EVALUATION AND CIRCUIT OPERATION

Typical and maximum ac specifications for the NEC GaAs digital device given on the data sheet[4] are shown in Table 2. The power supply voltage requirement is -5.2 V dc at a current of 135 mA maximum. The input/output logic levels are compatible with standard ECL logic family. As suggested by the manufacturer, each output must be pulled down with a 51 Ω resistor to -2 V dc.

TEST RESULTS

Measurements were made on a microstrip test-board with the device configured as a divider similar to the application of the Harris device described above. A dual power supply,

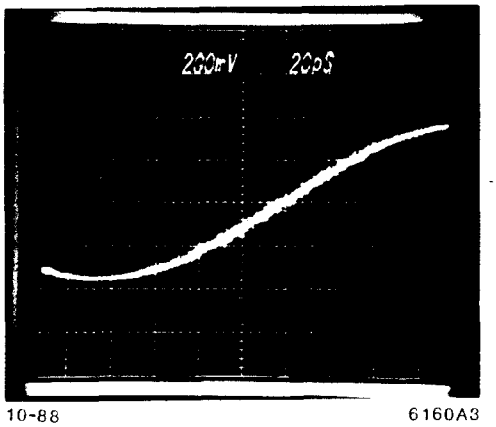

Fig. 3. Sampling scope display of 2856 MHz RF waveform triggered on trailing edge of output from S-Band Synchronizer circuit.

Table 2. NEC UPG700B master/slave *D*-type flip-flop specifications.

• Maximum Clock Frequency	3.2 GHz
• Propagation Delay	400–800 ps
• Output Rise Time	130–250 ps
• Output Fall Time	120–250 ps
• Setup Time	100–200 ps
• Hold Time	100–200 ps

+2.0 V dc and −3.2 V dc, was used for convenience of having the inputs and outputs with a logic level referenced to ground.

Propagation delays were measured and found to be within the published data-sheet limits. Measurements of the performance of the device for asynchronous resetting using the Reset and $\overline{D}$ inputs, shown in Fig. 4, demonstrate the expected operation as a toggling flip-flop with no observable "wake-up" effects. Note that the outputs also show the expected full period spread, 350 psec, for asynchronous resetting with our 2856 MHz clock.

Our tests show the NEC device is inherently faster than the Harris device and is better behaved in gating and toggling. The lower power requirement of the NEC is also an advantage, while the −2.0 V dc termination is convenient when the circuits are used in conjunction with standard ECL family devices.

OPERATIONAL EXPERIENCE

Using these GaAs IC's in microstrip circuits, we have constructed and operated in the accelerator a complete GaAs RF control system as shown in Fig. 1. We have successfully used this system to fill both the PEP and SPEAR storage rings using bunched beams from the SLC damping rings. The measured accuracy of the delivered beams is close to the expected 350 psec spread due to the linac 2856 MHz RF system.[1] In addition, we have been able to restore SLC timing using a synchronous trigger signal on a pulse-to-pulse basis.

Our operational experience to date has been mainly with Harris GaAs circuits. At this time for multiple beam operation with both synchronous and asynchronous triggers interleaved, we have measured a timing jitter of about 100 psec due to the system noise level and relatively slow risetimes from ancillary ECL circuits. This jitter has lead to a reset error rate of 0.1–1.0%, where an error occurs when the damping ring and

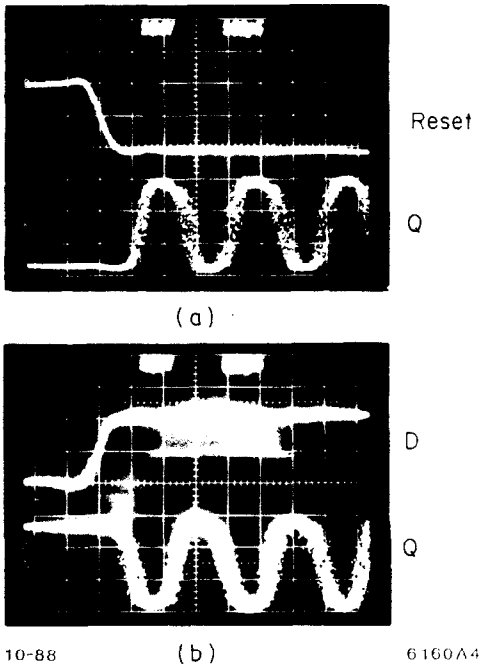

Fig. 4. Displays of asynchronous resetting of a NEC device[4] using both the RESET and $\overline{D}$ inputs for phase shifting.

subharmonic buncher RF are not reset to the same RF bucket. However, this error leads to only a small inefficiency in filling the storage rings and is not relevant to SLC CW operation.

We are in the process of improving system noise levels and the risetime of buffer and receiver circuits. We expect to switch to new circuits using the NEC chip before long.

ACKNOWLEDGMENTS

The conceptual design of the Timing system upgrades for filling the PEP and SPEAR storage rings was defined by the authors and J. Fox, R. Hettel, A. Odian, M. Ross, H. Schwarz and J. Vancraeynest. The use of resettable GaAs digital circuits for controlling the subharmonic buncher used with the SLC electron gun was first suggested by Marc Ross soon after GaAs IC's appeared on the market in 1984. Jan Vancraeynest provided the layout design for the Harris microstrip circuits. We have benefitted from useful discussions with H. G. Jackson and representatives of Harris Microwave and California Eastern Laboratories on the design and implementation of high frequency GaAS microstrip circuits.

RERERENCES

1. M. T. Ronan et al., *"Timing and RF Synchronization for Filling PEP/SPEAR with the SLC Damping Rings,"* 1989 Particle Accelerator Conference, Chicago IL, March 20–23, 1989.
2. *"Harris GaAs Digital IC: Master/Slave D-Type Flip-Flop, HMD-11131-2,"* August 1986, Harris Microwave Semiconductor, 1530 McCarthy Boulevard, Milpitas, CA 95035.
3. *"RT/6006 Duroid":* Rogers Corporation, 100 S. Roosevelt, Chandler, AZ 85226
4. *"NEC GaAs Digital IC: Master/Slave D-Type Flip-Flop, UPG 700B,"* March 1987, California Eastern Laboratories, Inc., 3260 Jay Street, Santa Clara, CA 95054.