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TUNNEL DIODE BUFFER STORAGE UNITS*

They're fast, simple, and reliable

Suppose you were faced with the problem of building a buffer storage unit (BSU) capable of responding to low-level nanosecond pulses. Several simple solutions would immediately suggest themselves. For example, you might use a pulse stretcher followed by a conventional flip-flop for each input channel. If the problem were altered slightly and you were faced with the task of adding a common strobed input to an eight channel BSU, most conventional approaches would lead to complex solutions. However, tunnel diodes used as memory devices driven by strobed differential amplifiers would provide an economical, simply implemented solution.

Two BSU's are described here, both containing the same basic memory cell. An unstrobed unit is considered first. By adding only a single transistor per channel, one can realize a BSU which has a gated input.

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THE BASIC CIRCUIT

All of the circuits considered are derived from the basic configuration shown in Figure 1A. A tunnel diode TD is inserted in one arm of a differential amplifier containing transistors Q1 and Q2. The current through the tunnel diode branches into the collector of Q2 and into resistor R5. Transistor Q2 is biased so that negligible collector current flows in the absence of an input signal applied to the base of transistor Q1. Consequently, the steady-state current through the tunnel diode is equal to the bias current flowing through the normally closed reset switch. However, when a sufficiently large negative voltage is impressed across resistor R1, appreciable current will flow into the collector of Q2. A switching action can occur in the tunnel diode when the total current either increases to a level greater than I_P or when the current decreases to less than I_V as described in the following paragraphs.

The switching action that occurs in tunnel diode TD can be understood with the aid of Figure 1B which shows the current versus voltage characteristic of a typical germanium tunnel diode. At time t=0, assume that the base of Q1 is at ground potential and that Reset Switch S1 is open. Since Q2 is cut off, no current flows through the tunnel diode; and the operating point at t=0 is at the origin of the current versus voltage characteristic. At $t=t_1$, S1 is closed and the locus of the operating point moves from the origin to point No. 1 ($V=V_1$, $I=I_1$) as determined by the current $I_{BIAS} = I_1$ flowing through R5. At time $t=t_2$, collector current through Q2 adds to the quiescent current through R5 so that the total current through TD exceeds I_P. The operating point therefore moves from (V_1, I_1) to (V_2, I_2). After the negative input voltage applied to the base of Q1 is removed, the current through the TD is equal to I_3 at time $t=t_3$. Operating point No. 3 at time t_3 is then located at (V_3, I_3) where $I_3 \cong I_1$. However, voltage V_3 is many times larger than V_1. To restore the operating state to point No. 1, it is only necessary to reduce the current through TD momentarily to a value less than I_V. This is accomplished by opening S1 when zero signal is applied to the base of Q1 so that the operating point moves from point No. 3 to point No. 1 via point No. 0.

DESIGNING FOR HIGH SWITCHING SPEED

The TD switching time from point No. 1 to point No. 3 will be equal to the sum of the times required to shift from (V_1, I_1) to (V_P, I_P) and from (V_P, I_P) to (V_3, I_3). The transition time required to shift the operating point from (V_1, I_1) to (V_P, I_P) depends almost entirely on the propagation delay of the differential amplifier. However, the TD switching time from (V_P, I_P) to (V_3, I_3) is essentially independent of the current through the TD provided only that it exceeds I_P. The TD switching time t_s from (V_P, I_P) to (V_3, I_3) is given approximately by [1]

$$t_s = C\,(V_3 - V_P)/(I_P - I_V)$$

where C, the sum of the TD internal capacitance and the external shunt capacitance, is typically 10 to 30 pf. Since t_s usually lies between .5 and 1.0 ns for many of the available TDs, the switching speed depends largely on the propagation delay of the differential amplifier. The bias current through the TD must therefore be selected so that the threshold current flowing into the collector of Q2 just equals $I_P - I_{BIAS}$. In other words, the bias current must be selected as large as temperature and manufacturing tolerances permit without exceeding I_P.

Since the differential amplifier need deliver only a small current and since the TD experiences only a small voltage swing, the design of the differential amplifier is limited only by stability considerations. Delay time is minimized by setting the resistances in the collector circuits of Q1 and Q2 to zero. If multiple buffers are packed onto a single card, coupling problems may arise and result in oscillation. Consequently, it may not be advisable to reduce R6 and R7 to zero since the collector resistors can supply sufficient damping to prevent instability. As an alternate to using resistors R6 and R7 to introduce damping, one can set the quiescent collector current of Q1 so that the

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1. General Electric Tunnel Diode Manual (1961) p. 44.

differential amplifier has a gain-bandwidth product less than the maximum realizable one.

The step-by-step design of the basic configuration shown in Figure 1A proceeds as follows:

1. Select the type of transistor to be used for Q1 and Q2. The choice of Q1 and Q2 depends on a compromise between the maximum switching speed of the transistor versus the component cost. Selecting a low current transistor minimizes the power supply requirements. To illustrate the design procedure, the 2N709 is selected as an example of a moderately low cost, high speed device. From the manufacturer's data sheet, one observes that at a collector current of approximately 8 ma, a current minimum exists for contours of constant gain bandwidth product. From curves of pulsed dc current gain versus collector current, one observes that the decrease from maximum current gain is less than 20 percent for currents down to 1 ma. By using the 2N709, one therefore enjoys considerable flexibility in selecting the quiescent collector current of Q1.

2. Choose a suitable TD having an $I_P \geq 1/2\ I_{C1}$. Since the quiescent collector current of Q1 can range between 1 ma to 8 ma, considerable freedom is afforded in the choice of the TD. The 1N3717 is chosen for the sake of illustration even though equally good results could be realized by using a lower current device such as the 1N3713. The 1N3717 has an absolute maximum rating of 25 ma for forward current at 25°C. Derating at 1 percent per °C for temperatures above 25°C, one can safely operate to I_{FMAX} = 12.5 ma at 75°C. The 1N3717 has a self-resonant frequency of 1.9 MHz and a resistive cutoff frequency of 3.4 MHz. This indicates a potential switching speed of 0.5 ns.

3. Select a safe value for I_1. The 1N3717 has a nominal peak current I_P = 4.7 ma at 25°C with a guaranteed spread from nominal not exceeding ±.12 ma. Examining I_P as a function of temperature and V_P, it is seen that I_P varies less than ± 10 percent for a temperature range from -40°C to +65°C for all values of V_P. Consequently, it is safe to select a value for operating point No. 1 letting

$$I_1 = (0.9)\, I_{PMIN} = 4.1 \text{ ma}$$

where $I_{PMIN} = 4.58$ ma is the guaranteed lower limit for I_P at 25°C. Since the buffer storage may not be required to operate over the range -40°C to +65°C as implied in calculating I_1, the above value of I_1, is somewhat conservative.

4. Select the positive supply voltage V(+), and calculate the value of R5. The selection of the positive supply voltage involves a compromise between dissipating low power in Q1 and choosing V(+) large enough so that the bias current through R5 is not affected greatly by the variation in voltage drop across S1 in the normally closed switch position. S1 consists of an NPN transistor operated as a saturated switch. Assuming the collector to emitter saturation voltage $V_{CE} = 0.3$ volts and negligible base current flow, one can select V(+) arbitrarily as 4.5 volts. R5 is then calculated as follows:

$$R5 \cong \frac{V(+) - V_V - V_{CE}}{I_1}$$

$$= 1 \text{ K}\Omega \pm 1 \text{ percent}$$

5. Select relative values for biasing resistors R3 and R4.

The base of Q2 should be set to provide a threshold voltage equal to half the nominal input signal voltage. Since the nominal signal input is $V_{IN} = -0.7$ volts, the voltage divider should supply the base with approximately -0.35 volts. Neglecting base current and setting the current through R4 to be 10 ma, R4 is found to be 33 Ω. Assuming V(-) at least 10 times as large as the base voltage at Q2, then

$$\frac{R3}{R4} \cong \frac{V(-)}{0.33}$$

or

$$R3 \cong \frac{33}{0.33} V = 100 \frac{\text{ohms}}{\text{volt}} \cdot V(-)$$

6. Select the negative supply voltage V(-), and calculate R2 and R3. The selection of the negative supply voltage is not critical and is usually dictated by convenience and availability of the power source. The magnitude of V(-) need only be chosen large enough to assure that the current through R2 is approximately constant. Since the emitter voltage will vary by approximately 0.35 volts when Q1 is switched off and Q2 is switched on, the emitter current will vary by approximately 3 percent for V(-) = -12 volts. Choosing V(-) as -12 volts, one can now proceed to calculate R2 and R3.

Since I_1 = 4.1 ma by step 3, Q1 can be operated at approximately 8 ma for maximum current gain and maximum gain-bandwidth product without exceeding any maximum ratings on the TD. Referring to the manufacturer's data for collector current versus base-to-emitter voltage drop at 25°C, it is seen that V_{BE} = 0.86 volts. Since R1 is returned to ground and the base current is small compared to the collector current, the emitter potential is approximately V_E = -0.86 volts. The current through R2 is therefore

$$IE \leq \frac{12 - 0.86}{R2} = 8 \text{ ma}$$

Solving for R2 and I_E, one obtains R2 = 1.5 K and I_E=7.4 ma. When Q1 is switched off and Q2 is on, the collector current of Q2 will be approximately equal to 7.2 ma.

To calculate for R3, using the results of step 5,

$$R3 = 100 \frac{\text{ohms}}{\text{volt}} \cdot 12$$

$$= 1.2 \text{ kilohms}$$

Note that the actual absolute levels of R3 and R4 are not critical. R4 need be chosen only large enough to provide some damping and R3 is then implied directly.

7. Experimentally determine values for R6 and R7. By careful layout,

it should be possible to reduce R6 and R7 to zero for maximum switching speed. However, if one is not striving for anything better than 5 ns switching speeds, it generally pays to let R6 and R7 be equal to about 100 Ω.

8. Select a comparison voltage for the differential comparator. In a practical design, the voltage drop across the tunnel diode is not observed directly. Instead, the state of the tunnel diode is observed by comparing the voltage at the junction of the TD and resistor R5 with a fixed reference voltage V_{REF}. Let $V_{REF} = V(+) - V1 - (V_2 - V_1)/2$

$$= 4.5 - 0.65 - (.51 - 065)/2$$

$$= 4.2 \text{ volts.}$$

In a practical buffer incorporating decoupling, the important parameter will be $V(+) - V_{REF} = 0.3$ volts.

DESIGN OF AN UNSTROBED-INPUT, STROBED-OUTPUT BUFFER STORAGE UNIT

The basic design configuration described in the previous section can be incorporated with minor changes into a practical 8-channel buffer storage unit (BSU) organized as shown in Figure 2A. The BSU is packaged in a standard Nuclear Instrumentation Module.[2] Since the NIM System provides ± 12 vdc, there is no problem of compatibility with power supplies. It is convenient to use the +12 volt supply for the comparator and for the reset switch driver. The 4.5 volt power supply is derived from the +12 volt supply. Finally, the -12 volt supply is compatible with the selection of V(-).

The basic configuration shown in Figure 1A undergoes several minor modifications when incorporated into the 8-channel BSU shown in Figure 2B. The component numbering system is changed for convenience. Components associated with the +4.5 volt power supply, the reset circuit, and the output gate are labeled sequentially beginning at 1. However, components unique to channel 1 are labeled from 101. For example, R203 refers to

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2. Standard Nuclear Instrument Modules , TID-20893 (Rev. 2), United States Atomic Energy Commission (Jan. 1968) Prepared by Louis Costrell, NBS.

resistor R3 of channel 2. Since extra components have been added in the 8-channel BSU, the correspondence between component numbers in Figure 1A and those in Figure 2B breaks down quickly. However, the component values determined for the basic configuration are incorporated without change. Since channels No. 1 through No. 8 incorporate the same elements, the description will consider only channel No. 1.

Input No. 1 is terminated by R101 and the base of Q101 to present a 50 Ω impedance to the signal input. It is assumed that careful layout has obviated the need for damping resistors in the collector circuits of Q101 and Q102. Since the +4.5 volt power supply is now shared by several channels, it is necessary to incorporate the decoupling network consisting of R107 and C101 to avoid interaction through the power supply. The flow of collector current into Q1 plus bias current through R105 results in a voltage drop across R107 equal to

$$V = (I_{C1} + I_{BIAS})\ (R107)$$

$$= (7.4 + 4.0)\ (18)\ MV$$

$$= 0.2 \text{ volt}$$

Therefore V(+) is now only 4.3 volts rather than the 4.5 volts selected previously. An individual resistive divider network consisting of R108 and R109 is used to derive the reference voltage for the comparator. R108 and R109 are chosen so that $V(+) - V_{REF} = 0.3$ as before. Small shifts in the voltage level of the +4.5 volt power supply are unimportant since the nominal +4.5 volts, V(+), and V_{REF} all vary in direct proportion.

The comparator A101 consists of an integrated circuit such as the RCA type CA3000 differential amplifier. The pin numbers indicated refer to the CA3000. The positive voltage for A101 is derived from the +12 volt supply through a decoupling network consisting of R110 and C102. When tunnel diode CR101 is in state No. 1 ($I_i = 4.0$ ma and $V_1 = .065$ volt), the output voltage of A101 is approximately +12 volts. After switching to state No. 3, the output of A101 is approximately 4 volts.

A level shifter is provided following the comparator to provide a voltage level of 0 volts corresponding to a ZERO logic level and a positive voltage corresponding to a ONE logic level. The level shifter built around Q103 incorporates R114 in the emitter circuit to limit output current to 10 ma. Thus, if the load consists of a 510 Ω resistor to ground, the ONE logic level will be +5.1 volts.

The 8-channel BSU shares the following circuits shown in Figure 3:

(1) A 4.5 volt power supply
(2) A reset circuit
(3) An output gate

These will be described in the order listed.

The +4.5 volt power supply is derived directly from the +12 volt supply using a voltage divider and emitter follower. The voltage divider incorporates CR1 to compensate for temperature variation and potentiometer R2 for minor adjustment of the voltage applied to the base of Q1. Therefore, the output voltage of the nominal +4.5 volt supply can be varied over a ±5 percent range to set the desired voltage and, correspondingly, the bias current through R5A. Resistors R4 and R5 limit the maximum dc current supplied by Q1 and reduces the heat dissipation of the transistor.

The reset switch transistor Q3 is controlled by the voltage applied through a diode "OR" gate containing CR2 and CR3. When a positive control voltage is applied at either CR2 or CR3, diode CR4 is back biased and base current can flow into Q2. Transistor Q2 saturates and Q3 is therefore cut off. In the absence of a positive control signal, Q2 is cut off and Q3 is saturated. Q3 need handle only 33 ma.

The functioning of the output gating circuit is similar to that of the reset circuit except that the gating transistor Q5 is a PNP device. To gate the output current into the load, a positive signal is applied to either CR7 or CR8. CR8 is then back biased so that current flows into the base of Q4. Consequently, base current is also drawn from Q5 which acts as a saturated switch. By successively strobing a string of BSU's, 8-bit words may be multiplexed onto an 8-line data bus.

DESIGN OF A STROBED INPUT BUFFER USING A SHUNT GATE

The basic channel shown in Figure 2B can be modified by adding a shunt switch between the collector and emitter of Q101. If the switch is closed, current flow to R102 through the switch will keep Q102 cut off independent of the signal input applied to the base of Q101. The shunt switch is implemented as shown in Figures 4A and 4B by adding the gating transistor Q104. The strobe input is terminated by a single 51 Ω resistor, R16, shared by all eight channels. To prevent possible interactions which could lead to high-frequency oscillations, R115 is inserted in series with the base of Q104 to provide some damping. In normal operation, a nominal -0.7 volt signal must be applied to both the strobe input and the signal input to turn on Q102. If either the strobe or signal input is zero, Q102 will remain cut off. A switch S1 is provided to cut off Q104 so that the strobe feature is disabled. When S1 is closed, the BSU functions as a simple buffer like that shown in Figure 2B.

STABILITY PROBLEMS

When the buffer storage unit contains only a single channel, there is no great difficulty in achieving switching speeds of 2 ns even for rather poor physical layouts. However, considerable care is required to realize the full potential in terms of high switching speed and reliable operation when multiple channels are packaged together. Only a few general rules can be presented as follows:

1. Minimize lead lengths, especially in the portions of the circuit connecting to Q X01, Q X02 and Q X03 (X = 1, 2 - - - - 8).

2. Avoid interactions through portions of the BSU shared in common by all channels. Make liberal use of decoupling circuits. Use individual voltage dividers and current dividers.

3. Use a grounding system incorporating a ground plane.

4. Incorporate damping by inserting resistors in the base and collector circuits.

5. If at first you don't succeed, check that proper attention has been paid to suggestions 1 through 4.

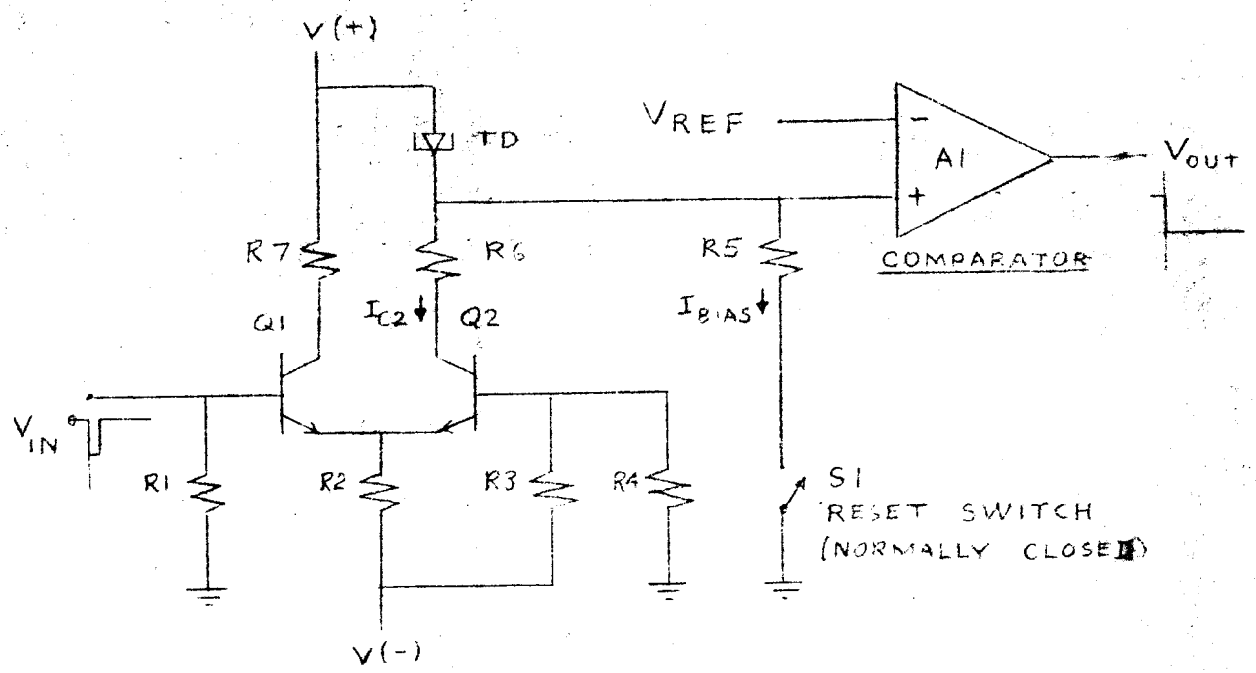

FIGURE 1A. BASIC CONFIGURATION OF TUNNEL DIODE MEMORY CELL

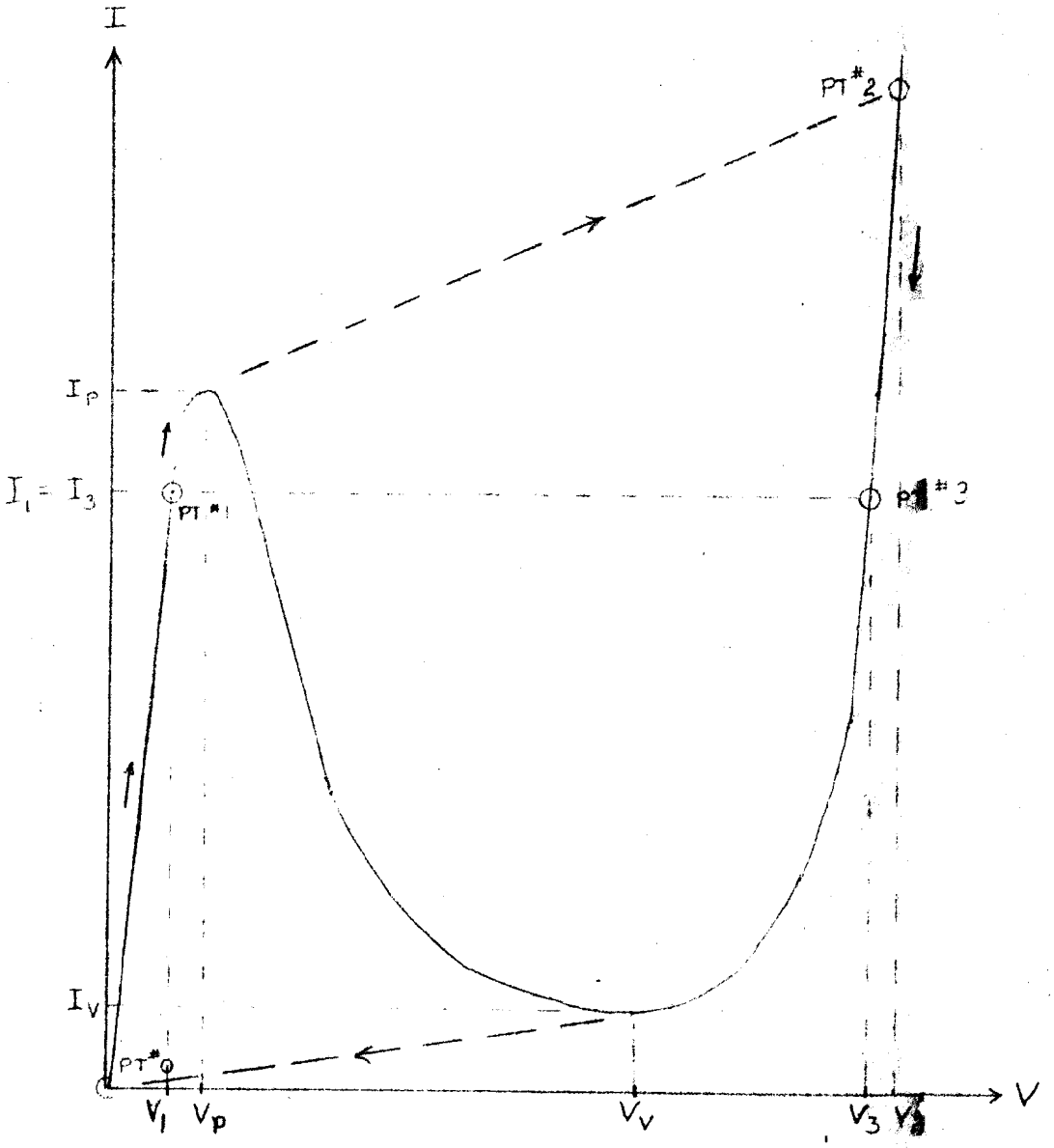

FIGURE 13. CURRENT VERSUS VOLTAGE CHARACTER OF TYPICAL GERMANIUM TUNNEL DIODE SHOWING CHANGE IN OPERATING POINT

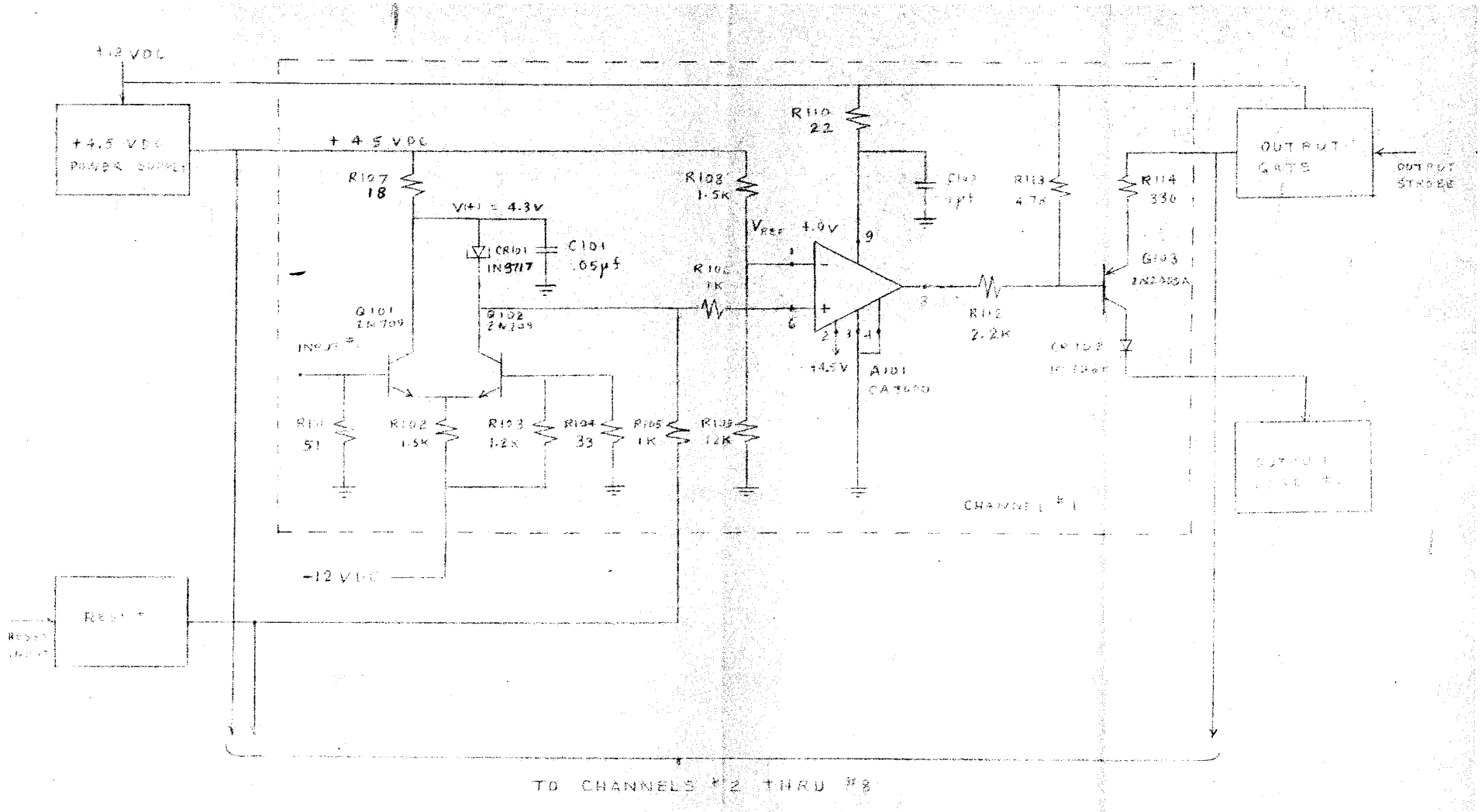

FIGURE 2.5 . CIRCUIT DIAGRAM OF BSU CHANNEL #1

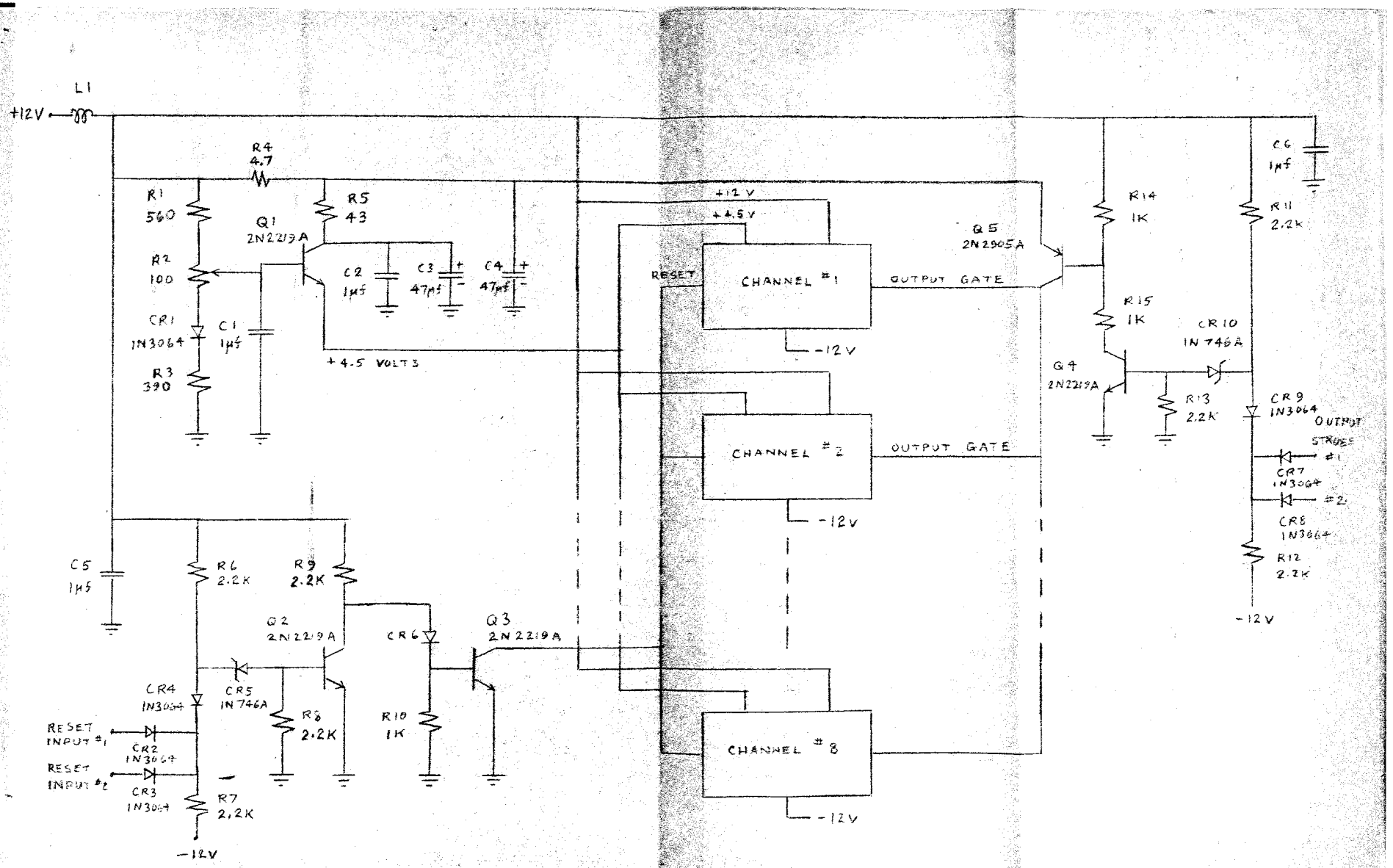

FIGURE 3. POWER SUPPLY, RESET CIRCUIT AND OUTPUT GATE

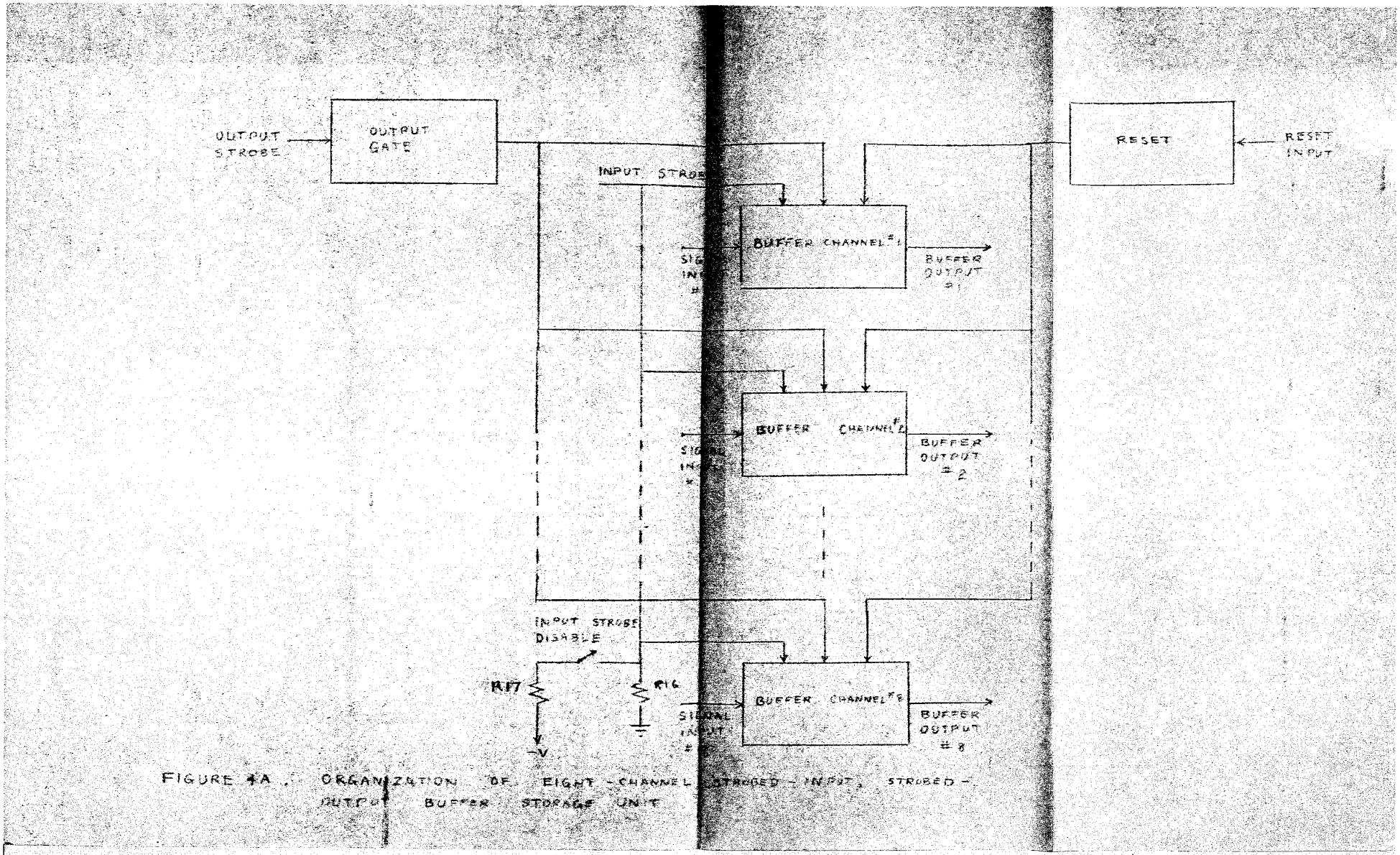

FIGURE 4A. ORGANIZATION OF EIGHT-CHANNEL STROBED-INPUT, STROBED-OUTPUT BUFFER STORAGE UNIT

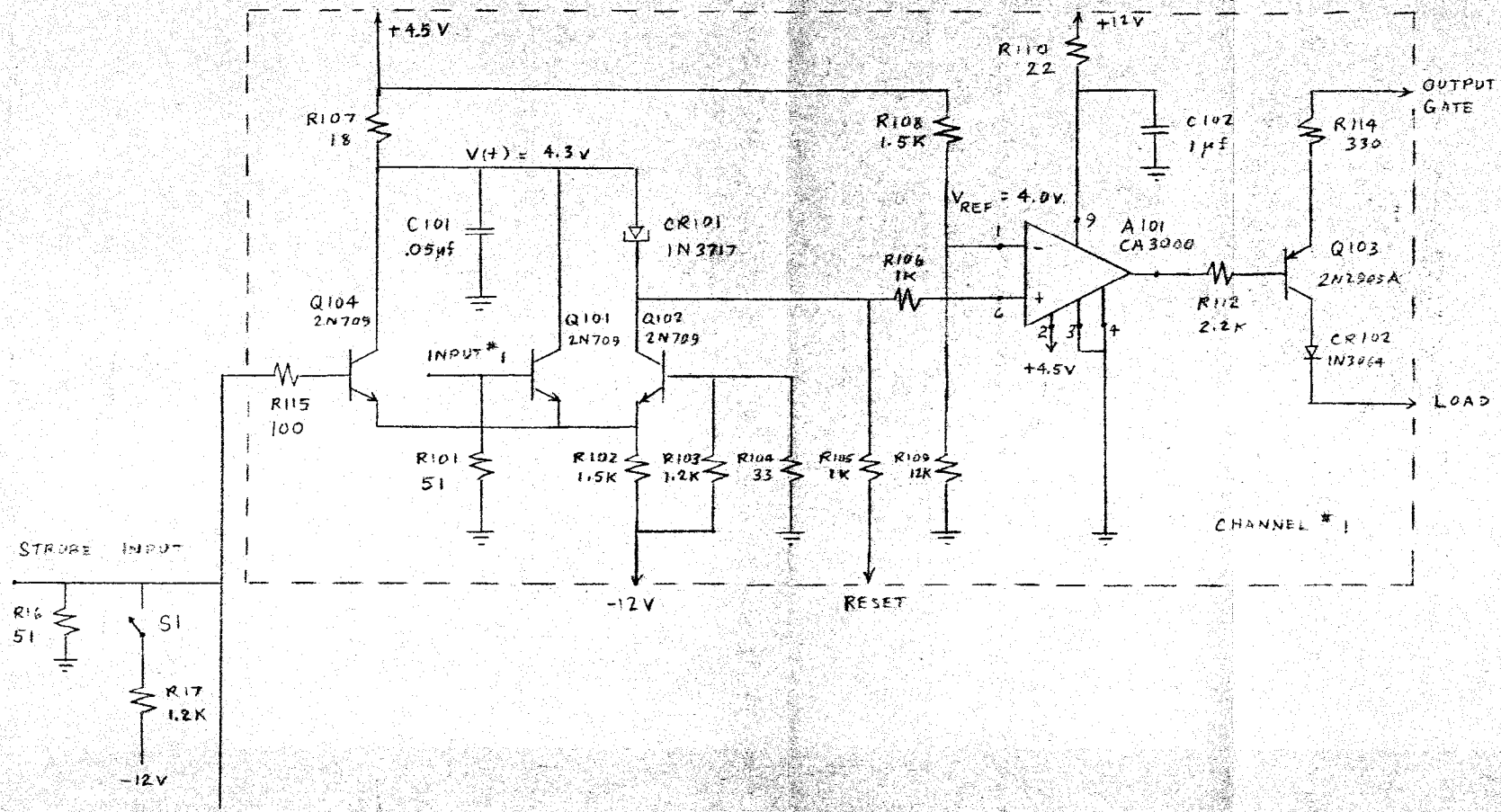

FIGURE 48. CIRCUIT DIAGRAM OF B3U CHANNEL #1