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SEVEN-BIT ANALOG-TO-DIGITAL CONVERTER FOR NANOSECOND PULSES*

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ABSTRACT

The time integral of nanosecond pulses is digitized with a linearity, resolution and stability $< 1\%$. The sensitivity of the circuit is 1.2 pCoul/count. The circuit can also be utilized for measurement of short time intervals. In this mode its sensitivity, for standard logic pulses (- 0.7 volts), is ~ 80 ps/count.

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I. Introduction

The availability of digital computers for high-energy physics experiments generates the demand for interface circuitry between the experimental apparatus and the computer. Digital data are commonly pre-processed in fast logic blocks, and their rate is reduced considerably before being sent to the computer. The problem in such a case reduces to matching pulse shapes at the interface. However, analog signals of nanosecond duration require either linear time scaling (stretching) or a fast A-D converter, since computers cannot as yet accept such signals directly.

A K_2^o experiment[1] is being built up in which two analog-type data of nanosecond and sub-nanosecond duration have to be measured: (a) pulse height information from 66 shower counters to measure γ-ray energies. (b) Time-of-flight analysis for particle identification.

The circuit described below is capable of performing either function. Its specifications are:

Data Input:	- 150 pCoul, max. (e.g., - 15 mA, 10 nsec pulse); input impedance 50 ohms.
Gate Input:	- 0.7 volts into 50 ohms, i.e., standard NIM logic ONE. Minimum duration 4 nsec.
Linearity:	Better than 1%, integral.
Resolution:	> 7 binary bits.
Analog Output (PHA):	Delivers a negative pulse proportional to the time integral of the input signal and matching input characteristics of pulse-height analyzers. Rise time (10 to 90%) = 0.6 μs, Decay time constant (to 1/e) = 3.2 μs.

Digital Outputs:	(a) "SCALER". Delivers number of pulses (at 10 MHz rate) proportional to the time integral of the input signal. Output is - 0.2 volts into 50 ohms, nominal.
	(b) Delivers + 4 volts (logic "1") into 100 ohms. Outputs can be 'OR'-ed on 8 data bus lines for manual or computer sequential read-out of several ADC's.
Overflow:	Eighths bit available when data exceed 127 counts. Circuit limits around 160 counts.
Output Strobe:	+ 4 volts into 2.7 K, pulse or level. Enables data to be presented on the data bus lines as long as STROBE is ON.
Visual Indicators:	(a) DATA pilot light shows when data are present on weights 2^2 through 2^6.
	(b) OVERFLOW pilot light indicates that counts exceed 127.

Reset and timing functions are provided by one control circuit capable of serving 11 ADC's (see Section II).

II. Circuit Description

Figure 1 shows a block diagram of the analog-to-digital converter (ADC). Transistor numbers in the blocks identify the relevant components also shown in greater detail in the circuit diagrams, Fig. 2 through Fig. 5. The operation of the instrument will be described with help of Fig. 1 and the timing diagram of Fig. 6.

An input pulse, such as from a fast photomultiplier, applied to the grounded-base stage, Q1, will pass to the amplifier-integrator, provided it is coincident in time with a gate signal. The linear gate is of the matched-quad type and is driven from the gate amplifier Q2 through Q5. The subsequent stages, Q6 through Q11 are used for quasi-integration and amplification of the signal. AC coupling has been used throughout since the instrument was designed to serve in experiments at the Stanford Linear Accelerator Center (SLAC), whose short beam pulse of 1.6 μs together with a 360 pps repetition rate exclude any possibilities of pile-up. The amplifier-integrator could thus be designed for good noise rejection at low frequencies in addition to the usual high-frequency noise rejection due to integration. Q12 and Q13 are a feedback pair delivering a negative pulse, Fig. 6(a), whose characteristics match the input requirements of several commercially available pulse-height analyzers (PHA). This output facilitates monitoring selected channels during an experiment that involves a number of ADC's, and aids in adjusting to zero the gate pedestal.

The peak detector utilizes a differential amplifier Q14, Q15 which controls a current source Q17, Q18 to charge a capacitor (C45) to the peak value of the integrated pulse. The signal appearing at the input of the peak detector (Q14A) has a rise time of 2.0 μsec (10 to 90%), and a decay time constant of 6.0 μsec, Fig. 6(b). The finite response time of the peak detector would result in a non-linear relationship of input charge versus number of counts, had the pulse not been slowed down prior to peak detection. Q41 exhibits sharp cut-off characteristics to limit the signal amplitude to 4.6 volts, and protects the gate-source junctions of Q14 and the base-emitter junctions of Q15. Q14 is a matched pair of FET's; the gate of Q14B presents a high impedance across C45 permitting the peak value of the integrated pulse to be kept for relatively long time intervals with little loss of amplitude. The present circuit has a time constant of 5 ms.

(Time constants of the order of 1 sec are possible with minor modifications and may be of use where a considerable number of analog data is multiplexed into one A to D converter.) Current source Q18 charges C45 as long as the output of the peak detector is lower than the input signal to the differential amplifier Q14, Q15. Otherwise it is turned off, and between incoming data it is also clamped to prevent its accidental actuation by noise.

C45 is kept fully charged for a duration of approximately 15 μsec determined by the monostable Z51 and the "Sample" flip-flop F1. This allows for the signal at the gate of Q14A to decay completely before analog-to-digital conversion is initiated.

The analog-to-digital conversion is of the capacitor-discharge type. Briefly, the comparator, A1, senses the voltage across C45 and assumes a logic ONE state when $V_{C45} > V_{REF}$. After some delay of 15 μsec, this state actuates the current discharge source Q19 through Q23 which discharges linearly C45 resulting in the waveform as in Fig. 6(c).

A more detailed description follows: the output from the comparator (Q26, Q27, A1) is as shown in Fig. 6(d). For $V_{C45} \leq V_{REF}$, the output is - 0.7 volts. When $V_{C45} > V_{REF}$, it rises to about 0 volts and cannot rise further due to the action of the SAMPLE flip-flop, F1, which inhibits the comparator output for 15 μsec. A logic ONE from F1 permits the output to rise to + 6 volts, enabling G4 and thus allowing the 10 MHz clock signal to be applied to the 8-bit binary counter composed of two integrated circuits A5 and A6. When $V_{C45} \leq V_{REF}$, the comparator returns to its ZERO state, inhibiting further clock pulses from arriving at the 8-bit counter, and turning off the discharge current source. The trailing edge of the comparator output resets the SAMPLE flip-flop which in turn disables the comparator. It also actuates the CLAMP flip-flop which clamps

C45 via Q25 to a slightly negative potential, see Fig. 6(c), and relaxes tolerances on leakage currents which may build up a charge on C45 between signals.

The clamp on C45 is released approximately 1 μsec after receipt of new data. C45 is thus protected from noise in the time interval when the environmental noise is highest, e.g., due to spark chambers or other pulsed apparatus.

The digital information, stored in the binary counter, is strobed out via NAND gates G9 - G16. The output amplifiers Q33 - Q40 can deliver 40 mA into 100 ohm transmission lines. The SCALER output delivers a number of pulses proportional to the time integral of the input signal and can be used for monitoring selected channels or for calibration of the instruments when a computer is not available.

One pilot light provides visual indication of overflow conditions, (2^7-th bit), the other is actuated by an OR circuit of weights 2^2 - 2^6 to indicate that DATA are available.

RESET can be accomplished in three ways:

(a) Push-button reset required when the equipment is energized.

(b) External reset, requiring a positive pulse of 70 nsec and 3.5 volts, minimum.

(c) Internal reset. In this mode one preserves the digital information in the binary counter until arrival of a new event. The gate signal, allowing this event to be measured, is utilized to produce a reset pulse. Thus the digital part of the circuit is reset whilst the analog signal is being processed. In the experiment under consideration (see Section I) a spark chamber is actuated whenever an event is recognized by fast logic circuitry. It is important, therefore, to protect against noise

those circuits that are located in the proximity of spark chambers. Such problems are typical in an experimental situation. Q69 - Q71 generate a 1 μsec reset signal which keeps all bistable circuit elements in the OFF state well after the spark chamber noise has decayed.

The 1 μsec monostable also releases the clamping action on C45 and on the peak detector via the CLAMP flip-flop, F2, and via swtiches Q16 and Q25. Thus the clamp is released 1 μsec after receipt of new data and actuated immediately after completion of the analog-to-digital conversion, Fig. 6(e).

It was stated earlier that the SAMPLE and CLAMP flip-flops are reset by the trailing edge of the comparator output. However, an experimental situation is likely where some ADC channels did not receive data, though an event has been recorded which initiates the unclamping of C45, etc. In such a case no trailing edge is available from the comparator for resetting the SAMPLE and CLAMP flip-flops. Gates G5 - G7 sense such situations and generate the requisite reset signal typically within 90 nsec.

The circuit shown above the dashed line of Fig. 1 (details in Figs. 2 and 3) was packaged in a standard AEC No. 1 module. The circuit containing some 330 components, including transistors and integrated circuits, was constructed using printed-board techniques. The part of the circuit shown below the dashed line of Fig. 1 (details in Figs. 4 and 5) provides control functions and was constructed similarly. A standard AEC nuclear instrumentation chassis can thus hold one control module providing the functions of gating, clock and timing for eleven measuring modules. Power is obtained from a supply, model AEC-320-3 and an auxiliary source of + 5.5 volts for the integrated circuits. In larger systems it is convenient to supply the pilot lamps from an unregulated source.

A study was made of two different ways to multiplex the analog information for conversion into digital form. The time constant at the peak detector can be lengthened by increase of R90, C45 and the charging current in Q17, Q18. A fast analog-to-digital converter can then be used for 100 channels or more in a multiplexing scheme. One multiplexing arrangement studied involves the use of analog switches. The other solution utilizes the binary states at the output of a comparator to monitor whether C45 has been fully discharged, indicating that the analog-to-digital conversion has been completed.

III. Results

Figure 8 shows the number of counts versus input amplitude for pulses of 10 nsec duration. The maximum input amplitude for 1% linearity is - 0.7 volts, however the useful range is up to - 1.1 volts at which point the sharp cut-off characteristics of the limiter (Q41) take over.

The circuit can be utilized for measurements of sub-nanosecond time intervals such as in time-of-flight analysis. In this mode one applies a signal of standard amplitude and duration to the DATA terminal of the instrument. This input stage together with its linear gate form an "overlap-coincidence" circuit, the output of which is then integrated and digitized. Figure 9 shows results obtained by moving the GATE signal in time with respect to the DATA input signal. The observed slope of 12.6 counts/nsec can be changed by altering the input amplitude of the DATA signal or the gain of the amplifier.

A small system of 10 measuring modules and one control module was built and operated reliably. The system under construction utilizes sixty-six instruments which are multiplexed, together with other data, into a PDP-9 computer.

ACKNOWLEDGMENTS

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REFERENCE

1. Measurements of the magnitude of η_{00} and its phase relative to η_{+-}. D. Dorfan, M. Schwartz, and S. Wojcicki, SLAC Proposal No. 31, Stanford Linear Accelerator Center, Stanford University, Stanford, California, (October, 1967) unpublished.

FIGURE CAPTIONS

1. Analog-to-digital converter for nanosecond pulses. Block diagram.
2. Linear gate and amplifier-integrator.
3. Peak detector, ADC and output stages.
4. Control circuit. Gate fan-out.
5. Control circuit. Clock, timing and reset.
6. Waveforms and timing signals. Horizontal scale: 3μsec/cm. Vertical scale (a), (b) and (c): 0.5 V/cm; (d) and (e): 2V/cm.
   (a) Output at PHA
   (b) Input to peak detector
   (c) Waveform at C45. The flat portion represents the peak detector output. The trailing edge is due to the discharge current source. Note the negative step at 0 volts caused by the clamp.
   (d) Comparator output
   (e) Clamp signal
7. (a) Analog-to-digital converter
   (b) Control module
8. Number of counts versus input amplitude. Input pulse: 10 nsec, rise and fall time = 1 nsec.
9. Number of counts versus overlap-coincidence of DATA and GATE. Both signals are of 11 nsec duration, - 0.7 volts amplitude.

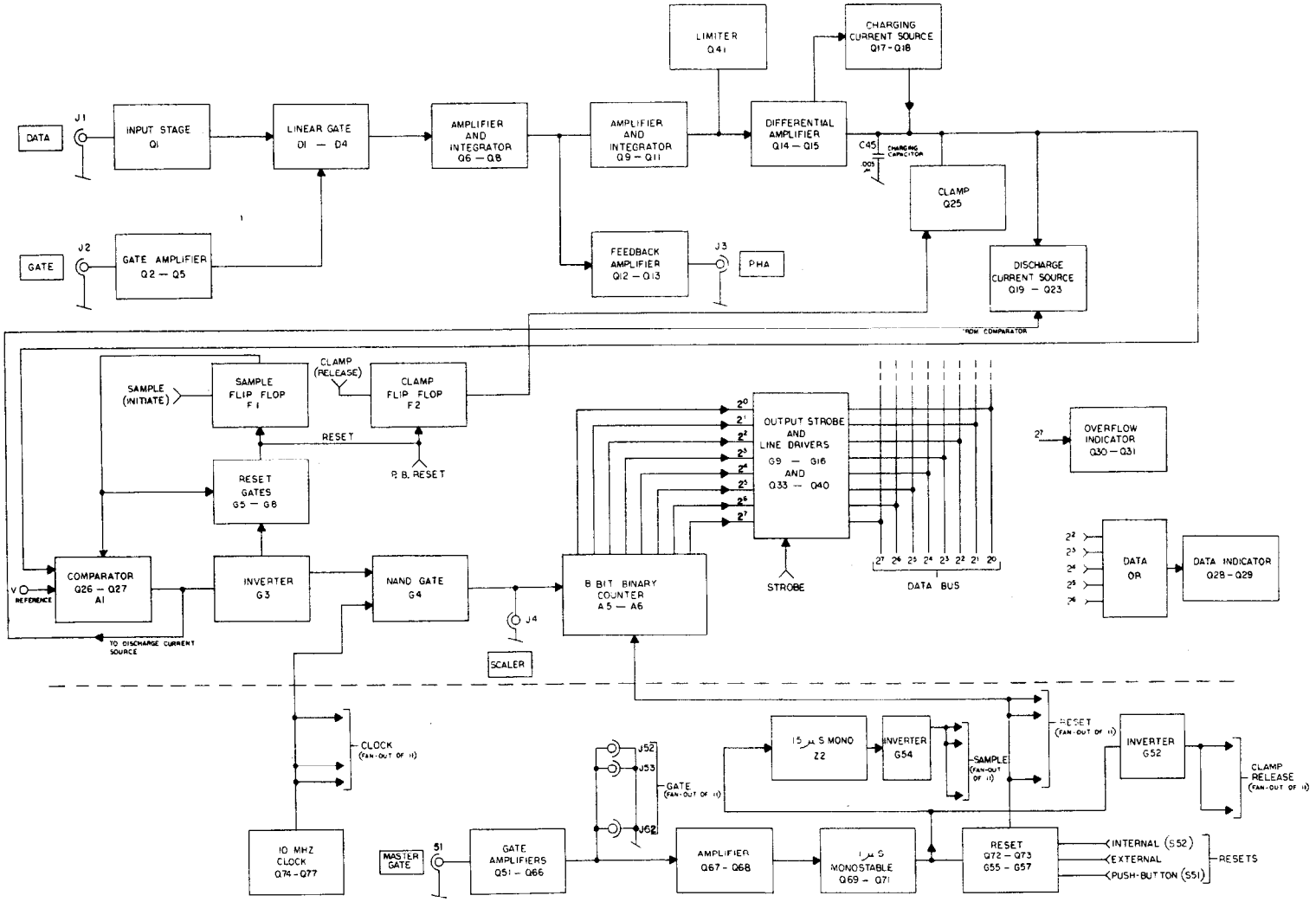
DATA
J1
INPUT STAGE Q1
LINEAR GATE D1 – D4
AMPLIFIER AND INTEGRATOR Q6 – Q8
AMPLIFIER AND INTEGRATOR Q9 – Q11
LIMITER Q41
DIFFERENTIAL AMPLIFIER Q14 – Q15
CHARGING CURRENT SOURCE Q17 – Q18
C45
CHARGING CAPACITOR
Q25
CLAMP Q25
GATE
J2
GATE AMPLIFIER Q2 – Q5
FEEDBACK AMPLIFIER Q12 – Q13
J3
PHA
DISCHARGE CURRENT SOURCE Q19 – Q23
FROM COMPARATOR
SAMPLE (INITIATE)
SAMPLE FLIP FLOP F1
CLAMP (RELEASE)
CLAMP FLIP FLOP F2
RESET
P.B. RESET
RESET GATES G5 – G8
OUTPUT STROBE AND LINE DRIVERS G9 – G16 AND Q33 – Q40
STROBE
DATA BUS
OVERFLOW INDICATOR Q30 – Q31
DATA OR
DATA INDICATOR Q28 – Q29
V REFERENCE
COMPARATOR Q26 – Q27 A1
INVERTER G3
NAND GATE G4
TO DISCHARGE CURRENT SOURCE
J4
SCALER
8 BIT BINARY COUNTER A5 – A6
CLOCK (FAN-OUT OF 11)
10 MHZ CLOCK Q74 – Q77
MASTER GATE
J1
GATE AMPLIFIERS Q51 – Q66
J52
J53
J62
GATE (FAN-OUT OF 11)
AMPLIFIER Q67 – Q68
MONOSTABLE Q69 – Q71
RESET Q72 – Q73 G55 – G57
INTERNAL (S52)
EXTERNAL
PUSH-BUTTON (S51)
RESETS
SAMPLE (FAN-OUT OF 11)
INVERTER G54
RESET (FAN-OUT OF 11)
INVERTER G52
CLAMP RELEASE (FAN-OUT OF 11)

Fig. 1

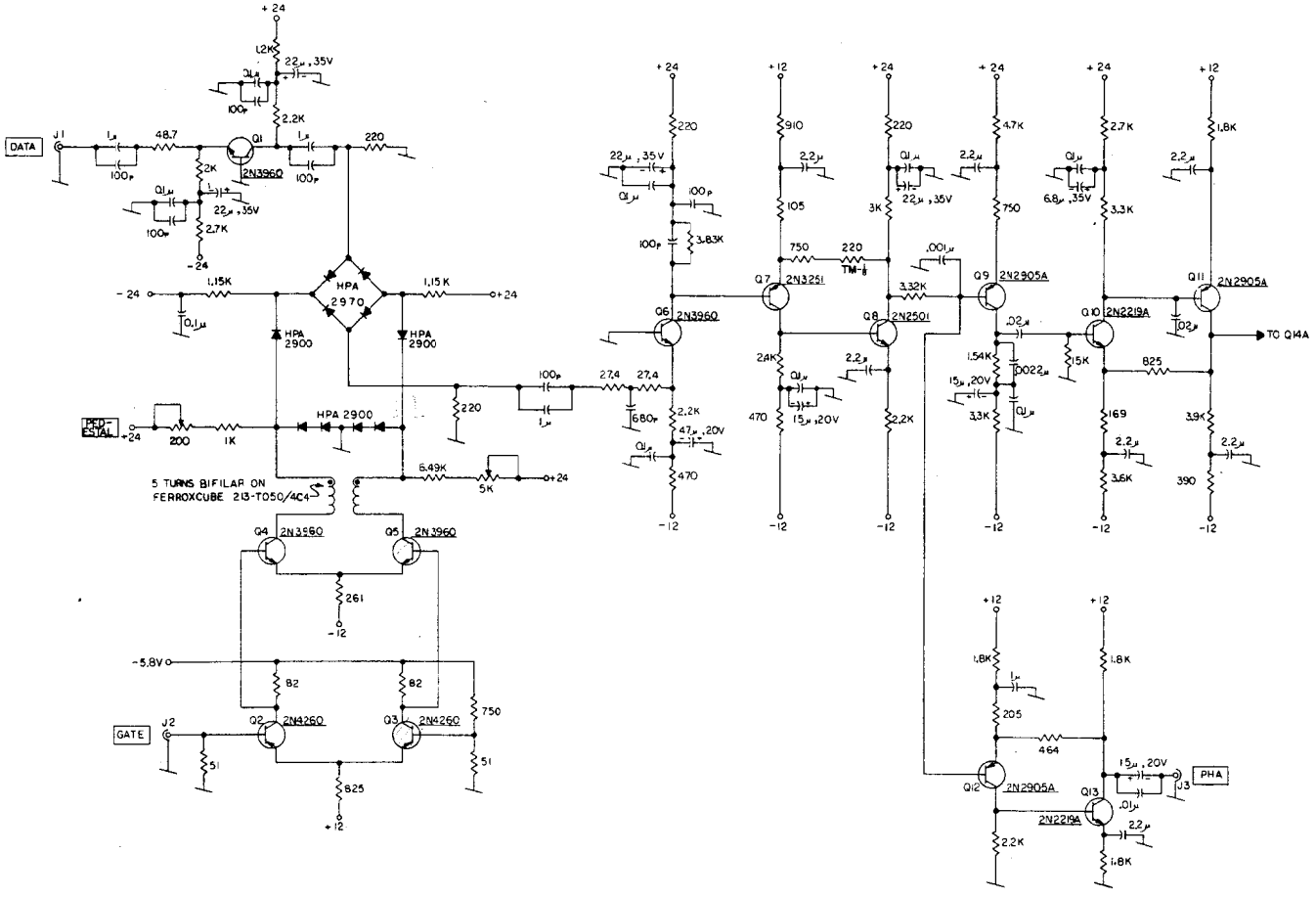
DATA
J1
Q1
2N3960
HPA 2970
HPA 2900
HPA 2900
HPA 2900
HPA 2900
PRF-EXT
J2
GATE
5 TURNS BIFILAR ON FERROXCUBE 213-T050/4C4
Q4 2N3960
Q5 2N3960
Q2 2N4250
Q3 2N4250
Q6 2N3960
Q7 2N3251
Q8 2N2501
Q9 2N2905A
Q10 2N2219A
Q11 2N2905A
Q12 2N2905A
Q13 2N2219A
TO Q14A
PHA
J3
+24
-24
+12
-12
-5.8V

Fig. 2

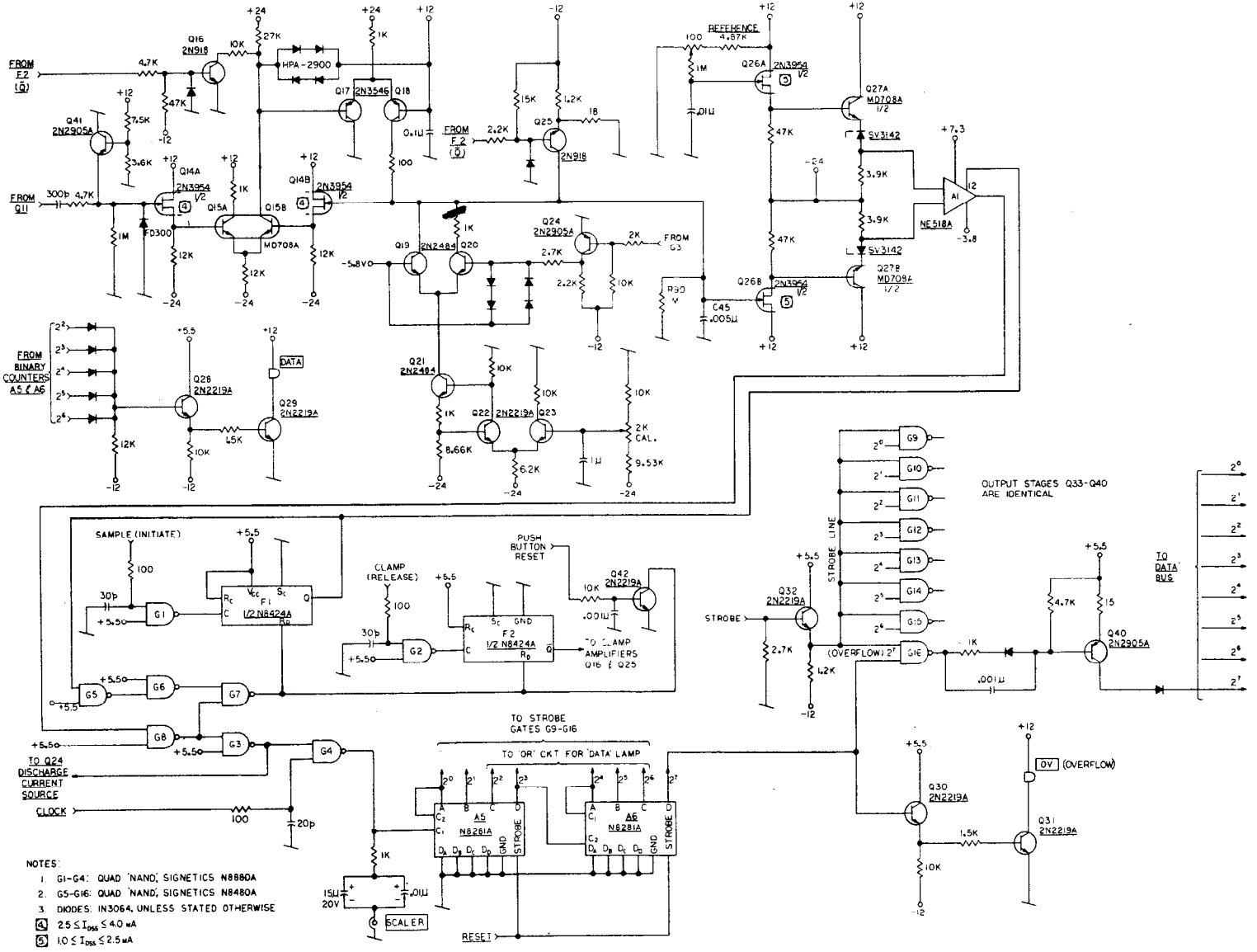
FROM F2 (Q)
FROM Q11
FROM BINARY COUNTERS A5 & A6
FROM F2 (Q̄)
FROM Q3
REFERENCE 4.87K
OUTPUT STAGES Q33-Q40 ARE IDENTICAL
STROBE LINE
TO DATA BUS
SAMPLE (INITIATE)
CLAMP (RELEASE)
PUSH BUTTON RESET
"TO" CLAMP AMPLIFIERS Q16 & Q25
TO Q24 DISCHARGE CURRENT SOURCE
CLOCK
TO STROBE GATES G9-G16
TO 'OR' CKT FOR 'DATA' LAMP
STROBE
(OVERFLOW) 2⁷
OV (OVERFLOW)
SCALER
RESET
NOTES:
1. G1-G4: QUAD 'NAND', SIGNETICS N8880A
2. G5-G16: QUAD 'NAND', SIGNETICS N8480A
3. DIODES: IN3064, UNLESS STATED OTHERWISE
4. 2.5 ≤ I_DSS ≤ 4.0 mA
5. 1.0 ≤ I_DSS ≤ 2.5 mA

Fig. 3

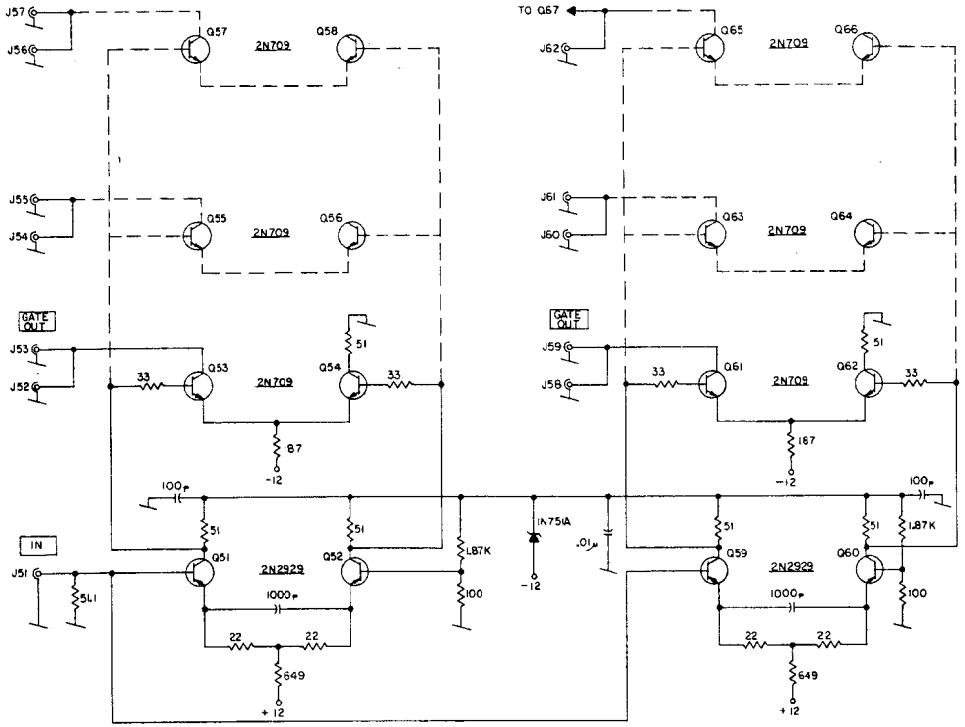
J57
J56
Q57
2N709
Q58
TO Q67
J62
Q65
2N709
Q66
CIRCUITS FOR Q55 – Q58
AND Q63 – Q66
ARE IDENTICAL TO
Q53 – Q54
J55
J54
Q55
2N709
Q56
J61
J60
Q63
2N709
Q64
GATE OUT
J53
J52
33
Q53
2N709
Q54
33
51
87
-12
GATE OUT
J59
J58
33
Q61
2N709
Q62
33
51
187
-12
100p
51
51
1.87K
IN
J51
Q51
2N2929
Q52
1.87K
100
1N751A
.01µ
Q59
2N2929
Q60
100
5.1
1000p
22
22
649
+12
1000p
22
22
649
+12

Fig. 4

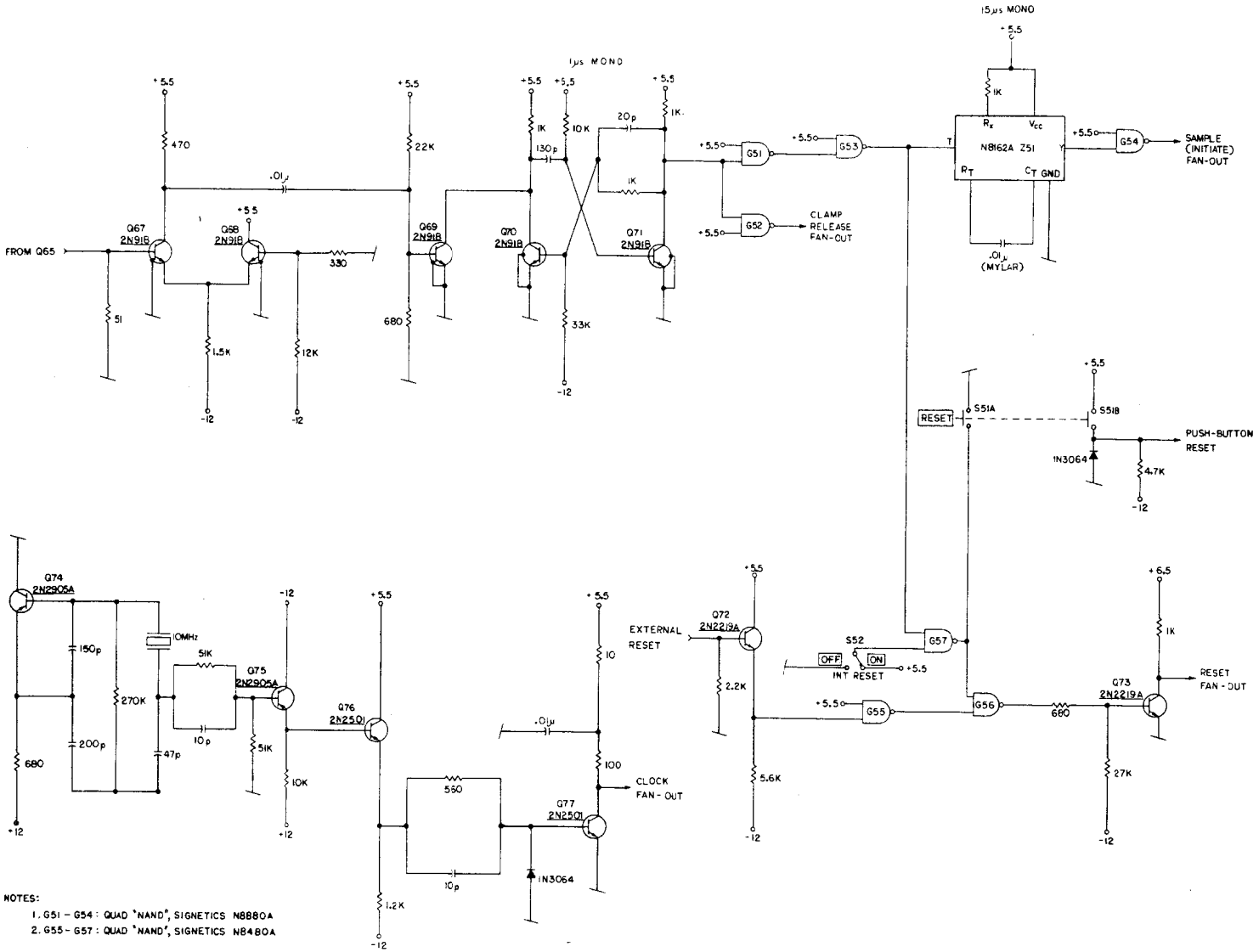
1µs MONO
15µs MONO
+5.5
470
.01µ
Q67 2N918
Q68 2N918
FROM Q65
330
51
1.5K
12K
-12
22K
Q69 2N918
680
IK
10K
130p
20p
1K
Q70 2N918
Q71 2N918
33K
G51
G52
G53
CLAMP RELEASE FAN-OUT
N8162A Z51
R_x
V_{cc}
R_T
C_T GND
.01µ (MYLAR)
G54
SAMPLE (INITIATE) FAN-OUT
RESET
S51A
S51B
PUSH-BUTTON RESET
IN3064
4.7K
Q74 2N2905A
150p
270K
200p
47p
10MHz
51K
10p
Q75 2N2905A
Q76 2N2501
10K
560
1.2K
10
.01µ
100
CLOCK FAN-OUT
Q77 2N2501
IN3064
EXTERNAL RESET
Q72 2N2219A
2.2K
5.6K
S52
OFF
ON
INT RESET
G55
G56
G57
680
Q73 2N2219A
27K
+6.5
RESET FAN-OUT
NOTES:
1. G51 – G54 : QUAD 'NAND', SIGNETICS N8880A
2. G55 – G57 : QUAD 'NAND', SIGNETICS N8480A

Fig. 5

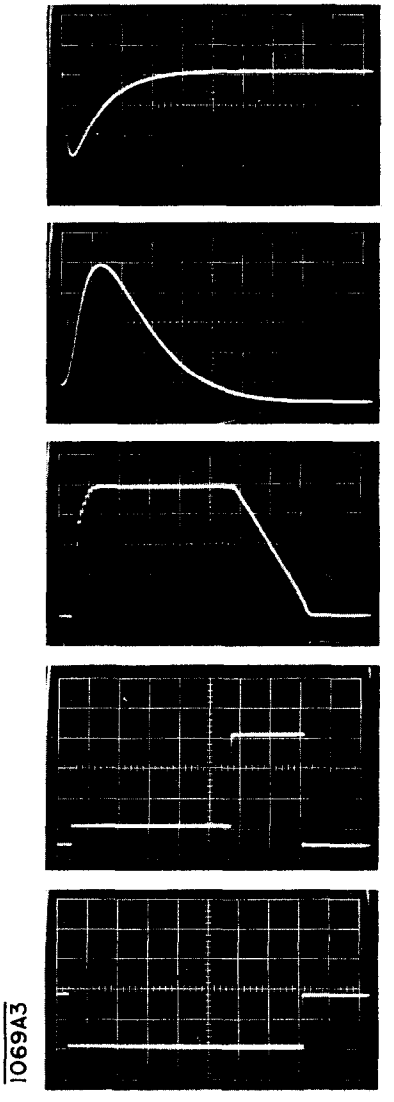

Fig. 6

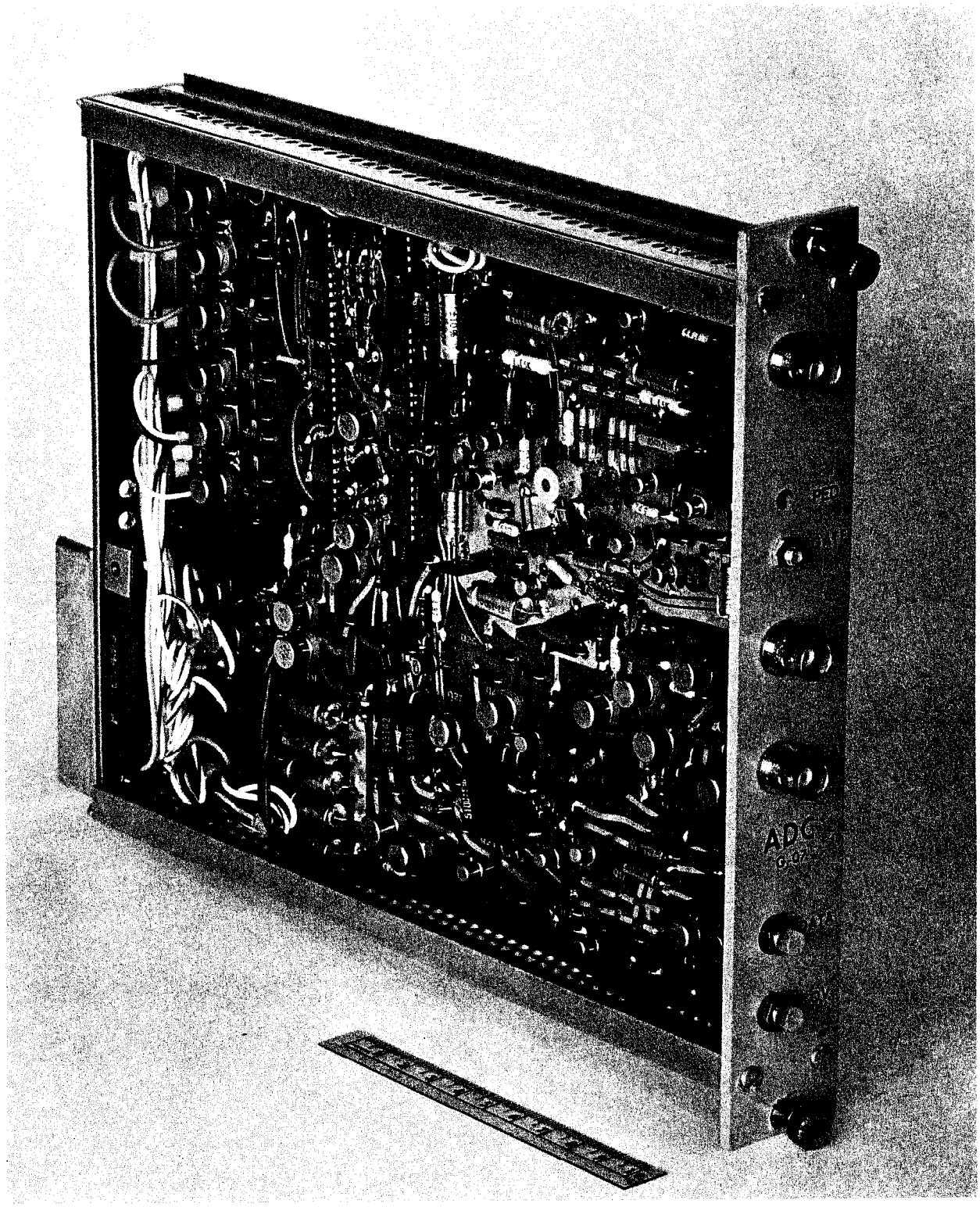

Fig. 7a

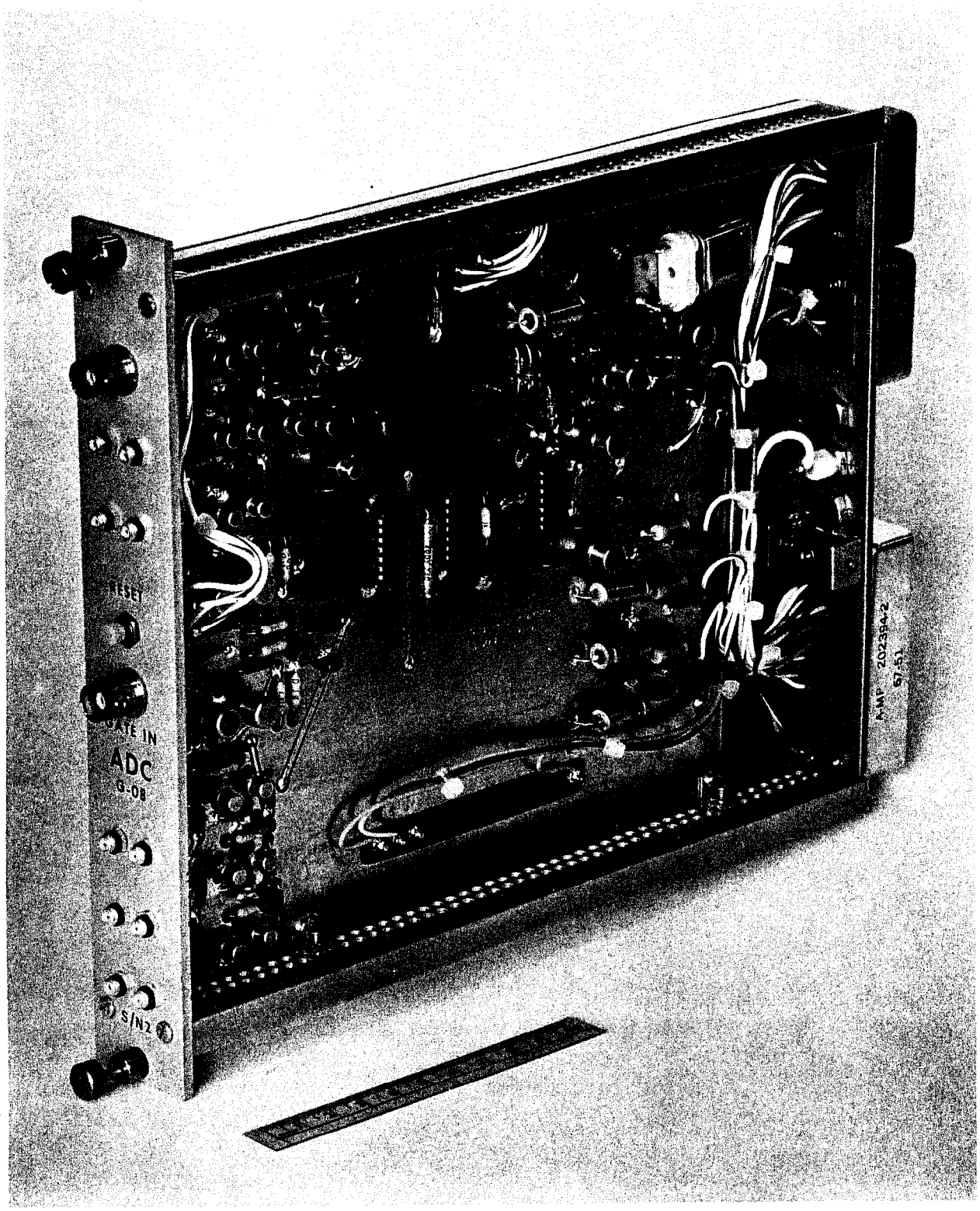

Fig. 7b

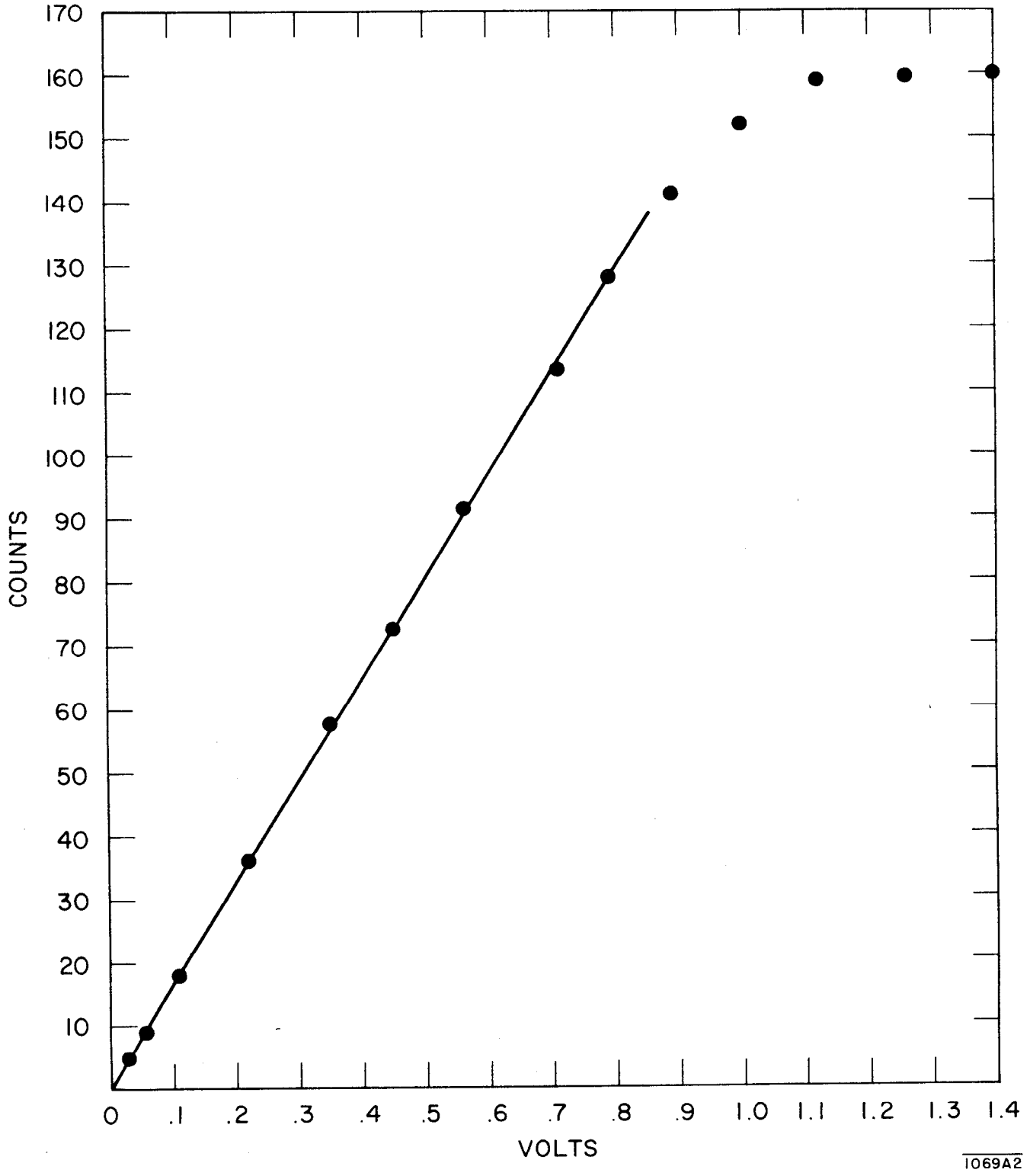
170
160
150
140
130
120
110
100
90
80
70
60
50
40
30
20
10
COUNTS
0
.1
.2
.3
.4
.5
.6
.7
.8
.9
1.0
1.1
1.2
1.3
1.4
VOLTS
1069A2

Fig. 8

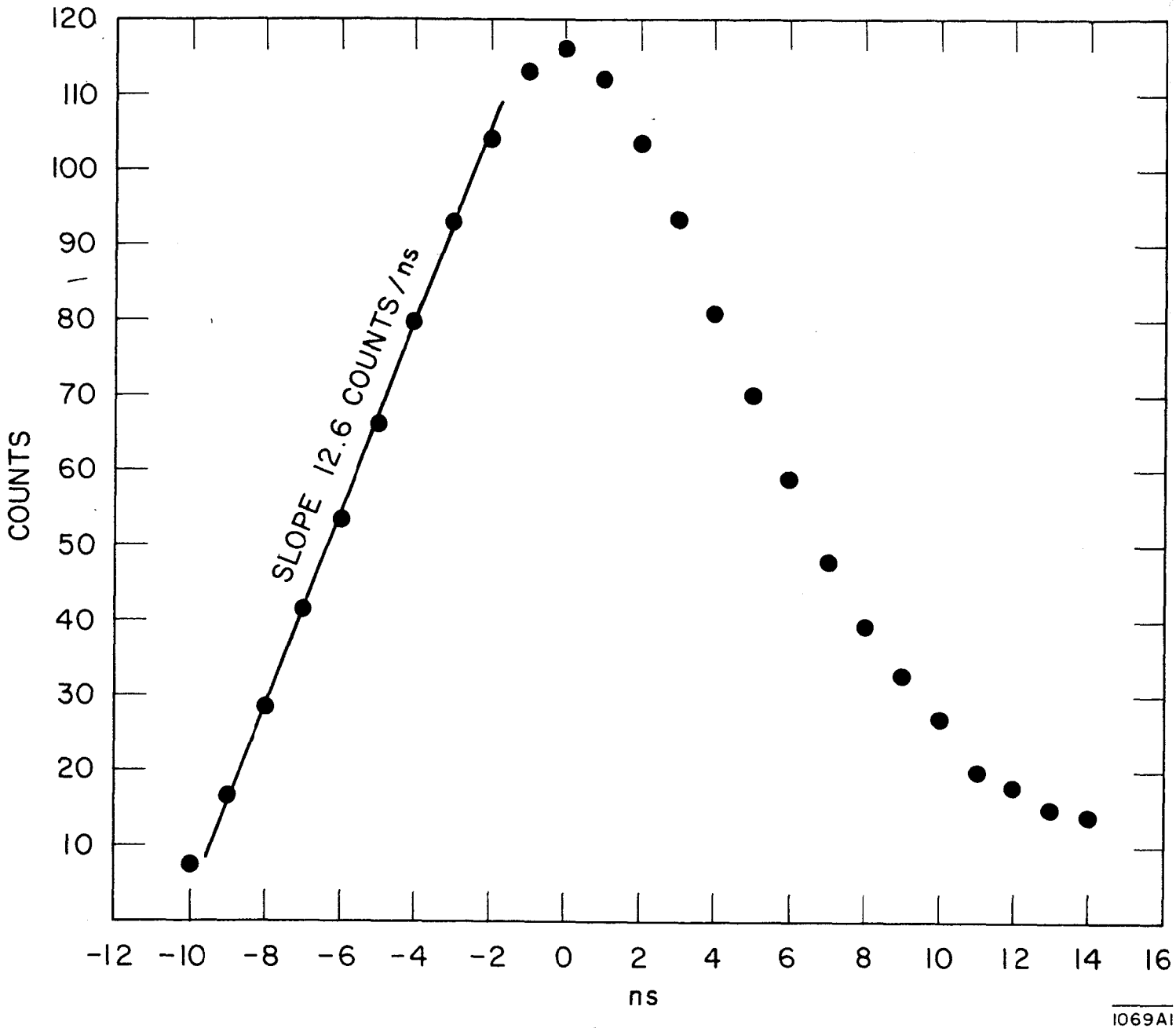
120
110
100
90
80
70
60
50
40
30
20
10
COUNTS
SLOPE 12.6 COUNTS/ns
-12
-10
-8
-6
-4
-2
0
2
4
6
8
10
12
14
16
ns
1069A1

Fig. 9