Final Scientific Report for DOE/EERE

Project Title:	III-V/Active-Silicon Integration for Low-Cost High-Performance Concentrator Photovoltaics
Project Period:	01/01/12 – 12/31/15
Reporting Period:	01/01/12 – 12/31/15
Reporting Frequency:	Final Report
Submission Date:	12/22/17
Recipient:	The Ohio State University
Recipient DUNS #:	832127323
Address:	Department of Electrical and Computer Engineering 2015 Neil Avenue Columbus, OH 43210
Website (if available)	emdl.osu.edu
Award Number:	DE-EE0005398
Awarding Agency:	DOE EERE SETP CSP subprogram
Working Partners:	SolAero Technologies (formerly Emcore Photovoltaics) National Renewable Energy Laboratory (NREL) Massachusetts Institute of Technology (MIT)
Cost-Sharing Partners:	SolAero Technologies (formerly Emcore Photovoltaics)
Principal Investigator:	Steven A. Ringel Neal Smith Chair and Professor of Electrical Engineering Director, OSU Institute for Materials Research Phone: 614-292-6409 Fax: 614-292-9562 Email: ringel@ece.osu.edu
DOE Contracting Officer:	Diana Bobo
DOE Project Manager:	Daniel Stricker

12/22/2017

Signature **Date**

Acknowledgment

This material is based upon work supported by the Department of Energy under award number DE-EE0005398.

Disclaimer

Executive Summary

This FPACE project was motivated by the need to establish the foundational pathway to achieve concentrator solar cell efficiencies greater than 50%. At such an efficiency, DOE modeling projected that a III-V CPV module cost of $0.50/W or better could be achieved. Therefore, the goal of this project was to investigate, develop and advance a III-V/Si mulitjunction (MJ) CPV technology that can simultaneously address the primary cost barrier for III-V MJ solar cells while enabling nearly ideal MJ bandgap profiles that can yield efficiencies in excess of 50% under concentrated sunlight. The proposed methodology was based on use of our recently developed GaAsP metamorphic graded buffer as a pathway to integrate unique GaAsP and Ga-rich GaInP middle and top junctions having bandgaps that are adjustable between 1.45 – 1.65 eV and 1.9 – 2.1 eV, respectively, with an underlying, 1.1 eV active Si subcell/substrate. With this design, the Si can be an active component sub-cell due to the semi-transparent nature of the GaAsP buffer with respect to Si as well as a low-cost alternative substrate that is amenable to scaling with existing Si foundry infrastructure, providing a reduction in materials cost and a low cost path to manufacturing at scale. By backside bonding of a SiGe, a path to exceed 50% efficiency is possible.

Throughout the course of this effort, an expansive range of new understanding was achieved that has stimulated worldwide efforts in III-V/Si PV R&D that spanned materials development, metamorphic device optimization, and complete III-V/Si monolithic integration. Highlights include the demonstration of the first ideal GaP/Si interfaces grown by industry-standard MOCVD processes, the first high performance metamorphic tunnel junctions designed for III-V/Si integration, record performance of specific metamorphic sub-cell designs, the first fully integrated GaInP/GaAsP/Si double (1.7 eV/1.1 eV) and triple (1.95 eV/1.5 eV/1.1 eV) junction solar cells, the first high performance GaAsP/Si double junction cell, the demonstration of a new method that allow for rapid, quantitative and non-destructive characterization of dislocations (ECCI-electron channeling contrast imaging), the first observation, explanation and solution of the now commonly reported lifetime degradation and recovery phenomena in III-V/Si MOCVD growth, the first demonstration of a high performance SiGe cell with a bandgap of 0.9 eV, amongst other highlights. The impact of the program on the international community has been significant. At the start of our FPACE1 project and for the immediate prior years, 1-2 conference papers/annually were presented at IEEE PVSC. Once FPACE1 commenced in 2011, related efforts sprouted across the US, Europe and Asia and by 2015 there were 26 papers presented on III-V/Si multijunctions in the 2015 PVSC, demonstrating the excitement that was stimulated by the results of this FPACE1 effort.

Comparison of Proposed versus Realized Project Goals

The following table summarizes the project's proposed goals versus actual progress for each task. Deviations between an Initial negotiated deliverables / milestones and an actual deliverable / milestone are discussed in the "Deliverable / Milestone Deviations" section of the Technical Narrative.

Task #	Task description	Initial Negotiated Deliverable / Milestone	Actual Deliverable / Milestone
1.1	GaAsP buffer at target lattice constant with TDD < 1-2 x10^7 cm^{-2}	09/30/12	09/30/12
1.1	GaAsP buffer at target lattice constant with TDD < 6-8 x10^6 cm^{-2}	06/30/13	04/30/13
1.2	XTEM identifying defect modes in GaP/Si MOCVD interface	09/30/12	09/30/12
1.2	Demonstration of complete APD and stacking fault free bulk GaP-on-Si beyond 100nm of the GaP/Si interface	03/31/13	01/31/13
1.3	Growth of GaAsP and GaInP DHs at target bandgaps	12/31/12	12/31/12
1.3	TRPL bulk lifetime > 1ns for GaAsP measured by NREL	06/30/13	Unrealized
1.4	Down selection of Si cell configuration (n+p or p+n) and method of formation	12/31/12	06/30/13
1.4	Demonstration of 2J GaAsP/Si sub-cell structure with profiles confirmed by SIMS within 10% of design targets	06/30/13	06/30/13
1.4	Material Go/No-Go Metric = Demonstration of 3J (1.9-2.2eV / 1.5-1.75eV / 1.1eV) monolithically integrated structure	06/30/13	06/30/13
2.1	1D multi-junction performance model will be demonstrated, and a report delivered with the results for the optimal band gap combination //	09/30/12	06/30/12
2.1	2D multi-junction performance model will be demonstrated and a report delivered with the results for the incorporation of the 1.12 eV Si sub-cell into the MJ device	06/30/13	04/30/13
2.2	Report describing the system cost model with the key parameters that are included in determining the LCOE for the system	06/30/12	07/31/12
2.2	Report with the results from the system cost analysis and a recommendation will be made as to the best system approach for achieving the lowest LCOE	12/31/12	11/30/12
3.1	Milestone and Device Go/No-Go Metric = Demonstration of a GaAsP-on-Si single junction PV sub-cell with a 10% efficiency at AM1.5 under 1-sun	06/30/13	4/31/13

3.2	Demonstration of SiGe layer on Si at target bandgap (0.67-0.8eV) with TDD < $1x10^6$ cm^{-2} measured by TEM	12/31/12	10/31/12
3.2	SIMS verification of n+p doping profile in SiGe consistent with modeling targets, in a sub-cell growth structure having TDD < $1x10^6$ cm^{-2}	06/30/13	03/31/13
4.1	Demonstration of GaAsP sub-cell on Si with Voc > Eg/q – 0.5 eV	12/31/13	Unmet - 0.55eV
4.1	Demonstration of GaInP sub-cell on Si with Voc > Eg/q – 0.5 eV	06/30/14	Unmet – 0.79eV
4.2	Demonstration of a SiGe sub-cell (0.67-0.8eV) with IQE > 70% across a Si-filtered spectrum	12/31/13	9/30/2014
4.2	Demonstration of a dual-junction GaAsP/Si sub-cell with target AM1.5 (1-sun) efficiency > 25% (accounting for surface reflection)	06/30/14	Unrealized >20% Projected 1.7/1.1 eV design
5.1	GaAsP and GaInP-based tunnel diodes will be demonstrated with a series resistance of <1 $x10^{-3}$ ohm-cm^2 and a Jp of >15 mA/cm^2	12/31/13	GaAsP – 10/1/2013 (met) GaInP – 10/1/2014
5.1	GaAsP and GaInP- based tunnel diodes will be demonstrated with a series resistance of <1 $x10^{-4}$ ohm-cm^2 and a Jp of >15	06/30/14	GaAsP – $R_s = 2.1x10^{-4}\ \Omega \cdot cm^2$ GaInP – $Rs = 5.3x10^{-4}\ \Omega \cdot cm^2$
5.2	Demonstration of robust ohmic contact design on 2 eV GaInP with Rc less than 1x10^-3 ohm-cm2 //	12/31/13	11/30/13
5.2	Demonstration of robust ohmic contact design on 2 eV GaInP with Rc less than 1x10^-5 ohm-cm2	06/30/14	11/30/13
5.3	Report with the optical modeling indicating the design necessary to achieve an average reflectance of 6% from 300 to 1600 nm	03/31/14	03/31/14
5.3	Demonstration of high performance, broadband ARC on 3J GaInP/GaAsP/Si laboratory cell structure with reflectivity < 6% from 300 to 1600 nm	12/31/14	Unrealized
6	Integration of GaInP, GaAsP and Si sub-cell components on Si into a laboratory cell structure to enable initial characterization of device performance metrics under concentration //	06/30/14	12/31/15
6	Fabrication and device characterization of a mechanically stacked 4J cell using a SiGe bottom cell // Testing and characterization of 3J GaAsP/GaInP/Si laboratory cells under concentration levels (from < 100x to ~ 1000x) and at one sun measured by NREL with target efficiency of 40% at 500x	12/31/14	Unrealized

Technical Narrative

Project Objective

The goal of this project is to investigate, develop and advance a III-V/Si mulitjunction (MJ) CPV technology that can simultaneously address the primary cost barrier for III-V MJ solar cells while enabling nearly ideal MJ bandgap profiles that can yield efficiencies in excess of 50% under concentrated sunlight. This will be achieved by using a recently developed GaAsP metamorphic graded buffer as a pathway to integrate unique GaAsP and Ga-rich GaInP middle and top junctions having bandgaps that are adjustable between 1.45 – 1.65 eV and 1.9 – 2.1 eV, respectively, with an underlying, 1.1 eV active Si subcell/substrate. With this design, the Si can be an active component sub-cell due to the semi-transparent nature of the GaAsP buffer with respect to Si. The process is also amenable to including a 4th SiGe low bandgap junction, through which efficiencies even greater than 50% can be achieved under concentration. Specific objectives include determination of relevant structural-electronic property correlations (e.g. carrier lifetimes versus defect densities) within metamorphic GaAsP and GaInP sub-cell materials, using this information in device models for optimization, investigating and developing a Si 1.1eV sub-cell process that is compatible with III-V epitaxy, and establishing a compatible SiGe 0.7 eV sub-cell grown on Si to serve as an optimum 4th junction. The sub-cell components will be integrated into optimum three and four junction cell structures for testing at both low and high solar concentration. The program incorporates extensive system and device modeling, which reveals this to be a viable path to achieve $0.50/W module costs for CPV systems.

Background

The use of a Si substrate for III-V PV cells is hardly a new idea. Previous work by our group has led to breakthrough advances via the use of SiGe interlayers as “defect filters” between Si and III-V single and MJ cells. That work was based on our earlier demonstrations of very high quality III-V materials on Ge, by *simultaneously* solving the problems of (1) polar/nonpolar epitaxy (leading to anti-phase domain free GaAs and GaInP on Ge/SiGe/Si substrates), (2) interdiffusion and autodoping (leading to achievement of both n$^+$p and p$^+$n polarity III-V cells on Si with total control over the III-V/IV interface down to the nanometer level), and (3) maintaining a low dislocation density in the III-V overlayers (leading to record long minority carrier lifetimes in metamorphic III-V materials). However, the use of a SiGe metamorphic interlayer, which will filter the transmitted light due to its reduced bandgap (vs. Si), relegated the Si substrate to

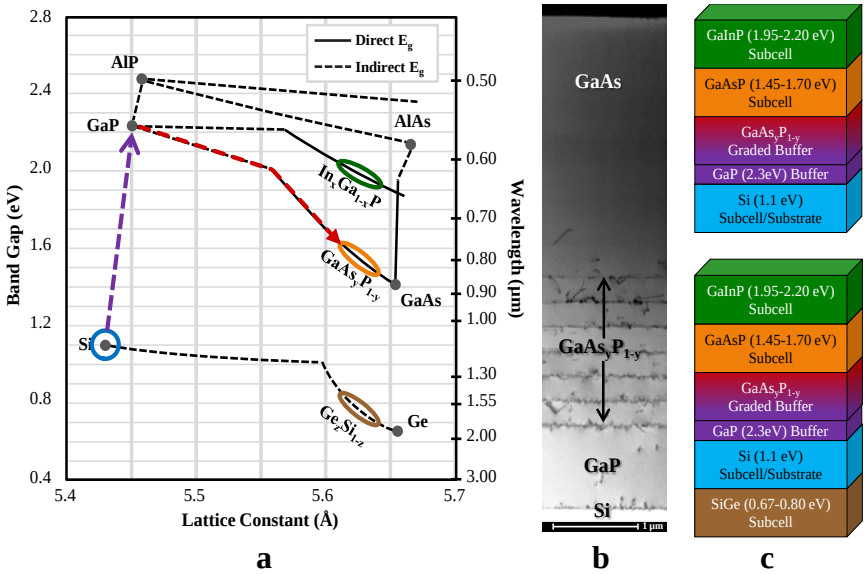


Figure 1. (a) Semiconductor bandgap vs. lattice constant chart for Si to GaAs/Ge range. (b) XTEM of terminal GaAs layer on a $GaAs_yP_{1-y}$ step-graded buffer grown on a Si substrate. (c) Diagrams of proposed ideal III-V/Si(Ge) 3J (top) and 4J (bottom) devices.

serve only as a support structure. More recently, we have begun to explore a parallel path to integrate III-V's on Si via the use of $GaAs_yP_{1-y}$ metamorphic buffer layers. Throughout its compositional range, $GaAs_yP_{1-y}$ spans the same range of lattice constants as SiGe, thus capturing the same range of ideal III-V bandgap combinations, but $GaAs_yP_{1-y}$ has the significant advantage of possessing a bandgap much higher than that of Si; thus $GaAs_yP_{1-y}$ layers on Si can serve as a semi-transparent metamorphic buffer that enables series connection between III-V subcells and the underlying active Si subcell/substrate. This is summarized by Figure 1.

The well-known road block in this path has for years been the GaP/Si interface, which is far more complex than the analogous GaAs/Ge interface due to P-Si reactions at growth temperature, which causes rough surface morphology and nucleates an extensive array of defect microstructures, including stacking faults and twin planes, along with the expected presence of dislocations and anti-phase domains (APDs). [1,2] However, after extensive fundamental growth research at OSU for the past few years involving an understanding of in-situ interface chemistry at the atomic scale, we have achieved a solution that *simultaneously* eliminates all nucleation-related extended defects without needing non-standard interfacial layers, leaving only misfit dislocations, as expected for the GaP/Si system with its 0.37% lattice mismatch. [3] This is depicted in the XTEM image of Figure 2, making this an excellent starting point for the proposed work.

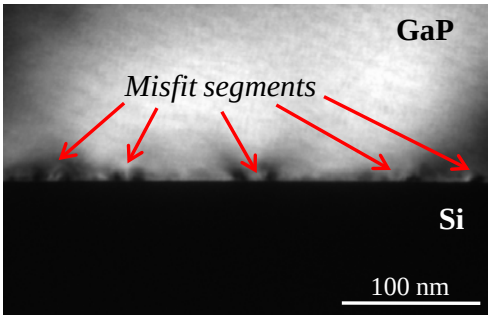


Figure 2. XTEM of the GaP/Si interface of a high-quality heteroepitaxial sample, free of nucleation-related defects and displaying only the desired misfit dislocations needed to relax the small lattice mismatch (0.37% at room temp).

Significant Accomplishments

Many key findings were obtained during the course of this project that have substantially advanced progress toward a III-V on Si PV technology and have provided fundamental insights into optimizing metamorphic III-V/Si heterostructures for PV applications. This in-depth report highlights these accomplishments in a task-wise structure, and provides information to alert the reader to the most appropriate publications. However, several of these achievements transcended being tied to a single task element, and are proving to be of particularly widespread impact. These select accomplishments are listed below as they demonstrate the broad impact of our FPACE program, before continuing into the detailed, comprehensive report where task-specific accomplishments are described.

A. *The first demonstration of antiphase- and stacking fault-free GaP/Si interfaces grown by MOCVD:* This seminal work, published in 2013, demonstrated the first MOCVD-grown GaP on Si (001) truly free of APDs and SFs. [4] This work has already been cited 71 times and downloaded well over 161 times (note: *APL* only tracks since Dec. 2016, so this is heavily underestimated).

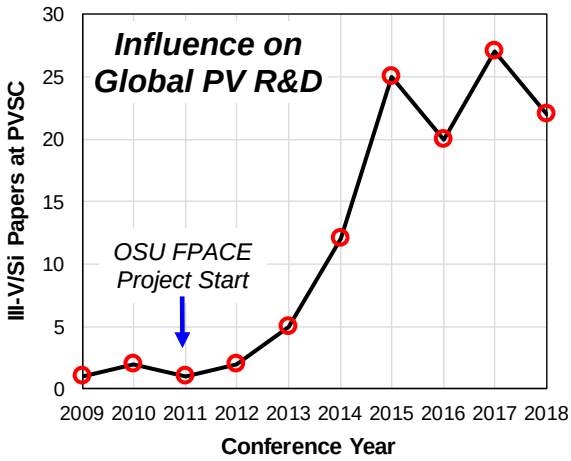


Figure 3: Number of IEEE Photovoltaic Specialists Conference (PVSC) papers on III-V/Si per year since 2009. Steep increase follow start of the OSU FPACE program indicates the strong influence this work had on the global growth of this field.

B. *The first reported monolithic, all-epitaxial GaAsP/Si multijunction (tandem) solar cell grown by MOCVD*: This work, first presented at the *39th IEEE PVSC* (2013), and then published (after significant refinement) in 2016, also clearly demonstrated a much-needed technology transfer from basic research/university-oriented MBE to industry-compatible MOCVD. [5] This work, including both multiple presentations and publications, arguably re-invigorated the field of III-V/Si PV, as witnessed by the resurgent large funding programs in the EU (e.g. Fraunhofer ISE and Ilmenau Univ. of Technology in Germany, Univ. Grenoble Alpes in France, and Univ. Politécnica de Madrid in Spain), the massive growth of III-V/Si at NREL, significant activities levels at Yale/UIUC, GaP/Si carrier-selective contact work at ASU/Caltech, and so forth.

C. *The first demonstration of a III-V/active-Si fully epitaxial triple junction solar cell.* This device was the ultimate program goal at the outset of FPACE. Although this device was not actually demonstrated until shortly following the close of the project, and presented at the *43rd IEEE PVSC* (2016), in working toward achieving this device our group had to develop many "first-ofs" all across the associated materials and device space. Such accomplishments include the aforementioned MOCVD-grown GaP/Si integration, metamorphic tunnel junctions at both the 2J ($GaAs_{0.75}P_{0.25}$) and 3J ($GaAs_{0.90}P_{0.10}$) lattice constants, respectively (with record peak currents for such lattice constants), discovery of an important (and universal) Si lifetime degradation and recovery mechanism during III-V processing, demonstration of the first III-V 2J (GaInP/GaAsP) grown directly on Si (i.e. not via Ge/Si or SiGe grading), and so forth.

D. *The establishment of ECCI as a go-to method rapid, quantitative, and non-destructive dislocation characterization in heteroepitaxial III-V (and IV) materials:* Since our seminal work that demonstrated the utility of ECCI in PV characterization, the method has been quickly adopted in groups that include NREL, Yale, UIUC, UCSB, IBM, Fraunhofer, and more. Since first publishing in 2014 (with additional papers in following years), our ECCI work has cumulatively yielded at least 41 known citations and well over 825 known (*APL* only tracks since Dec. 2016) downloads, plus 1622 views of our *Journal of Visualized Experiments* video on the subject. ECCI has quickly become a standard tool in not only the metamorphic III-V PV community, but in an increasing range of other III-V heteroepitaxy fields, as well.

Task 1.0: Material Quality and Interface Control [Development and Characterization]
This task focused on the *material and interface development* required to realize the four independent PV junctions (SiGe, Si, GaAsP and GaInP) starting from a Si substrate. High quality GaP transition layers on Si combined with the anion-based $GaAs_yP_{1-y}$ metamorphic buffers provided a lattice transition to enable high quality 1.5eV GaAsP and 2.0eV GaInP materials on Si. SiGe metamorphic buffers on Si provided a lattice transition to access 0.67eV-0.8eV SiGe. This tasked focused on the optimization of growth processes to achieve PV-quality materials and interfaces required to enable each of the sub-cells. Significant accomplishments related to this task included:

- First APD-free, SF-free GaP/Si interfaces by MOCVD; successful transition from MBE
- Identified crystallographically compatible (311) interface facets resulting from MOCVD GaP/Si(100) nucleation
- Developed high temperature growth conditions for high quality, graded GaAsP from GaP to GaAs on Si (001)
- Pioneered application of ECCI (electron channeling contrast imaging) method as rapid SEM-based characterization tool for III-V/Si PV; revealed ability to sort out different dislocation types, leading to new fundamental science
- First true device quality GaAsP/Si materials grown by MOCVD
- Discovered and explained Si lifetime degradation/recovery mechanism for III-V/Si MOCVD
- Achieved TDD of $6x10^5$ cm^{-2} in relaxed $Si_{0.15}Ge_{0.85}$ 0.8 eV material

While many of these efforts were regularly reported in conference presentations and proceedings, the most significant of these accomplishments were highlighted in a number of journal papers published throughout this program. Partial summaries of key findings are provided below. Associated publications which include additional details are also listed below with brief abstracts included.

Highlight 1: GaP/Si growth by MOCVD

The concentration of this program task was the transition of a previously-developed MBE-based process for the heteroepitaxy of GaP on Si substrates to the MOCVD growth regime. From initial MBE-based research, a set of key elements necessary for successful suppression of all defects related to the heterovalent (polar/non-polar) nucleation – antiphase domains (APDs), stacking faults (SFs), and microtwins (MTs) – was identified: (1) use of vicinal Si(100) substrates to promote biatomic step formation, (2) proper Si substrate preparation to ensure a pristine surface for GaP nucleation, and (3) the use of carefully-calibrated, Ga-initiated migration enhanced epitaxy (MEE) for GaP nucleation. Additionally, to enable use as a virtual substrate for subsequent high-temperature epitaxy, a process involving multi-temperature GaP "bulk" growth was developed, which included an initial thin, low-temperature layer to provide sufficient film thickness for stability (cohesion) at elevated temperatures, followed by high-temperature annealing and growth to promote efficient dislocation glide and relaxation.

For the transition to MOCVD, initial GaP/Si development concentrated on the Si surface preparation via homoepitaxial Si growth and the GaP atomic layer epitaxy (ALE) nucleation process, the MOCVD equivalent of MEE. The resulting Si and GaP surfaces, produced over a range of process conditions, including growth temperatures and Ga and P precursor dose times

and pressures, were initially characterized by AFM with the goal of producing a nucleation layer surface morphology similar to that of the MBE-based growths, as discussed in previous reports. Following successful achievement in this regard, work was then focused on the subsequent low-temperature "bulk" layer growth, looking at various growth conditions (growth rate, temperature, V:III ratio, etc.), as well as small refinements of the established nucleation conditions, in order to again produce the best, most MBE-like resultant surface morphology. This work turned out to be very non-trivial due to the very small window of high-quality low-temperature GaP growth conditions. Nonetheless, a process was eventually developed that resulted in 250 nm thick GaP films grown on Si(100) substrates with smooth, epi-ready surfaces upon which subsequent high-temperature GaP (or GaAsP) epitaxy could be performed. X-ray diffraction measurements showed these films to be fully relaxed, and cross-section TEM (XTEM) imaging revealed GaP/Si interfaces that were indeed devoid of any nucleation-related defects.

Figure 4 provides a comparison between an "uncontrolled" MOCVD-grown GaP/Si interface (Fig. 4a), which is ridden with nucleation-related defects, including large APDs, SFs, and MTs, and a successfully controlled interfaces (Fig. 4b), which possesses no such defects. Interesting, it was discovered within this effort that our particular Si homoepitaxial growth conditions yielded a large degree of step-bunching, which led to the formation of (311)-oriented facets on the surface, as shown in Fig. 4c. Fortuitously, such higher-index surfaces, similar to the use of biatomic stepped surfaces, have been previously demonstrated by Kroemer [6] and Narayanan [7] to promote APD-free III-V/IV heteroepitaxy; these features were indeed found to be benign (and possibly even beneficial) to the heterovalent nucleation process.

Highlight 2: Si lifetime dependence on MOCVD processing

During the optimization the epitaxial Si PV cell, one key finding from this task was that the expected performance increase when incorporating high lifetime, float-zone (FZ) Si substrates over Czochralski (CZ) Si was not realized. Specifically, the long lifetime FZ Si was expected to provide an increase in quantum efficiency for long wavelength photons over that of the lower lifetime CZ material. To investigate this lack of performance enhancement, photoconductive decay (PCD) measurements were completed on Si substrates at various points throughout the formation of the MOCVD GaP/Si epitaxial sub-cell on both FZ and CZ Si substrates. For PCD analysis, it is important that the Si surface be well passivated on the front and back of the wafer to provide accurate lifetime measurements. During this investigation, we utilized a solution of quinhydrone and methanol to provide that passivation and complete the PCD measurements under illumination. In the cases where the Si substrates were exposed to

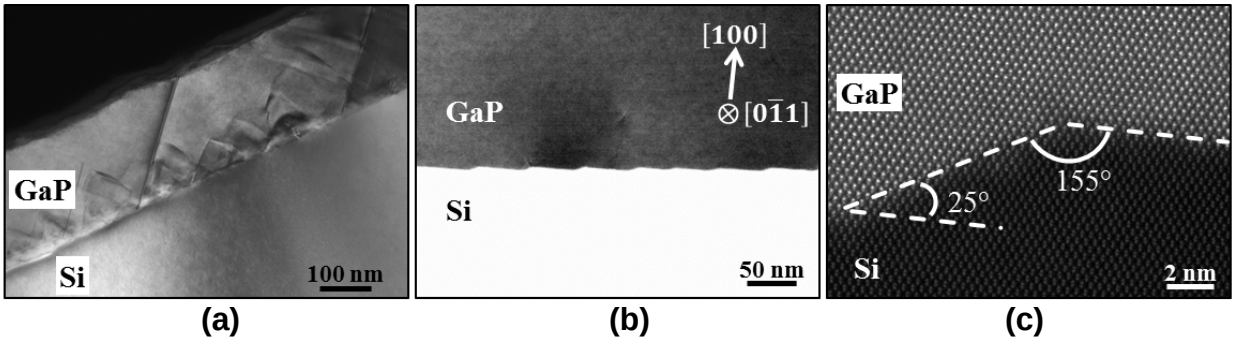


Figure 4: Cross-sectional TEM of (a) an uncontrolled GaP/Si MOCVD interface [g220] and (b) an optimized MOCVD GaP/Si interface [g220] demonstrating nucleation-related defect control. (c) Atomically resolved STEM imaging shows the (311) step-bunch facet geometry and an atomically sharp interface free of defects.

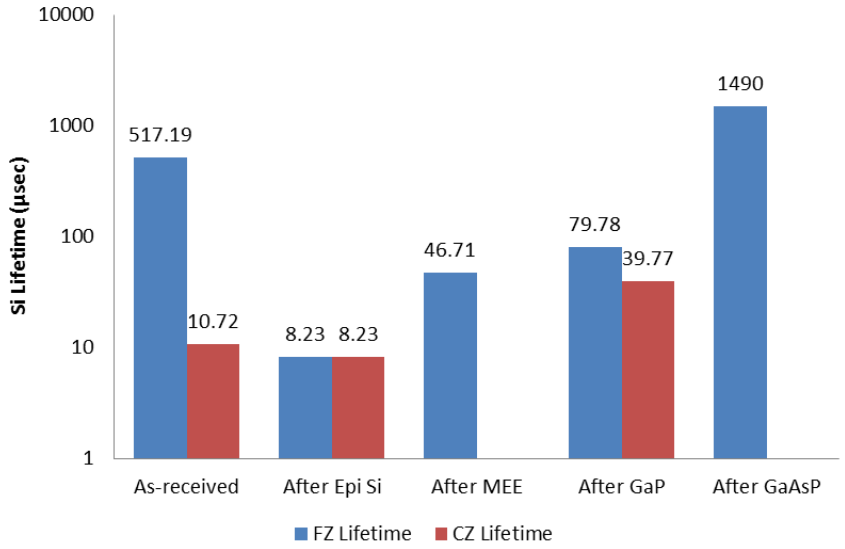
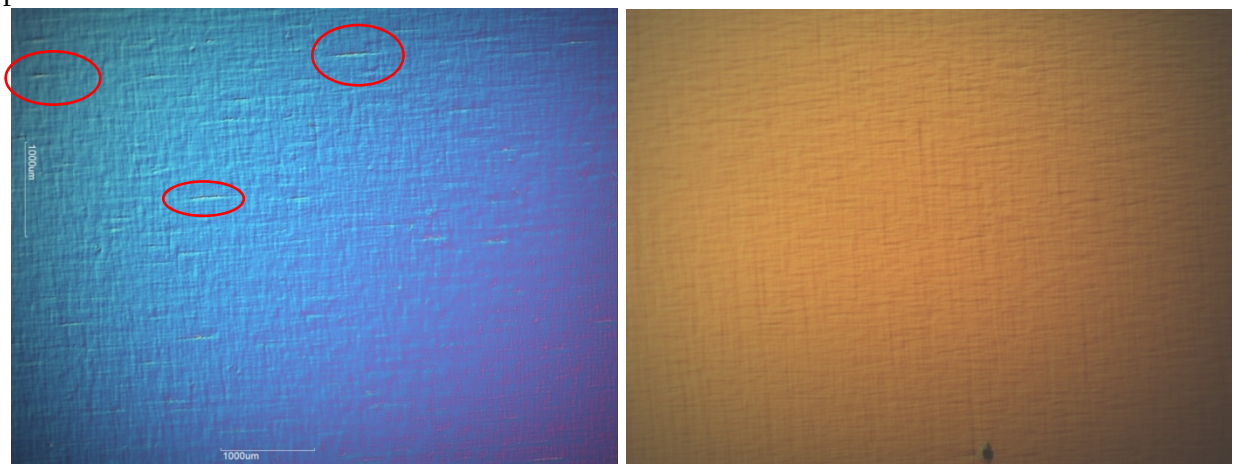


Figure 5. Evolution of Si lifetime via PCD on both FZ and CZ Si substrates at various stages during the MOCVD process used to create GaAsP/GaP/Si templates.

epitaxial processes for the growth of Si, GaP or GaAsP, all epitaxial layers were etched away prior to PCD analysis, leaving only the "bulk" Si substrate. Figure 5 shows a summary of the Si lifetime data collected. While the "as-received" FZ Si substrates do indeed possess a high lifetime, as expected, initial processing (Si epitaxy) in the MOCVD environment immediately degrades the Si lifetime more than an order of magnitude from >500 µsec to ~8 µsec, making it comparable to the low-quality CZ Si and significantly limiting the efficiency that can be expected from the Si sub-cell. With additional MOCVD epitaxy, both steps in the GaP interface initiation process (MEE and 580^{o}C "bulk" GaP deposition) do recover some of this initial lifetime degradation resulting in a final lifetime of only 80 µsec for the 250nm GaP/Si templates, which have been used to optimize the Si epitaxial sub-cell performance. While these lifetimes are insufficient to enable collection of the long wavelength photons absorbed deep in the thick Si substrates and explain the lower than expected quantum efficiencies near the Si absorption edge, all of these steps are critical to the MOCVD GaP/Si interface control and cannot be omitted to maintain the bulk Si lifetime. Fortunately, further high temperature MOCVD epitaxy of the GaAsP metamorphic buffer shows an amazing recovery of the Si lifetime to even higher values, up to almost 3X, than the as-received substrates. These results do agree with reports of Si lifetime degradation in various annealing ambients, but the mechanism of lifetime recovery and the impact of further GaAsP and GaInP epitaxy to complete the MJ stack is currently unknown. Next period, these initial investigations into the Si lifetime will continue and the impact of the full III-V epitaxial process by MBE and MOCVD will be investigated.

Highlight 3: GaAsP Step Graded Buffer Optimization

During this task effort was dedicated to the optimization of the GaAsP step graded buffer (SGB). While many prior efforts to optimize the SGB design have been motivated by the reduction of TDD in the terminal composition, in this instance the motivation was driven by larger physical defects visible on the surface of the terminal layer. Figure 6(a) shows a microscope image of a SGB grown on Si out to a composition of $GaAs_{0.9}P_{0.1}$. As shown, the surface is decorated with sizeable "trenches" of varying length. Characterization of these surface features on processed devices by electron beam induced current (EBIC) does not show any signs of increased recombination which would be indicative of a source of shunt current. However, previous experience with the design of step graded buffers suggests that such surface features can be an easy source of dislocation pinning and encourage the formation of dislocation pile-ups which can be deleterious to device performance. Therefore, here we considered methods to eliminate the formation of these surface features. While a much thinner SGB could be utilized toward this end, in order to achieve the lowest TDD we are unable to take advantage and choose to initially consider only solutions which maintain the same thickness and compositional grade design as the sample shown in Figure 6(a). As such, flexibility of the SGB design is limited to considering growth rate, substrate offcut, growth technique and growth temperature. While all of these may impact the terminal surface morphology, looking at prior data led us to concentrate our investigation on the impact of the growth temperature. In addition to the temperature impacting the surface mobility and surface morphology, prior analysis of XRD maps of SGBs demonstrated "kinking" at various locations/compositions throughout the grade which were also shown to be temperature dependent. While there is no direct correlation between the surface trenches and the kinking seen in the XRD maps, the kinking is indicative of a change in the magnitude of the surface tilt during the grade which has not been seen in other systems. In an attempt to minimize the surface tilt, we developed multi-temperature grades and investigated the resulting surface morphology of the terminal GaAsP. Results of one such design are shown in Figure 6(b). For this design a simple 2-step temperature profile was used with the 0-50% grade completed at 725°C and the 50-90% grade completed at 650°C. With no adverse impact on the TDD measured in the terminal layer, the modified design provided significant reduction in the presence of faceted surface trenches.



(a) **(b)**

Figure 6: Nomarski optical microscope images of tensile $GaAs_{0.9}P_{0.1}$ step graded buffers grown on Si with varying temperature profiles. (a) Constant temperature of 725°C and (b) 2-step temperature profile 725°C/650°C with lower temperature after $GaAs_{0.5}P_{0.5}$.

Highlight 4: Electron Channeling Contrast Imaging: GaP/Si Interface and GaAsP Material Quality Characterization

During the initial phase of this program, one limitation that became apparent was the lack of a metrology technique that could be easily utilized to provide quick, detailed and reliable analysis of the structural quality of the GaP/Si and GaAsP/Si metamorphic films. Currently, transmission electron microscopy (TEM) is the most widely used characterization technique used to study extended defects (e.g. dislocations, stacking faults, etc.) in single crystals. Unfortunately, samples imaged by TEM must be transparent to an electron beam, which requires that a sample be thinned down. This thinning commonly occurs by chemical/mechanical polishing or focused ion beam milling, processes that can make TEM prohibitively time consuming and expensive to use in applications that either require a large number of samples to be characterized or characterization over a large area in one sample. In recent years, electron channeling contrast imaging (ECCI) has attracted attention as a complimentary technique to TEM because it can be used to characterize many of the same extended defects as TEM while avoiding the previously mentioned drawbacks. [8] During this period, to fill the characterization void realized during Phase I, we have investigated the application of this novel technique to the GaP/Si and GaAsP/Si system of interest in this work. We have been able to demonstrate the incredible promise of this technique for characterizing a wide range of crystalline defects in any metamorphic system. While ECCI is a method with many similarities to TEM, it also has some key advantages that address the shortcomings of TEM. First, ECCI can be performed in most any scanning electron microscope (SEM). This makes ECCI an economically attractive alternative to traditional TEM work, as it avoids the use of more expensive TEM equipment. Second, and perhaps more importantly, ECCI can be performed on as-grown samples with little to no sample preparation. This can save many hours of sample preparation and makes it possible to image over large areas of a sample with ease. Figure 7 shows a range of extended crystal defects which were successfully characterized on various GaP/Si samples without any "sample preparation" following the MOCVD epitaxial process. Threading dislocations within the bulk GaP film (Fig. 7a), misfit dislocations located at the GaP/Si interface (Fig. 7b), and stacking faults (fig. 7c) are all easily resolvable by ECCI and the stacking faults show the same thickness fringes commonly seen by TEM. Although imaging of all these defects can provide valuable analysis of the

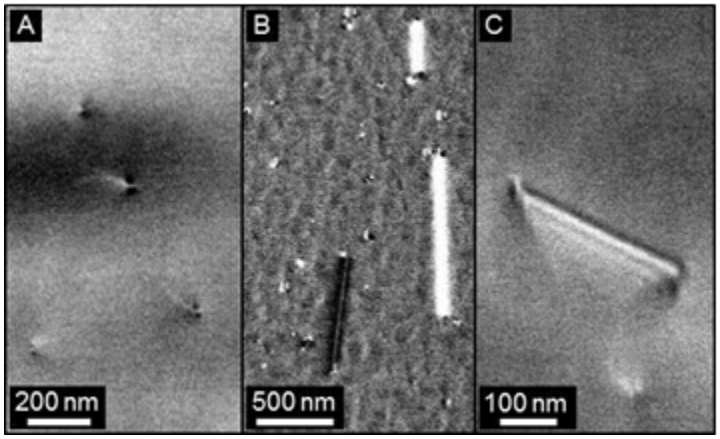


Figure 7. ECCI images of various GaP/Si samples showing A) Threading dislocations, B) misfit dislocations (appear in the ECCI micrograph as dark and bright lines where the contrast corresponds to the Burgers vector of the dislocation), and C) a stacking fault.

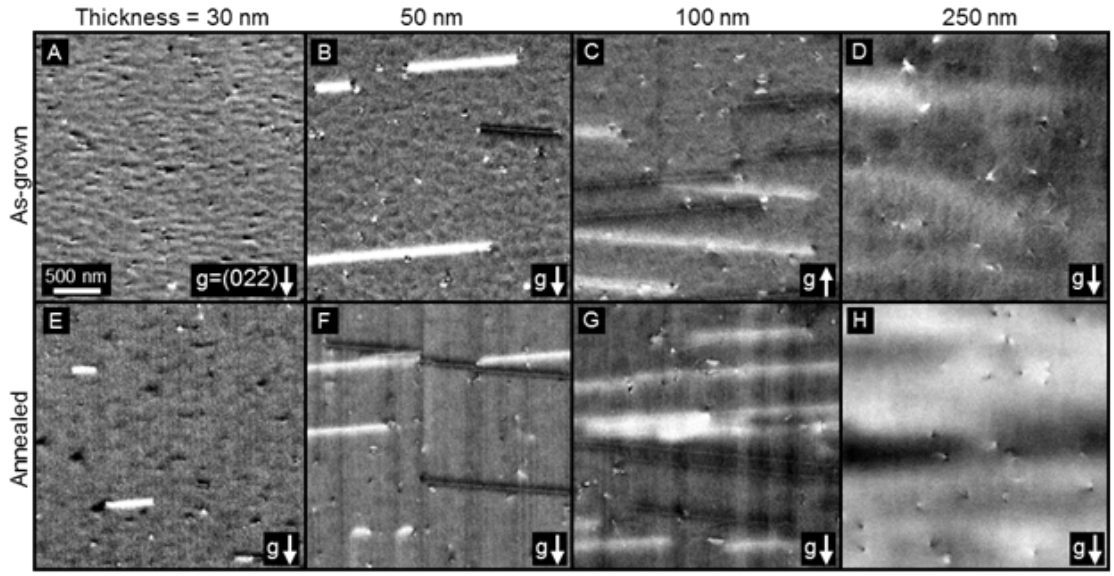


Figure 8. ECCI micrographs of varying GaP thickness from 30nm to 250nm on Si. (A-D) are for as-grown samples while (E-H) are for the same samples after a 725ºC anneal in PH3.

structural quality of the GaP/Si film, the ability to image misfit dislocations at a buried interface on an as-deposited metamorphic sample is quite powerful and is not easily accessible, if at all, by other metrology techniques. Of particular note, the developed ECCI technique enabled the investigation of the nucleation of misfit dislocations versus GaP thickness for GaP/Si films as well as their evolution with varying thermal cycles during the MOCVD process. Figure 8 shows a series of ECCI images for varying GaP thickness from 30nm to 250nm on Si. Images A-D are for as-grown samples while the corresponding images E-H are for the same samples after a 725C anneal.

Associated Publications:

Nucleation-related defect-free GaP/Si(100) heteroepitaxy via metal-organic chemical vapor deposition

T. J. Grassman, J. A. Carlin, B. Galiana, L. -. Yang, F. Yang, M. J. Mills and S. A. Ringel, *Appl. Phys. Lett.*, vol. 102, pp. 142102, Apr 8 (2013).

GaP/Si heterostructures were grown by metal-organic chemical vapor deposition in which the formation of all heterovalent nucleation-related defects (antiphase domains, stacking faults, and microtwins) were fully and simultaneously suppressed, as observed via transmission electron microscopy (TEM). This was achieved through a combination of intentional Si(100) substrate misorientation, Si homoepitaxy prior to GaP growth, and GaP nucleation by Ga-initiated atomic layer epitaxy. Unintentional (311) Si surface faceting due to biatomic step-bunching during Si homoepitaxy was observed by atomic force microscopy and TEM and was found to also yield defect-free GaP/Si interfaces.

Metamorphic epitaxy for multijunction solar cells

R. M. France, F. Dimroth, T. J. Grassman and R. R. King, MRS Bulletin 41, no. 3, 202 – 209 (2016).

Multijunction solar cells have proven to be capable of extremely high efficiencies by combining multiple semiconductor materials with bandgaps tuned to the solar spectrum. Reaching the optimum set of semiconductors often requires combining high-quality materials with different lattice constants into a single device, a challenge particularly suited for metamorphic epitaxy. In this article, we describe different approaches to metamorphic multijunction solar cells, including traditional upright metamorphic, state-of-the-art inverted metamorphic, and forward looking multijunction designs on silicon. We also describe the underlying materials science of graded buffers that enables metamorphic subcells with low dislocation densities. Following nearly two decades of research, recent efforts have demonstrated high-quality lattice mismatched multijunction solar cells with very little performance loss related to the mismatch, enabling solar-to-electric conversion efficiencies over 45%.

Rapid misfit dislocation characterization in heteroepitaxial III-V/Si thin films by electron channeling contrast imaging
S. D. Carnevale, J. I. Deitz, J. A. Carlin, Y. N. Picard, M. De Graef, S. A. Ringel and T. J. Grassman, *Appl. Phys. Lett.*, vol. 104, pp. 232111, Jun 9 (2014).

Electron channeling contrast imaging (ECCI) is used to characterize misfit dislocations in heteroepitaxial layers of GaP grown on Si(100) substrates. Electron channeling patterns serve as a guide to tilt and rotate sample orientation so that imaging can occur under specific diffraction conditions. This leads to the selective contrast of misfit dislocations depending on imaging conditions, confirmed by dynamical simulations, similar to using standard invisibility criteria in transmission electron microscopy (TEM). The onset and evolution of misfit dislocations in GaP films with varying thicknesses (30 to 250 nm) are studied. This application simultaneously reveals interesting information about misfit dislocations in GaP/Si layers and demonstrates a specific measurement for which ECCI is preferable versus traditional plan-view TEM.

Electron Channeling Contrast Imaging for Rapid III-V Heteroepitaxial Characterization
J. I. Deitz, S. D. Carnevale, S. A. Ringel, D. W. McComb, T. J. Grassman, *Journal of Visualized Experiments*, vol. 101, pp. e52745, Jul 17 (2015).

Misfit dislocations in heteroepitaxial layers of GaP grown on Si(001) substrates are characterized through use of electron channeling contrast imaging (ECCI) in a scanning electron microscope (SEM). ECCI allows for imaging of defects and crystallographic features under specific diffraction conditions, similar to that possible via plan-view transmission electron microscopy (PV-TEM). A particular advantage of the ECCI technique is that it requires little to no sample preparation, and indeed can use large area, as-produced samples, making it a considerably higher throughput characterization method than TEM. Similar to TEM, different diffraction conditions can be obtained with ECCI by tilting and rotating the sample in the SEM. This capability enables the selective imaging of specific defects, such as misfit dislocations at the GaP/Si interface, with high contrast levels, which are determined by the standard invisibility criteria. An example application of this technique is described wherein ECCI imaging is used to determine the critical thickness for dislocation nucleation for GaP-on-Si by imaging a range of samples with various GaP epilayer thicknesses. Examples of ECCI micrographs of additional defect types, including threading dislocations and a stacking fault, are provided as demonstration of its broad, TEM-like applicability. Ultimately, the combination of TEM-like capabilities – high

spatial resolution and richness of microstructural data – with the convenience and speed of SEM, position ECCI as a powerful tool for the rapid characterization of crystalline materials.

Applications of Electron Channeling Contrast Imaging for the Rapid Characterization of Extended Defects in III–V/Si Heterostructures
S. D. Carnevale, J. I. Deitz, J. A. Carlin, Y. N. Picard, D. W. McComb, M. De Graef, S. A. Ringel and T. J. Grassman," *IEEE J. Photovolt.*, vol. 5, pp. 676-682, Mar (2015).

Electron channeling contrast imaging (ECCI) is a nondestructive diffraction-based scanning electron microscopy (SEM) technique that can provide microstructural analysis similar to transmission electron microscopy (TEM). However, because ECCI is performed within an SEM and requires little to no sample preparation, such analysis can be accomplished in a fraction of the time. Like TEM, ECCI can be used to image a variety of extended defects and enables the use of standard invisibility criteria to provide further defect characterization (e.g., Burgers vector determination). Here, we use ECCI to characterize various extended defects, including threading dislocations, misfit dislocations, and stacking faults, in heteroepitaxial GaP/Si(1 0 0) samples. We also present applications for which ECCI is particularly well suited compared with conventional methods. First, misfit dislocations are surveyed via ECCI across the radius of a 4-in GaP/Si wafer, yielding a proof-of-concept rapid (~3 h) approach to large area defect characterization. Second, by simply wet etching away a portion of a thick epitaxial GaP-on-Si layer, we use ECCI to image specific targeted interfaces within a heterostructure. Both of these applications are prime examples of how ECCI is a compelling alternative to TEM in circumstances where the required sample preparation would be prohibitively time-consuming or difficult.

III-V/GaP Epitaxy on Si for Advanced Photovoltaics and Green Light Emitters
T. J. Grassman, C. Ratcliff, A. M. Carlin, J. A. Carlin, L. Yang, M. J. Mills and S. A. Ringel, *ECS Trans*. vol. 50(9), pp. 321, 2013.

A brief overview of work concerning the direct integration of metamorphic III-V photovoltaic and optoelectronic materials with Si substrates is given. This effort includes the defect-mitigated heteroepitaxial growth of GaP on Si(100) substrates, as well as band gap and lattice constant engineering of subsequent InGaP and GaAsP materials via GaAsyP1-y compositionally-graded buffers. Such an integrated materials system enables the achievement of not only spectrum-optimized band gap combinations for high efficiency, low-cost III-V/Si multijunction solar cells, but also hold promise for use in other important optoelectronic technologies, including light emitters, for which the elusive green wavelengths are realizable, and multi-band photodetectors.

Evolution of silicon bulk lifetime during III–V-on-Si multijunction solar cell epitaxial growth
E. García-Tabarés, J. A. Carlin, T. J. Grassman, D. Martín, I. Rey-Stolle and S. A. Ringel, *Prog. Photovoltaics*, DOI: 10.1002/pp.2703 (2016).

The evolution of Si bulk minority carrier lifetime during the heteroepitaxial growth of III–V on Si multijunction solar cell structures via metal-organic chemical vapor deposition (MOCVD) has been analyzed. In particular, the impact on Si lifetime resulting from the four distinct phases within the overall MOCVD-based III–V/Si growth process were studied: (1) the Si homoepitaxial emitter/cap layer; (2) GaP heteroepitaxial nucleation; (3) bulk GaP film

growth; and (4) thick GaAsyP1-y compositionally graded metamorphic buffer growth. During Phase 1 (Si homoepitaxy), an approximately two order of magnitude reduction in the Si minority carrier lifetime was observed, from about 450 to ≤1 μs. However, following the GaP nucleation (Phase 2) and thicker film (Phase 3) growths, the lifetime was found to increase by about an order of magnitude. The thick $GaAs_yP_{1-y}$ graded buffer was then found to provide further recovery back to around the initial starting value. The most likely general mechanism behind the observed lifetime evolution is as follows: lifetime degradation during Si homoepitaxy because of the formation of thermally induced defects within the Si bulk, with subsequent lifetime recovery due to passivation by fast-diffusing atomic hydrogen coming from precursor pyrolysis, especially the Group-V hydrides (PH3, AsH3), during the III–V growth. These results indicate that the MOCVD growth methodology used to create these target III–V/Si solar cell structures has a substantial and dynamic impact on the minority carrier lifetime within the Si substrate.

Task 2.0: Cell Performance, System Performance and Cost Modeling

One overarching task throughout the initial program effort was the modeling of both devices and systems to drive and optimize the various development efforts. Specifically, subtask 2.1 addressed theoretical modeling of device performance to reducing the time necessary for device optimization. Subtask 2.2 concentrated on system modeling. The purpose of the system modeling was to determine how to incorporate the Si based multi-junction cell into a final system, with the goal of minimal levelized cost of electricity (LCOE) for a given set of conditions. This subtask was expected to yield a determination of the final system design approach (high or low concentration) through determination of the LCOE for the different system designs. While many of these efforts were regularly reported in journals, conference proceedings and conference presentations, the most significant of these accomplishments related to modelling are highlighted below with a partial summary of key findings. Associated publications which include additional details are also listed below with brief abstracts included.

Highlight 1: Modeling for Multijunction Cell Optimization under Concentration

During this program SolAero was tasked with performing 2D modeling. Accounting for 2D effects, which often cannot be easily included in a 1D model, are of particular importance for concentrator cell designs. The 2D model not only aids in the design of the cell with regards to grid pattern optimization, but is also very useful for understanding issues such as the sheet resistance that must be achieved for acceptable efficiency, or how a non-uniform illumination pattern (as would be seen by a cell in a concentrator system) may influence device performance. As such, SolAero has leveraged an in-house quasi-3D model in support of this task. The quasi-3D methodology utilized here has been well described in the literature [9-11] and thus only minimal detail is provided in this report.

The quasi-3D model fundamentally represents the cell as a large circuit network in which the lateral resistance of the top emitter layer is embodied in an interconnected grid of resistors (which are related to the sheet resistance of the material). A simple, local device model (such as a simple ideal diode model) is utilized in the 3rd dimension to represent local current generation and recombination. Both the local device model and the resistor grid may change spatially across the device due to factors such as a non-uniform illumination pattern or the presence of grid lines or bus bars. A simple diagram of the model set up is illustrated in Figure 9.

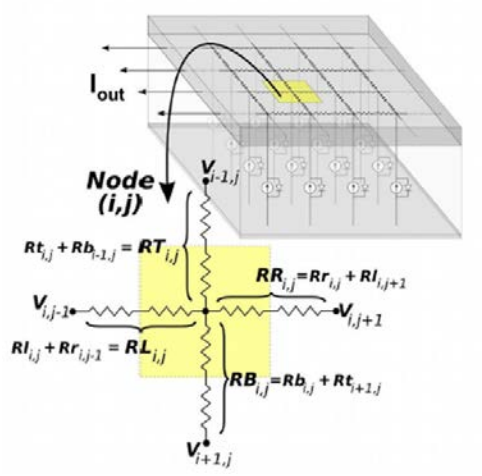


Figure 9. Diagram of fundamental quasi-3D model structure.

Note that the model is termed "quasi-3D" rather than simply a 3D model because the epitaxial structure of the device is not fully modeled. Such a model (many of which are commercially available) could be utilized for this purpose, but at much greater cost and complexity.

Using known device parameters (such as emitter sheet resistance or intrinsic dark-current density), a complex set of equations is formulated and solved simultaneously using numerical methods to determine the potential profile across the cell for a given output voltage or current. This can be accomplished via SPICE or MATLAB. An example of such a potential profile for a very simple cell with dual bus bars and perpendicular grid lines is shown in Figure 10; the plot shows the way in which the potential changes between grid lines and bus bars due to the lateral flow of current through the finite sheet resistance of the solar cell.

The applications of the quasi-3D model to the III-V/Si system are numerous; one such application of interest is to determine the necessary sheet resistance to achieve high efficiency. Figure 11 shows the absolute change in efficiency versus the sheet resistance of the cell, normalized to a sheet resistance that may be considered "state-of-the-art." The simulation assumed a 5mm x 5mm solar cell operating at 600X concentration, which is nearly optimal for this cell size with a "state-of-the-art" sheet resistance. The simulation data shows two important characteristics of the III-V/Si system: (1) even a 2X increase in sheet resistance from "state-of-the-art" would be expected to result in only a 0.5% decrease in efficiency, and (2) due to the lower current (but higher voltage) of the III-V/Si system, this technology is less sensitive to sheet resistance than a standard 3J concentrator device, and may provide some advantages for operation at high concentration.

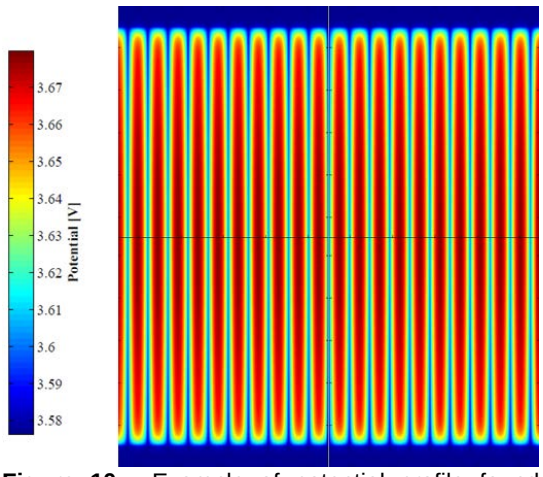


Figure 10. Example of potential profile found using quasi-3D model. Cell design has dual bus bars (top and bottom) and perpendicular grid lines. Potential builds between grid lines and bus bars in the active, illuminated area of the cell.

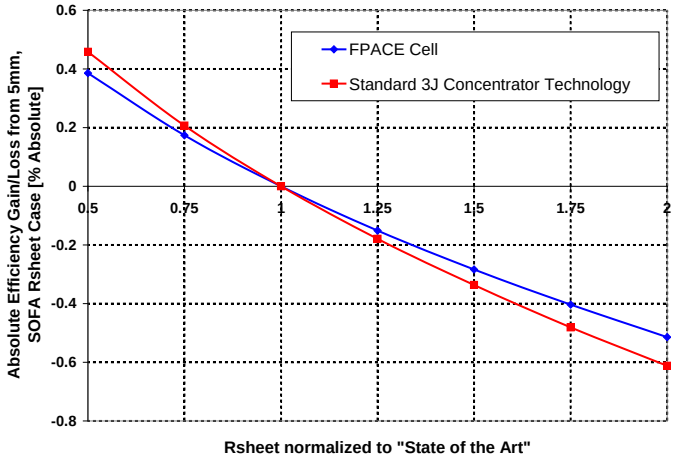


Figure 11. Absolute efficiency change versus sheet resistance, normalized to a "state-of-the-art" sheet resistance.

Highlight 2: Determination of the LCOE for System Design Optimization

A primary advantage of the III/V on active Si CPV system is the significant potential for cell- and system-level cost reductions. These reductions not only result from the decreased cost of the semiconductor substrate, but also by potential cost-reducing system changes that the decreased substrate cost would enable. Understanding the potential cost savings of the III/V on Si system as compared to a traditional Ge-based system is very difficult due to the complex nature of these systems and difficulty in projecting how the fundamental system design would change as the cost of the solar cell approaches zero.

As a result, SolAero developed a cost model aimed at estimating the LCOE (in cents/kWh) of the III/V on Si system. This model leverages cost models already in place at SolAero and uses SolAero's Gen3 system as a starting place. The cost model utilizes a set of system design parameters and cost factors to array for a given cell performance. A summary of the key input parameters to determine the tracker-array cost, which is used as a building block to ultimately determine system LCOE, is given in Table 3. In the context of this report, a receiver assembly consists of a solar cell (with all of the necessary sub-components), a heat sink, and all of the necessary optical components; a module consists of many receiver assemblies with all of the necessary enclosures and interconnects; finally, a tracker-array consists of many modules mounted on a tracking system. Shipping and freight costs are included at the module level while all of the remaining variable and fixed costs related to installation, permitting, land usage, etc. are included at the tracker-array level. The specifics of the Gen3 system are SolAero proprietary, so sub-component costs have largely been grouped into more general cost factors, as shown in Table 3. Note that many of the items given here include several individual components that are not listed separately.

The cell efficiency input is typically simulated using the Hovel's or long-term performance models. This efficiency is also derated throughout the cost calculation for factors such as inverter losses. The remaining performance and cost inputs are either known or

Table 3. Key cost model input parameters. Note that many of these items include several individual components.

Input	Units	Primary Impact on Tracker-Array Cost
Geometric concentration	Suns	Receiver and module components, tracker cost, array power output
Wafer diameter	mm	Receiver assembly cost via wafer packing factor
Cell size	mm	Cell performance, receiver assembly cost
Cell efficiency	%	Array power output
Optical efficiency	%	Array power output
Tracker area	m^2	Array power output
Module area	m^2	Module and array power output
Tracker cost	$/tracker	Array cost
Wafer cost	$/wafer	Receiver assembly cost
Wafer processing/labor cost	$/wafer	Receiver assembly cost
Automation of assembly	Yes/No	Receiver, module, and array cost
Receiver assembly components	$/receiver	Receiver assembly cost, array power output
Module components	$/module	Module cost
Freight	$/container	Module cost
Fixed costs (inverters, permitting, etc.)	$/W	Array cost

Table 4. Key input parameters for LCOE calculation. Note that the tracker-array cost (TC) is pre-calculated using the inputs given in Table 3.

Input	Units	Purpose/Impact
Monthly DNI (DNI)	kW/m^2/month	Determine available solar energy, system energy output
Effective system efficiency (η)	%	Determine system energy output
Nominal system size (S)	W	Determine number of tracker-arrays (initial capital), required system area
Tracker-array cost at operating temperature (TC)	$/W	Determine total capital cost, calculated using factors from Table 3
Margin (M)	%	Seller margin
Investment Tax Credit (c)	%	Tax credit for investment
Discount Rate (r)	%	Calculate net present value (NPV)
Array derating (ad)	%	Account for soiling, inverter losses, shadowing, etc.
Array degradation rate (ar)	%/yr	Yearly power degradation of each array
O&M Costs (OM)	%/yr	Operation and maintenance costs as a percentage of capital investment
Operational years (N)	yr	Number of years of operation
Inverter replacement cost (ir)	$/W	Cost to replace inverters
Inverter lifetime (IL)	yr	Length of time until inverter replacement

estimated based on available data. In very general terms, the cost of a tracker-array in $/W is simply the sum of the cost of the modules that fit onto a single tracker and the cost of the tracker itself, divided by the total power produced by the modules. The cost of the module is further divided into module and receiver costs, with the receiver costs broken down even further into sub-components.

Module level or tracker-array level costs are typically reported in $/W under standard conditions (28C, AM1.5D); however, because cell temperature has a significant impact on system efficiency, it must be included in the LCOE calculation. An approximation of the operational cell temperature can be achieved using estimated thermal resistance values. The effective on-sun system efficiency that results is used to calculate the required number of tracker-arrays for a nominal system size. The effective system efficiency and system size ultimately determine both the yearly energy production of the system as well as the initial capital that is required. The remaining key input parameters that are needed to calculate system LCOE are given in Table 4.

In general, LCOE can be expressed using the following expression,

$$LCOE = \frac{\text{Total Lifetime Costs}}{\text{Total Lifetime Energy Production}} \tag{3}$$

Here both the cost and energy production terms must be expressed in terms of their present value. For an initial capital investment, I_0, costs incurred in year t, I_t, and energy produced in year t, E_t,

$$LCOE = \frac{I_0 + \sum_{t=1}^{N} \frac{I_t}{(1-r)^t}}{\sum_{t=1}^{N} \frac{E_t}{(1-r)^t}} \quad (4)$$

In the model presented here, I_t is composed only of operations and maintenance costs as well as a full inverter replacement at year IL. The initial capital investment includes seller margin and the available tax credit. Energy produced depends upon the DNI of the chosen location, the system size/area, as well as derating factors that account for yearly array degradation and array derating. Using the input variables defined in Table 4,

$$LCOE = \frac{(TC \times (1+M) \times S \times (1-c)) \left[1 + OM \sum_{t=1}^{N} \frac{1}{(1+r)^t} \right] + \frac{ir \times S}{(1+r)^{IL}}}{DNI \times A \times \eta \times ad \times \sum_{t=1}^{N} \left(\frac{1-ar}{1+r} \right)^t}. \quad (5)$$

Note that all variables show in units of % must be applied to Equation 5 as fractions.

It is worth noting that numerous methods are available for calculating LCOE. The more accurate the method, the more information must be known about the cost structure and energy production. The method constructed here is still relatively simple but includes enough factors for reasonable accuracy.

Associated Publications:

Analysis of Short- and Long-Term Performance Goals for III/V on Active Si Concentrator Solar Cells

Alexander Haas, Paul Sharps, Daniel Aiken, Tyler Grassman, John A. Carlin, and Steven Ringel, *Proc. of 39th IEEE Photovoltaic Specialists Conference*, Tampa, FL (June 16-21, 2013).

A primary goal of terrestrial photovoltaics is to reach grid cost parity. This is a difficult task, largely due to the seemingly inverse relationship between efficiency and cost. Multijunction III/V solar cells on an active Si substrate may break this relationship by providing high efficiency with much lower material cost than traditional concentrator solar cells. This paper employs device models in the analysis of short- and long term performance goals and expectations for this material system. The modeling results presented here indicate that the III/V on active Si technology may be anticipated to achieve nearly 48% efficiency at 600 suns concentration in a long-term, high volume manufacturing regime and almost 39% in the short-term.

Designing Bottom Silicon Solar Cells for Multijunction Devices

Ibraheem Almansouri, Stephen Bremner, Anita Ho-Baillie, Hamid Mehrvarz, Xiaojing Hao, Gavin Conibeer, Tyler J. Grassman, John A. Carlin, Alexander Haas, Steven A. Ringel, and Martin A. Green, *IEEE J. Photovolt.*, vol. 5, pp. 683-690, 2015.

We report on efforts to design high-efficiency silicon homojunction subcells for use in multijunction stack devices. Both simulation and experimental works have been performed looking at a silicon solar cell under a truncated spectrum below 1.5 eV filtered by the upper layers in the multijunction stack. Good agreement is seen between the modeling and experimental results, identifying different emitter design requirements when the solar cell

operates under a full or truncated spectrum. A well-passivated front surface, i.e., with low-interface surface recombination velocity, required a lightly doped emitter profile to maximize open-circuit voltage (*V*OC), while a high-interface recombination surface requires a heavily doped for higher *V*OC values. The impact on short-circuit current density (*J*SC) is found to be minimal, even with large variations in the interface recombination and emitter profiles. In a tandem stack, an interface with low- and high-interface recombination velocities would require lightly doped and intermediate-doped emitters, respectively, for maximum conversion efficiency (η).

Task 3.0: Initial single junction sub-cell structures and prototyping
Task 4.0: Single junction sub-cell prototype optimization
Utilizing the PV-quality materials enabled in Task 1 of the program, these two tasks (through Phase I and Phase II) focused on the growth, fabrication and metrology of individual sub-cells integrated on Si at each bandgap of interest determined from modeling. Specifically, single junction GaAsP, GaInP, Si and SiGe PV devices were fabricated and device performance characterized. The effort yielded growth, fabricated and test of single junction devices to obtain performance characteristics and verify material and interface quality. Significant accomplishments related to these tasks included:

- First all-epitaxy GaP/Si subcell, formed within III-V MOCVD
- First integration of GaP on ex-situ Si PERT cell
- Designed optimal Si sub-cell for application in GaInP/GaAsP/active-Si 3J
- Demonstrated good performance 1.55 eV GaAsP metamorphic cell on Si for middle junction
- Demonstrated 2 eV GaInP Ga-rich metamorphic cell on Si for top junction
- Demonstrated SiGe 4th junction with 325 mV Voc to enable back-bonded Si-based 4J

While many of these efforts were regularly reported in journals, conference proceedings and conference presentations, the most significant of these accomplishments related to the sub-cell prototyping are highlighted below with a partial summary of key findings. Associated publications which include additional details are also listed below with brief abstracts included.

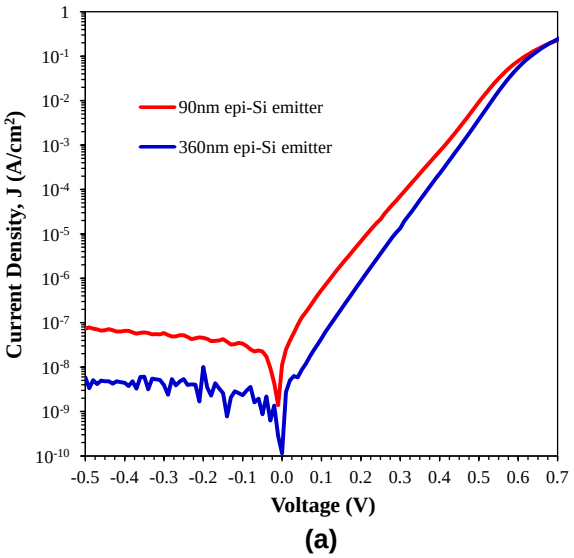
Highlight 1: Epitaxial Si sub-cell optimization

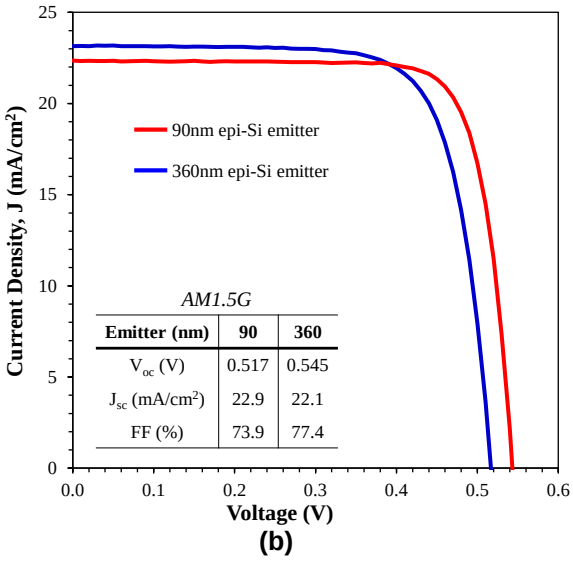
Optimization of the single-junction sub-cells was one key effort of this task building to the multi-junction devices. Here, to demonstrate the bottom cell GaP/active-Si epitaxial Si prototype devices were grown, fabricated into solar cells, and tested. In these devices the GaP served as front-side electrical contact (via metal grid) and window layer, with no further anti-reflection coating or texturization employed; back-side contact was achieved using blanket metal coverage, with no BSF layer or passivation employed. While these test structures were expected to yield substantial overall under-performance due to the lack of back-side minority carrier reflection and high SRV, the goal was to analyze the junction formation approach in general, as well as the performance of the GaP as a window layer.

Two different n-type ($N_D \sim 5x10^{17}$ cm^{-3}) epitaxial Si emitter thicknesses, 90 nm and 360 nm, were investigated, and measurement results are presented in Figure 12, including dark I-V (DIV), lighted I-V (LIV), and external/internal quantum efficiency (EQE/IQE). The important initial observation was that epitaxial junction formation, even in these early-stage, non-optimized

devices, was found to be successful, and yielded decent quality cells. Significant differences were found to exist between the two structures. Double-diode analysis of the dark I-V data (Fig. 12a) showed larger values of J_{01}, J_{02}, and n_2 for the thinner emitter structure, indicating a higher degree of carrier recombination within the device. Light I-V analysis (Fig. 12b) confirmed such a difference, with the thicker emitter structure yielding significantly larger average V_{oc} and FF values, 545 mV and 77.4%, versus the thin emitter's 517 mV and 73.9%, respectively. However, the thin emitter was found to yield a higher J_{sc}, 22.9 mA/cm^2, versus 22.1 mA/cm^2 for the thick emitter. IQE measurements (Fig. 12c) indicated that the difference in current was stemming from a reduction in short-wavelength performance for the thicker emitter structure, suggesting increased carrier loss within the emitter layer or at the front surface/interface. In both cases the poor performance in the long-wavelength region is due to the aforementioned lack of back-side processing (i.e. no BSF, no passivation, no texturization).

In order to better understand these experimental results, especially the differences in LIV and short-wavelength IQE between the two emitter layer thicknesses, the device structures in question were modeled using PC1D, the results of which are displayed in Figure 13. Empirical data and nominal/measured device structure details were





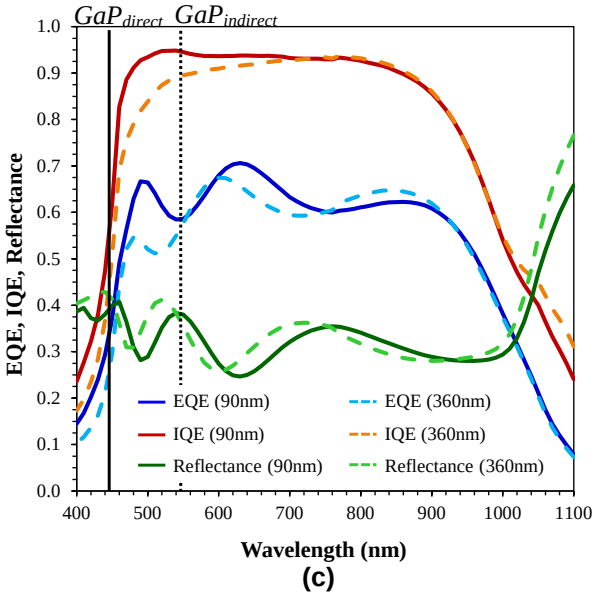


Figure 12. (a) Dark current-voltage, (b) AM1.5G illuminated current-voltage, and (c) quantum efficiency measurements of 90 nm and 360 nm thick epitaxial *n*-Si emitter GaP/Si prototype sub-cell structures. The solid and dotted vertical lines in part (c) denote the cutoff wavelengths corresponding to the minimum direct (2.78 eV, 446 nm) and indirect (2.27 eV, 546 nm) band gaps of GaP.

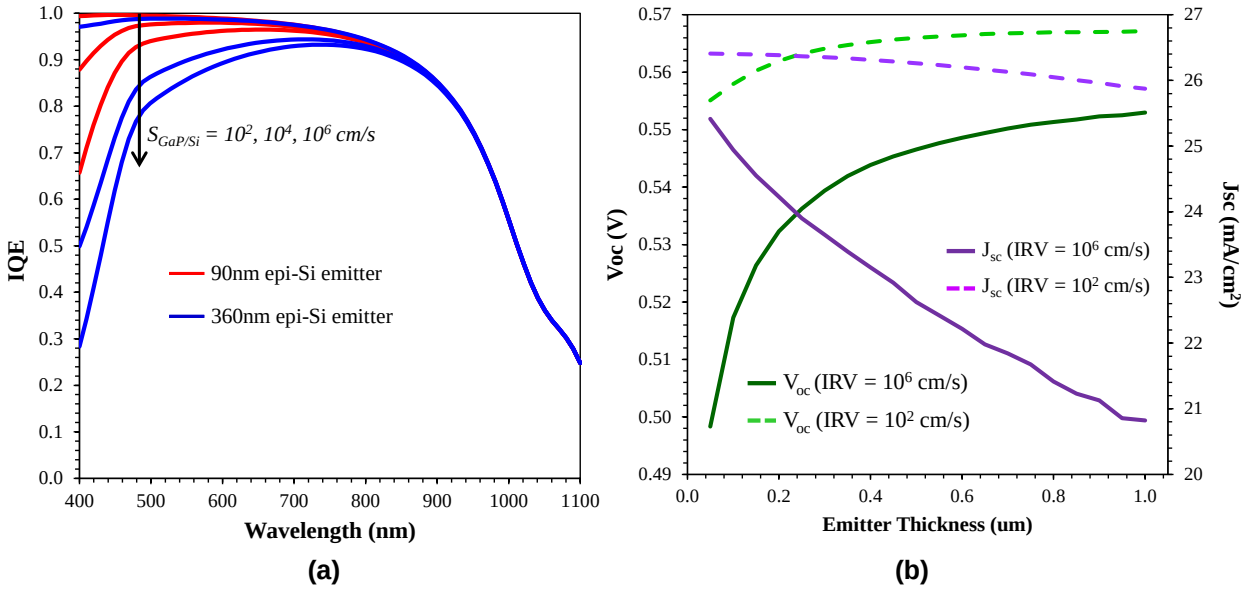


Figure 13. PC1D simulation results showing (a) IQE spectra of the two epitaxial Si emitter thicknesses (90 nm and 360 nm) over a range of GaP/Si IRV ($S_{GaP/Si}$), and (b) J_{sc} and V_{oc} trends versus emitter thickness for high (10^6 cm/s) and low (10^2 cm/s) IRV values.

used for input where possible and any remaining parameters were chosen to achieve reasonable agreement with the experimental LIV and EQE/IQE data (i.e. EQE/IQE shapes and approximate magnitudes; LIV-based V_{oc} and J_{sc}). All parameters, other than emitter layer thickness and any other specific material/structure parameter of interest, were identical and fixed for the two sub-cell structures. Fig. 13a presents simulated IQE spectra for the two structures with respect to a range of GaP/Si interface recombination velocity (IRV) values, ranging from relatively low (100 cm/s) to relatively high (10^6 cm/s). Of note here is the substantially higher sensitivity of the thicker emitter structure to higher IRV values, and the difference in short-wavelength response between the two different structures at higher IRV values that is consistent with experimental results. This modeling then suggests that the IRV at the GaP/Si interface in these unoptimized test devices is likely in the range of 10^4 – 10^6 cm/s. With respect to LIV measurements, Fig. 13b presents a comparison of J_{sc} and V_{oc} versus emitter thickness for low (100 cm/s) and high (10^6 cm/s) IRV values. Here again we find that the simulated results for the higher IRV value are consistent with those measured from the test devices, confirming the conclusion of relatively high GaP/Si IRV and its impact on the relative performance for different emitter layer thicknesses.

These results indicate that a significant engineering window for further device performance improvement is available and can be expected with continued growth optimization of both the GaP/Si interface and the epitaxial Si emitter. Dislocation reduction and general interfacial defect mitigation, efforts that are currently in progress, as well as the possible introduction of a thin, highly-doped Si minority carrier reflection layer immediately below the GaP/Si interface, should yield significantly improved IRV numbers, while optimization of MOCVD Si growth methods and conditions will ensure that the epitaxial emitter is not a limiting agent. Additionally, as is the case for all Si-based photovoltaics, back-side processing, using either a BSF or dielectric passivation to provide for minority carrier reflection and low SRV, as well as some kind of photon management through texturization or even just a planar reflector,

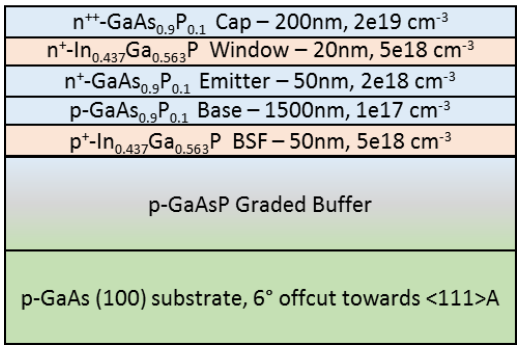


Figure 14. GaAsP subcell design grown by MOCVD.

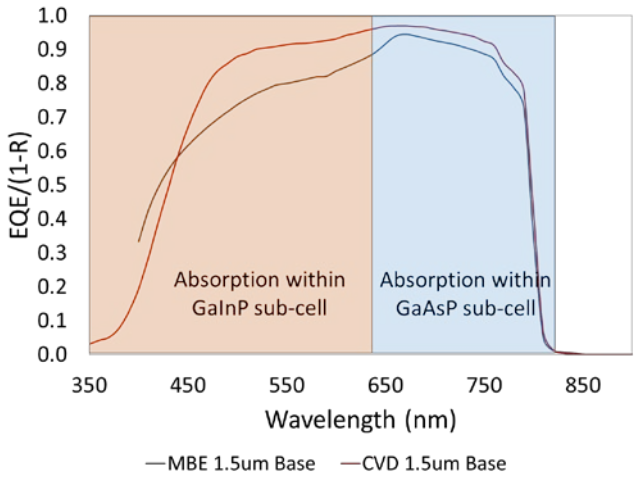


Figure 15. Quantum efficiency [EQE/(1-R)] comparison of MOCVD and MBE grown GaAsP subcells. Improved short wavelength response is primarily due to the reduced thickness in the window layer.

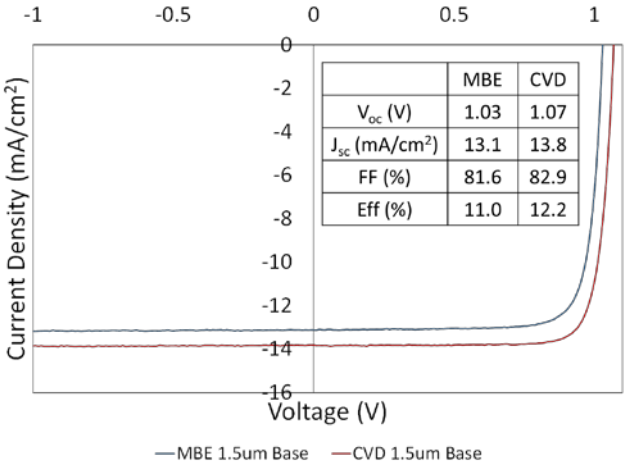
will substantially improve long-wavelength response and will provide for a large boost in overall active-Si junction performance.

Highlight 2: MOCVD GaAsP Middle Subcell Development

This task also resulted in the successful growth of a GaAsP subcell via MOCVD on a $GaAs_{0.9}P_{0.1}/GaAs_yP_{1-y}/GaAs$ SGB template prior to moving to a Si substrate. The cell design, similar to that of a prior prototype grown via MBE, is shown in Figure 14. Figure 15 shows the quantum efficiency, EQE/(1-R), results for the MOCVD growth in comparison the that obtained for prior samples grown by MBE. No anti-reflection coating was applied to either cell. As shown in Figure 15, the MOCVD grown subcell demonstrates a slightly improved collection efficiency compared to it's MBE counterpart within the target bandwidth for the GaAsP subcell (nominally > 630nm in the targeted MJ design). Note that the the significant improvement at short wavelengths is attributed to the thinner window used in the MOCVD subcell design. Figure 16 shows a 1-sun AM1.5G lighted JV comparison for the same two cells. Noting that the higher Jsc for the MOCVD grown subcell is in large part due to the thinner window design, relative to the MBE cell design, the initial MOCVD cell shows an increase in V_{oc} (from 1.03V to 1.07V), efficiency (from 11.0% to 12.3%) and fill factor (from 81.5% to 82.9%) indicating very promising material quality for these initial growth conditions, prior to systematic optimization.

Highlight 3: MOCVD GaInP Top Subcell Development

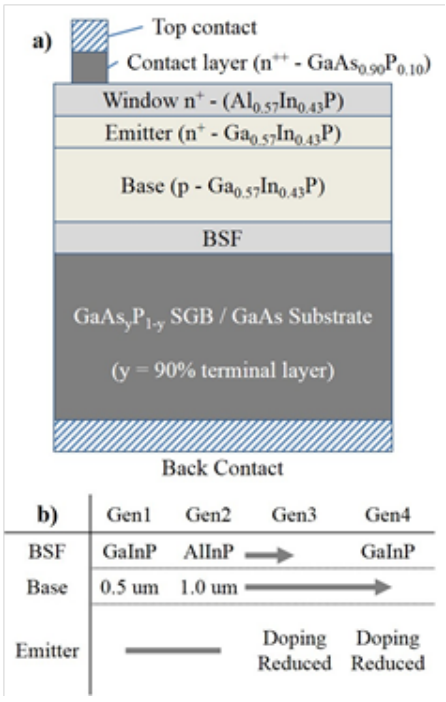
This section describes key optimization effort for the single-junction $Ga_{0.57}In_{0.43}P$ top cell grown by MOCVD. The basic cell design is shown in Figure 17(a) and various design modifications investigated this period are shown in Figure 17(b). The initial target doping levels of the p-type base and n-type emitter were $N_A(Zn) = 5\times10^{16}$ cm^{-3} and $N_D(Si) = 2\times10^{18}$ cm^{-3}, respectively. As noted in Fig. 17(b), the cells are referred to as Gen1, Gen2, Gen3, and Gen4 for convenience. The quantum efficiency and lighted current-voltage results are shown in Figures 18 and 19, respectively, and the tabulated LIV parameters are given in Table 5.



	MBE	CVD
V_{oc} (V)	1.03	1.07
J_{sc} (mA/cm²)	13.1	13.8
FF (%)	81.6	82.9
Eff (%)	11.0	12.2

Figure 16. Lighted JV curves under 1-sun AM1.5G of original MBE cell and initial CVD cell design. The improved design results in an overall improvement in cell performance. (No ARC applied)

Of the first two cells grown, Gen1 and Gen2, Gen1 was designed to mimic the structure of the best of previously grown MBE cells, with an n^+-$Al_{0.57}In_{0.43}P$ window and a p^+-$Ga_{0.57}In_{0.43}P$ doping-offset BSF. Gen2 used a thicker, 1.0 µm, base and a p^+-$Al_{0.57}In_{0.43}P$ BSF. While the EQE curves clearly show the benefit of using the thicker base, these two cells were severely limited by some detrimental front-side effect, indicated by the poor short wavelength response. This kind of effect could be due to a poor window/emitter interface in which a high interface recombination velocity acts as a sink for carriers, killing the collection of any minority carriers (rather than reflecting them) that make it to the front-side interface, or a poor quality emitter in which the probability of minority carriers recombining before diffusing to the depletion region is high. Several experiments involving test layers mimicking the target compositions and doping levels of the window and emitter were carried out to solve this problem. It was determined that the dopant concentration in the emitter was substantially higher than intended; C-V measurements revealed a carrier concentration of just over 1×10^{19} cm^{-3} and Hall effect returned 4.5×10^{18} cm^{-3}. (A discrepancy in these measurements is typically due to the fact that C-V is sensitive to the total ionized donor concentration, while Hall effect concerns only the free carriers.) This result indicates a significantly different cracking efficiency of silane in the growth of $Ga_xIn_{1-x}P$ than for GaAs and $GaAs_{0.90}P_{0.10}$, which were used as doping calibrations grown at 600°C and 650°C; this is the subject of ongoing investigation.



b)	Gen1	Gen2	Gen3	Gen4
BSF	GaInP	AlInP →		GaInP
Base	0.5 um	1.0 um →		
Emitter	—		Doping Reduced	Doping Reduced

Figure 17: (a) General structure of the MOCVD-grown $Ga_{0.57}In_{0.43}P$ solar cells. (b) Table indicating the changes made to the BSF material, base thickness, and emitter doping during the optimization process of these devices.

Gen3 and Gen4 designs were grown with emitter doping levels reduced by 3x and 5x versus the Gen2 values, respectively. The result of this change is evident in the quantum efficiency curves (Figure 18), which show an enormous improvement not only in the short wavelength region, but over the entire range of response. This improved carrier collection is also evident in the associated LIV data (Figure 19, Table 5). The magnitude of this impact shows that the excess Si dopant present in the emitter wreaked havoc with the material quality of

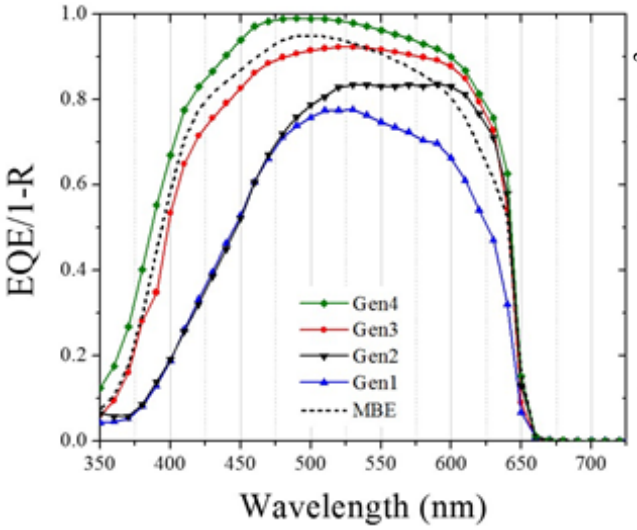


Figure 18. Quantum efficiency measurements performed on the MOCVD-grown solar cell structures from Figure 16(b). The best performing MBE-grown solar cell is shown for comparison and represented by the dashed line.

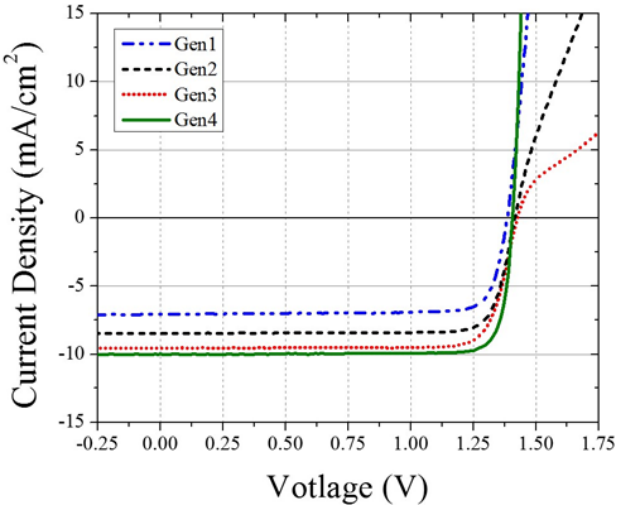


Figure 19: LIV characteristics comparing MOCVD-grown solar cells grown at 625°C.

Table 5: One-sun, room temperature, AM1.5G LIV measurement results of $Ga_{0.57}In_{0.43}P$ solar cells grown on GaAs substrates following the optimization routine depicted in Figure 16. The best performing MBE-grown solar cell is also included for comparison.

Sample	Gen1	Gen2	Gen3	Gen4	MBE
V_{OC}(V)	1.39	1.40	1.42	1.41	1.34
J_{SC} (mA/cm^2)	7.06	8.48	9.55	9.98	9.56
FF (%)	85.4	84.2	82.9	86.5	86.4

the layer. As Si is known to occupy group V sites at sufficiently high concentrations, compensating Si acceptor levels were also likely present, further inducing carrier recombination.

C-V based measurements of the resultant emitter doping concentration in the Gen3 structure (as determined using independently grown test layers) determined a carrier concentration of 5.6×10^{18} cm^{-3}. This is still larger than the target, and the additional carrier collection observed from Gen3 to Gen4, with an additional reduction in silane flow, reflects this. The J_{SC} measured for Gen4 exceeds that of the best MBE-grown cell. Despite a slight reduction in V_{OC} from Gen3 to Gen4, likely the result of the reduced emitter doping (and thus smaller emitter-to-base ratio), the overall cell performance was much improved, with both J_{SC} and fill factor (FF) showing significant increases. Note that these latter improvements are likely due to a combination of both emitter and BSF optimization, as discussed below.

Another point of investigation during the design optimization was the BSF layer. Gen2 and Gen3, which used an $Al_{0.57}In_{0.43}P$ BSF, each had lower fill factors than Gen1 and also displayed a very strong series resistance-like effect on the current just past V_{OC}, as seen in the LIV curves of Figure 19. To investigate this issue, an independent $Al_{0.57}In_{0.43}P$ test layer was grown and characterized. Results from Hall effect measurements revealed the p-type carrier

concentration to be only 1×10^{17} cm^{-3}, more than an order of magnitude below the target value, 3×10^{18} cm^{-3}. Due to its wide bandgap and reasonably favorable conduction band offset (assuming high achievable doping in the BSF layer) with respect to $Ga_xIn_{1-x}P$ (at least as reported for $Ga_{0.51}In_{0.49}P$ lattice matched to GaAs [12]), this layer was expected to provide an effective blocking layer for minority carriers, and as such the long wavelength response for Gen3 appeared to support this. However, an important consequence of the low doping is that a significant portion of the band offset actually ends up residing within valence band (i.e. a thick band discontinuity tunnel barrier), thereby impeding majority carrier flow in the device. The IV data suggests that at some forward bias, just past V_{OC}, this effect dominates the transport in the device and results in an effective series resistance.

For Gen4, along with the continued decrease in emitter doping, the BSF was switched back to a homojunction p^+-$Ga_{0.57}In_{0.43}P$ doping offset layer. Although this approach will yield a much smaller degree of minority carrier reflection than a proper heterojunction structure, the fill factor for Gen4 was the best of all cells measured, including the previous MBE cells. Removing the low doped, resistive $Al_{0.57}In_{0.43}P$ layer most likely results in a lower overall series resistance and a better quality diode.

The inability to highly dope $Al_{0.57}In_{0.43}P$ with Zn in the MOCVD system is actually a well-known issue, with its origins in the LED field since these high bandgap materials were of interest to achieve different wavelengths of visible emission [13]. There are several issues with dimethyl zinc (DMZn) as a p-type dopant for $Al_xIn_{1-x}P$. First, as the Al content is increased, the ionization energy of the Zn acceptors increases, reducing the concentration of free carriers at room temperature. Second, higher compositions of Al incorporate higher concentrations of oxygen, which act as compensating deep levels. Finally, DMZn is volatile and requires a very high partial pressure to achieve high doping, which can lead to material quality problems. This was observed in this work when an attempt to increase the doping of the $Al_{0.57}In_{0.43}P$ layers by increasing the Zn flow resulted in visibly non-specular samples.

Just as for the MBE-grown cells, more investigation is needed to fully exploit the potential benefits of large bandgap, Al-containing BSF layers. In contrast to the MBE-grown samples, where p^+-$Al_{0.57}In_{0.43}P$ could be used as the BSF material, the difficulty in achieving highly doped p-type $Al_{0.57}In_{0.43}P$ in the MOCVD growth system precludes it from consideration. Lower Al-content quaternary compounds should allow for higher p-type doping. One composition is currently under investigation and in fact a preliminary $(Al_{0.15}Ga_{0.85})_{0.57}In_{0.43}P$ sample grown by MOCVD successfully demonstrated p-type doping to a target concentration of 1×10^{18} cm^{-3}. Additionally, according to literature on LED materials lattice-matched to GaAs [12], a composition of $(Al_{0.55}Ga_{0.45})_{0.57}In_{0.43}P$ should actually provide the best combination of large conduction band offset and minimal valence band offset, making it a worthwhile target for further investigation.

Associated Publications:

MOCVD-Grown GaP/Si Subcells for Integrated III–V/Si Multijunction Photovoltaics
T. J. Grassman, J. A. Carlin, B. Galiana, F. Yang, M. J. Mills and S. A. Ringel, *IEEE J. Photovolt.*, vol. 4, pp. 972-980, May (2014).

Enabled by a heteroepitaxial nucleation process that yields GaP-on-Si integration free of heterovalent-related defects, GaP/active-Si junctions were grown by metalorganic chemical vapor deposition. n-type Si emitter layers were grown on p-type (1 0 0)-oriented Si substrates, followed by the growth of n-type GaP window layers, to form fully active subcell structures

compatible with integration into monolithic III–V/Si multijunction solar cells. Fabricated test devices yield good preliminary performance characteristics and demonstrate great promise for the epitaxial subcell approach. Comparison of different emitter layer thicknesses, combined with descriptive device modeling, reveals insight into recombination dynamics at the GaP/Si interface and provides design guidance for future device optimization. Additional test structures consisting of GaP/active-Si subcell substrates with subsequently grown GaAs$_y$P1$-y$ step-graded buffers and GaAs0.75P0.25 terminal layers were produced to simulate the optical response of the GaP/Si junction within a theoretically ideal dual-junction solar cell.

Ga-rich $Ga_xIn_{1-x}P$ solar cells on Si with 1.95 eV bandgap for ideal III-V/Si photovoltaics
Chris Ratcliff, T.J. Grassman, J.A. Carlin, D.J. Chmielewski, S.A. Ringel, *Proc. SPIE* 8981, Physics, Simulation, and Photonic Engineering of Photovoltaic Devices III, 898118 (7 March 2014).

Theoretical models for III-V compound multijunction solar cells show that solar cells with bandgaps of 1.95-2.3 eV are needed to create ideal optical partitioning of the solar spectrum for device architectures containing three, four and more junctions. For III-V solar cells integrated with an active Si sub-cell, GaInP alloys in the Ga-rich regime are ideal since direct bandgaps of up to ~ 2.25 eV are achieved at lattice constants that can be integrated with appropriate GaAsP, SiGe and Si materials, with efficiencies of almost 50% being predicted using practical solar cell models under concentrated sunlight. Here we report on Ga-rich, lattice-mismatched Ga0.57In0.43P sub-cell prototypes with a bandgap of 1.95 eV grown on tensile step-graded metamorphic GaAsyP1-y buffers on GaAs substrates. The goal is to create a high bandgap top cell for integration with Si-based III-V/Si triple-junction devices. Excellent carrier collection efficiency was measured via internal quantum efficiency measurements and with their design being targeted for multijunction implementation (i.e. they are too thin for single junction cells), initial cell results are encouraging. The first generation of identical 1.95 eV cells on Si were fabricated as well, with efficiencies for these large bandgap, thin single junction cells ranging from 7% on Si to 11% on GaAs without antireflection coatings, systematically tracking the change in defect density as a function of growth substrate.

Ideal GaP/Si Heterostructures Grown by MOCVD: III-V/Active-Si Subcells, Multijunctions, and MBE-to-MOCVD III-V/Si Interface Science
S. A. Ringel, J. A. Carlin, T.J. Grassman, B. Galiana, A.M. Carlin, C. Ratcliff, D. Chmielewski, L. Yang, M.J. Mills, Al Mansouri, S. P. Bremner, A. Ho-Baillie, X. Hao, H. Mehrvarz, G. Conibeer, and M. A. Green, *Proc. of 39th IEEE Photovoltaic Specialists Conference*, Tampa, FL (June 16-21, 2013).

High-quality, heterovalent nucleation of defect-free epitaxial GaP on (100)-oriented Si substrates is an enabling accomplishment toward a pathway for the creation of III-V/Si multijunction photovoltaic devices in which the Si growth substrate can simultaneously act as a near-ideal sub-cell through a monolithic metamorphic GaInP/GaAsP/Si structure. While recent efforts have achieved this goal via molecular beam epitaxy (MBE), the science developed in those efforts is fundamental to the GaP/Si interface. Here this knowledge is utilized to achieve the successful transition from MBE to an all-MOCVD (metal-organic chemical vapor deposition) process, in which all nucleation-related defects are simultaneously and totally avoided for ideal GaP/Si interfaces and subsequent metamorphic III-V materials. Four main topics are presented: (1) GaP/Si(100) grown by MOCVD free of antiphase domains and stacking

defects; (2) growth, fabrication, and testing of GaP/active-Si sub-cells; (3) MOCVD/MBE-grown GaAsP/active-Si multijunction structures and component cells having target lattice constants and bandgaps for high efficiency dual and triple junction cells, and (4) comparative interface studies of MBE- and MOCVD-grown III-V/GaP/Si cell architectures.

Task 5.0: Multijunction Cell Component Development

In addition to the active photon-collecting sub-cell components of a multijunction device, the final conversion efficiency achievable is also dictated by additional internal and external components required to integrate the sub-cells into a full device. This task concentrated on tunnel junctions, ohmic contacts and anti-reflection coatings which all play a major role in final device performance. Fortunately, a successful ohmic contact was realized using a similar design to that already established by SolAero for their 3J production devices. The realization of an optimized metamorphic tunnel junction however required much more development. Significant accomplishments related to this task included:

- Developed and demonstrated first robust metamorphic tunnel junctions at target lattice constants on Si by MBE and MOCVD that can withstand high concentration, exceeds all comparable devices with record peak current achieved *[J_p = 245A/cm^2 (1.55eV), J_p = 140A/cm^2 (1.95eV)]*
- Developed very high performance ohmic contacts on metamorphic GaInP with contact resistance < 5x10^{-6} ohm-cm^2
- Developed ARC design achieving 3.9% SWR (3J) and 5.2% (4J)

While much of the development efforts were regularly reported in journals, conference proceedings and conference presentations, the most significant of these accomplishments related to the component development are highlighted below with a partial summary of key findings. Associated publications which include additional details are also listed below with brief abstracts included.

<u>Highlight 1: GaAsP Tunnel Junction Development – OSU (MOCVD)</u>

A significant effort during this task was concentrated on the development of a GaAsP homojunction tunnel junction (TJ) and double hetero-structure TJ (DHTJ) via MBE and the transition of those structures to the MOCVD environment. For this effort a new carbon doping source ($CBrCl_3$) was added to OSU's MOCVD system for the specific purpose of providing p-type doping in tunnel junctions. Carbon is known for its low diffusivity and high incorporation/activation, as well as small/negligible memory effects compared to Zn (the other p-type dopant available on the system), which makes it ideal for use in tunnel junctions where it should provide better thermal stability than that achieved with the available MBE precursors, Si and Be. After installation, we grew a number of different C-doped GaAs and $GaAs_{0.9}P_{0.1}$ samples to calibrate doping with the new source. The hole concentration in C-doped GaAs for various combinations of precursor flow, V/III ratio, and substrate temperature are shown in Figure 20. From Fig. 20A it is clear that there is a "sweet spot" in precursor flow for achieving the highest possible doping. At too low of a flow, not enough C is incorporated. At too high of a flow, the chlorine and bromine containing precursor etches the GaAs as it grows (determined by *in situ* monitoring of film growth rates). At higher flows the etch rate increases and the doping achieved decreases. For our desired range of growth conditions, a flow of 25 sccm of $CBrCl_3$

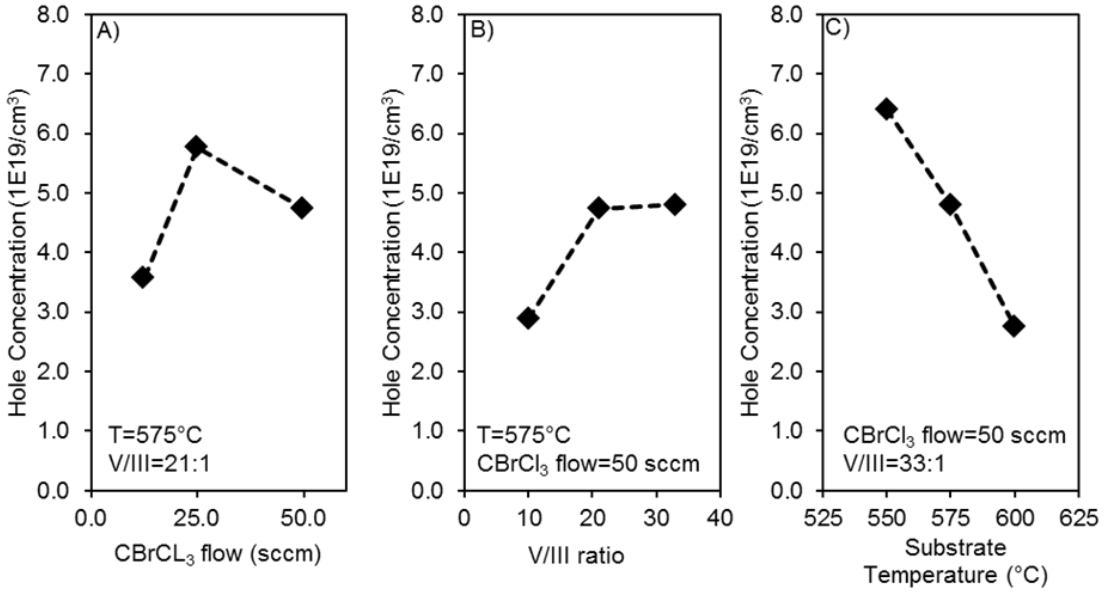
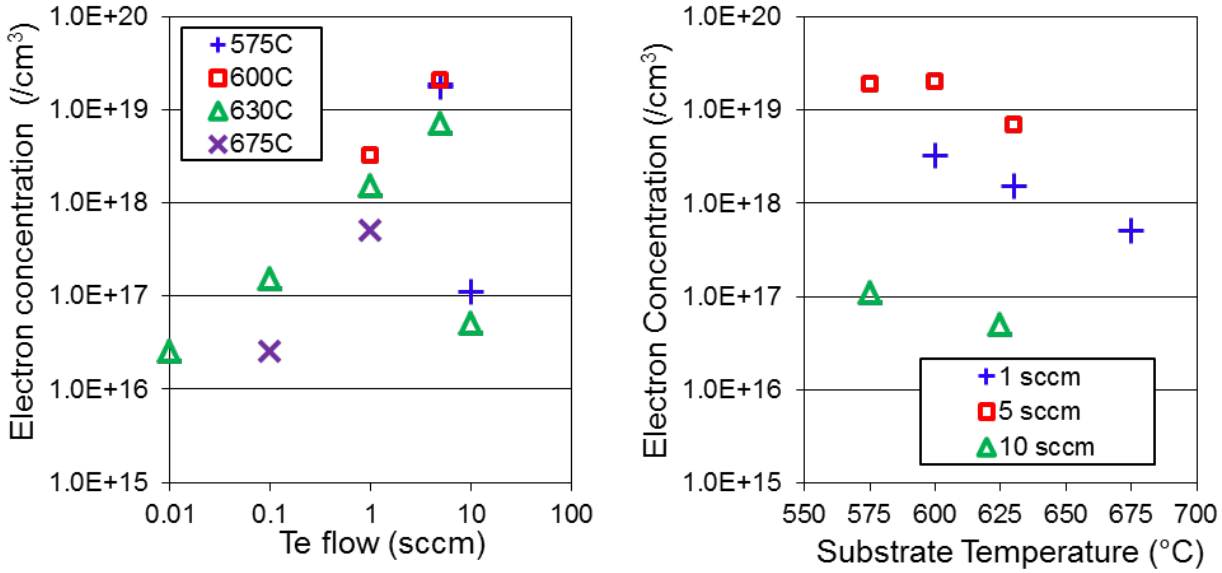


Figure 20: Hole concentration in MOCVD grown GaAs epilayers as a function of A) C precursor flow, B) V/III ratio, and C) substrate temperature.

was found to provide optimum doping. In Figure 20B, hole concentration as a function of V/III ratio is also provided. Intuitively, one might think that a lower V/III would increase hole doping since C dopants sit on group V lattice sites and a reduced V/III will lead to less competition to populate those sites. However, our findings show that a lower V/III actually *decreases* hole concentrations. This is again apparently related to etching during deposition. At reduced V/III ratios etching from $CBrCl_3$ is increased, which we believe is leading to the counter-intuitive results decreasing hole concentrations from lower V/III ratios. Finally, in Figure 20C hole concentration as a function of substrate temperature is shown. The trend is clear in this case; lower substrate temperature leads to higher hole concentrations. However, growing by MOCVD places some restrictions on the range of convenient temperatures that can be used during growth (mostly due to reduced precursor cracking at low temperatures). With this in mind a growth temperature of 575°C was selected for high C-doped GaAs or $GaAs_{0.9}P_{0.1}$.

Additional calibrations of Te-doped layers (DETe precursor) were also needed to form tunnel junctions. Luckily, previous samples grown on the OSU MOCVD system had already been used to calibrate Te doping from as low as 1×10^{16} cm^{-3} to as high as 1×10^{18} cm^{-3}. Therefore, only a small number of samples were needed to push the doping higher, targeting the low 10^{19} cm^{-3} range. Different combinations of Te-doped GaAs and $GaAs_{0.9}P_{0.1}$ are shown in Figure 21. Either Hall or Hg probe measurements were used to determine electron concentrations in all samples. The plot of electron concentration vs. Te flow [Figure 21(a)] shows that doping increases with flow until roughly 5 sccm. After this point there is a sharp decrease in doping, possibly due to the formation of a Te-based precipitate within the GaAs(P) matrix. The same data is plotted again in Figure 21(b), only with electron concentration plotted as a function of the substrate temperature during growth. When viewed this way, it appears that the maximal doping incorporation comes at ~600 °C. However, since there is very little drop off between 575 and 600 °C and since it would be beneficial to grow both sides of the tunnel junction at the same substrate temperature to avoid the incorporation of unwanted/uncontrolled impurity at the



(a)

Figure 21: Electron concentrations in Te doped GaAs and $GaAs_{0.9}P_{0.1}$ samples as a function of Te precursor (DETe) flow and substrate temperature.

interface between the two sides, 575°C was also the growth temperature chosen for the Te-doped side of the tunnel junction.

With high doping in both n-$GaAs_{0.9}P_{0.1}$ and p-$GaAs_{0.9}P_{0.1}$ achieved, it is possible to form tunnel junctions at the correct lattice constant for integration into the overall target multijunction solar cell. However, as modelled and discussed in prior reports, forming a tunnel junction using this alloy lead to significant optical absorption in the top tunnel junction, thus taking photons away from middle sub-cell. To prevent this, highly doped materials with band gaps wider than that of $GaAs_{0.9}P_{0.1}$ need to be investigated further. On the n-type side, we chose InGaP and on the p-type side of the tunnel junction we chose AlGaAsP, both lattice-matched to $GaAs_{0.9}P_{0.1}$. In the former case, we observed very similar doping levels to what was achieved in GaAs and $GaAs_{0.9}P_{0.1}$ layers doped under similar conditions. In the case of C-doped AlGaAsP, we expected much larger doping levels compared to GaAs and $GaAs_{0.9}P_{0.1}$ since Al is known to getter C atoms. However, our initial attempts did not show any increase when Al was added to the layers. Because initial attempts to achieve higher hole concentrations in C-doped AlGaAsP (compared to what we had previously achieved in C-doped GaAs and GaAsP) were unsuccessful, we began investigating post-growth anneals of AlGaAsP samples.

The plot in Figure 22 shows hole concentrations measured in the same samples before and after annealing. All samples in this plot were annealed for 5 minutes at 480 °C under a nitrogen overpressure. The anneal drives off hydrogen atoms that have bonded to (and thus passivated) C dopants. [14] While providing some increase in the effective doping for all the C-doped materials, Figure 22 demonstrates that the effect of the anneal is strongest in C-doped AlGaAsP. After the anneal, multiple samples were shown to have hole concentrations higher than 1×10^{20} cm^{-3}. None of the C-doped GaAs or GaAsP samples showed doping in this range before the anneal. The data in Figure 22 also shows a slight decrease in electron concentration after annealing in Te-doped layers However, the reduction in electron concentration of Te-doped

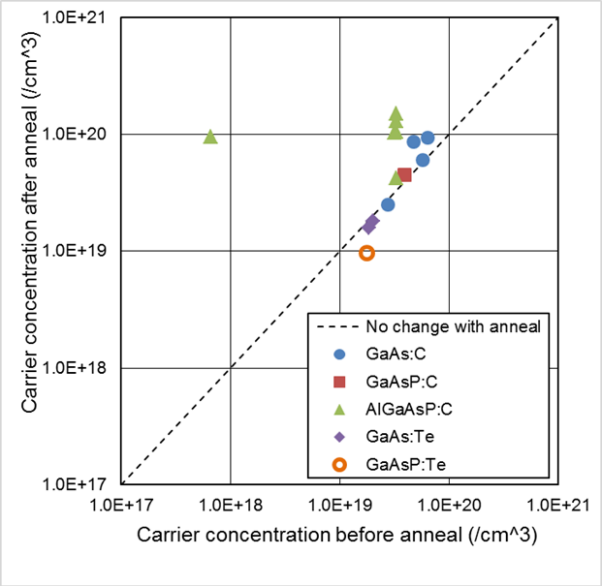
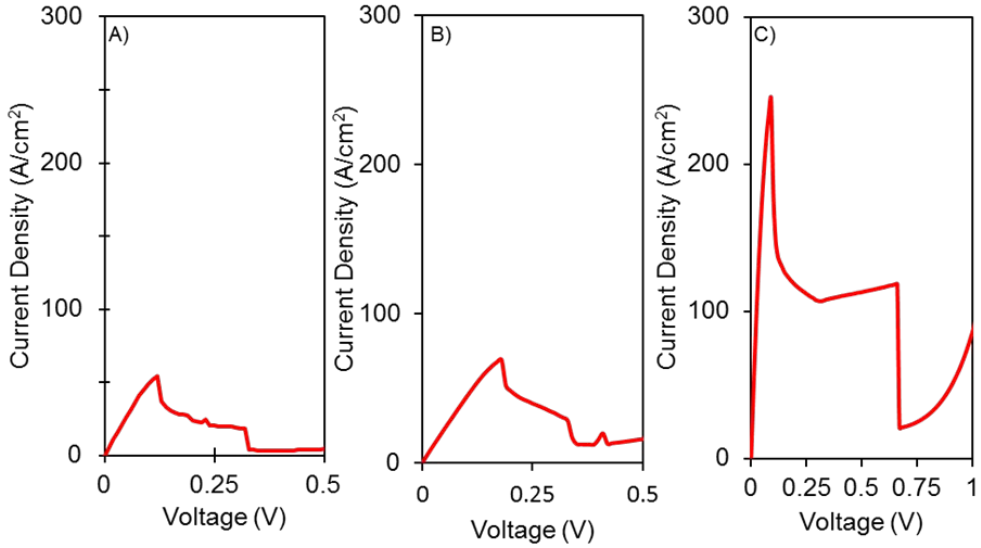


Figure 22: Carrier concentrations before and after anneal in a variety of C and Te doped alloys.

samples is small compared to the increase in hole concentration seen in C-doped AlGaAsP. Therefore, post growth anneals of tunnel junctions can be used to effectively activate doping in future devices. Once the doping was calibrated, it was possible to try a range of tunnel junction structures. Results from three such trial structures are shown in Figure 23. All n- and p-type layers in the tunnel diode structures described in Figure 22 are 25 nm thick.

As an initial trial we formed a GaAs homojunction tunnel junction on GaAs (shown in Figure 23A). While the devices demonstrated lower performance than similar device structures grown via MBE, the peak tunneling current and junction resistance are a successful proof-of-concept for the first tunnel diodes grown with OSU's MOCVD system. Since a GaAs homojunction tunnel junction cannot be used within our target multijunction design, this device was not pursued beyond the first sample grown in favor of concentrating on lattice matched designs. Therefore, as a next step we formed another



Tunnel Junction (TJ) Name	n-type side of TJ	p-type side of TJ	Peak Tunneling Current [A/cm²]	Resistance-area product [Ω-cm²]
A: GaAs homojunction	GaAs:Te	GaAs:C	52.9	1.41E-03
B: GaAsP homojunction	$GaAs_{0.9}P_{0.1}$:Te	GaAs0.9P0.1:C	69.3	2.00E-03
C: GaAsP/AlGaAsP	$GaAs_{0.9}P_{0.1}$:Te	$Al_{0.4}Ga_{0.6}As_{0.9}P_{0.1}$:C	244.6	2.10E+04

Figure 23: Current-voltage characteristics for three tunnel junctions designs, along with relevant device characteristics.

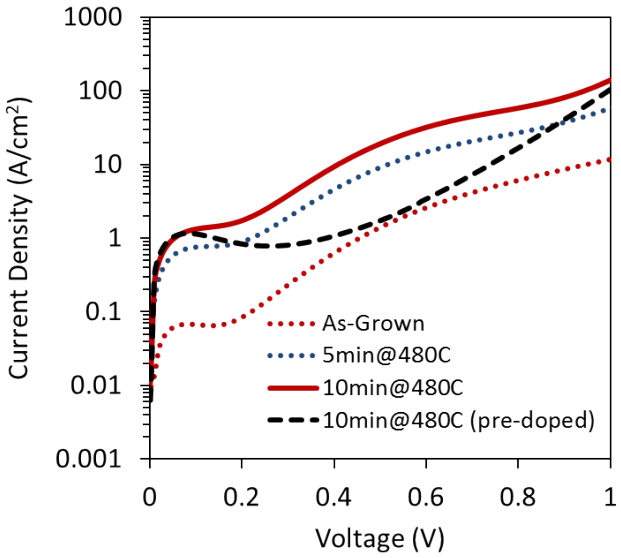


Figure 24: Current-voltage characteristics of different variations of an n-InGaP/p-AlGaAsP tunnel junction heterostructure.

homojunction tunnel junction, this time consisting of highly doped p- and n-$GaAs_{0.9}P_{0.1}$ on a tensile buffer on GaAs. Somewhat surprisingly, this structure outperformed the GaAs tunnel junction in terms of peak tunnel current (see Figure 23B), though the difference between the two could be attributed to variations in processing or even slight variations in the c doping level as discussed later. While this device works well and has the correct lattice parameter to be added into our multijunction design for the bottom tunnel junction, it cannot be used as the upper tunnel junction due to parasitic optical absorption with respect to the middle sub-cell. Furthermore, this design does not take advantage of the high p-doping demonstrated in C-doped AlGaAsP quaternary. With this in mind, a third tunnel junction structure using n-GaAsP and p-AlGaAsP was grown. The I-V characteristics for a representative device are shown in Figure 23C. By replacing GaAsP with AlGaAsP in the p-type side only, the peak tunneling current increased by more than a factor of 3, suggesting that the higher hole concentration in the p-type side of the junction (which should increase tunneling by narrowing the junction depletion region) more than offsets the reduction one would anticipate by using the wider gap AlGaAsP material (which would serve to increase the barrier height of the junction). Even though the device performance of the p-AlGaAsP/n-GaAsP tunnel junction is impressive, the 25 nm of n-GaAsP is still undesirable due to unwanted optical absorption. For this reason we have also investigated replacing the n-GaAsP with wider band gap n-InGaP and creating an p-AlGaAsP/n-InGaP structure similar to that demonstrated by SolAero last period. The I-V characteristics for several variations on this structure are shown in Figure 24. Initially the structure was grown using our typical growth procedures and processed in three variations; (1) as-grown, (2) annealed for 5 minutes and (3) annealed for 10 minutes at 480°C in the RTA for doping activation. As expected, the 5 minute anneal resulted in increased device performance, approximately an order of magnitude, while additional annealing resulted in only slightly more improvement. However, the peak tunneling current (somewhat ambiguous do to the high excess tunneling current beyond ~0.2V) is only ~1A/cm^2 at ~0.1V, and the zero-bias resistance is high at 4×10^{-2} Ω·cm^2. While neither meets the target milestones, based on the doping studies and prior SolAero characterization results of InGaP, it seems reasonable to assume that the Te doping of InGaP is likely limiting the device performance. Not only is the Te doping level much lower than that of C but Te has also been shown to have an onset effect in CVD in which Te does not incorporate immediately into the growing layer. [15] Thus, it is possible that even though our doping study results indicated that we were achieving doping around 2×10^{19} cm^{-3} in ~1μm thick Hall samples, the doping could be lower in the thin 25nm layer in the tunnel junction. As a result, an additional structure was grown including a Te pre-doping step in the n-type tunnel

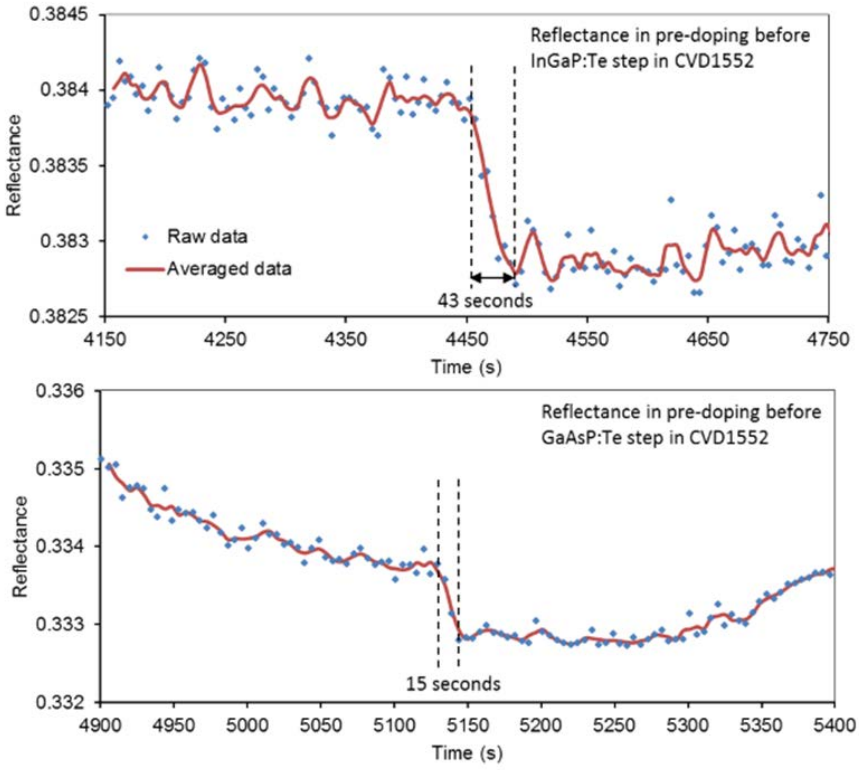


Figure 25: Pre-doping of InGaP and GaAsP during growth stop. The onset of the change in reflectance signifies the beginning of the pre-doping. The reflectance stabilized a period of time later.

junction layer. As demonstrated by other groups, the idea is that Te saturates on the surface and incorporates more uniformly from the epi onset, ideally achieving 25nm of n-InGaP doped at 2×10^{19} cm^{-3}. Figure 25 demonstrates the change in surface reflectivity measured *in situ* during the CVD growth for various layers pre-doped with DETe. As layers of InGaP and GaAsP are pre-doped (signified by the onset of the sharp change in reflectivity), changes in reflectivity are observed for 43s and 15s, respectively. While this change is not well understood presently, it may indicate the saturation of Te on the surface and that a longer time is required for Te to saturate on the surface of InGaP (which corresponds to approximately the length of time required to grow the 25nm layer). Figure 24 shows the results for a p-AlGaAsP/n-InGaP tunnel junction where the surface was pre-doped with DETe prior to the start of the InGaP growth. A 10 minute dopant activation anneal was also performed to be consistent with the best p-AlGaAsP/n-InGaP devices. While the excess tunneling current component (between 0.2V and 0.9V) was reduced, resulting in a negative differential resistance region commonly seen in ideal tunnel junctions, unfortunately, no improvement in the peak current is realized. A more in depth analysis of the pre-doped layer under various growth conditions is required to optimize the pre-doping conditions and determine if the pre-doping step is causing any real impact on the doping profile. Another potential pathway for improving tunnel junction performance is simply further optimization of the Te growth conditions to increase the achievable Te doping level. Although recent results from SolAero suggest that high n-type doping in the InGaP layer is non-trivial, the exponential dependence of peak tunneling current on carrier concentration suggests that achieving higher electron concentration would result in a major improvement in device

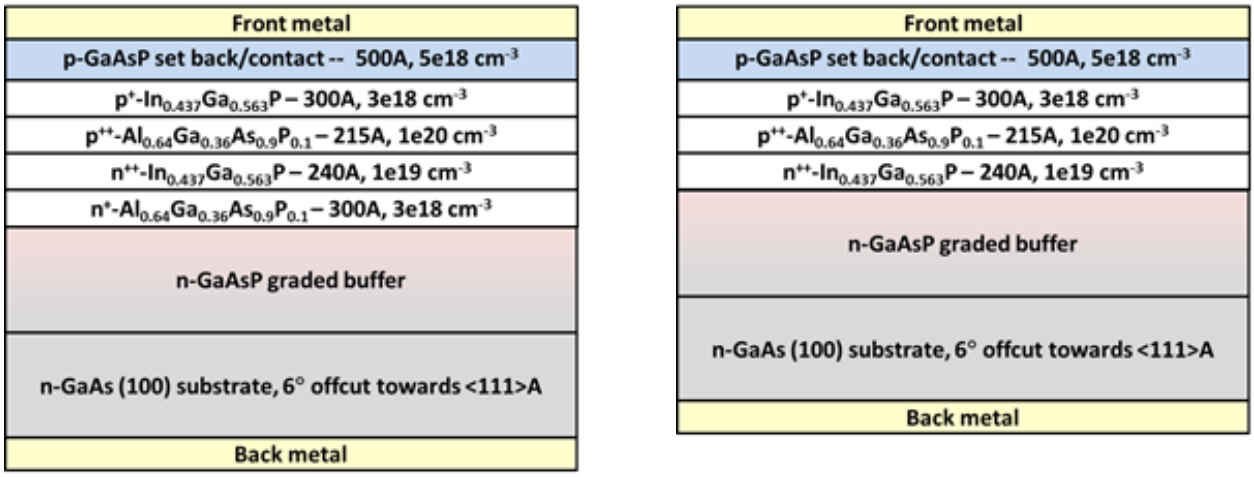


Figure 26: Diagrams of (a) initial and (b) redesigned top-to-middle tunnel junction demonstration structures, with target thicknesses and doping density.

performance. In particular, our prior efforts on tunnel junctions by MBE showed that increasing n-type doping with Si from 1×10^{19} cm^{-3} to 2×10^{19} cm^{-3} improved the peak tunnel current by 40x.

Highlight 2: InGaP Tunnel Junction Development – SolAero (MOCVD)

A second significant effort of this task was the demonstration of the more complicated wide bandgap tunnel junction which was led by SolAero. The intended diode design followed a standard form for concentrator cells, as illustrated in Figure 26(a). Note that this is a test structure used for design work only with the active tunnel diode grown on a GaAs/GaAsP growth template. While calibrating doping density, it was found that the n-type AlGaAsP layer could not be grown due to very high background carbon, which resulted in p-type rather than n-type material. As such, this layer was eliminated from the structure with the expectation of eventually replacing it with something more viable once good tunneling has been achieved. The updated tunnel diode test structure is shown in Figure 26(b).

Tunnel diodes designed for use with high bandgap subcells are especially challenging, as the density of charge carrier states tends to increase with band gap and thus very high doping densities have to be achieved to promote tunneling. Two layers in the above structure are of particular concern in this regard – the AlGaAsP (p-type) layer and the GaInP (n-type) layer. P-type doping of the AlGaAsP layer to high density is non-problematic due to high levels of background carbon. SolAero's doping calibration work for this layer indicated a doping density of 1e20 cm^{-3} without significant difficulty. Because the estimated density of states for this material is 1-2e19 cm^{-3}, this layer is degenerate and thus should promote carrier tunneling. Much more difficulty was encountered in achieving high doping in the n-type GaInP layer.

The required doping density for GaInP to promote carrier tunneling is on the same order as AlGaAsP, 1-2e19 cm^{-3}. Unfortunately, material calibration efforts at SolAero showed a maximum doping density of ~7e18 cm^{-3}. However, due to some uncertainty regarding the accuracy of this calibration value for the actual tunnel diode (due to some differences regarding how this particular layer is calibrated versus utilized in the tunnel diode); devices were built using the highest doping that was achieved. Note that the calibration activities used to maximize the doping density considered a variety of controllable growth parameters such as gas flow rates, III/V ratios, and growth temperature.

Devices grown using the achieved n-GaInP material were processed and tested. A

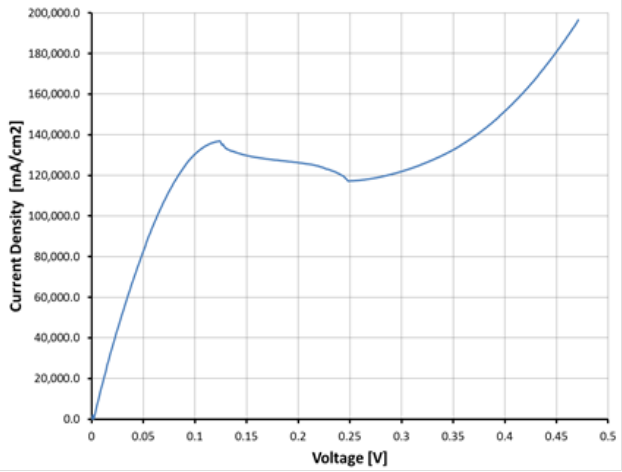


Figure 27. IV curve (forward bias only) of representative InGaP tunnel diode.

representative tunnel diode IV curve is shown in Figure 27. The measured IV curves for these tunnel diodes show clear tunneling in both forward and reverse bias with very high peak current density (~140 A/cm^2). Due to the very high peak current, which is difficult to achieve for high band gap materials, it was suspected that this was an artifact of the device processing in which the tunnel diodes may not have been adequately isolated. Inadequate isolation would result in larger than expected active area and thus an over estimation of the peak current density of the device. However, samples were analyzed via optical and electron microscopy and both methods confirmed good device isolation.

It should be noted that the high peak current, despite relatively low doping density, and the shallow valley in the IV curve (see Figure 27) and low turn on of diffusion current, indicates that the current may not be fully dominated by band-to-band tunneling. Rather, significant shunt and/or defect-assisted tunneling (excess) current components may be playing a significant role. This could be a concern for reliability/repeatability of the tunnel diode when operating at high current and high temperature (under concentration) as well as for the quality of the InGaP subcell that will eventually be grown on top of the tunnel diode and warrants further investigation.

Highlight 3: Ideal Anti-Reflection Coating (ARC) Modelling

Another key cell component of the multijunction design which received effort for this task was the ARC simulation/design models, which were implemented in FTG Software's FilmStar. The metric of interest for ARC design is spectrally weighted reflectance (SWR, formally defined in the last report, IQE = 1 is assumed here), though ultimately maximization of subcell current generation would be the preferable metric. However, this requires measured subcell IQE data, which was not yet available for this program. Due to unknowns regarding the final device design as well as the optical properties of the constituent materials, these ARC models are preliminary. Though inexact these models may be, they still provide a good starting point and some information regarding what SWR values may reasonably be expected for this device design. Figure 28 shows simulated reflectance profiles for SolAero's current 3J and 4J ARC designs. Note that the models differ only in the optimized ARC layer thicknesses and the inclusion of a 10 µm SiGe layer below the Si substrate in the 4J case.

As is clear, the reflectance profile for the 3J and 4J cases differ mainly in the 1100nm to 1350nm range. This is due to absorption in the SiGe layer that was included in the 4J model. Note that the reflectance step in the 4J model at 1320nm is due to the location of the direct band edge for SiGe, which depends upon the composition of the SiGe material that is ultimately used in the 4J device. Simulated SWR values (under AM1.5D) for the 3J design (300 – 1100 nm) is 3.9%, while for the 4J design (300 – 1600 nm) is 5.2%. These ARC designs utilize simple, dual layer Al_2O_3/TiO_x structures. Such materials were used for preliminary optimization because they

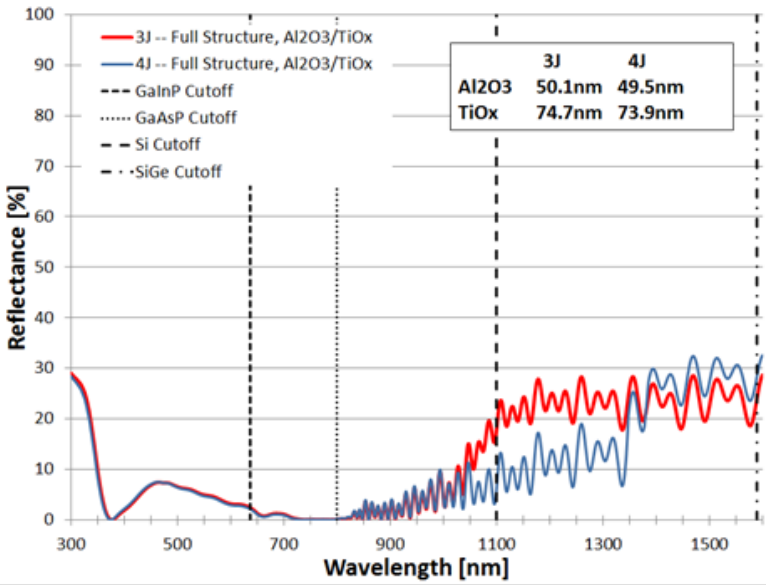


Figure 28: Simulated optimal reflectance characteristics for 3J and 4J models

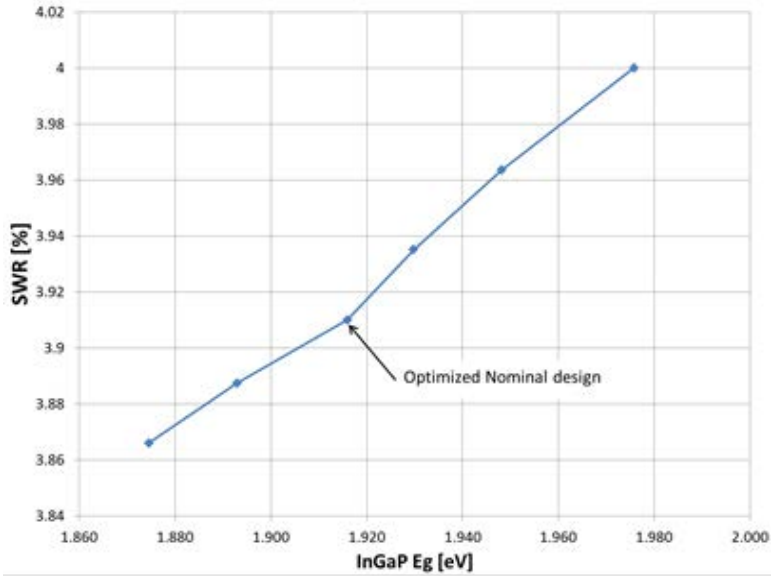


Figure 29. Results of band gap sensitivity study. It was assumed at the InGaP and GaAsP sub-cells are lattice matched and thus do not vary independently.

Table 6: Results of absorber layer thickness sensitivity study. Note that nominal design has an MC thickness of 1550 nm and a TC thickness of 580 nm.

		TC Absorber [nm]		
		250	580	1000
MC Absorber [nm]	500	3.95	3.95	3.94
	1550	3.91	3.91	3.93
	2500	3.92	3.91	3.94

are well known and easily obtained, though other material options may be considered to achieve even lower SWR. Device layer thickness for non-critical layers (such as the buffer structure) may be included in the optimization process to further reduce the SWR of these designs.

Because many of the specific details regarding the final 3J or 4J device design are not yet optimized (e.g. layer thicknesses, window and/or BSF compositions, etc.), a first-order sensitivity study was also conducted using the 3J model. The focus of the study was absorber layer (base) thickness and bandgap for the top (GaInP) and middle (GaAsP) sub-cells. The thickness and bandgap were varied independently about the nominal design and with reasonable range. Note that for the bandgap study it was assumed that the top and middle subcells are lattice matched, and thus the bandgap of these two materials are not independent. The results of the base thickness sensitivity study are shown in Table 6 and suggest very low sensitivity with an SWR change of < 0.1%. Similarly, the results of the band gap sensitivity study are shown in Figure 29 and again suggest very low sensitivity with a comparable SWR change of < 0.1%. It should be noted that the performance of the ARC will also be affected by many other device layers which were not studied here.

Associated Publications:

Metamorphic GaAsP Tunnel Junctions for High-Efficiency III–V/IV Multijunction Solar Cell Technology
D. J. Chmielewski, T. J. Grassman, A. M. Carlin, J. A. Carlin, A. J. Speelman and S. A. Ringel, *IEEE J. Photovolt.*, vol. 4, pp. 1301-1305, Sep (2014).

Metamorphic $GaAs_{0.9}P_{0.1}$ tunnel diodes, designed for application to heteroepitaxial GaInP/GaAsP/Si multijunction solar cells, were grown on compositionally graded $GaAs_yP_{1-y}$ /GaAs buffers by molecular beam epitaxy. Optimal growth conditions for high impurity doping were determined and tested using fabricated tunnel diode structures. Peak current densities of 103.9 $A{\cdot}cm^{-2}$ and resistance-area products of $4.5\times10^{-4}\ \Omega \cdot cm^2$ were obtained. Strong agreement between simulated and fabricated devices indicates excellent device quality with respect to optimized growth conditions and near-nominal operation. These results suggest that the optimized structures are promising for use within III–V/Si multijunction solar cells operating under high concentration.

Task 6.0: Integration of GaInP/GaAsP/Si 3J devices

This task was designed to integrate all the component development completed throughout the program to realize the growth, fabrication and testing of prototype ~1.95/1.55/1.1 eV III-V/active-Si 3J cells at various concentration levels. While fully integrated 3J devices were not ultimately realized during the timeline of this program, a number of significant achievements were accomplished and reported in journals, conference proceedings and conference presentations. The most significant of these accomplishments related to the integration of multijunction devices on Si is highlighted below with a partial summary of key findings. Associated publications which include additional details are also listed below with brief abstracts included.

- First demonstration of GaAsP/Si (1.72/1.1eV) tandem cell
- First demonstration of a GaInP/GaAsP 1.95/1.55eV metamorphic tandem on Si
- First Si 3J based on GaInP/GaAsP/Si grown with ideal bandgap profile
- III-V/Si PV added as technology on ITRPV Roadmap

Highlight 1: Multijunction Integration $GaAs_{0.75}P_{025}$/Si Dual Junction

Although not originally a target of this FPACE project, we recognized from the beginning that the $GaAs_{0.75}P_{025}$/Si 2J design, which is a near-ideal bandgap pairing of 1.7 eV / 1.1 eV, is made accessible via the work toward the main $Ga_{0.57}In_{0.43}P/GaAs_{0.90}P_{0.10}$/Si 3J target. Indeed, the 75% As lattice constant is *passed* on the way to the 90% lattice constant. As such, it was deemed worthwhile to pursue a small amount of preliminary effort toward this 2J, since it actually requires a smaller degree of metamorphic grading due to the reduced lattice mismatch—that is, 3.2% vs. 3.7% misfit, which translates to at least 1 μm less graded buffer thickness. It was anticipated that our existing device structures, especially the tunnel junction, the performance of which depends strongly on bandgap, would not be optimized for the 2J, but may work well enough for an initial demonstration. We also note that the preliminary 2J was performed first via MBE, and then via MOCVD as a follow-up. The results of this work is shown in Figure 30.

Initial attempts at the 2J structure via MBE resulted in devices in which the tunnel junction failed. The tunnel junction structure used was an unoptimized version of the high-performance double-heterostructure design developed for the 3J, but adjusted to compositions lattice-matched to the 75% As lattice constant (i.e. $Ga_{0.64}In_{0.36}P/GaAs_{0.75}P_{0.25}$). As-grown test device analysis of this DHTJ indicated peak tunneling of up to ~14 A/cm^2, which degraded to zero after exposure to a thermal budget that approximates that of the growth of the $GaAs_{0.75}P_{0.25}$ top cell under standard conditions (~600°C and 1 μm/hr). The most likely cause of this failure is dopant diffusion across the n^{++}/p^{++} $GaAs_{0.75}P_{0.25}$ homojunction; Be (the *p*-type dopant) is known to be relatively mobile, so this was not a major surprise. To reduce the thermal budget in the hopes that the DHTJ might survive, another attempt was made, but with a top cell growth temperature of only 500°C and growth rate of 1.5 μm/hr. The expectation was that these growth conditions would result in a poor-quality top cell due to significant point defect incorporation. Nonetheless, as shown in Fig. 30, this adjustment, while indeed yielding a poor-quality top cell, was successful in maintaining the tunneling interconnect. The low fill factor, versus the J_{SC}-V_{OC} measurement, appears to be the result of both voltage dependent current collection (most likely due to low minority carrier lifetime) *and* series resistance, suggesting that the tunnel junction was degraded, but not completely to non-working condition. Altogether, as indicated in Table 7, this working MBE-grown 2J resulted in an in-house (single-zone simulator) measured AM1.5G efficiency (with no ARC) of 9.4%.

Following the MBE demonstration, we deemed it worthwhile to attempt the 2J structure via MOCVD, where the dopants used for the tunnel junctions (i.e. C for *p*-type, Te for *n*-type) should provide a higher degree of robustness against the top cell growth thermal budget. Additionally, further work on the tunnel junctions had indicated that the use of a p^{++}-AlGaAsP/n^{++}-GaAsP heterostructure design could match or even outperform the GaInP/GaAsP DHTJ design used previously. As such, an unoptimized 2J structure, making use of our rudimentary Si bottom cell (i.e. no BSF), and tunnel junction and top cell structures that were merely compositionally-shifted from the 3J design, was grown. Data of the resulting cells are provided in Fig. 30, which also provides comparison against the MBE-grown cell. Despite the complete lack of optimization, this preliminary attempt provided a 13.6% AM1.5G efficiency (nearly 20% if we assume a 5% spectral weighted reflectance ARC). Additionally, compared to the J_{SC}-V_{OC} analysis, we find that there is little FF degradation due to series resistance, suggesting that the new tunnel junction design is indeed much more robust than that used in the MBE growths. The greatly reduced voltage dependent carrier collection also confirms a much higher quality $GaAs_{0.75}P_{0.25}$ material in the MOCVD-grown structure, which was grown at our standard conditions. While the performance of this 2J structure is still far from its ultimate potential, it nonetheless provides an excellent demonstration of architecture, which is significantly simpler than the target 3J and thus worthy of continued investigation.

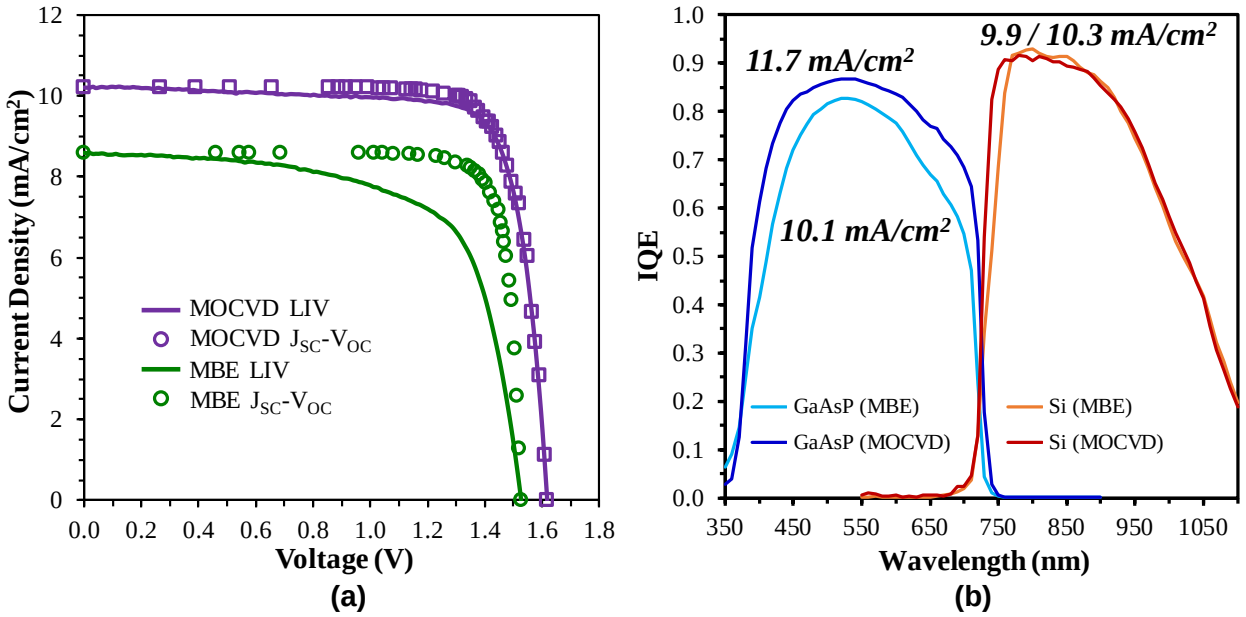


Figure 30: (a) AM1.5G LIV, J_{SC}-V_{OC} and (b) quantum efficiency of a $GaAs_{0.75}P_{0.25}$/Si dual-junction solar cells. Both cells used an MOCVD-grown GaP/Si active bottom cell template; the graded buffer, tunnel junction, and top cell were grown via either MBE or MOCVD, as indicated. Integrated EQE subcell J_{SC} values are given in (b).

Table 7. Measured AM1.5G LIV metrics for the MBE and MOCVD grown GaAsP/Si 2J cells.

	MBE	MOCVD
V_{OC} (V)	1.52	1.62
J_{SC} (mA/cm²)	8.9	10.5
FF (%)	69.3	80.0
Efficiency (%)	9.4	13.6

Highlight 2: Multijunction Integration – $Ga_{0.57}In_{0.43}P$ / $GaAs_{0.90}P_{0.10}$ Dual Junction

Following the successful demonstration of good quality subcells and tunnel junctions from prior tasks, our next integration effort focused on the GaInP and GaAsP top and middle cells of the 3J design at the desired lattice constant. This was done, in part, as a test of the newest design of the double-heterostructure tunnel junction (DHTJ) with respect to survivability during subsequent subcell growth, as well as its performance within a realistic device structure. A $Ga_{0.57}In_{0.43}P/GaAs_{0.90}P_{0.10}$ (1.95 eV/1.54 eV) dual junction was grown by MBE on a $GaAs_{0.9}P_{0.1}/GaAs_yP_{1-y}$/GaAs virtual substrate. This structure was fabricated into active dual-junction solar cells, AM1.5G lighted I-V (LIV) and quantum efficiency data from which are presented in Figure 31. The LIV data, Figure 31(a), shows clear addition of the sub-cell V_{OC}'s with no significant loss, indicating a working (at least under one-sun illumination). The measured J_{SC} (~6.5 mA/cm²) is below what was expected, but this value is likely an artifact of the poor spectral match with our single-zone solar simulator; this is also the source of the downward sloping top portion of the LIV curve (i.e. not shunt). Integrated EQE values, displayed in Figure 31(b), indicate a slightly higher J_{SC} (~7.1 mA/cm²), while also showing a slight current

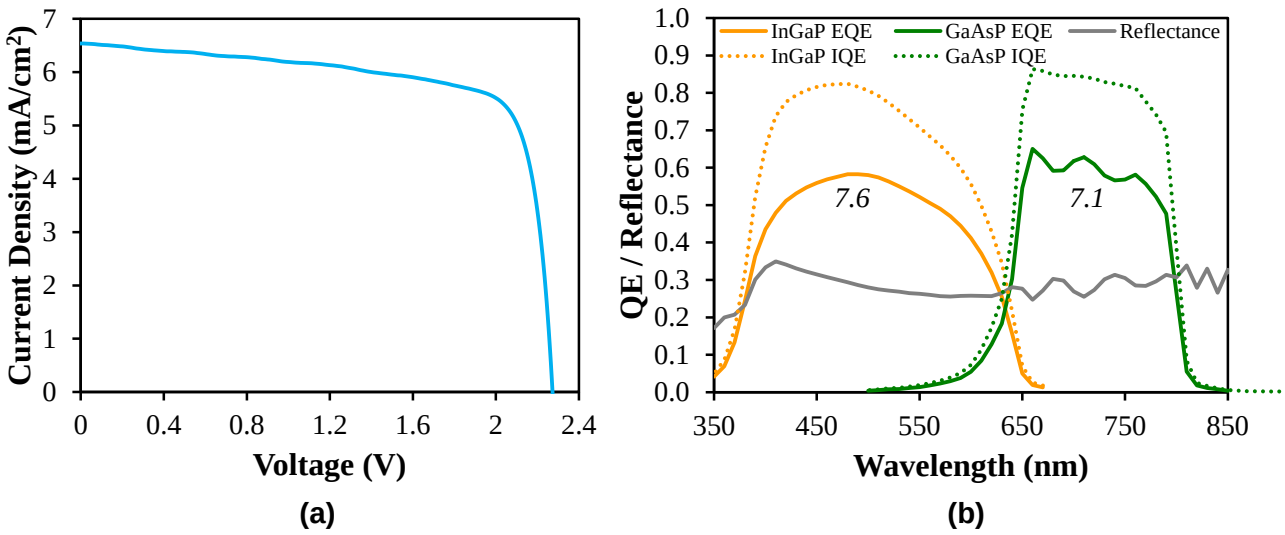


Figure 31: (a) AM1.5G LIV and (b) quantum efficiency of a $Ga_{0.57}In_{0.43}P/GaAs_{0.90}P_{0.10}$ dual-junction solar cell grown on a $GaAs_{0.9}P_{0.1}/GaAs_yP_{1-y}$/GaAs virtual substrate. Integrated EQE for each sub-cell are given in (b).

mismatch. Additionally, we can see an average (absolute) reflectance of about 30%, meaning application of a high-quality broadband ARC alone should increase the current to around 10 mA/cm^2. Nonetheless, we also see that the IQE – actually EQE/(1-R) here, with very little transmission expected for the thicker GaAsP cell, and potentially more significant transmission for the GaInP cells – for both cells is lower than what was observed for their MBE-grown single-junction isotypes. In fact, both single-junctions achieved around (or better than) 90% IQE, so the lower values here are somewhat unexpected. While it is possible that this is partially an artifact of the measurement due to insufficient subcell isolation via light-biasing during the QE measurement, (efforts are underway to improve our instrumental setup) the known thermal sensitivity of the tunnel junction grown by MBE also precluded the ability to anneal the GaInP materials after epitaxy which has been shown previously to improve the GaInP cell performance. Nonetheless, these results successfully demonstrated a multijunction cell stack on Si at the desired lattice constant and that the DHTJ design is capable of providing good quality interconnection.

Associated Publications:

GaAs0.75 P0.25/Si Dual-Junction Solar Cells Grown by MBE and MOCVD
T. J. Grassman, D. J. Chmielewski, S. D. Carnevale, J. A. Carlin and S. A. Ringel, *IEEE J. Photovolt.*, vol. 6(1), pp. 326-331 (2016).

Monolithic, epitaxial, series-connected $GaAs_{0.75}P_{0.25}$/Si dual-junction solar cells, grown via both molecular beam epitaxy (MBE) and metal–organic chemical vapor deposition (MOCVD), are reported for the first time. Fabricated test devices for both cases show working tandem behavior, with clear voltage addition and spectral partitioning. However, due to thermal budget limitations in the MBE growth needed to prevent tunnel junction failure, the MBE-grown GaAs0.75P0.25 top cell was found to be lower quality than the equivalent MOCVD-grown device. Additionally, despite the reduced thermal budget, the MBE-grown tunnel junction exhibited degraded behavior, further reducing the overall performance of the MBE/MOCVD combination cell. The all-MOCVD-grown structure displayed no such issues and yielded

significantly higher overall performance. These initial prototype cells show promising performance and indicate several important pathways for further device refinement.

Deliverable / Milestone Deviations

The ambitious goals of this FPACE program anticipated many activities and successes, and these are accounted for in this report. However, as with any healthy research program, new phenomena were uncovered, unanticipated scientific complexities were encountered and several unexpected but high impact opportunities were revealed along the way (e.g. ECCI). Efforts to advance our understanding on these were undertaken as part of the process to achieve the project goals, and these activities resulted in critical new knowledge and developments, much of which has been disseminated within various publications. This created some deviations from the original, notional program timeline so that we could solve these issues and make meaningful contributions to the field. These and some equipment-related delays contributed to a few delays in reaching some milestones, especially later in the program. Below is a table containing a summary of all of the milestones that were either achieved after the planned delivery date, unmet at the anticipated level of performance or unrealized at the end of the program timeline as well as a brief description for each of the milestones limitations. As this program was afforded a 1-year extension, various milestones, especially in the later years of the program, were achieved but later than originally planned.

Task #	Task description	Initial Negotiated Deliverable / Milestone	Actual Deliverable / Milestone
1.3	TRPL bulk lifetime > 1ns for GaAsP measured by NREL	06/30/13	Unrealized
1.4	Down selection of Si cell configuration (n+p or p+n) and method of formation	12/31/12	06/30/13
2.2	Report describing the system cost model with the key parameters that are included in determining the LCOE for the system	06/30/12	07/31/12
4.1	Demonstration of GaAsP sub-cell on Si with Voc > Eg/q – 0.5 eV	12/31/13	Unmet - 0.55eV
4.1	Demonstration of GaInP sub-cell on Si with Voc > Eg/q – 0.5 eV	06/30/14	Unmet – 0.79eV
4.2	Demonstration of a SiGe sub-cell (0.67-0.8eV) with IQE > 70% across a Si-filtered spectrum	12/31/13	9/30/2014
4.2	Demonstration of a dual-junction GaAsP/Si sub-cell with target AM1.5 (1-sun) efficiency > 25% (accounting for surface reflection)	06/30/14	Unrealized >20% Projected 1.7/1.1 eV design
5.1	GaAsP and GaInP-based tunnel diodes will be demonstrated with a series resistance of <1 x10^{-3} ohm-cm^2 and a Jp of >15 mA/cm^2	12/31/13	GaAsP – 10/1/2013 (met) GaInP – 10/1/2014
5.1	GaAsP and GaInP- based tunnel diodes will be demonstrated with a series resistance of <1 x10^{-4} ohm-cm^2 and a Jp of >15	06/30/14	GaAsP – R_s = 2.1x10^{-4} Ω · cm^2 GaInP – Rs = 5.3x10^{-4} Ω · cm^2
5.3	Demonstration of high performance, broadband ARC on 3J GaInP/GaAsP/Si laboratory cell structure with reflectivity < 6% from 300 to 1600 nm	12/31/14	Unrealized
6	Integration of GaInP, GaAsP and Si sub-cell components on Si into a laboratory cell structure to enable initial characterization of device performance metrics under concentration	06/30/14	12/31/15
6	Fabrication and device characterization of a mechanically stacked 4J cell using a SiGe bottom cell // Testing and characterization of 3J GaAsP/GaInP/Si laboratory cells under concentration levels (from < 100x to ~ 1000x) and at one sun measured by NREL with target efficiency of 40% at 500x	12/31/14	Unrealized

Subtask 1.3: GaAsP and GaInP carrier lifetimes, interface recombination velocities and creating TDD-recombination phenomenological models: This task focused on the generation of GaAsP and GaInP double heterostructures (DHs) to evaluate carrier lifetimes and interface recombination velocities in GaAsP and GaInP on GaP and Si substrates. This subtask was expected to yield lifetime and interface recombination velocity analysis via time resolved photoluminescence (TRPL) for GaAsP and GaInP layers having ideal bandgap values at ideal lattice constant values. While DH structures for both GaAsP and GaInP at the desired lattice constants were grown, on both GaP and Si substrates, and measured by TRPL at NREL, the data collected for the sample set was inconsistent. While individual layer results indicated a lower lifetime for the samples on Si over those on GaP as expected, analysis did not allow for accurate extraction of the lifetime or interface recombination velocities. In lieu of completing additional samples for lifetime analysis effort was instead dedicated further to materials development and development of the new ECCI technique to provide rapid material feedback.

Subtask 1.4: Process development of Si sub-cell compatible with III-V integration techniques: Several methods were explored to develop a high quality 1.1 eV Si sub cell compatible with the required III-V integration pathway. This subtask to yielded the development of an initial growth and integration methodology to demonstrate an active Si sub-cell beneath III-V epitaxial layers. One of the primary milestones for this subtask was the down selection of the formation process for the Si sub-cell in Q4. However, a request was made, and granted by EERE in Q3 to push back the down-selection date for the Si sub-cell to Q6. While we made outstanding progress on the epitaxial Si sub-cell development, delays in the procurement of ex-situ Si PV cell "templates" limited the ability to fully characterize that option. Moreover, our new collaboration with the Martin Green/Stephen Bremner group at UNSW was looking extremely promising and we pursued that additional avenue aggressively and in parallel with our other Si cell development efforts. The modified Q6 down-select target was met but additional improvements and analysis of the important Si sub-cell continued throughout the program.

Subtask 2.2: System modeling: This subtask focused on system modeling to determine how to incorporate the Si based multi-junction cell into a final system, with the goal of minimal levelized cost of electricity (LCOE) for a given set of conditions. This subtask yielded a Report describing the system cost model with the key parameters that are included in determining the LCOE for the system. That delay in delivery largely resulted from a lack of knowledge in the PV community as to how to address/predict the costs of a III-V/Si solar technology that is built on a silicon platform using Si electronics-style manufacturing and unknowns associated with the GaAsP material system employed in this PV technology. However, while this milestone was past the delivery date it was only delayed by one month.

Subtask 4.1: GaAsP and GaInP single junction sub-cell prototypes: This task focused on development of initial single junction GaAsP and GaInP PV devices, fabrication and device performance characterization. This subtask yield growth, fabricated and test of single junction devices on both GaP and Si. Two milestones included the realization of Voc > Eg/q – 0.5 eV for both GaInP and GaAsP sub-cells on Si. However, while aggressive goals these values were not quite met throughout the optimization process. W_{oc} for a GaAsP sub-cell on GaAs (tensile) yielded a W_{oc} = 0.51V and on Si yielded W_{oc} = 0.55V. For a InGaP sub-cell, the best results yielded W_{oc} = 0.53V and 0.79V on GaAs (tensile) and Si respectively.

Subtask 4.2: Si and SiGe single junction sub-cell prototypes: The primary goals of this task was 1) to build on the Phase 1 material and process development to fabricate, measure and

optimize the Si and SiGe sub-cells and 2) provide additional input into MJ stack designs. As the SiGe sub-cell was intended to be used as a mechanically stacked sub-cell it was measured independently with one milestone to achieve IQE > 70% across a Si-filtered spectrum. While this milestone was significantly delayed due to errors in the SiGe sub-cell design and extended downtime of the SiGe epitaxial growth system, the milestone was successfully demonstrated on the second generation of the SiGe device design and did not impact the development of any of the other sub-cells. A second milestone of this task was to demonstrate a 2J GaAsP/Si stack with a >25% projected efficiency as an integral advance toward the 3J device. However, this goal was not well constructed as a 25% 1-sun efficiency for a 1.55eV/1.1eV bandgap pair (part of the 1.95/1.55/1.1eV 3J target) is unrealistic since the bandgap design is not optimized when limited to the 2J design. We did however realize multiple 2J designs (1.55/1.1eV and 1.95/1.55eV) in the final year of the program which were also integral in testing of the various tunnel junction designs. As a separate thrust, work was also completed to realize a more optimum 2J design of 1.7/1.1eV. We were able to demonstrate a reasonable efficiency (>20% projected with ARC) although this device was not afforded any optimization efforts.

Subtask 5.1: Tunnel junction growth, processing and optimization: This task focused on the demonstration of stable, degenerately doped, optically semi-transparent tunnel junctions between each pair of cells at the same lattice constant as the MJ stack. While desiring a GaAsP-containing (low bandgap) and a GaAsP-free (high bandgap) design, this task proved to require much more effort than expected and warranted the addition of a significant modeling effort which proved very valuable. While exploring multiple device designs informed from the modelling effort, record peak current densities were demonstrated for a metamorphic tunnel junction and warranted multiple publications. For the milestones, while the initial, lower performance, target was finally met for both the GaAsP-containing and GaAsP-free designs, the second milestone was not realized for either design. While the peak current spec was greatly exceeded in both cases, the best resistance values in each were just above spec at $2.1 \times 10^{-4}\ \Omega \cdot cm^2$ and $5.3 \times 10^{-4}\ \Omega \cdot cm^2$ for the GaAsP and GaInP designs respectively. While investigation into the various tunnel junction designs persisted through the end of the program and reasonable performance was achieved, this is certainly one area where further investigation into novel designs (and investigating stability under epitaxial heating and concentration operation) would be warranted.

Subtask 5.3. Antireflection coating development and testing: This task focused on the development of a high quality, broad band anti-reflection coating (ARC). Optical modeling was completed to design a broad band ARC with a spectral weighted reflectance (SWR) <6% [3.9% 3J and 5.9% 4J], meeting one milestone for Task 5.3. Unfortunately, due to a lack of fully grown devices being available by the end of the program we were unable to deposit and characterize the designed ARCs to attempt the second milestone. Although untested, the preferred ARC design was limited to two materials successfully used in SolAero's current ARC process (Al_2O_3/TiO_x) and we had a high confidence the milestone was achievable.

Task 6.0: Integration of GaInP/GaAsP/Si 3J devices*:* The focus of this task was the integration of the component development completed in all prior tasks into prototype III-V/active-Si 3J (1.95/1.55/1.1 eV) cells for characterization at various concentration levels up to 1000x. While the 1-year extension of the programs end date from 12/2014 to 12/2015 did enable the realization of the milestone to grow, fabricate and test the final 3J (1.95/1.55/1.1 eV) design, this device was only achieved at the end of the program and measurement under concentration

was not possible due to the device size (too small for measurement in SolAero's characterization systems). Additionally, as the integration of the 3J stack was only realized at the end of the program, the integration and characterization of a 4J design with the mechanical stacking of the developed SiGe subcell was also not possible.

Outputs Developed Under the Award

Patents / Licensing Agreements

None.

Honors and/or Awards

Name	MS/Ph.D.	Started	Graduated (Defense Date)
Chris Ratcliff	Ph.D.	Oct-08	10/20/2014
Dan Chmielewski	Ph.D. (Candidate)	Sep-12	Expected 2018
Elisa Garcia-Tabares	Ph.D. (Candidate); visiting student from UPM		Spring 2015
Nathan Vaughn	Ph.D. (Pre-Candidate)	Aug-14	Expected 2020
Julia Deitz	Ph.D. (Candidate)	Aug-13	Expected 2019
Deep Shah	Undergraduate	Aug-13	5/10/2015

Awardee	Award	Sponsor	Date of Award
Julia Deitz	Best Student Paper (Winner)	42nd IEEE PVSC	June 2015
Julia Deitz	Presidential Scholar Award	Microanalysis Society	August 2015
Dan Chmielewski	Best Student Paper (Finalist)	42nd IEEE PVSC	June 2015
Dan Chmielewski	Best Student Paper (Finalist)	39th IEEE PVSC	June 2013

Publications

Journal

1. T. J. Grassman, D. J. Chmielewski, S. D. Carnevale, J. A. Carlin and S. A. Ringel, "GaAs0.75P0.25/Si Dual-Junction Solar Cells Grown by MBE and MOCVD", *IEEE J. Photovolt.*, vol. 6(1), pp. 326-331, 2016.
2. R. M. France, F. Dimroth, T. J. Grassman and R. R. King, 2016, “Metamorphic epitaxy for multijunction solar cells”, MRS Bulletin 41, no. 3, 202 – 209.
3. E. García-Tabarés, J. A. Carlin, T. J. Grassman, D. Martín, I. Rey-Stolle and S. A. Ringel, "Evolution of silicon bulk lifetime during III–V-on-Si multijunction solar cell epitaxial growth", *Prog. Photovoltaics*, DOI: 10.1002/pip.2703, 2016.
4. J. I. Deitz, D. W. McComb, and T. J. Grassman, “Advancement of Heteroepitaxial III-V/Si Thin Films through Defect Characterization,” Microsc. Microanal., 22, S3, pp. 1538–1539, July 2016
5. J. I. Deitz, S. D. Carnevale, S. A. Ringel, D. W. McComb, T. J. Grassman, “Electron Channeling Contrast Imaging for Rapid III-V Heteroepitaxial Characterization,” *Journal of Visualized Experiments*, vol. 101, pp. e52745, JUL 17, 2015.
6. S. D. Carnevale, J. I. Deitz, J. A. Carlin, Y. N. Picard, D. W. McComb, M. De Graef, S. A. Ringel and T. J. Grassman. "Applications of Electron Channeling Contrast Imaging for the Rapid Characterization of Extended Defects in III-V/Si Heterostructures," *IEEE J. Photovolt.,* vol. 5, pp. 676-682, MAR, 2015.
7. S. D. Carnevale, J. I. Deitz, J. A. Carlin, Y. N. Picard, M. De Graef, S. A. Ringel and T. J. Grassman. "Rapid misfit dislocation characterization in heteroepitaxial III-V/Si thin films by electron channeling contrast imaging," *Appl. Phys. Lett.,* vol. 104, pp. 232111, JUN 9, 2014.
8. D. J. Chmielewski, T. J. Grassman, A. M. Carlin, J. A. Carlin, A. J. Speelman and S. A. Ringel. "Metamorphic GaAsP Tunnel Junctions for High-Efficiency III-V/IV Multijunction Solar Cell Technology," *IEEE J. Photovolt.,* vol. 4, pp. 1301-1305, SEP, 2014.
9. T. J. Grassman, J. A. Carlin, B. Galiana, F. Yang, M. J. Mills and S. A. Ringel. "MOCVD-Grown GaP/Si Subcells for Integrated III-V/Si Multijunction Photovoltaics," *IEEE J. Photovolt.,* vol. 4, pp. 972-980, MAY, 2014.
10. T. J. Grassman, C. Ratcliff, A. M. Carlin, J. A. Carlin, L. Yang, M. J. Mills and S. A. Ringel, "III-V/GaP Epitaxy on Si for Advanced Photovoltaics and Green Light Emitters," *ECS Trans*. vol. 50(9), pp. 321, 2013.
11. T. J. Grassman, J. A. Carlin, B. Galiana, L. -. Yang, F. Yang, M. J. Mills and S. A. Ringel. "Nucleation-related defect-free GaP/Si(100) heteroepitaxy via metal-organic chemical vapor deposition," *Appl. Phys. Lett.,* vol. 102, pp. 142102, APR 8, 2013.

Conference Proceedings

Full Author List	Article Title	Conference Proceedings Title or Conference Name	Dates	Vol	pp. (Paper Number)
T. J. Grassman, A. M. Carlin, J. Grandal, C. Ratcliff, L. Yang, M. J. Mills and S. A. Ringel	Spectrum-optimized Si-based III-V multijunction photovoltaics	Proceedings of the SPIE	Feb 6-10, 2012	8256	82560R-1-7
A.M. Carlin, T. J. Grassman, M. R. Brenner, J. Grandal, C. Ratcliff, L.-M. Yang, M. J. Mills, P. Sharma, E. A. Fitzgerald, S. A. Ringel	Lattice-Matched GaP/SiGe Virtual Substrates for Low-Dislocation Density GaInP/GaAsP/Si Solar Cells	Proceedings of the 38th IEEE PVSC	June 3-8, 2012		918-921 (H17)
D. J. Chmielewski, T. J. Grassman, A. M. Carlin, J. A. Carlin, A. Speelman, S. A. Ringel	Metamorphic Tunnel Junctions for High Efficiency III-V/IV Multi-Junction Solar Cell Technology	Proceedings of the 39th IEEE PVSC	June 16-21, 2013		0882 – 0885 (249)
T. J. Grassman, J. A. Carlin, C. Ratcliff, D. J. Chmielewski, S. A. Ringel	Epitaxially-Grown Metamorphic GaAsP/Si Dual-Junction Solar Cells	Proceedings of the 39th IEEE PVSC	June 16-21, 2013		0149 – 0153 (52)
S. A. Ringel, J. A. Carlin, T. J. Grassman, B. Galiana, A. M. Carlin, C. Ratcliff, D. Chmielewski, L. Yang, M. J. Mills, I. Al-Mansouri, S. P. Bremner, A. Ho-Baillie, X. Hao, H. Mehrvarz, G. Conibeer, M. A. Green	Ideal GaP/Si Heterostructures Grown by MOCVD: III-V/Active-Si Subcells, Multijunctions, and MBE-to-MOCVD III-V/Si Interface Science	Proceedings of the 39th IEEE PVSC	June 16-21, 2013		3383 – 3388 (942)
A. Haas, P. Sharps, D. Aiken, T. J. Grassman, J. A. Carlin, S. A. Ringel	Analysis of Short- and Long-Term Performance Goals for III/V on Active Si Concentrator Solar Cells	Proceedings of the 39th IEEE PVSC	June 16-21, 2013		0867 – 0872 (246)
I. Al-Mansouri, S. P. Bremner, A. Ho-Baillie, H. Mehrvarz, X. Hao, G. Conibeer, M. A. Green, T. J. Grassman, J. A. Carlin, S. A. Ringel	Design of Bottom Silicon Solar Cell for Multijunction Devices	Proceedings of the 39th IEEE PVSC	June 16-21, 2013		3310-3314 (919)
Martin A. Green, X. Hao, S. Bremner, G. Conibeer, I. Al Mansouri, N. Song, Z. Liu, S.A. Ringel, J.A. Carlin, T.J. Grassman, B. Galiana, A.M. Carlin, C. Ratcliff, D. Chmielewski, L. Yang, M.J. Mills, G. Teeter and M. Young	Silicon Wafer-Based Tandem Cells: The Ultimate Photovoltaic Solution	Proceedings of 28th EU PVSEC	September 30, 2013		(1AP.1.2)
T. J. Grassman, C. Ratcliff, A. M. Carlin, J. A. Carlin, L.-M. Yang, M. J. Mills, and S. A. Ringel	III-V/GaP Epitaxy on Si for Advanced Photovoltaics and Green Light Emitters	ECS Transactions	Oct 7-12, 2013	**50**(9)	321-332 (E17-3135)

Full Author List	Article Title	Conference Proceedings Title or Conference Name	Dates	Vol	pp. (Paper Number)
Chris Ratcliff, T. J. Grassman, J. A. Carlin, S. A. Ringel	Development of Ga(x)In(1-x)P on Si for High Performance, Low Cost Multijunction Photovoltaics	Proceedings of 23rd PVSEC	October 28-November1, 2013		(1472)
Chris Ratcliff, T. J. Grassman, J. A. Carlin, D.J. Chmielewski, S. A. Ringel	Ga-rich $Ga_xIn_{1-x}P$ solar cells on Si with 1.95 eV bandgap for ideal III-V/Si photovoltaics	Proceedings of the SPIE	February 1-6, 2013		(8981-41)
T. J. Grassman, J. A. Carlin, S. D. Carnevale, D. J. Chmielewski, E. García-Tabarés, I. Rey-Stolle, I. Al Mansouri, H. Mehrvarz, S. Bremner, A. Ho-Baillie, M. A. Green, S. A. Ringel	Progress Toward a Si-Plus Architecture: Epitaxially-Integrable Si Sub-Cells for III-V/Si Multijunction Photovoltaics	Proceedings of the 40th IEEE PVSC	June 8-13, 2014		(776)
S. D. Carnevale, J. I. Deitz, J. A. Carlin, Y. N. Picard, M. De Graef, S. A. Ringel, T. J. Grassman	Rapid Characterization of Extended Defects in III-V/Si by Electron Channeling Contrast Imaging	Proceedings of the 40th IEEE PVSC	June 8-13, 2014		2800-2803 (780)
D. J. Chmielewski, T. J. Grassman, S. D. Carnevale, J. A. Carlin, S. A. Ringel	High-Performance Metamorphic Tunnel Junctions on Si for III-V/Si Multijunction Solar Cells	42nd IEEE PVSC	Jun 14-19, 2015		1-4 (81)
E. García-Tabarés, D. Martín, I. Rey-Stolle, T. J. Grassman, J. A. Carlin, S. A. Ringel	Evolution of the Silicon Bottom Cell Photovoltaic Behavior during III-V on Si Multi-junction Solar Cells Production	42nd IEEE PVSC	Jun 14-19, 2015		1-6 (82)
T. J. Grassman, D. J. Chmielewski, S. D. Carnevale, J. A. Carlin, S. A. Ringel	Progress in the Development of Epitaxial GaAsP/Si Dual-Junction Solar Cells	42nd IEEE Photovoltaic Specialists Conference	Jun 14-19, 2015		1-5 (79)
D. W. Cardwell, C. Ratcliff, N. R. Vaughn, S. D. Carnevale, T. J. Grassman, S. A. Ringel	Investigations of Metamorphic (Al)GaInP for III-V Multijunction Photovoltaics	42nd IEEE PVSC	Jun 14-19, 2015		1-4 (22)
J. I. Deitz, S. D. Carnevale, S. A. Ringel, D. W. McComb, T. J. Grassman	Extending Characterization Applications of Electron Channeling Contrast Imaging	42nd IEEE PVSC	Jun 14-19, 2015		1-4 (294)

Presentations

Full Author List	Paper Title	Presented in the Session / Conference	Location, Dates
S. A. Ringel, T. J. Grassman, A. M. Carlin, J. Grandal, C. Ratcliff, L. Yang, M. J. Mills	**(INVITED)** Spectrum-optimized Si-based III-V multijunction photovoltaics	"Physics, Simulation, and Photonic Engineering of Photovoltaic Devices" at SPIE Photonics West 2012	San Francisco, CA Feb 6-10, 2012
Steven A. Ringel	**(INVITED)** Challenges and Roles of Universities in Solar Photovoltaics: A Faculty Innovator's Perspective	1st American Public Land Grant University - Energy Forum	Columbus, OH Apr 30 - May 1, 2012
Steven A. Ringel and Tyler J. Grassman	**(INVITED)** III-V/Si Integrated Multijunction Solar Cells for High Efficiency Photovoltaics at Reduced Cost	3rd Annual Symposium on Solar and Sustainable Energy	Gwangju, Korea May 8, 2012
A.M. Carlin, T. J. Grassman, M. R. Brenner, J. Grandal, C. Ratcliff, L.-M. Yang, M. J. Mills, P. Sharma, E. A. Fitzgerald, S. A. Ringel	Lattice-Matched GaP/SiGe Virtual Substrates for Low-Dislocation Density GaInP/GaAsP/Si Solar Cells	38th IEEE PVSC	Austin, TX June 3-8, 2012
T. J. Grassman, A. M. Carlin, C. Ratcliff, D. Chmielewski, J. Grandal, J. Carlin, B. Galiana, L.-M. Yang, M. J. Mills, and S. A. Ringel	**(INVITED)** Heterovalent Integration and Metamorphic Materials Engineering for III-V/Si Photovoltaics and Optoelectronics	International Materials Research Congress XXI	Cancun, Mexico Aug 12-17, 2012
S. A. Ringel, T. J. Grassman, C. Ratcliff, A. M. Carlin, J. A. Carlin, L.-M. Yang, M. J. Mills	**(INVITED)** III-V/GaP Epitaxy on Si for Advanced Photovoltaics and Green Light Emitters	ECS Prime 2012	Honolulu, HI Oct 7-12, 2012
S.A.Ringel, T.J. Grassman, J.A. Carlin	**(INVITED)** III-V/active-Si multijunctions by MOCVD and MBE for future photovoltaics	Workshop on Compound Semiconductor Materials and Devices	New Orleans, LA Feb 17-20, 2013
D.J. Chmielewski, T.J. Grassman, A.M. Carlin, C. Ratcliff, S.A. Ringel	Metamorphic tunnel junctions for high efficiency III-V/IV multi-junction solar cell technology	"III-V on Si Solar Cells" at 39th IEEE PVSC	Tampa, FL June 16-21, 2013
S.A. Ringel, J.A. Carlin, T.J. Grassman, B. Galiana, A.M. Carlin, C. Ratcliff, D. Chmielewski, J. Yang, M.J. Mills, A. Mansouri, S.P. Bremner, A. Ho-Baillie, X. Hao, H. Mehrvarz, G. Conibeer and M.A. Green	**(INVITED)** Ideal GaP/Si heterostructures grown by MOCVD: III-V/active-Si subbcells, multijunctions and MBE-to-MOCVD III-V/Si interface science	"Advances in IIII-V Heteroepitaxial Materials and Devices" at 39th IEEE PVSC	Tampa, FL June 16-21, 2013

Full Author List	Paper Title	Presented in the Session / Conference	Location, Dates
T. J. Grassman, J. A. Carlin, S. A. Ringel	Epitaxially-Grown Metamorphic $GaAs_{0.7}P_{0.3}$/Si Dual-Junction Solar Cells	"Advances in Science and Engineering of Multijunction Devices" at 39th IEEE PVSC	Tampa, FL June 16-21, 2013
Alexander Haas, Paul R Sharps, Daniel Aiken, Tyler Grassman, John A Carlin, Steve Ringel	Analysis of Short- and Long-Term Performance Goals for III/V on Active Si Concentrator Solar Cells	In session III-V on Si Solar Cells at 39th IEEE PVSC	Tampa, FL June 16-21, 2013
Ibraheem Al Mansouri, Stephen Bremner, Anita Ho-Baillie, Hamid Mehrvarz, Xiaojing Hao, Gavin Conibeer, Martin A. Green, Tyler J. Grassman, John A. Carlin, and Steven A. Ringel	Design of Bottom Silicon Solar Cell in Multijunction Stacks	"Single-Junction III-V Cells" at 39th IEEE PVSC	Tampa, FL June 16-21, 2013
Martin A. Green, X. Hao, S. Bremner, G. Conibeer, I. Al Mansouri, N. Song, Z. Liu, S.A. Ringel, J.A. Carlin, T.J. Grassman, B. Galiana, A.M. Carlin, C. Ratcliff, D. Chmielewski, L. Yang, M.J. Mills, G. Teeter and M. Young	**(INVITED PLENARY)** Silicon Wafer-Based Tandem Cells: The Ultimate Photovoltaic Solution	"Material Studies, New Concepts, Ultra-High Efficiency and Space Technology" at 28th EU PVSEC	Paris, France September 30, 2013
Chris Ratcliff, T. J. Grassman, J. A. Carlin, S. A. Ringel	Development of Ga(x)In(1-x)P on Si for High Performance, Low Cost Multijunction Photovoltaics	"Concentrator Photovoltaics, III-V and Space" at 23rd PVSEC	Taipei, Taiwan October 28-November1, 2013
S. A. Ringel, T. J. Grassman, J. A. Carlin, C. Ratcliff, D. Chmielewski	**(INVITED)** Heteroepitaxial III-V/Si for Advanced Multijunction Photovoltaics	"Electronic Materials and Processing" at 60th AVS International Symposium	San Francisco, CA Oct 28 - Nov 1, 2013
S. A. Ringel, T. J. Grassman, J. A. Carlin, C. Ratcliff, D. J. Chmielewski, S. P. Bremner, I. Al-Mansouri, M. A. Green, E. Garcia-Tabares, I. Rey-Stolle, C. Algora del Valle	**(INVITED)** Advances in III-V/active-silicon multijunction photovoltaics for high Efficiency	"Advances Toward Tandems with Active Silicon Subcells" at SPIE Photonics West	San Francisco, Ca February 1-6, 2014
Chris Ratcliff, T. J. Grassman, J. A. Carlin, D.J. Chmielewski, S. A. Ringel	Ga-rich $Ga_xIn_{1-x}P$ solar cells on Si with 1.95 eV bandgap for ideal III-V/Si photovoltaics	"Advances in Multijunction Materials and Devices" at SPIE Photonics West	San Francisco, Ca February 1-6, 2014

Full Author List	Paper Title	Presented in the Session / Conference	Location, Dates
S. D. Carnevale, J. I. Deitz,T. J. Grassman, J. A. Carlin, Y. N. Picard, M. De Graef, S. A. Ringel	Rapid Characterization of Extended Defects in III-V/Si by Electron Channeling Contrast Imaging	"III-V on Si Solar Cells" at 40th IEEE PVSC	Denver, CO June 8-13, 2014
T. J. Grassman, J. A. Carlin, S. D. Carnevale, D. J. Chmielewski, I. Al Mansouri, S. Bremner, A. Ho-Baillie, E. García-Tabarés, I. Rey-Stolle, M. A. Green, S. A. Ringel	**(INVITED)** Progress Toward a Si-Plus Architecture: Epitaxially-Integratable Si Subcells for III-V/Si Multijunction Photovoltaics	"III-V on Si Solar Cells" at 40th IEEE PVSC	Denver, CO June 8-13, 2014
S. D. Carnevale, J. I. Deitz,T. J. Grassman, J. A. Carlin, Y. N. Picard, M. De Graef, S. A. Ringel	Rapid Misfit Dislocation Characterization in Heteroepitaxial III-V/Si Thin Films by Electron Channeling Contrast Imaging	"Compound Semiconductor Growth on Si Substrates and Si-Based Heterojunctions" at 56th MRS EMC	Santa Barbara, CA Jun 25-27, 2014
T. J. Grassman, J. A. Carlin, S. D. Carnevale, I. Al Mansouri, S. Bremner, A. Ho-Baillie, E. García-Tabarés, I. Rey-Stolle, M. A. Green, S. A. Ringel	Progress Toward a Si-Plus Architecture: Epitaxially-Integratable Si Subcells for III-V/Si Multijunction Photovoltaics	"Solar Cell Materials and Devices" at 56th MRS EMC	Santa Barbara, CA Jun 25-27, 2014
D. J. Chmielewski, T. J. Grassman, C. Ratcliff, J. A. Carlin, S. A. Ringel	Metamorphic III-V Sub-Cells and Tunnel Junctions for III-V/Active-Si Multijunction Solar Cells	"Solar Cell Materials and Devices" at 56th MRS EMC	Santa Barbara, CA Jun 25-27, 2014
J. I. Deitz, S. D. Carnevale, J. A. Carlin, D. McComb, M. De Graef, Y. N. Picard, S. A. Ringel, T. J. Grassman	Using Electron Channeling Contrast Imaging for Misfit Dislocation Characterization in Heteroepitaxial III-V/Si Thin Films	"Nano-Characterization of Emerging Photovoltaic Materials and Devices" at Microscopy & Microanalysis 2014	Hartford, CT Aug 3-7, 2014
S. A. Ringel, T. J. Grassman, J. A. Carlin, S. D. Carnevale, D. J. Chmielewski, C. Ratcliff	**(INVITED)** Defects in Photovoltaics: III-V/Si Multijunction Solar Cells	"Materials for Photovoltaics" at Gordon Conference (Defects in Semiconductors: Power, Efficiency, and Functionality)	Waltham, MA Aug 3-8. 2014
T. J. Grassman, S. D. Carnevale, J. I. Deitz, J. A. Carlin, D. McComb, S. A. Ringel	Rapid Extended Defect Characterization in Semiconductor Heterostructures by ECCI	23rd Space Photovoltaic Research and Technology (SPRAT) Conference	Cleveland, OH Oct 28 - 30, 2014
D. W. Cardwell, C. Ratcliff, N. Vaughn, S. Carnevale, T. J. Grassman, S. A. Ringel	Metamorphic and Lattice-Matched Wide-Gap AlGaInP-based Top-Cell Materials and Cells for III-V Multijunction Photovoltaics	23rd Space Photovoltaic Research and Technology (SPRAT) Conference	Cleveland, OH Oct 28 - 30, 2014
T. J. Grassman, D. J. Chmielewski, C. Ratcliff, S. D. Carnevale, J. A. Carlin, S. A. Ringel	**(INVITED)** Advances in III-V/Active-Silicon Multijunction Photovoltaics: Progress Toward a Si-Plus Architecture	"State-of-the-Art Program on Compound Semiconductors" at 227th Electrochemical Society Meeting	Chicago, IL May 24-28, 2015

Full Author List	Paper Title	Presented in the Session / Conference	Location, Dates
D. J. Chmielewski, T. J. Grassman, S. D. Carnevale, J. A. Carlin, S. A. Ringel	High-Performance Metamorphic Tunnel Junctions on Si for III-V/Si Multijunction Solar Cells	"III-V on Si via Direct III-V/Si Heteroepitaxy" at 42nd IEEE PVSC	New Orleans, LA Jun 14-19, 2015
E. García-Tabarés, D. Martín, I. Rey-Stolle, T. J. Grassman, J. A. Carlin, S. A. Ringel	Evolution of the Silicon Bottom Cell Photovoltaic Behavior during III-V on Si Multi-junction Solar Cells Production	"III-V on Si via Direct III-V/Si Heteroepitaxy" at 42nd IEEE PVSC	New Orleans, LA Jun 14-19, 2015
T. J. Grassman, D. J. Chmielewski, S. D. Carnevale, J. A. Carlin, S. A. Ringel	**(INVITED)** Progress in the Development of Epitaxial GaAsP/Si Dual-Junction Solar Cells	"III-V on Si via Direct III-V/Si Heteroepitaxy" at 42nd IEEE PVSC	New Orleans, LA Jun 14-19, 2015
D. W. Cardwell, C. Ratcliff, N. R. Vaughn, S. D. Carnevale, T. J. Grassman, S. A. Ringel	Investigations of Metamorphic (Al)GaInP for III-V Multijunction Photovoltaics	"III-V Solar Cells - Metamorphic Multijunctions" at 42nd IEEE PVSC	New Orleans, LA Jun 14-19, 2015
J. I. Deitz, S. D. Carnevale, S. A. Ringel, D. W. McComb, T. J. Grassman	Extending Characterization Applications of Electron Channeling Contrast Imaging	"Characterization of Multijunction and Concentrator Cells" at 42nd IEEE PVSC	New Orleans, LA Jun 14-19, 2015
T. J. Grassman, D. J. Chmielewski, S. D. Carnevale, J. A. Carlin, S. A. Ringel	Advances in the Development of Epitaxial GaAsP/Si Dual-Junction Solar Cells	"Solar Cells - Wide Bandgap and Tandem Cells" at 57th EMC	Columbus, OH Jun 24-26, 2015
J. I. Deitz, S. D. Carnevale, S. A. Ringel, D. W. McComb, T. J. Grassman	Extending Characterization Applications of Electron Channeling Contrast Imaging	"Nanoscale Characterization and Microscopy" and 57th EMC	Columbus, OH Jun 24-26, 2015
D. J. Chmielewski, T. J. Grassman, S. D. Carnevale, J. A. Carlin, S. A. Ringel	High-Performance Metamorphic Tunnel Junctions on Si for III-V/Si Multijunction Solar Cells	"Solar Cells - Wide Bandgap and Tandem Cells" at 57th EMC	Columbus, OH Jun 24-26, 2015
J. I. Deitz, S. D. Carnevale, S. A. Ringel, D. W. McComb, T. J. Grassman	Extending Characterization Applications of Electron Channeling Contrast Imaging	"Advances in Electron Diffraction and Automated Mapping Techniques" at Microscopy & M 2015	Portland, OR Aug 2-6, 2015
D. J. Chmielewski, T. J. Grassman, S. D. Carnevale, J. A. Carlin, S. A. Ringel	High-Performance Metamorphic Tunnel Junctions on Si for III-V/Si Multijunction Solar Cells	Materials Science & Technology 2015	Columbus, OH Oct 4-8, 2015
T. J. Grassman, D. J. Chmielewski, C. Ratcliff, S. D. Carnevale, J. A. Carlin, S. A. Ringel	**(INVITED)** Advances in III-V/Si Structures for Multijunction Solar Cells	Materials Science & Technology 2015	Columbus, OH Oct 4-8, 2015

Software

None

Other

None

References

1. V. Narayanan, S. Mahajan, K. J. Bachmann, V. Woods and N. Dietz, Philos. Mag. A **82**(4), 685 (2002).
2. V. Narayanan, S. Mahajan, K. J. Bachmann, V. Woods and N. Dietz, Acta Mater. **50**(6), 1275 (2002).
3. T. J. Grassman, M. R. Brenner, S. Rajagopalan, R. Unocic, R. Dehoff, M. Mills, H. Fraser and S. A. Ringel, Appl. Phys. Lett. **94**(23), 232106 (2009).
4. T. J. Grassman, J. A. Carlin, B. Galiana, L.-M. Yang, F. Yang, M. J. Mills and S. A. Ringel, "Nucleation-related defect-free GaP/Si(100) heteroepitaxy via metal-organic chemical vapor deposition," *Applied Physics Letters **102**(14)*, 142102 (2013).
5. T. J. Grassman, D. J. Chmielewski, S. D. Carnevale, J. A. Carlin and S. A. Ringel, "$GaAs_{0.75}P_{0.25}$/Si Dual-Junction Solar Cells Grown by MBE and MOCVD," *IEEE Journal of Photovoltaics **6**(1)*, 326 (2016).
6. H. Kroemer, *J. Cryst. Growth **81**(1-4)*, 193 (1987).
7. V. Narayanan, S. Mahajan, N. Sukidi, K. J. Bachmann, V. Woods and N. Dietz, *Philos. Mag. A **80**(3)*, 555 (2000).
8. Y. N. Picard, R. Kamaladasa, M. De Graef, N. T. Nuhfer, W. J. Mershon, T. Owens, L. Sedlacek and F. Lopour, Microscopy Today 20, 12, 2012.
9. Haas, A. W.; Wilcox, J. R.; Gray, J. L. & Schwartz, R. J. “Numerical modeling of loss mechanisms resulting from the distributed emitter effect in concentrator solar cells.” Photovoltaic Specialists Conference (PVSC), 2009 34th IEEE, 2009
10. Haas, A. W. “Computer-aided Analysis of Multijunction Solar Concentrator Cells and Systems.” PhD Thesis. Purdue University, 2011
11. Galiana, B.; Algora, C.; Rey-Stolle, I. & Vara, I. G. “A 3-D Model for Concentrator Solar Cells Based on Distributed Circuit Units.” IEEE Transactions on Electron Devices, 2005, 1, 1-7
12. Kish, F. A. and Fletcher, R. M.,"AlGaInP Light-Emitting Diodes," in *Semiconductors and Semimetals: High Brightness Light Emitting Diodes*, vol. 48, edited by Stringfellow (Academic Press, 1997)
13. Chen, C. H., Stockman, S. A., Peanasky, M. J. and Kuo, C. P.,"OMVPE Growth of AlGaInP for High-Efficiency Visible LEDs," in *Semiconductors and Semimetals: High Brightness Light Emitting Diodes*, edited by Stringfellow (Academic Press, 1997)
14. Kazuo Watanabe and Hajime Yamazaki, "Annealing effect on the carrier concentration in heavily C-doped p^+-AlGaAs," *Applied Physics Letters **60**(7)*, 847-849 (1992).
15. C. Ebert, Z. Pulwin, D. Byrnes, A. Paranjpe, and W. Zhang, "Tellurium doping of InGaP for tunnel junction applications in triple junction solar cells," *Journal of Crystal Growth **315**(1)*, 61-63 (2011).