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13. SUPPLEMENTARY NOTES

14. ABSTRACT
This innovation to fiber optic component technology increases the performance, reduces the size and reduces the power consumption of optical communications within dense network systems, such as advanced distributed computing systems and data centers. VCSEL technology is enabling short-reach (< 100 m) and >100 Gbps optical interconnections over multi-mode fiber in commercial applications.

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1. Executive Summary

This program developed high-data-rate fiber optic transceivers for the "embedded optical module" (EOM) market. With increasing data rates, there is a trend within computing systems to place the fiber optic component near the high-performance ASIC within the PCB chassis. Placing the optical conversion close to the electronic device reduces the length of high-speed electrical paths, and reduces the power consumption and costs associated with overcoming electrical signal loss and distortion on copper traces.

The current approach to manufacturing and fielding EOM transceivers is expensive. Today's EOMs are assembled with a number of complex, low-yielding, and precisely aligned sub-components. The plastic components used for optical coupling are not compatible with the solder reflow process (due to both the high temperature and the solder washing process, which would contaminate the lenses). Therefore, the EOM devices are fielded in a pluggable socket or land-grid-array connector, which adds expense to both the PCB and component, and requires extra PCB real-estate for the connector mechanism. Secondly, the EOM components are not rated to work at temperatures greater than 70 C (primarily due to optical mis-alignment and the lack of laser calibration). This requires special precautions to limit the EOM temperature (extra cooling on the EOM or limiting the chassis temperature).

This program leveraged transceiver chip-scale-packaging (CSP) concepts developed for aerospace applications. These applications have severe restrictions on component size and require operation in a high temperature environment. There are five key elements that this program brought to the EOM market:

High temperature operation – the CSP transceiver utilizes an 'expanded beam optical interface' (EBOI) that provides efficient optical coupling over wide temperature ranges (up to 100 C). The lens array is formed in wafer scale in a glass with a matching coefficient of thermal expansion (CTE) to the laser array substrate.

Solder reflow compatibility – the CSP transceiver is made of materials of matching CTE in an assembly of multiple 'planar' structures that are easily aligned and stacked. This structure greatly reduces the assembly complexity and is robust enough for solder reflow.

Sealed optics – the lens components are sealed from contamination, which is important for two reasons: 1) protection from the solder-reflow 'wash' cycle, and 2) will operate in a fluid submersion environment – which is a method of cooling being considered for high-end, high-density computing systems[1, 2].

Reduced Cost – this program reduced the cost of manufacturing and fielding the transceiver by: 1) reducing the BOM count, 2) simplifying the manufacturing process, both in the number of assembly steps and by using standard flip-chip bonding processes to achieve optical alignment, 3) pre-screening VCSEL devices, and 4) eliminating the need for a mechanical socket. The number of transceivers utilized in supercomputers can be in the 100's of thousands, as they replace copper wiring at shorter distances, and therefore, transceiver cost is an important issue.

Optimized performance – the CSP packaging approach creates high-speed electrical paths that are precisely controlled (photo-lithographically define), with flip-chip assembly replacing wire-bonds. This offers the lowest electrical parasitic and reduces the need for active equalization and/or clock-and-data recovery (CDR), which increases the overall power consumption. We expect CSP technology to support components having data rates to 56 Gbps or higher, and with 24 channels, for greater than 1 Tbps data transmission in single component.

The Phase II program created and demonstrated VCSEL-array based transceiver CSP components operating at the 28 Gbps node. These parts will operate as a 4-lane Tx + 4-lane Rx devices (100 Gbps bi-directional). The overall goal was to create a compact and cost-effective packaging platform to accommodate dense, high-speed optical interconnects.

A key metric utilized in the data communications industry is the energy/bit transmitted over a link. This energy is dominated by the ASICs [3]. We achieved the best-in-class energy/bit by utilizing the lowest-power transceiver ASICs commercially available. Macom is supplier of CMOS transceiver ASICs that are the lowest-power consumption at the 25 Gbps node (8 pJ/bit for end-to-end link).

2. Phase II Accomplishments

The following is a summary of the Phase II program accomplishments in the development and prototype testing of the CSP transceiver. These accomplishments are described below in four sections, Design Review, Fabrication, Test Results, Impact on Industry and Follow-on Activity.

2.1. Design Review

The program started with a detailed design review of the CSP transceiver having 4 transmitter channels and 4 receiver channels at 28 Gbps data rate per channel. The design can be configured to have 12 transmitter and 12 receiver channels (the optics and fiber connector has 12 channels). Figure 1 shows the final design. The body of the transceiver is 10.6 mm wide and 8.6 mm deep. The height of the transceiver is 2.1 mm. The CSP has a fiber connector interface that is formed with 0.4 mm thick metal. This metal piece is bonded to the CSP carrier and hold the RVCON fiber connector in place.

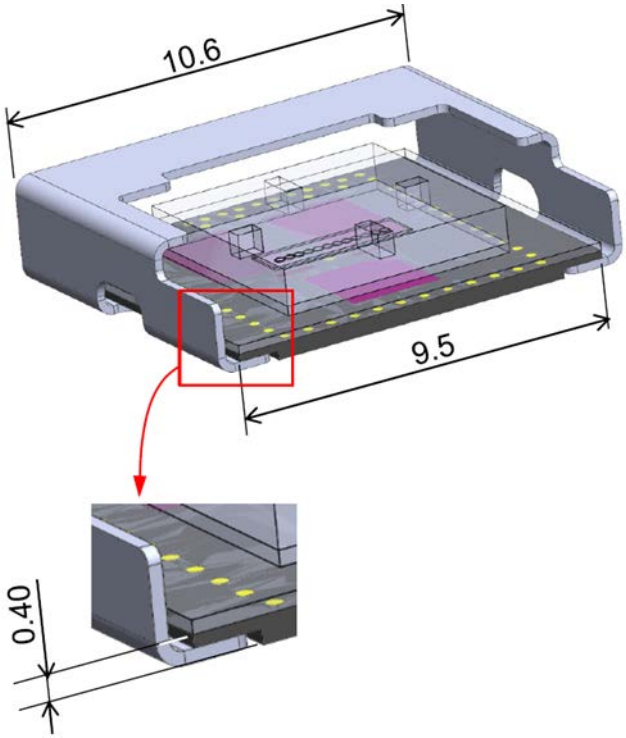


Figure 1: CSP transceiver design

The RVCON fiber connector is the optical interface to the CSP transceiver. The RVCON is a molded component. A stainless steel latch was designed to mate the RVCON to the CSP. The latch has 'wings' that engage with the metal housing on the CSP. A slider engages the connector to the CSP.

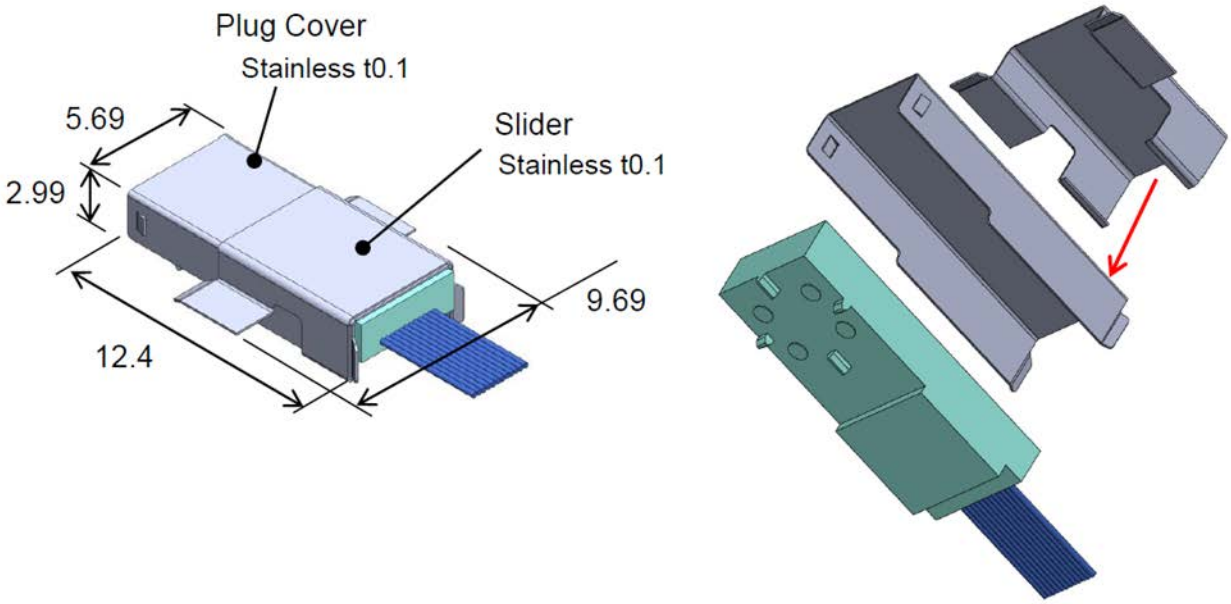


Figure 2:RVCON fiber connector with stainless steel plug cover and 'winged' slider.

The CSP footprint is shown in Figure 3. This is a copper-pillar with solder-cap interface to the customer PCB. The pitch of the pin-out is 0.3 mm (12 mil), a pitch that is commonly available to PCB manufacturers. The PCB space required is 8.6 x 9.5 mm^2. The central area of the CSP is the thermal interface to the customer PCB.

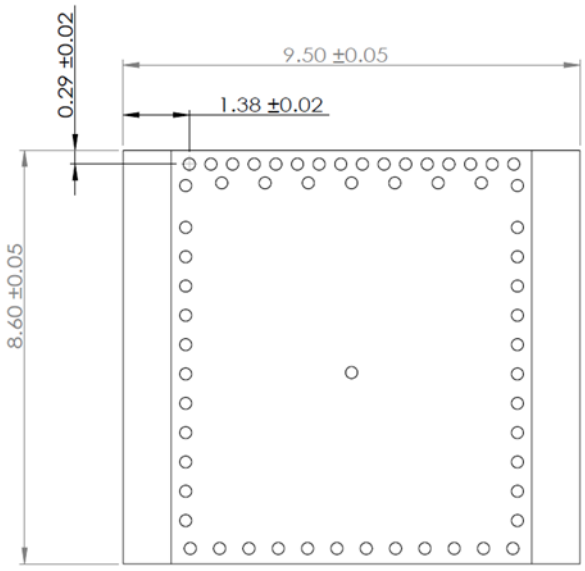


Figure 3: CSP footprint on customer PSB.

The layout of the CSP carrier is shown in Figure 4. The carrier is transparent substrate with metal on one-side. This metal is used to form bumps for mounting ASICs and OE devices (VCSELs, PINs), routing signals between components, and copper pillar I/O. The carrier has flip-chip attach patterns for a microcontroller (MCU), a 1 x 4 VCSEL array, a 1 x 4 PIN array, and the two transceiver (TRX) ASICs. The TRX ASICs are SiGe ASICS, a VCSEL driver and a receiver ASIC.

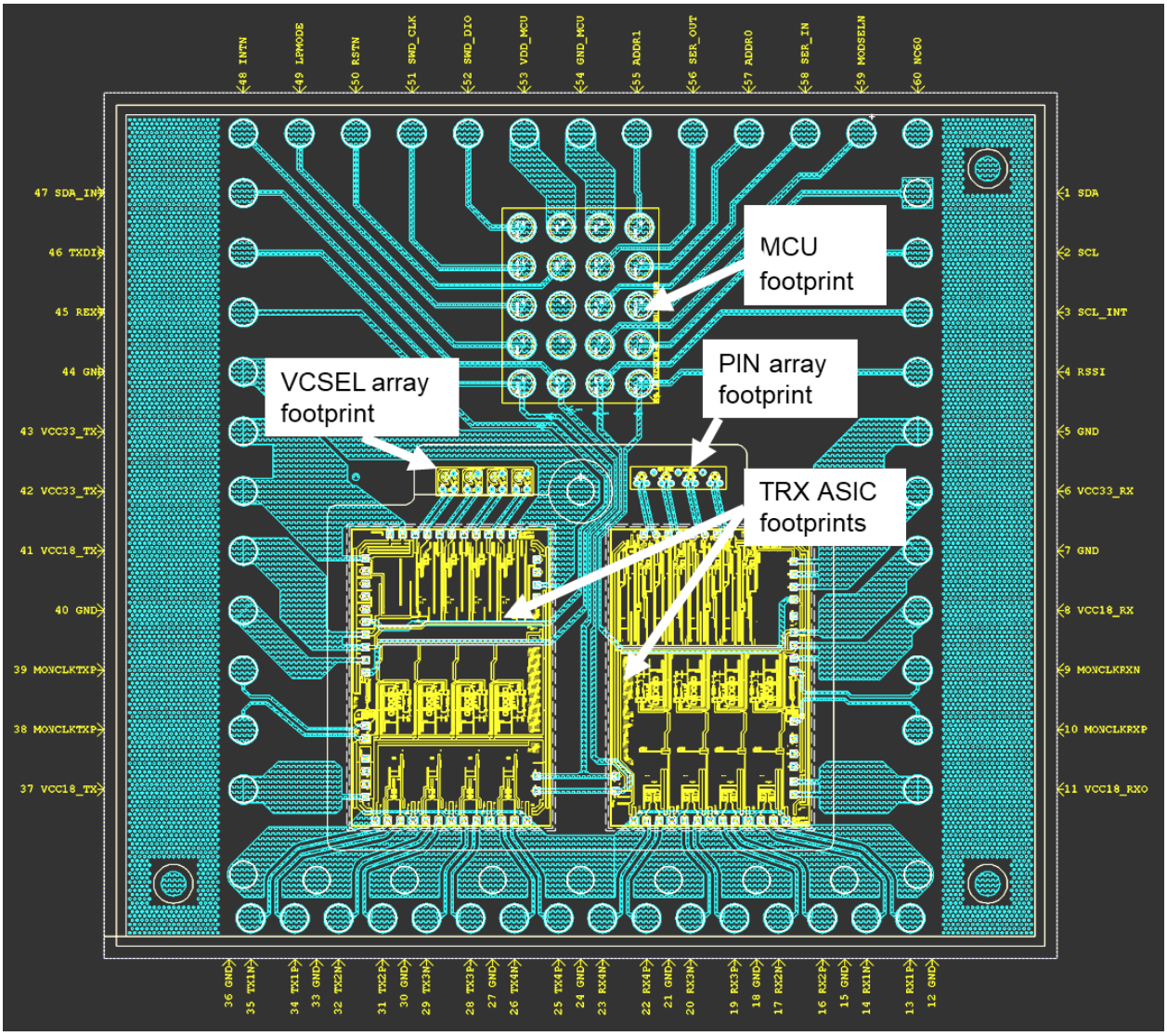


Figure 4: Layout of the CSP carrier.

Of particular concern is the electrical I/O between the TRX ASICs on the CSP and the customer PCB. We performed simulations on this I/O and optimized for 28G data transport (see Figure 5). If we can achieve a clean electrical interface, some applications will benefit from reduced power consumption.

The portion of the electrical traces on the carrier substrate were designed to be 100 Ω differential waveguides. These waveguides were modeled and optimized with a 2-D field solver. The electrical traces on the PCB (not shown) were also 100 Ω differential waveguides on PCB modeled using 2-D field solver.

The copper pillar interface between substrate and PCB are 300 microns in diameter and 300 microns tall. A 3-D field solver modeled and optimized this portion of the interface.

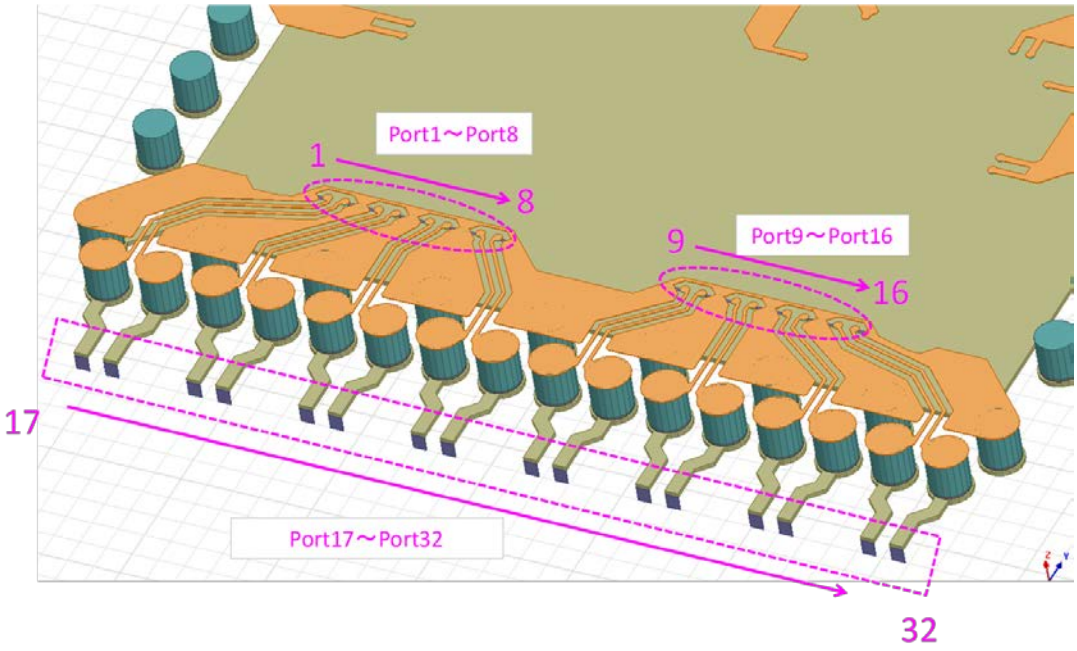


Figure 5: Design of electrical I/O to customer PCB.

The results of the modeling are shown in Figure 6. Simulation was performed up to 84 GHz. Single-ended thru is plotted in dashed lines. 3 dB bandwidth of differential thru is indicated on top of each plot. For good performance at 28 Gb/s we would like to have bandwidth > 21 GHz (0.75 * data-rate). This condition is met comfortably.

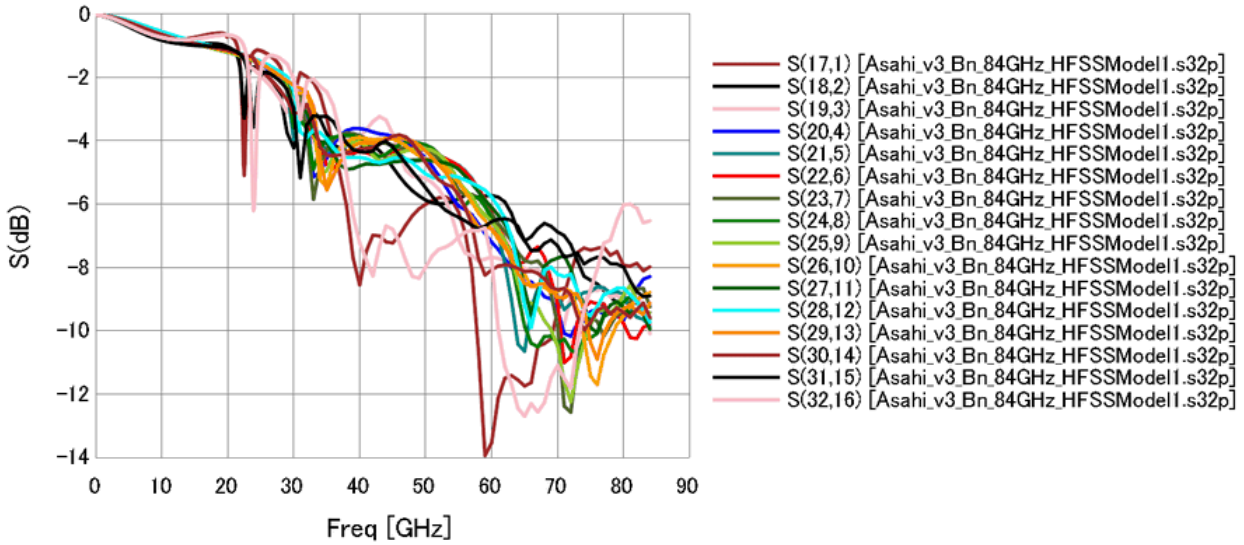


Figure 6: Electrical I/O simulation results.

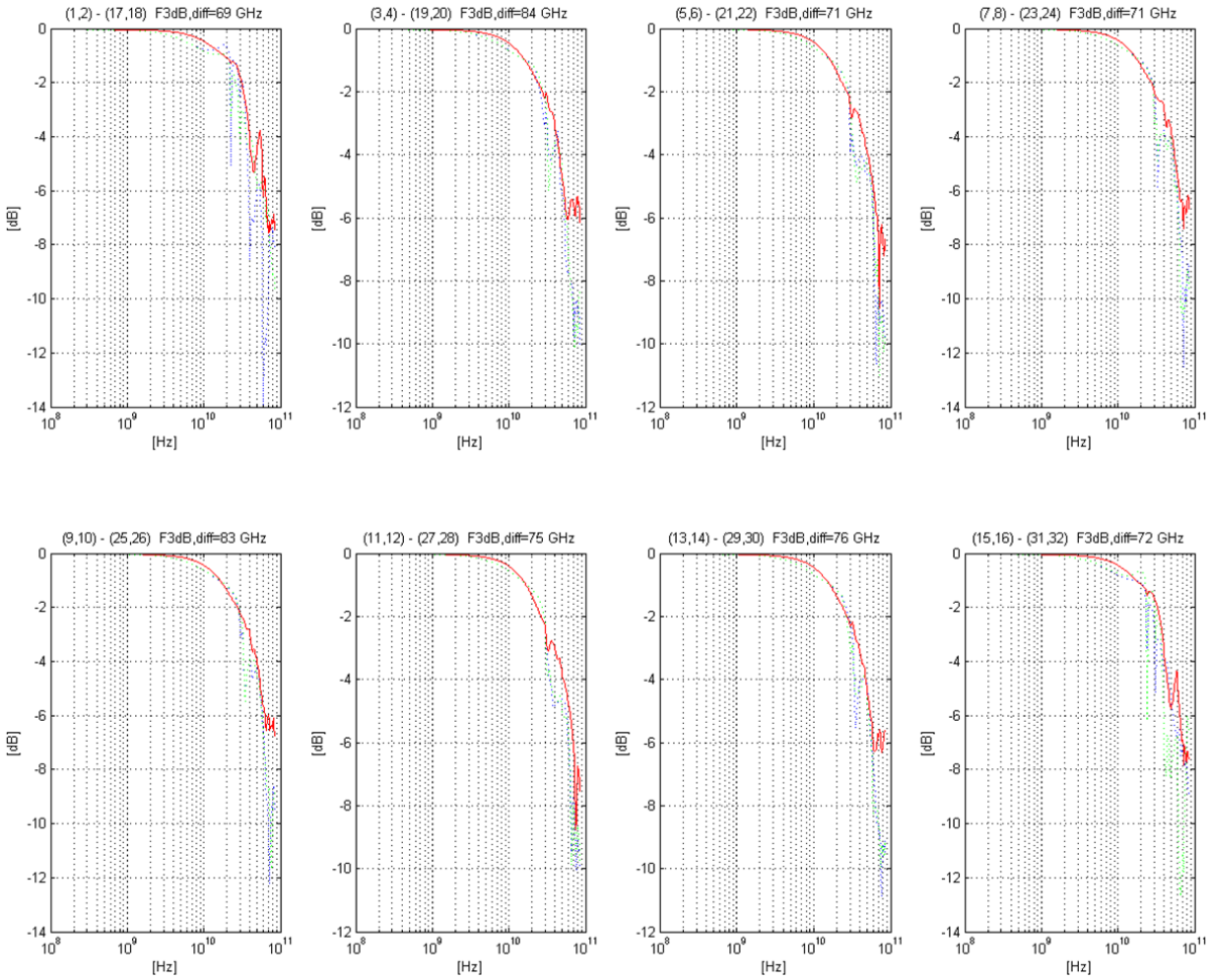


Figure 7: Thru signal simulations.

The four-port s-parameters of each channel mapped into differential two-port and shown in Figure 7. The differential thru is plotted in solid red lines, and the single-ended thru is plotted in dashed lines. The 3 dB bandwidth of differential thru is indicated on top of each plot. For good performance at 28 Gb/s we would like to have bandwidth > 21 GHz (0.75 * data-rate). This condition is met comfortably

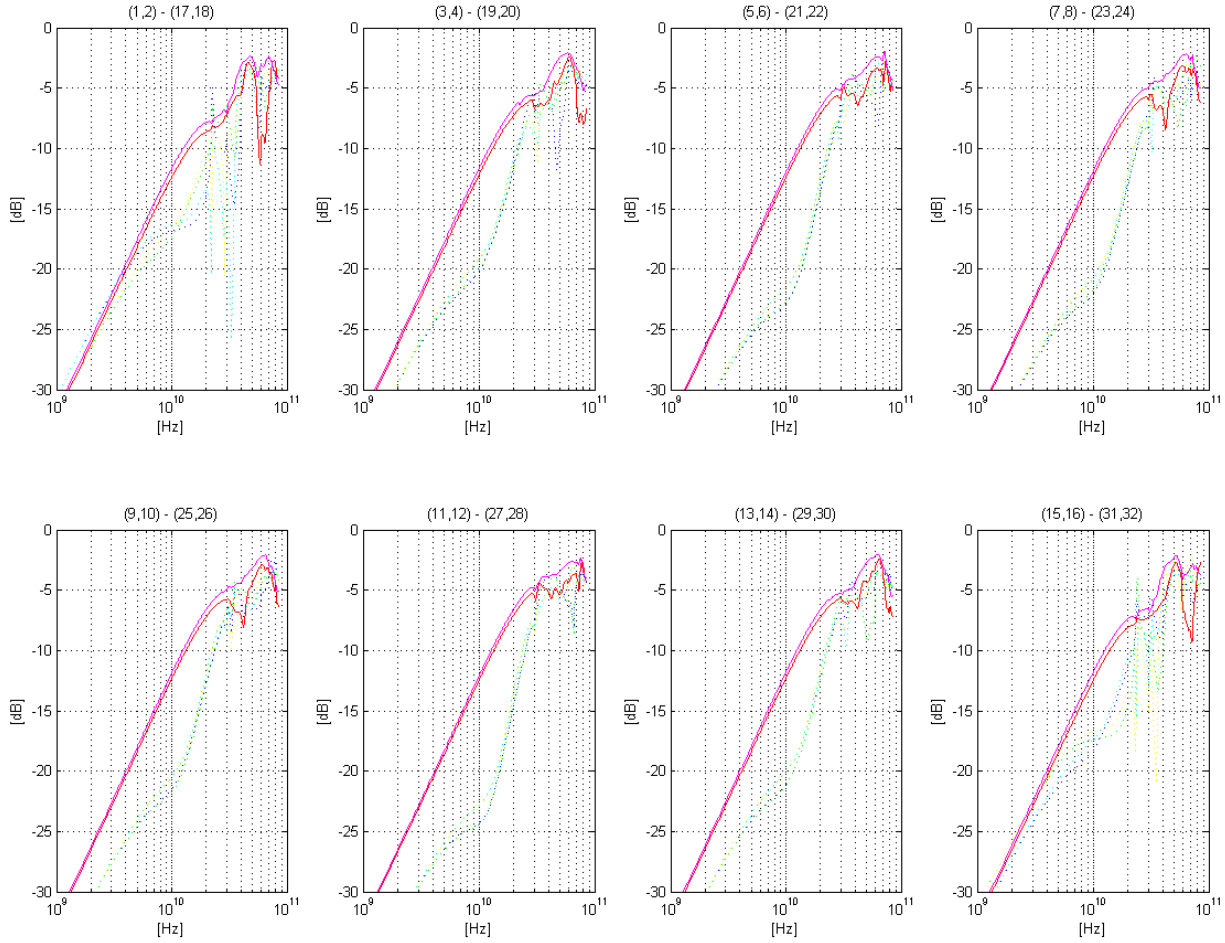


Figure 8: Reflection signal simulations.

The four-port s-parameters of each channel mapped into differential two-port and shown in Figure 8. Differential reflections from each direction are plotted in solid lines. Single-ended reflections from each direction are plotted in dashed lines. These results are good, and met the specific reflection requirements called out by our customer. However, other customers may have other requirements, which can be adjusted either at CSP-level or PCB-level.

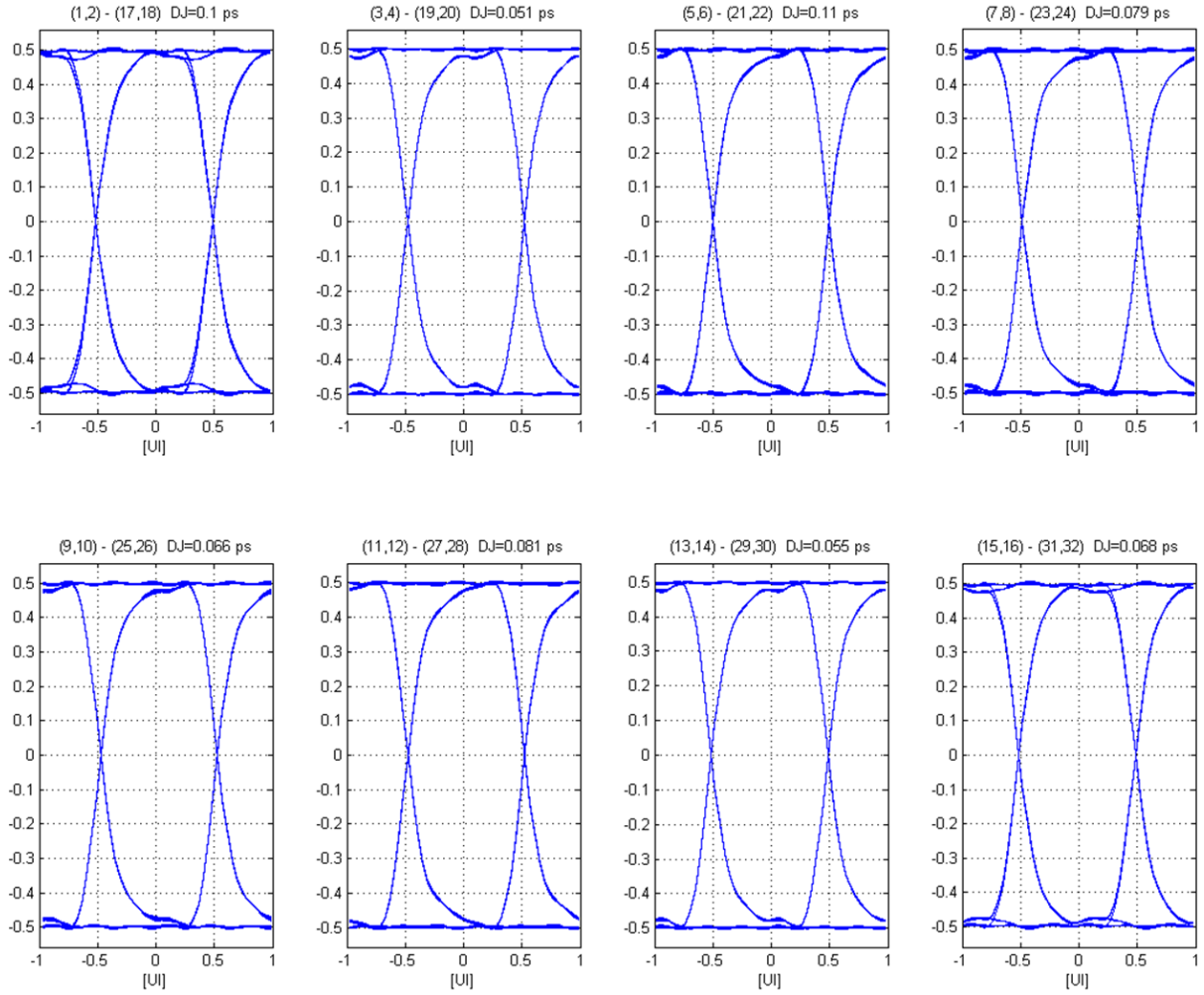


Figure 9: 28 Gbps data transmission.

The simulation of 28 Gbps data transmission modeled using differential thru response in Figure 9. The deterministic jitter (DJ) is noted above each plot. Performance is very good and exceeds commercial standards defined by IEEE for 28 Gbps data transport.

The MCU is an important part of high speed transceivers. The transceiver ASICs have a complex configuration. The configuration contains key parameters to optimize the performance, such as VCSEL biasing, signal equalization, and settings for internal CDRs. Many of these parameters need adjustment over temperature.

The CSP carrier has a second I2C bus to connect locally between MCU and TX/RX ASICs. The MCU implements this interface in software (no hardware I2C support). This is not as efficient as hardware I2C, but sufficient to control ASICs. The I2C interface presented to host is dedicated to the MCU. Multiple CSPs may be shard on the host interface. An additional control input, MODULE_SELECT, is

added to allow host to identify which CSP is being addressed. Two additional control pins, ADDR0 & ADDR1, are added to define the I2C address. Figure 10 shows the MCU interface scheme.

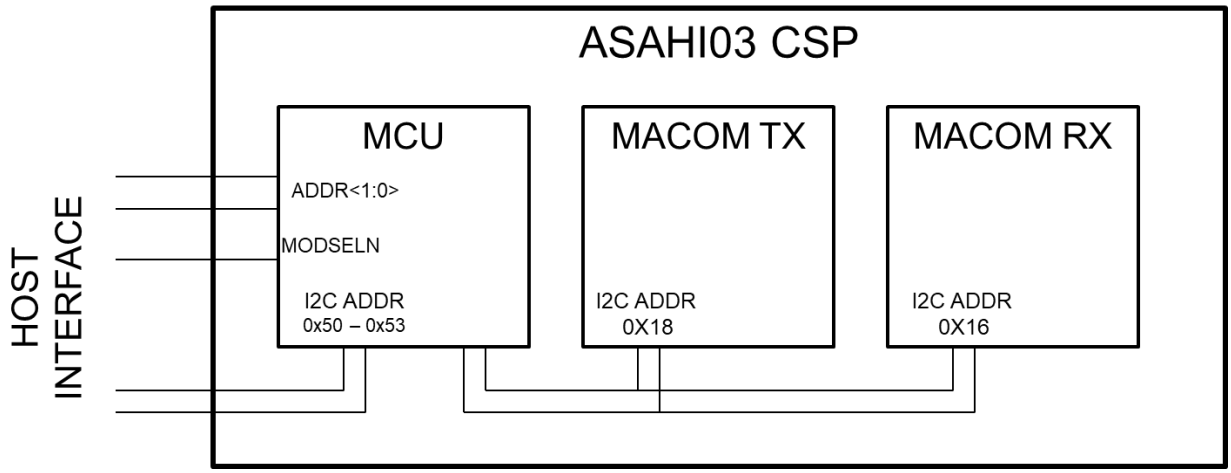


Figure 10: MCU signal routing.

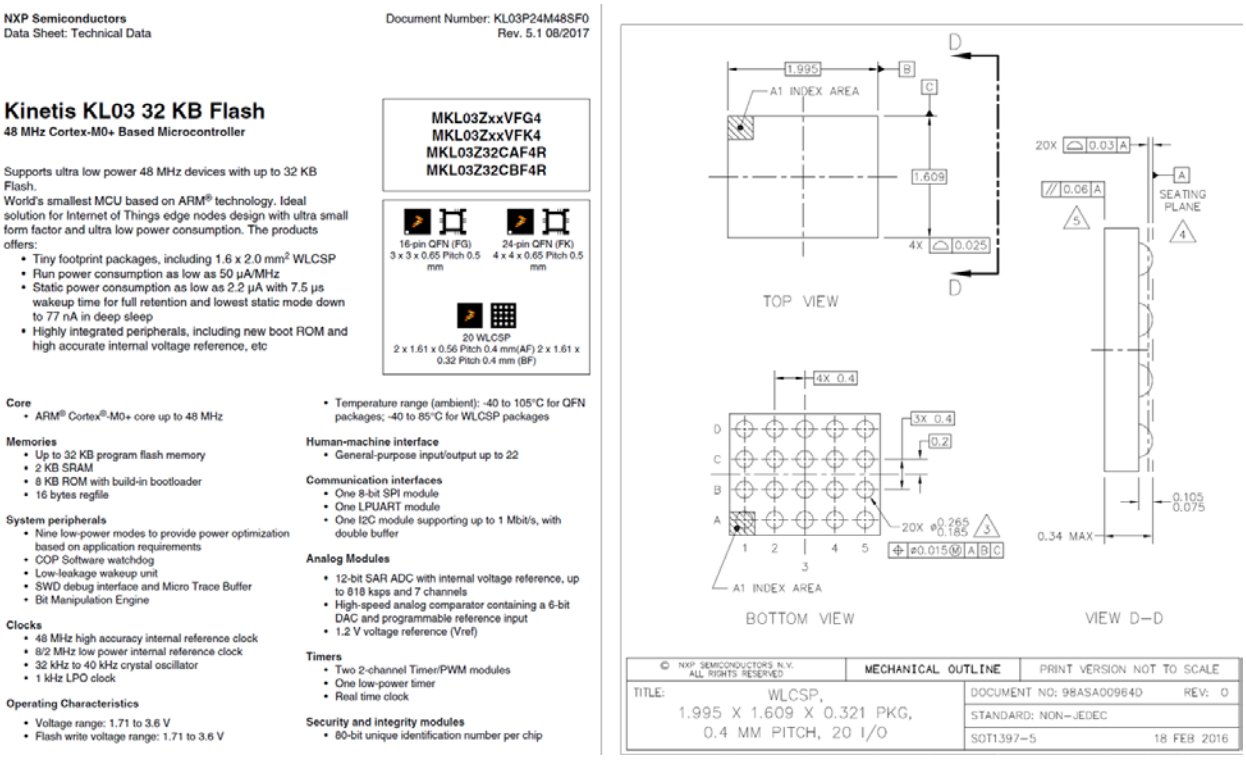


Figure 11: Information on the MCU.

The MCU that was incorporated in the CSP TRX is described in Figure 11. This is a low power ARM device with 32 KB flash memory. The MCU is itself a CSP package, making it very compact for this application.

Solder reflow is used to attach the MCU onto the carrier wafers. The polyimide opening: 215 um diameter. The Ni barrier / Au flash: 232 um diameter. The Au base pad: 250 um diameter. The escape routing: 50 um line / 50 um space.

The interface to the digital logic on the MCU and TRX ASICs is performed over the pins shown in Figure 12.

The CSP relied on II-VI 28G VCSEL devices (see Figure 13). The layout has two electrical pads (P and N), and one mechanical pad (M). The purpose of the mechanical pad is to provide support during the flip-chip process (ensuring the devices remains planar during assembly).

The CSP carrier footprint will provide Au bumps that are 25 um octagonal (printed as round ~34 um diameter). The devices are were bonded using an AuSn diffusion bond process. This process provided placement accuracy of 0.56 microns, well within the tolerance of our optical system.

Pin	Name	Description
1	SDA	I2C interface from host to MCU
2	SCL	
3	SCL_INT	Internal I2C interface between MCU and Macom ASICs. Pinned out to allow for placement of required pull-up resistor, and for testability.
47	SDA_INT	
57	ADDR0	Two-bit module address. I2C address of module defines as 0x50 + ADDR<1:0> for compatibility with QSFP DDMI standard.
55	ADDR1	
59	MODSELN	Module select input. MCU responds to I2C only when MODSELN is low.
48	INTN	Interrupt output generated by MCU ad defined by QSFP standard.
49	LPMODE	Low Power Mode control input as defined by QSFP standard.
46	TXDIS	Direct connection to Macom TX ASIC TXDIS input allowing interlocking (eye safety). This input is also monitored by MCU.
50	RSTN	Reset input to MCU
51	SWD_CLK	Firmware download and debug interface.
52	SWD_DIO	
56	SER_OUT	Asynchronous serial interface. Used to support production and qualification testing using over RS232.
58	SER_IN	
4	RSSI	Analog signal strength indicator output from Macom RX ASIC. Monitored by MCU. Requires external resistor.
~~44~~ 45	REXT	Current reference used by Macom TX ASIC. Required external resistor.

Figure 12: Pin definitions for digital interface.

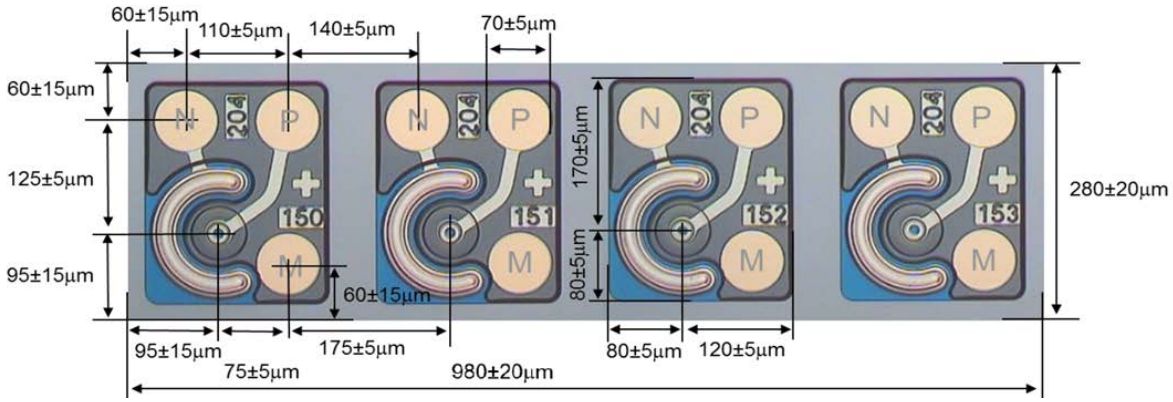


Figure 13: II-VI VCSEL devices.

The CSP carrier footprint will provide Au bumps for the PIN array (see Figure 14). The pads are 25 um octagonal (printed as round ~34 um diameter). The PIN devices are assembled with be Au-to-Au thermo-compression bonding.

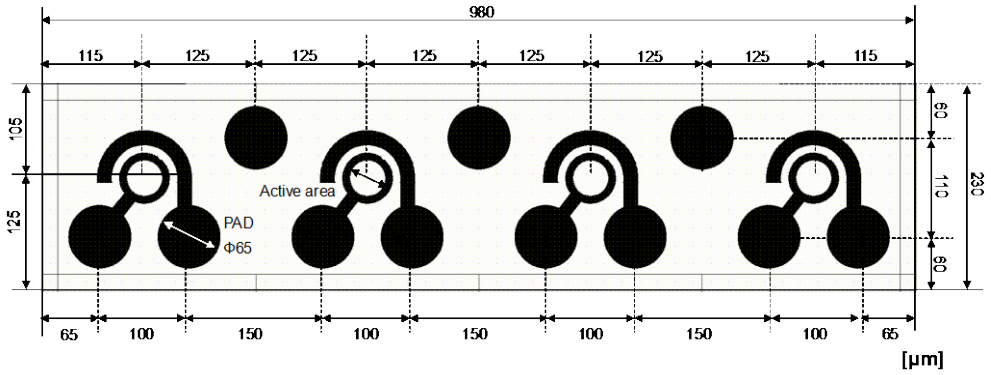


Figure 14: PIN array.

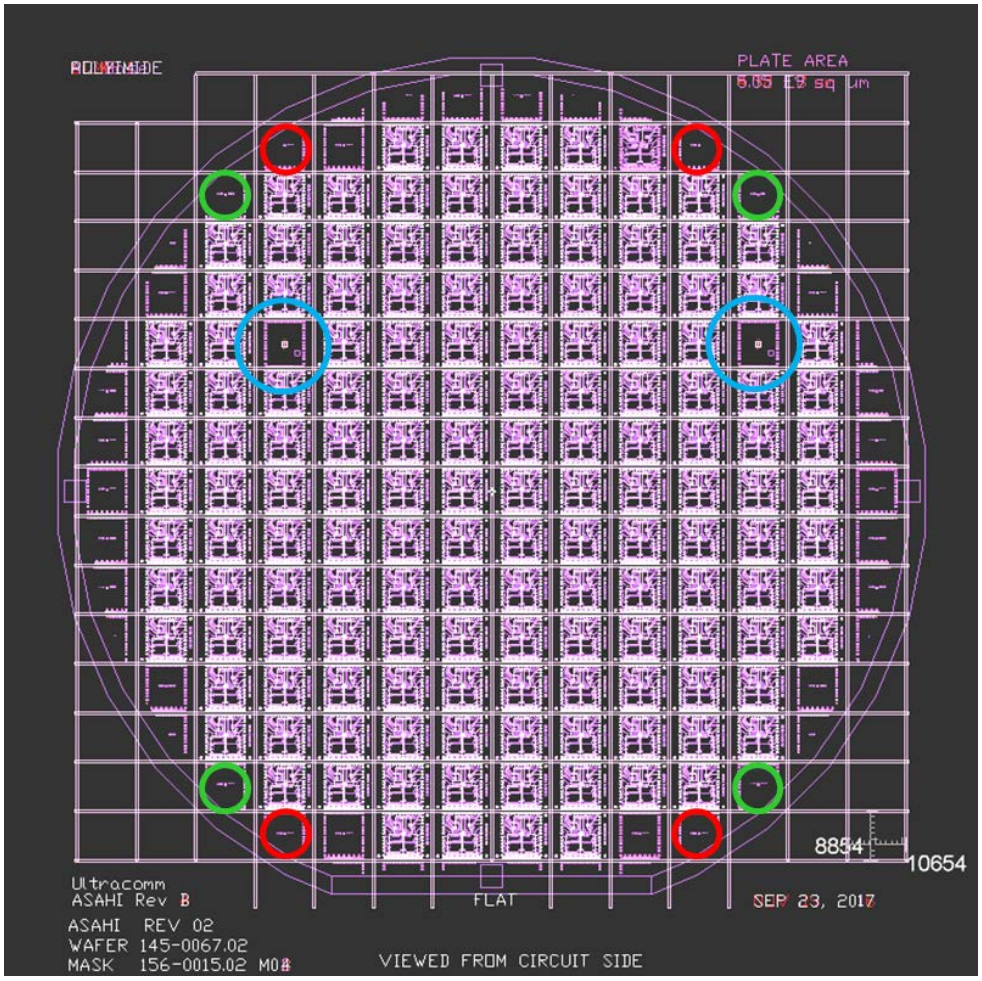


Figure 15: CSP carrier layout in wafer form.

The wafer level layout of the CSP carrier is shown in Figure 16. The wafer is sapphire material with a diameter is 150 mm and the wafer contained 142 copies of the carrier. This used a 254 um saw cut + 100 um clear substrate on each side of cut, for a finished size of diced carrier: 9.5 ± 0.05 mm x 8.6 ± 0.05 mm. The red, green and blue rings are fiducial marks for wafer processing.

2.2. Fabrication

The assembly flow of the CSP transceiver is shown in Figure 17. Here is a summary of the steps:

1. Flip-chip assembly of the ASICs, VCSEL array, PIN array and MCU to the carrier
2. Overmold the assembly, backgrind to expose copper, and add solder balls
3. Attach the collimating lens and lens guide (the lens guide performs two functions: sealing off the optical cavity and providing mechanical engagement to the RVCON)
4. Attach the metal housing for the RVCON connector latch.

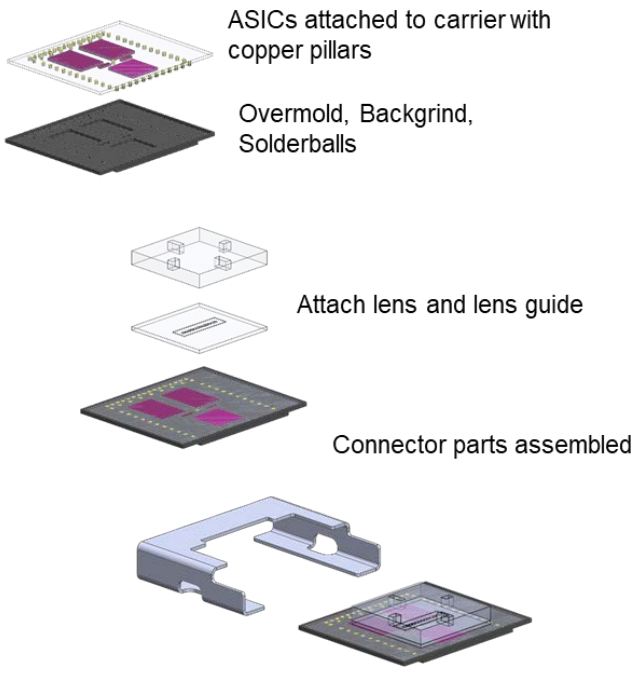


Figure 16: CSP transceiver assembly flow.

Figure 18 and Figure 19 are photographs of the assembly before the overmold is applied. Figure 18 shows the bottom side if the two TRX ASICS (quad VCSEL driver and Receiver), the VCSEL and PIN arrays, and the MCU. The copper pillars are around the periphery, with the high-speed traces using dual rows.

Figure 19 shows the topside of the CSP. The glass lens guide is the top structure with four slots that engage with four cleats on the RVCON. The 1 x12 array of micro-lenses are seen through the lensguide.

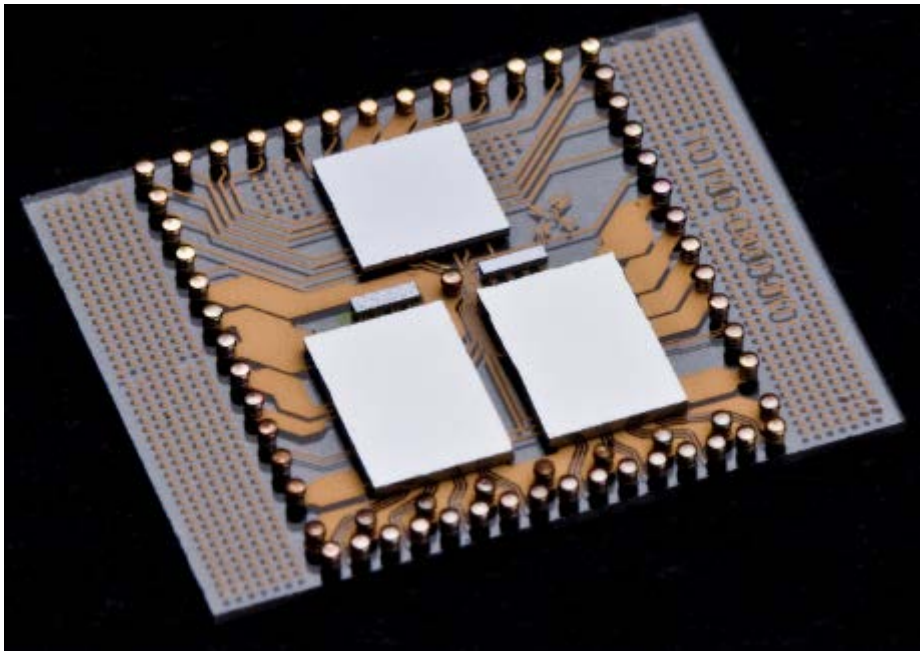


Figure 17: CSP transceiver (bottom side) before overmold.

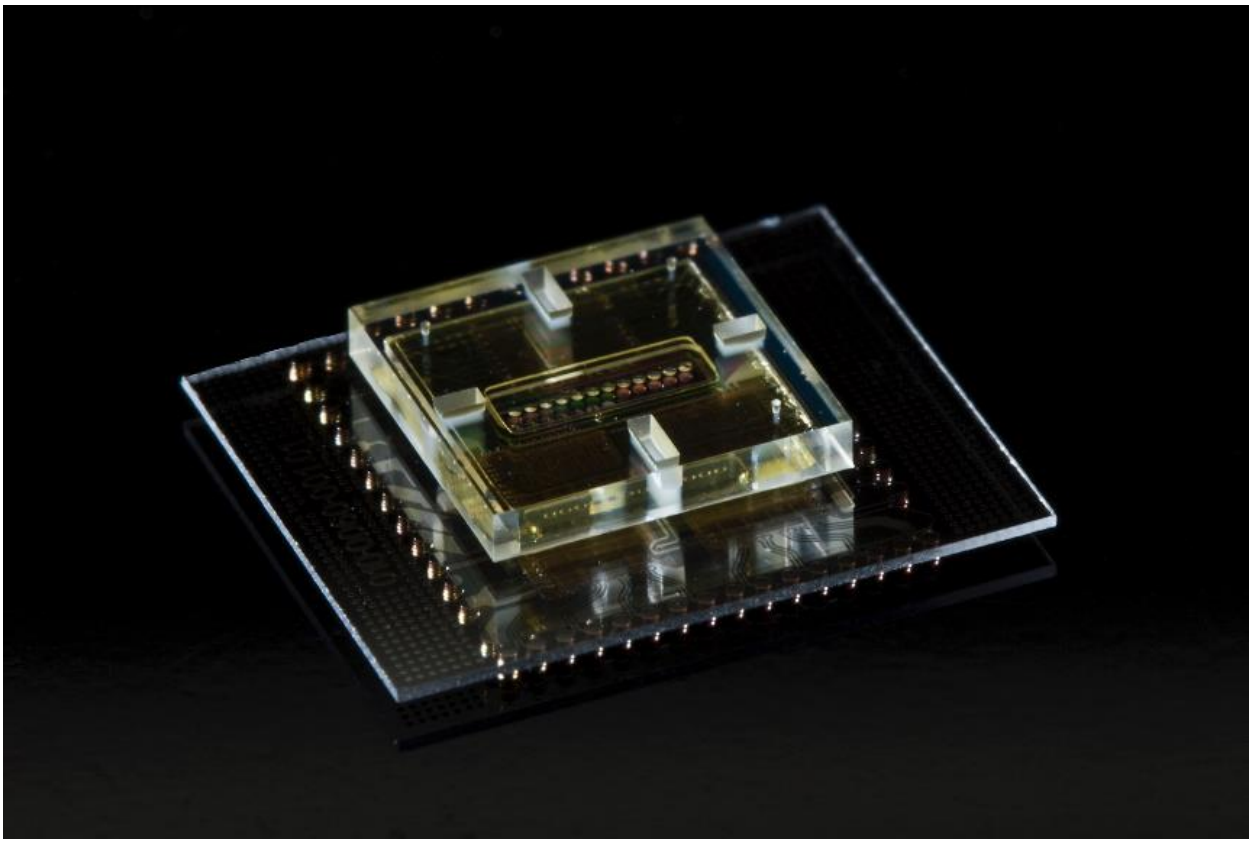


Figure 18: CSP transceiver (top side).

The CSP with the metal housing is shown in Figure 20. The metal housing provides the latching mechanism for the RVCON. The right side of Figure 20 shows the bottom side of the CSP (notice the overmolded components are no longer visible as they were in Figure 18)

Figure 19: The CSP transceiver fully assembled.

The CSP transceiver was soldered to a test board and the RVCON was attached for the testing described in the next section (see Figure 21).

Figure 20: CSP transceiver mounted to test board.

2.3. Test Results

The CSP transceiver were tested against the specifications in the IEEE 802.3bm Annex 83U (CAUI-4) as shown in Figure 22.

Based on IEEE 802.3bm Annex 83E (CAUI-4)

Parameter	Symbol	Min	Typ	Max	Units	Note
Transmitter Inputs						
Signaling rate, each lane		25.78125 ± 100 ppm			Gb/s	
Differential data input swing	$V_{IN,DIFF,PP}$			900	mV	
Differential input return loss		Per IEEE 802.3bm Annex 83E 3.3.1			dB	
Differential to common mode input return loss						
Differential termination mismatch				10	%	1
Module stressed input test Eye width 0.46 UI Eye height 95 mV		Per IEEE 802.3bm Annex 83E 3.4.1				
Single-ended voltage tolerance range	$V_{IN,PP}$	-0.4		3.3	V	2
Receiver Outputs						
Signaling rate, each lane		25.78125 ± 100 ppm			Gb/s	
AC common-mode output voltage, RMS				17.5	mV	
Differential data output swing	$V_{OUT,DIFF,PP}$			900	mV	
Eye width		0.57			UI	
Eye height, differential		228			mV	
Vertical eye closure	VEC			5.5	dB	
Differential Output Return Loss		Per IEEE 802.3bm Annex 83E 3.1.3			dB	
Common to differential mode conversion return loss						
Differential termination mismatch				10	%	1
Transition time (20% to 80%)		12			ps	3
Single-ended voltage tolerance range	$V_{IN,PP}$	-0.4		3.3	V	2

Notes:

1. Termination mismatch is the difference between the p- and n-side low-frequency impedances as a percentage of the average of p- and n-side low-frequency impedances (see IEEE 802.3-2012 86A.5.3.2).
2. Transmitter inputs and receiver outputs are AC coupled on the Paddle Card. Additional constraints on host common mode voltage range are not necessary.
3. This is a minimum transition time specification. The maximum rise/fall time is implicitly controlled by the eye width and vertical eye closure specifications.

Based on IEEE 802.3bm Clause 95 (100GBASE-SR4)

Parameter	Symbol	Min	Typ	Max	Units	Note
Transmitter Outputs						
Signaling rate, each lane		25.78125 ± 100 ppm			Gb/s	
Center wavelength	λ	840	850	860	nm	
RMS spectral width	SW			0.6	nm	
Average launch power, each lane	TXP	-8.4		2.4	dBm	4
Transmit OMA, each lane	TXOMA	-6.4		3	dBm	5
Transmit OMA minus TDEC		-7.3			dBm	
Transmit & dispersion eye closure, each Lane	TDEC			4.3	dBm	
Extinction ratio	ER	2			dB	
Optical return loss tolerance	ORLT	-12			dB	
Average launch power of OFF transmitter, each lane				-30	dBm	
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}		0.3, 0.38, 0.45, 0.35, 0.41, 0.5				6
Receiver Inputs						
Signaling rate, each lane		25.78125 ± 100 ppm			Gb/s	
Center wavelength	λ	840	850	860	nm	
Damage threshold	RXDT	3.4			dBm	7
Average receive power, each lane	RXP	-10.3		2.4	dBm	8
Receiver OMA, each lane	RXOMA			3	dBm	
Optical return loss	ORL			-12	dB	
Stressed sensitivity (OMA) , each lane	SRS			-5.2	dBm	9
Stressed eye closure (SEC)	SEC		4.3		dB	10
Stressed eye J2 jitter	J2		0.39		UI	10
Stressed eye J9 jitter	J4		0.53		UI	10
OMA of each aggressor lane			3		dBm	10
Stressed receiver eye mask definition {X1, X2, X3, Y1, Y2, Y3}		0.28, 0.5, 0.5, 0.33, 0.33, 0.4				10,11

Notes:

4. Minimum value is informative.
5. Even if the TDEC <0.9 dB, the OMA must exceed the min value.
6. Hit ratio = 1.5×10^{-5} hits per sample
7. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.
8. Minimum value is informative and not the principal indicator of signal strength.
9. Measured with conformance test signal coupled to a test cable attached to the CSP for a BER of 5×10^{-5}.
10. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.
11. Hit ratio = 5×10^{-5} hits per sample

Figure 21: Test specifications.

The test system (see Figure 23) consisted of the following equipment:

- Introspect BERT
  - "SV2C" is 28G version of existing "SV1C" 12.5G BERT
  - Complete measurement capability (i.e. jitter and eye measurement)
- Optical-to-Electrical conversion
  - A custom 4-channel 28G OE instrument using components from Picometrix ("PT-28B")
  - Keysight Oscilloscope 86100C
- FTS temperature forcing machine (for over temperature measurements)

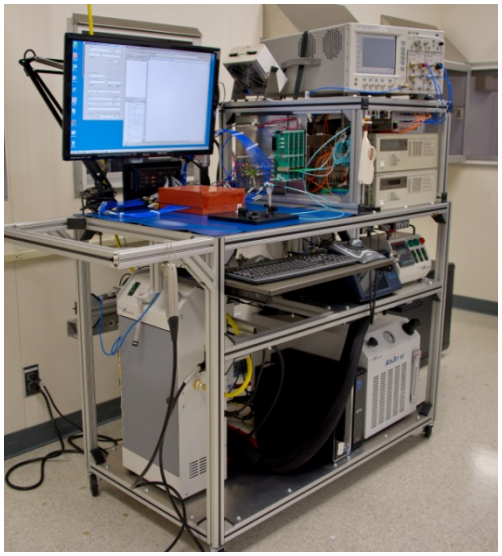


Figure 22: 28G Test system.

The test system schematic is shown below.

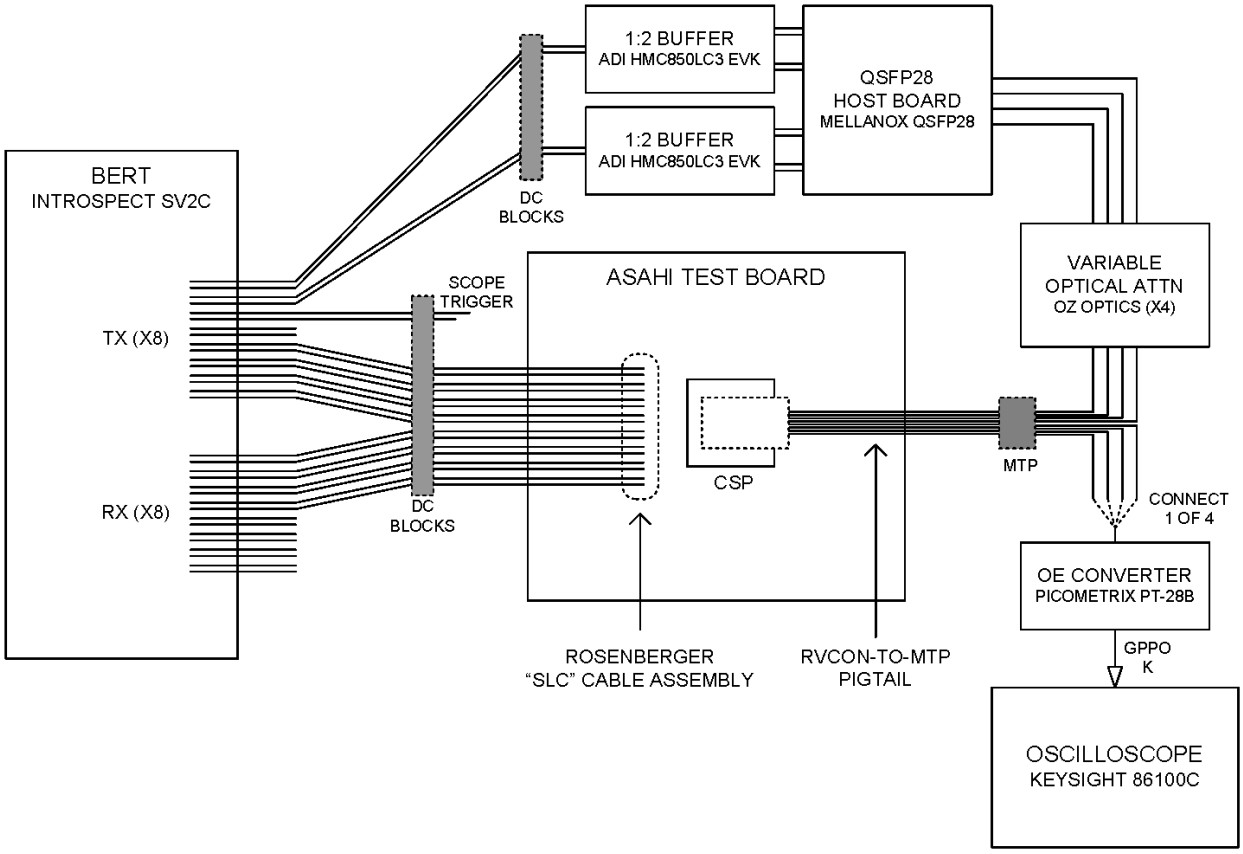


Figure 23: Test system schematic.

The test plan

- TX
  - Note: Only one OE converter available, so testing is manual, one channel at a time
  - Set VCSEL biasing based on vendor recommendations and optimize for room temperature operation
  - Measure PAV, OMA, ER, and eye mask compliance
  - Repeat at cold and hot with same bias settings
- RX
  - Use QSFP28 as source, min ATTN setting
  - Measure bathtub (jitter) and eye
  - Measure sensitivity (not intentionally stressed)
  - Repeat cold and hot
- Test temperatures
- Cold: -20 C
- Room: 30°C
- Hot: 85 C

The component showed -12 dBm sensitivity: BER 1E-12, at, 25.78 Gbps, ER=4 dB. The power consumptions was 177 mW/Ch or 130 mW/Ch with the CDR bypassed on the receiver side. On the transmitter, the power was 170 mW/Ch or 125 mW/Ch with the CDR bypassed. Figure 25 to Figure 31 show the eye diagrams of the transmitters and receivers operating at 25 Gbps.

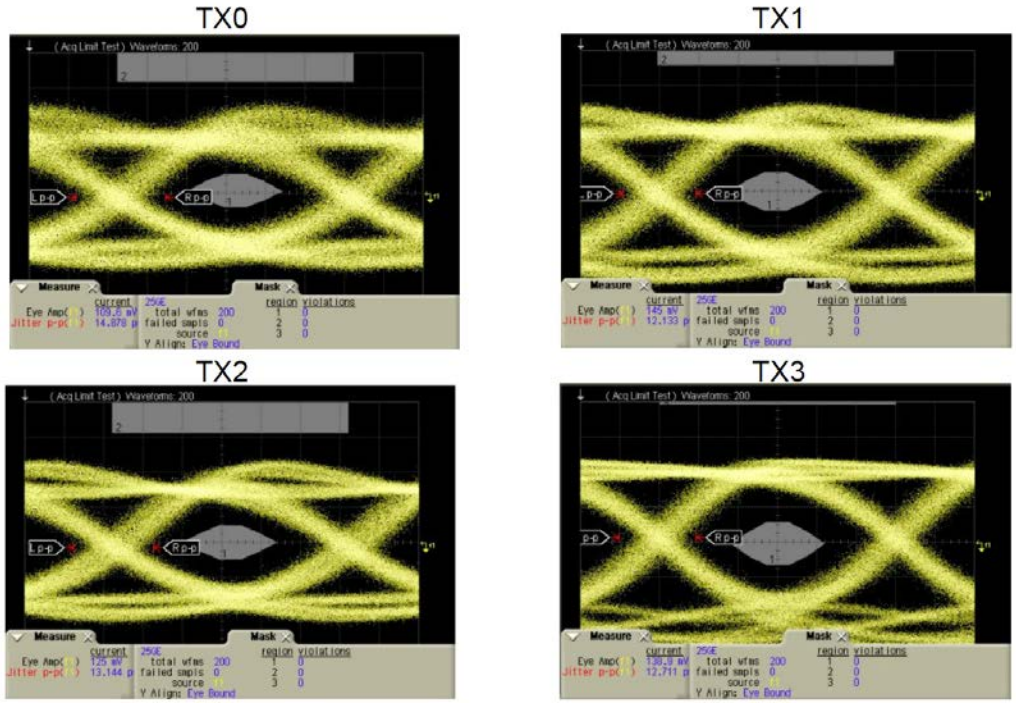


Figure 24:TX at 30 C

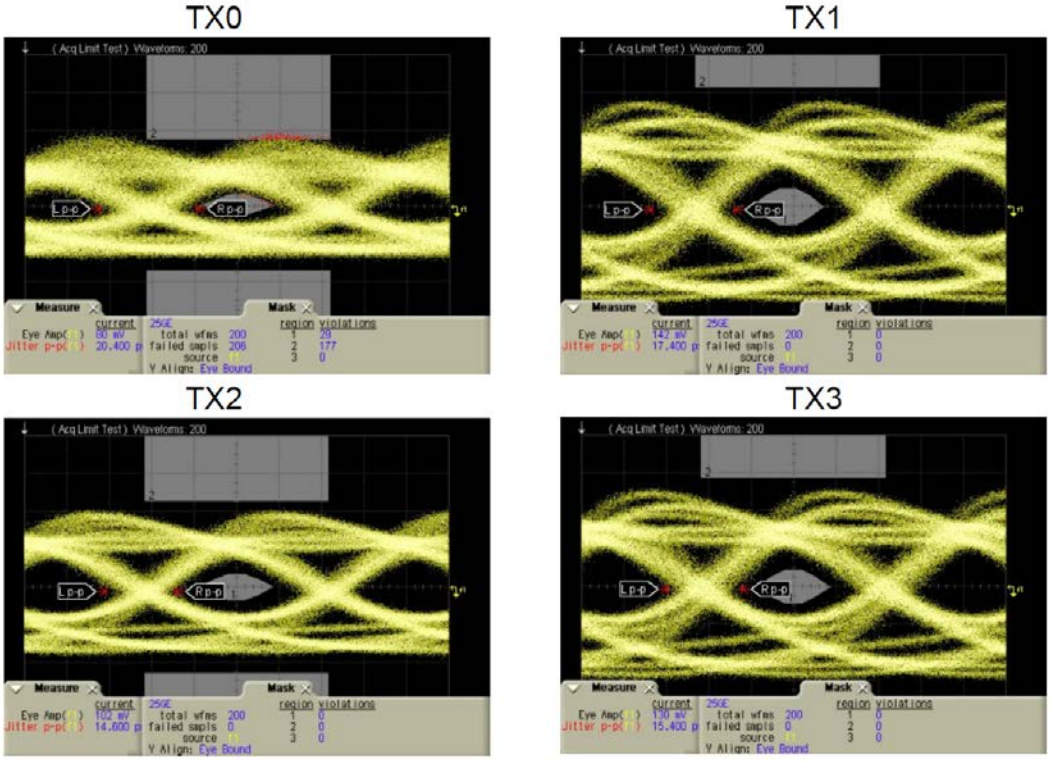


Figure 25:TX at 85 C

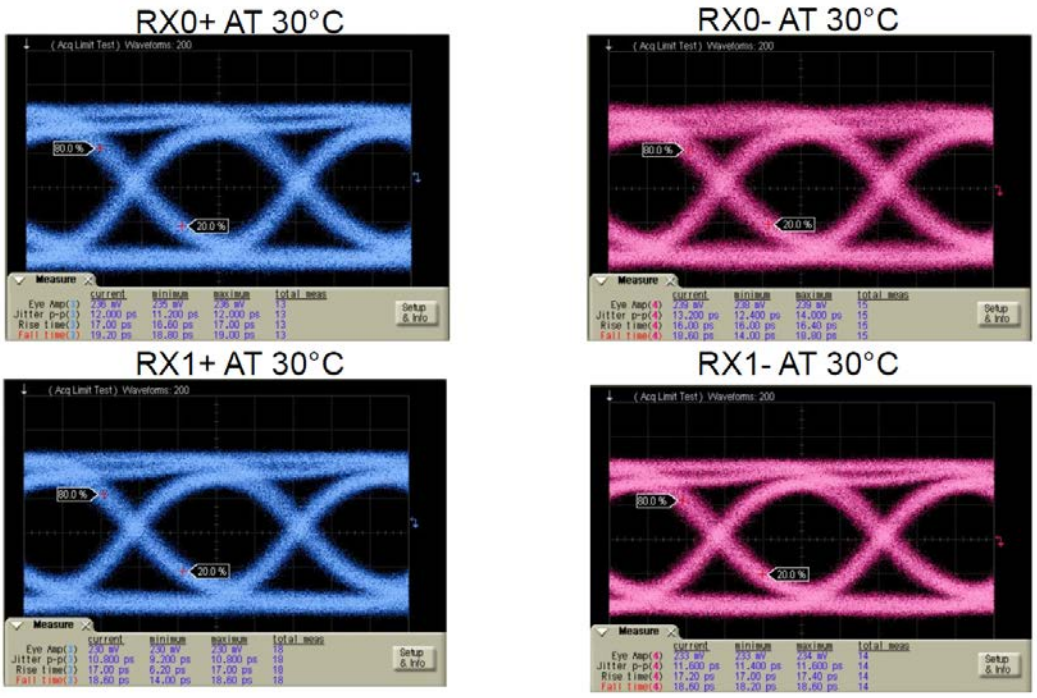


Figure 26:RX at 30 C

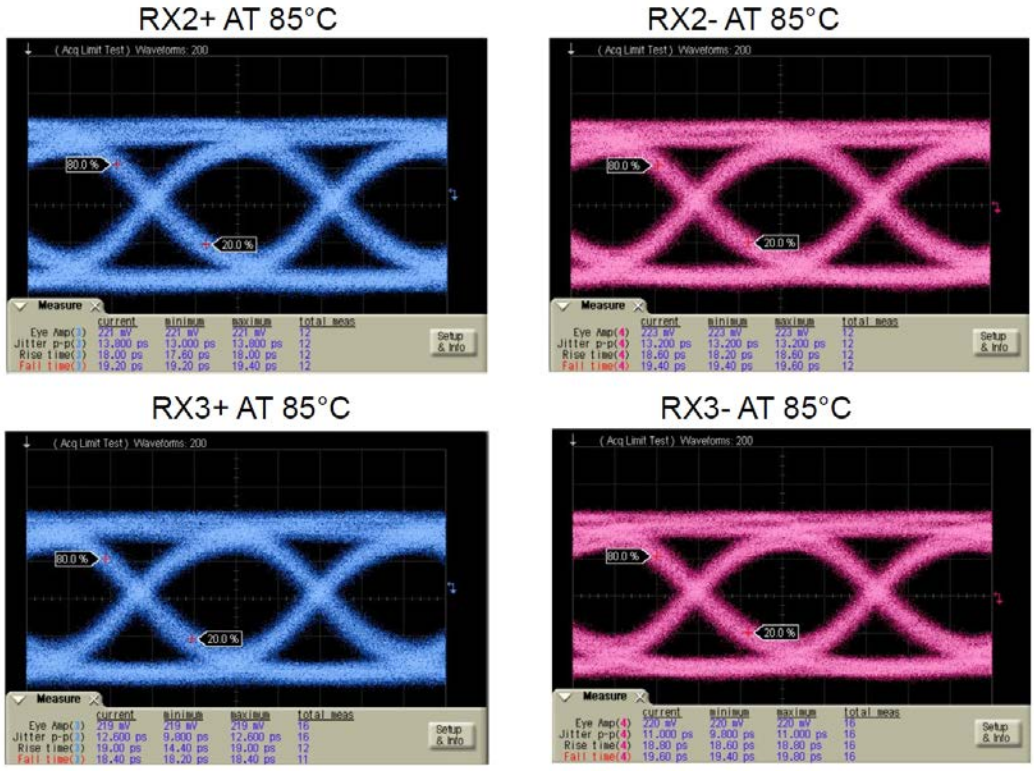
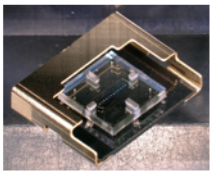
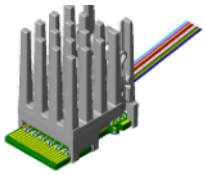


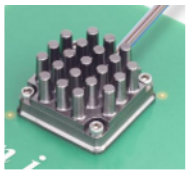
Figure 27:RX at 85 C

2.4. Impact on Industry

This DOE Phase II effort created the most compact and lowest cost solution to high speed fiber optic communication. This is the only solderable component (sealed to survive the solder wash). The soldering capability reduces the implementation by eliminating socket interface.







	DOE Phase II	TE Connectivity	FCI Electronics	Samtec	Finisar
PCB area (relative size, mm)	12 x 12	25 x 25	25 x 25	11 x 19	25 x 25
Volume (relative size, mm^3)	576	7,500	7,500	3,553	7,500
Solderable	✓	✗	✗	✗	✗
Sealed	✓	✗	✗	✗	✗
BOM count	10	> 25	> 25	> 20	> 20
Channels	12	24	24	12	12
Power	2.1 W*	4.5 W	3.0 W	TBD**	TBD**

* assumes 30% power consumption savings due to SOI integration
** Data published for 14G links only, not 28G

Figure 28: Technology comparison.

The DOE Phase II CSP transceiver reduces the cost by reducing the number of sub-components, see Figure 31.

BOM	CSP Transceiver	Competitor
VCSEL	$ 8.51	$ 8.51
PIN	$ 4.10	$ 4.10
ASIC (SOS) with Metalization	$ 13.52	$ 8.00
Lens Guide // Coupling Lenses	$ 3.28	$ 3.00
Subassembly substrate	-	$ 3.00
Rigid-Flex-Rigid Circuit	-	$ 8.00
Passives	-	$ 2.00
Electrical Socket (top)	-	$ 8.00
Electrical Socket (bottom)	-	$ 8.00
Mechanics for Electrical Socket		
Alignment Pins	-	$ 1.00
Screws	-	$ 1.00
Brackets	-	$ 2.00
Total BOM	$ 29.41	$ 56.61
Assembly / Test	$ 21.10	$ 63.30
Grand Total Cost	$ 50.51	$ 119.91

Figure 29: CSP cost breakdown.

2.5. The Market

Embedded optical transceivers are designed to be mounted adjacent to a host ASIC. High-speed signals are converted to optical signals and injected into optic fibers that “fly over” the PCB directly to the I/O panel. Reducing the length of copper traces on the board improves signal integrity, and potentially makes the board less expensive to manufacture. Optic links are terminated in a MPO or MPX high-density connector mounted on the faceplate, greatly increasing I/O signal density.

Embedded optical transceivers will not be replacing pluggable transceivers overnight, embedded transceivers enable system architectures to solve problems that cannot be addressed with pluggable I/O such as extreme port count in limited spaces. The following chart compares on-board transceivers with current pluggable alternatives.

Connection Type	Cost	Increases Reach	Improves Cabling Airflow	Simplifes Cable Management	Structured Cabling/Easy Install	Improves I/O Density	Improves Signal Routing	Solves Space Contraints	Thermal Optimization
Copper DAC	$								
AOC	$$	X	X	X					
Pluggable Trx	$$$	X	X	X	X				
OBT	$$$$	X	X	X	X	X	X	X	X

Amphenol FCI

Select applications in high-performance computing, storage, and networking may be candidates for replacement of pluggable I/O with embedded transceiver technology. As 50 Gb PAM4 signaling evolves to 50+ Gb NRZ, pluggables may not be able to provide the speed and density required, making embedded transceivers the best-performing and most cost-effective solution.

This is a challenging period for connector manufacturers to participate in the mid-board optical transceiver arena. Avago was the first to pioneer embedded optical modules, with the Snap12 product, and has since evolved to higher performance optical interconnects. “Flyover” optical cables were introduced by Avago for their MicroPOD optical modules. Finisar also introduced a board-mount optical assembly (BOA). The concept caught on with new market entrants, such as Samtec, with their Firefly Micro Flyover mid-board transmitter and receiver modules. A few years later TE Connectivity, Amphenol FCI, and Molex moved into the market with their own transceiver modules. Lack of an industry standard resulted in proprietary designs.

The last year has brought extensive change to this market segment. Avago sold their optical module product lines to Foxconn Interconnect Technology (FIT), which is continuing to support Mini and MicroPOD optical modules. Molex has temporarily withdrawn their QuatroScale Mid-Board transceiver until industry standards are defined for on-board optics. TE Connectivity discontinued its Coolbit Optical engine, along with much of its fiber optic connector lines, to focus on its rugged expanded beam optical interfaces. The Amphenol FCI Leap transceiver (12 channel x 25 Gb/s) and the Samtec Optical Flyover (12 channel x 14 Gb/s) are currently leading the industry in actively pursuing embedded optical module applications.

Until system designers reach the point where pluggable I/O simply cannot deliver the density and bandwidth required by new applications, embedded optics will remain a niche solution. When that day comes, the existence of an industry standard that can define electrical, mechanical, footprint, and thermal parameters would allow optical and footprint compatibility among competing suppliers. The creation of a standard will allow customers to choose between multiple compatible sources and

ultimately drive costs down. That challenge is being taken up by the recently formed Consortium for On-Board Optics (COBO) which is targeting early 2017 for completion of a MSA standard. Amphenol FCI, HUBER+SUHNER, Molex, Rosenberger, Samtec, Sumitomo, TE Connectivity, US Conec, and Yamaichi are associate members in this consortium.

Another issue yet to be resolved by the industry is the optimal number of duplex channels with which embedded transceivers should be configured. Transceivers currently on the market range from one to 12 duplex channels.

Industry forecasters have pegged aggregate I/O bandwidth demand to double every three years, with 50 Gb/s PAM4 channels being common by 2018. Cloud traffic will continue to increase as streaming video becomes pervasive and more devices are linked to the Internet of Things. Data centers will be driving the adoption of embedded I/O transceivers and have identified the ultimate target of tapping a 1U chassis with up to 12.6 Tb of I/O capacity. The current perceived limit of about 400 Gb for pluggable interfaces will likely be pushed to 800 Gb/s, enabling their continued use, but the density and thermal management advantages of embedded optical transceivers make them an important enabler in the roadmap to high-speed I/O.

3. Identification of Products

Publications: The following publications were a result of this Phase II effort:

1. J. Ahadian et al., “Chip-Scale Packaging for High-Temperature Embedded Optical Module Applications,” *GoMacTech* Session 10:Photonic Interconnects and Microphotonics (Paper No. 10.3), March 13 2013
2. J. Ahadian *et al*., "Chip-scale-packaging applied to optical transceivers," *2014 Optical Interconnects Conference*, San Diego, CA, 2014, pp. 89-90.
3. J. Ahadian *et al*., "Packaging technology for embedded optical modules," *2013 Optical Interconnects Conference*, Santa Fe, NM, 2013, pp. 15-16.

Collaborations Fostered: Key collaborations with *ASIC suppliers:* Macom, IPtronics (Menlo Park, CA) and Mind Speed (Newport Beach, CA) as enabling the performance of their ASIC devices; *VCSEL/PIN suppliers*: Murata, Sumitomo and Philips; Potential customer relationships were formed with Murata, and Mellanox (Sunnyvale, CA).

4. References

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10. Chun Lei, et. al. , “Emcore VCSEL Failure Mechanism and Resolution,” Proc. of SPIE Vol. 7615, 761504, 2010