

Fast Fiber-Coupled Imaging Devices

SBIR Phase 1 & 2

Final Report for the Period February 2013 - April 2017

April 2018

**PREPARED FOR THE UNITED STATES
DEPARTMENT OF ENERGY
OFFICE OF FUSION ENERGY SCIENCES**

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1 Abstract

HyperV Technologies Corp. has successfully designed, built and experimentally demonstrated a full scale 1024 pixel 100 MegaFrames/s fiber coupled camera with 12 or 14 bits, and record lengths of 32K frames, exceeding our original performance objectives. This high-pixel-count, fiber optically-coupled, imaging diagnostic can be used for investigating fast, bright plasma events. In Phase 1 of this effort, a 100 pixel fiber-coupled fast streak camera for imaging plasma jet profiles was constructed and successfully demonstrated. The resulting response from outside plasma physics researchers emphasized development of increased pixel performance as a higher priority over increasing pixel count. In this Phase 2 effort, HyperV therefore focused on increasing the sample rate and bit-depth of the photodiode pixel designed in Phase 1, while still maintaining a long record length and holding the cost per channel **to levels which allowed up to 1024 pixels to be constructed**. Cost per channel was \$53.31, very close to our original target of \$50 per channel. The system consists of an imaging “camera head” coupled to a photodiode bank with an array of optical fibers. The output of these fast photodiodes is then digitized at 100 Megaframes per second and stored in record lengths of 32,768 samples with bit depths of 12 to 14 bits per pixel. Longer record lengths are possible with additional memory. A prototype imaging system with up to 1024 pixels was designed and constructed and used to successfully take movies of very fast moving plasma jets as a demonstration of the camera performance capabilities. Some faulty electrical components on one of the 64 circuit boards resulted in only 1008 functional channels out of 1024 on this first generation prototype system. We experimentally observed backlit high speed fan blades in initial camera testing and then followed that with full movies and streak images of free flowing high speed plasma jets (at 30-50 km/s). Jet structure and jet collisions onto metal pillars in the path of the plasma jets were recorded in a single shot. This new fast imaging system is an attractive alternative to conventional fast framing cameras for applications and experiments where imaging events using existing techniques are inefficient or impossible. The development of HyperV’s new diagnostic was split into two tracks: a next generation camera track, in which HyperV built, tested, and demonstrated a prototype 1024 (1008 working) channel camera at its own facility, and a second plasma community beta test track, where selected plasma physics programs received small systems of a few test pixels to evaluate the expected performance of a full scale camera on their experiments. These evaluations were performed as part of an unfunded collaboration with researchers at Los Alamos National Laboratory and the University of California at Davis. Results from the prototype 1024-pixel camera are discussed, as well as results from the collaborations with test pixel system deployment sites.

2 Background - The Plasma Imaging Race

Whenever high velocity plasma is collided with a magnetized plasma (e.g. during tokamak disruption mitigation, refueling, ELM pacing, or in astrophysical jet dynamics), the time-scales for plasma jet interaction events can be as fast as 1-20 MHz. Imaging of these plasma events can provide critical insight into the dynamics at work. Plasma research programs are thus continually in search of imaging solutions with increased pixel count, sample rate, and record length. Imaging fast plasma events to understand turbulent mixing and ELM mode growth in tokamaks alone is absolutely vital to achieving the goals of Magnetic Confinement Fusion (MCF). For events which are not necessarily repeatable from shot to shot, or dynamic events in devices which are too large to accumulate event evolution over many shots, the development of a deep record length plasma imaging system would be a significant advantage over present single shot and burst shot imaging systems. However, when designing an imaging diagnostic, there exists a tradeoff between pixel count, frame rate, and number of frames. Intensified charge couple devices (ICCD) can have very high pixel counts, but also have data bottlenecks in acquiring information from the CCD array, since each pixel must be clocked out of the CCD chip individually to keep the chip pin count low[1]. Techniques for increased frame rates exist, but these often involve adding additional CCD devices to capture additional frames [2], or shifting images across the CCD, thereby sacrificing pixel count [3]. While insight can be aggregated over many shots by stepping the camera trigger through many delay settings, this presumes that each shot yields reproducible events, making stochastic events like plasma turbulence, or mixing, difficult to resolve. Additionally, the large number of shots required to scan a long time sequence with fine steps is not always feasible in larger experiments.

A solution to these problems is a plasma imaging device created by optically coupling an imaging head to a bank of amplified photodiodes. A fiber imaging grid allows for dense spatial resolution, while the fibers themselves allow signals to be distributed over a larger physical volume for dense time resolution. To achieve this new imaging diagnostic with both spatial and temporal resolution, a holistic design approach must be followed to optimize the cost and performance of the entire signal pathway, from the input of the fiber all the way through to the final storage of the images in memory. Thus, the cost of array deployment can be greatly reduced to maximize the number of pixels in the final imaging system. HyperV had demonstrated some of the power of this approach by constructing a 100 pixel streak camera in Phase 1. We have reapplied this same holistic signal pathway design approach in this Phase 2 effort to develop the 1024-pixel fast-framing camera with improved performance and new cost metric. The result is our two track camera development program, which sought to not only increase camera performance, but also to ensure that performance gains increased the utility of the diagnostic to the plasma physics community.

3 Phase 2 Goals and Tasks

This Phase 2 program built on the successes of the 100-pixel camera developed in Phase 1. Because of the positive response to our work by several plasma physics research groups, HyperV placed development of increased pixel performance over development of larger pixel

arrays. During Phase 2, we sought to scale the Phase 1 streak camera design up to a 1024 pixel framing camera capable of recording bursts of high speed plasma video at frames rates of 100 Megaframes per second. This program had the following two objectives.

Objective 1 Scale the existing 100 pixel streak camera design up to a 1024 pixel framing camera. We will first construct several test modules containing a few pixels (probably about 12-15 channel per module). Resolutions of 8, 10, and 12 bits per pixel will be evaluated for design impact, since different users will typically have different resolution requirements. The target recording rate will be 100 Megaframes per second with a record length of at least 2048 points. HyperV would then build and calibrate a fully functional prototype 1024 pixel framing camera evolved from these test designs. This full scale camera would then be tested by observing dynamic fast plasma jets produced by our already operational plasma accelerators.

Objective 2 We will provide several small photodiode test modules to potential end user sites for the purpose of identifying and addressing issues which arise from deploying and interfacing a camera diagnostic at locations other than HyperV’s laboratory. Camera systems have to fit into available experiment view access spaces, survive in laboratory EM noise environments, and communicate with an experiment’s timing and data acquisition systems. Since the performance of the entire array can be determined from the performance of a few test pixels, deploying small test units at potential end user research labs in advance of an entire camera assembly will help gauge the performance of the camera in that application. This will also identify places where additional design improvements may be necessary earlier in the camera development cycle, so that the camera can be constructed to target the needs of the plasma community.

These objectives were all accomplished by completing the following technical tasks, which will be described in more detail in the remainder of this report.

Evaluated Full-Scale Camera Designs The best way to reach our desired pixel count was to holistically design the entire signal path, from the input fiber to the storage of data in memory, to meet our end specification and our cost goals.

Constructed Small-Scale Samples of the Full-Scale Design After a design was selected, it was then constructed and bench tested at HyperV in small scale.

Tested Small-Scale Devices at HyperV After assembly and bench testing, the small scale system was tested on one of HyperV’s already operational Plasma Accelerators.

Constructed and Tested Small-Scale Devices Off-site The resulting small scale camera design was then duplicated and deployed to a selection of potential end users who volunteered to be unfunded collaborators in the project.

Constructed the Full-Scale Camera Only at this final stage was the construction of the full array necessary, as small scale testings were used to fully vet the capabilities of the full pixel array.

Tested Full-Scale device at HyperV After construction and bench testing of the full scale camera was complete, the fully functional full-scale camera was deployed to image one of HyperV’s plasma railgun accelerators. Since the focus of the Phase 2 was to maximize the capabilities of the full scale camera, conducting full scale tests at HyperV simplified the logistics of the deployment and reduced costs. The full scale camera was used to record operation of a HyperV plasma accelerator, and the results were compared to existing and concurrently recorded data. This allowed more project resources to be put toward improving the overall camera performance.

4 Results of Phase 2 Project

HyperV’s Phase 2 camera program consisted of two development tracks. The first track focused on the in-house development of the next generation camera system. Here, HyperV developed, tested, and deployed a 1008-pixel fiber-coupled imager with 100 MFrames/s acquisition rate and a pixel resolution of 12/14 bits. This included the development and construction of the set of front end optics, a 1024-pixel fiber imager bundle, as well as 1008 channels of fast fiber data acquisition (one of the 64 boards had a component failure), and its associated control circuitry. **Record lengths of 32,768 frames were achieved, far above the original target of 2048 frames.** This full-scale Fast Fiber-coupled Framing Camera (FFFC) was then deployed at HyperV to observe plasma jets created by railgun plasma accelerators both with and without obstructions, as well as brightly illuminated high speed fans as test subjects.

The second development track focused on involving the plasma physics community in the specification, design, and evaluation process of the Phase 2 camera to ensure that it will meet the needs of the community. As part of this track, we arranged to provide several small photodiode test modules to potential end user sites. Since the performance of the entire array can be determined from the performance of a few test pixels, deploying small test units at potential end user research labs in advance of an entire camera assembly can help gauge the performance of the camera in that application. Test boards with 16 channels were successfully sent to the Plasma Liner Experiment (PLX) [4, 5] Alpha group at Los Alamos National Laboratory (LANL) in New Mexico and the Compact Toroid Injection Experiment (CTIX) [6] at the University of California Davis (UC-Davis) in Livermore, California. Results of these deployments are discussed later. The specific accomplishments of this Phase 2 program are highlighted in Table 1

5 1024-pixel Camera Design

The Fast Fiber-coupled Framing Camera (FFFC) was **designed to trade some spatial resolution for high time resolution.** Visible light emitted by a plasma is collected with an optic and imaged onto a grid of fiberoptics for dense spatial resolution. As illustrated in Figure 1, the fiber optics then distribute signals over a modular array of boards of photodiode detectors with integrated digitization and memory for high time resolutions and long record-lengths. An embedded system is used to control each daughter board of N channels, where

Table 1 *Highlighted Accomplishments of Phase 2 Effort*

- Evaluated and selected a Design for a 1024 pixel full scale camera
- Evaluated the use of FPGA’s to improve board design
- Developed and tested 12-bit and 14-bit 16-pixel boards along with digital backends
- Designed and constructed Python driver software for an N-pixel camera
- **Exceeded projected expectations** with a 1008-pixel camera with:
 100 Megaframes/s, 12/14 bit resolution, and 32K points record length
- Cost per channel was \$53.31, very close to our target of \$50 per channel
- Channel readout time was reduced to ~ 13 mins
- Experimentally observed backlit high speed fan blades
- Experimentally observed high speed free moving plasma jets from a railgun plasma accelerator
- Experimentally observed collisions of high speed plasma jets with metal pillars
- Plasma observations required neutral density filters because of high camera gain
- Deployed modules of 16 test pixels to LANL and UC-Davis

N is typically 16 for these experiments. All daughter boards are then linked to a master computer through commercial USB connections. Since the FFFC is an array of identical pixels, this has the advantage of creating a modular system of scalable size. Thus, new pixel designs can be tested and demonstrated at small scales before committing to larger deployments. Key camera design features are shown in Table 2.

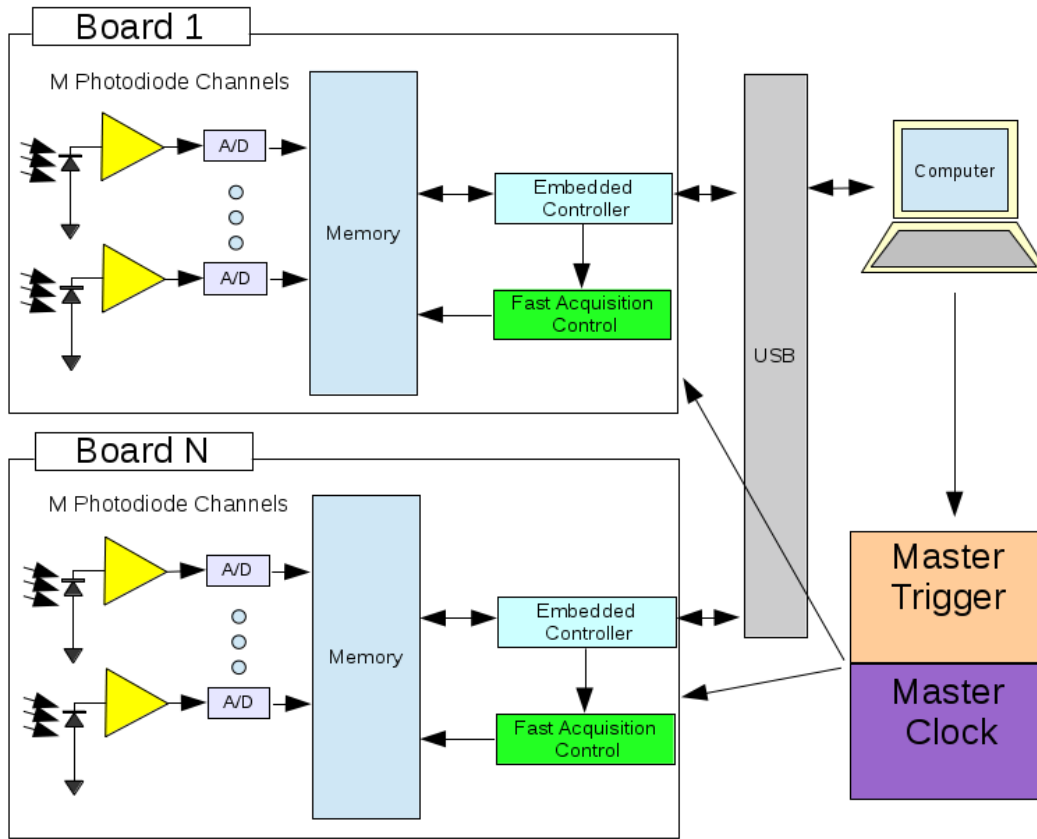


Figure 1 An embedded system can be used to control a daughter board of 16 channels. All daughter boards are linked to a master computer through commercial USB connections. This has the advantage of creating a modular system of scalable size, and new pixel designs can be tested and demonstrated at small scales before committing to larger deployments. A master trigger distribution network triggers the data acquisition.

Table 2 Key Camera Design Features

- Scalable Design - arrays of 16 to 4096 pixels could be constructed.
- Testable at small scale - Pixels are identical, so new designs can be tested cheaply.
- Configurable - Design uses a family of A/D converters and a family of memory chips so that performance can drive part cost.
- Fiber grids provide standoff - The fibers move the hardware away from dangerous or otherwise electrically noisy environments
- Fiber grids can be replaced - if degraded or destroyed by the experiment, the fiber grid can be replaced
- Fiber grids are modular- 1024 pixels could be fielded as 1024 pixel rectangular, square, or even two 512 pixel imaging grids, depending on experimental needs
- High time resolution over long record lengths - 100 MHz digitization for $327 \mu\text{s}$ allows evolution of fast events to be recorded in a single shot.

Emphasis was placed on designs that would allow boards for 1024 photodiode channels to fit into a single electronics rack, which kept the system electrically shielded and portable. At 16 channels per daughter card, 64 daughter cards allow 1024 channels. These boards were loaded into three custom crates. A single crate unit can hold 16-22 boards with good spacing for air and heat flow as well as cable access. Boards were mounted on guide channels to allow them to be disconnected and removed individually for inspection. Two cameras, shown in Figure 2, were designed and constructed. Camera 1 which used three racks of 21 boards provided 1008 pixels while Camera 2 employed four racks of 16 boards for 1024 pixels.



Figure 2 (Left) Emphasis was placed on designs that would allow boards for 1024 photodiode channels to fit into a single standard electronics rack, which assisted in keeping the system electrically shielded and portable. At 16 channels per daughter card, 64 daughter cards would allow 1024 channels. Two cameras were designed and constructed. Camera 1 (Center) used three racks of 21 boards to have 1008 pixels and Camera 2 (Right) employed four racks of 16 boards for 1024 pixels. (The two racks are actually the same height.)

The system architecture was selected based on the amount of control circuit duplication each board required and the path length high frequency signals would have to traverse. To function properly, channels needed to receive fast control signals for the start and stop of acquisition, as well as a clean sequential indexing of memory addresses to store data points as they are received. We used a low cost embedded system per board to control a group of 16 channels. All of these daughter boards were then linked to a master computer through commercial USB connections. This had the advantage of creating a modular system of scalable size, plus using USB allowed data from multiple boards to be retrieved in parallel reducing instrument readout times.



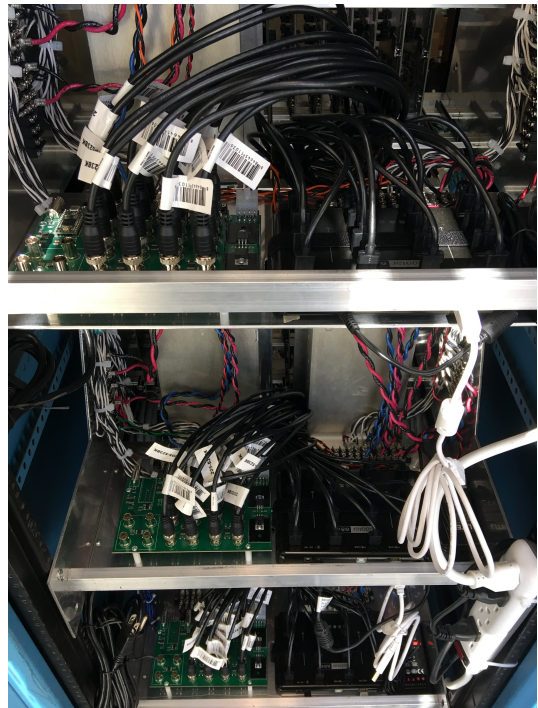
(a) Camera1 1024 fiber connections to electronics boards.



(b) Camera2 circuit boards prior to fiber connections.



(c) Rear view of Camera2 electronics boards.



(d) Closeup of trigger daughter cards.

Figure 3 *Various views of the circuit boards and fiber connections in the electronics racks.*

A 1U Dell Power Edge 860 was selected for the master control computer. It was necessary to recompile the Linux kernel drivers to support 128 ttyACM devices, since the default settings are either 16 or 32 maximum devices, depending on the specific computer OS. This computer was the main controller for the 1008 pixel Camera 1. It was fiber-optically linked to HyperV’s standard data acquisition computer for remote control of the camera diagnostic via VNC. Power for the racks was provided by installing a wiring harness that distributed power from a set of supplies. A backbone of 16 port USB hubs was created to link up all 63 boards, as well as a trigger distribution network.

A Teensy USB embedded system was selected for board control. While the Teensy USB is a Freescale K20 development board with intellectual property constraints, it is provided with libraries that allowed immediate communication with a full computer and facilitated camera driver software construction. This allowed prototype hardware to be diagnosed sooner, while also still allowing our own embedded solution to be added later. Jumping to our own embedded K20 solution was investigated, but the difficulty lies in establishing a boot loader program to “bless” new hardware to the point where it can receive programming and communication from the host computer. Composing this boot-loader appeared to be a significant undertaking, and thus was deferred to more advanced camera hardware in future development efforts.

5.1 Master Clock and Trigger Module

Special consideration was given to how clock and trigger signals would need to be synchronized over all the camera modules. At 16 pixels per board, at least 64 boards would be required to support 1024 pixels. At 100 MHz, control signals only have 10 ns (or ~ 6 feet in RG-58 cable) to propagate within a single shot. A master trigger breakout, shown in Figure 4 on the next page, was constructed to ensure that record lengths received simultaneous triggers from board-to-board. Four 16-channel trigger modules were constructed. A four-way BNC tee was used to trigger the 4 trigger modules, which in turn provided 64 board triggers for 1024 pixels. A master clock module was also added so that clock signals could be sourced to the rack from a single clock. While clock signals could have been synchronized board-to-board by using cables of the appropriate length to preserve clock phase, the external clock feature was not used in the final design because records should only differ from board-to-board by a phase variation of at most <10 ns. Such a small offset is negligible for typical HyperV experimental timescales.

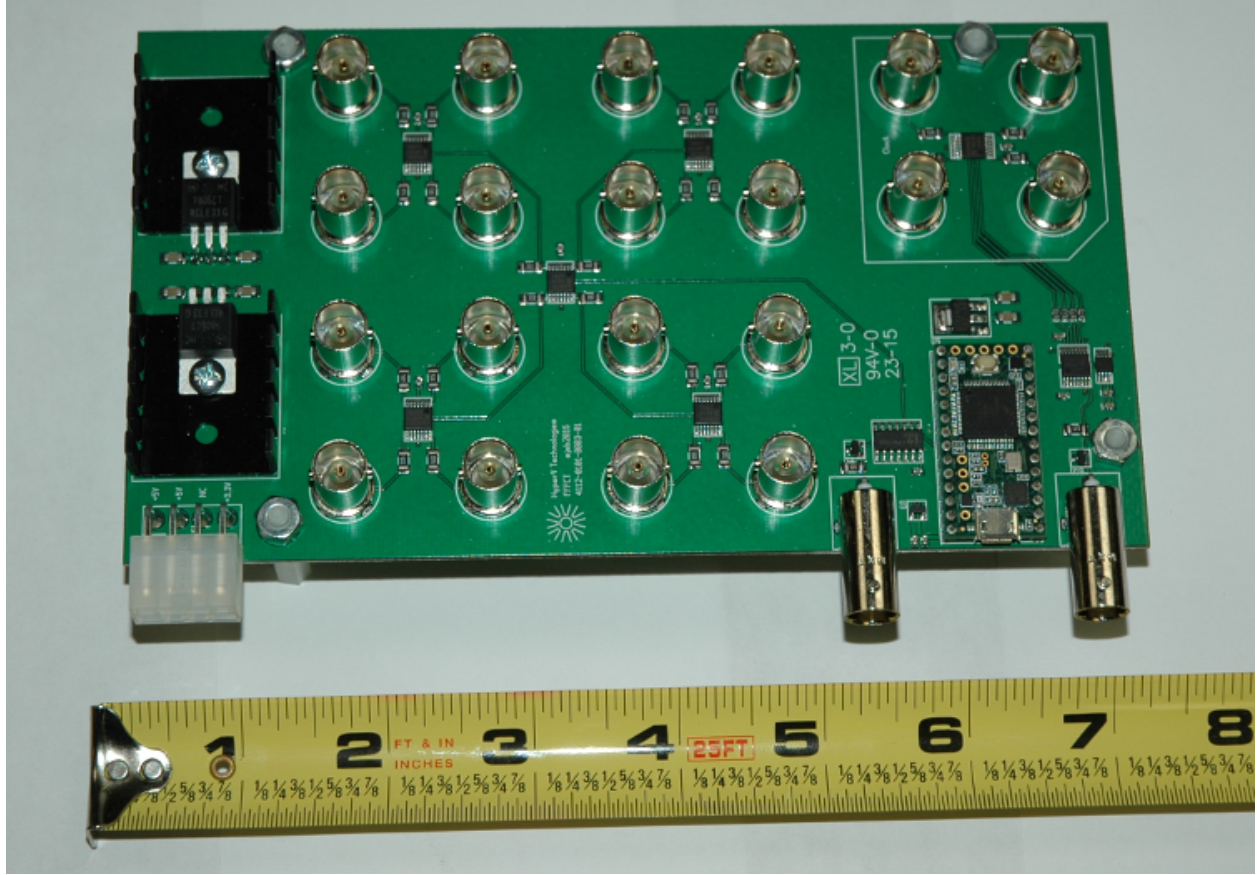


Figure 4 While clock signals can be synchronized board-to-board by using cables of the appropriate length to preserve clock phase, a master trigger breakout needed to be constructed to ensure that record lengths received simultaneous triggers from board-to-board. A master module is used to trigger four slave modules which internally provides 64 board triggers for 1024 pixels.

5.2 Final Pixel Design

HyperV’s iterative design process, highlighted in Table 3 on the next page yielded a board design with sixteen channels of photodiode acquisition laid out on six layers. The board, as currently implemented, is about 12in x 5.5in and serves as the base unit for both the camera array and the remote deployment sites. This was accomplished by arranging channel components so they could be placed on both the top and bottom of the board, halving the required area for channel layout. While support layout could be further reduced by using both faces, channel support is presently still about 20 in², still a significant improvement over the ~55 in² required for the Phase 1 streak camera, and was more than adequate for construction of the 1008 pixel prototype. General circuit topology was illustrated earlier in Figure 1.

Table 3 *Camera Design Iterations*

Board Version	Number Channels	Description
0101-1-5	3	3 single ADC’s into 1 memory
0101-2-1	4	Teensy integration test board
0101-3-1	4	12-bit dual ADC chip test
0101-5-1	16	16-channel 14-bit with channels on both sides
0101-5-2	16	15-bit address test
0101-2-2	16	VDC test board
0101-2-3	16	Camera 1 Final Board for ADC1412D
0105-1-1	16	Linear Technologies test board
0105-2-1	16	Camera 2 final board for LTC2284

At its core, the 1024-pixel fiber camera is a large array of a single photodiode pixel design. This topology is advantageous, since it allows performance and specification upgrades to be tested in small scale well in advance of construction of the entire camera. The principal forces driving cost per channel were the analog electronics, ADC converter, the PCB board, the photodiode, the fiber optic receiver, and memory. The Phase 2 camera also consists of an optical camera head fiber-optically coupled to a bank of amplified photodiodes. Furthermore, as the tasks for acquisition in Phase 2 are the same as in Phase 1, i.e. the ability to arm, acquire and clock out data, the diagram of the base channel was left unchanged. A sample rate of 100 MegaFrames/s was requested by end users, so this was our benchmark for selecting components. Photodiodes are amplified by a transimpedance gain stage followed by voltage gain stages, and are recorded by an A/D converter. For determining the photodiode, it is reasonable to assume that operation of the HyperV plasma railgun at the same settings will yield plasma emission signals of about the same intensity as those studied in Phase 1. By staying with the same 1024 μm unterminated jacketed fibers, we were able to continue using the same or similar IF-D91 fast photodiodes with a built in twist-lock fiber mounting, which reduced cost. Junction capacitance for this photodiode is 5 pF and the 10-90% rise time is 5 ns which is sufficient for a 10ns (100 MS/s) sample window. The photodiode was biased to maximize bandwidth. While higher resolution A/D solutions exist, we determined that 14-bit pixels are currently the most resolution which might still fit our cost metric at the 100 MHz sample rate. Since the 36-bit wide memory unit used in Phase 1 can accommodate up to 36 lines of data, is fast enough (100MHz), is deep enough (128 kframes), and is still cost competitive, it was selected to be used again. An alternative transimpedance op-amp with increased gain bandwidth product and improved noise characteristics was also successfully evaluated.

The final channel design arose from the best of three circuit topologies that were evaluated. A channel with 16 k Ω of transimpedance gain, 14 bits of acquisition, and memory for 128K frames worked best on optical test signals. Light wavelength response for the selected photodiode is shown in Figure 5 [7]. Junction capacitance is 5 pF and the 10-90% rise time is 5 ns which is sufficient for a 10 ns (100MS/s) sample window. Performance using 1MHz square wave test signals is shown in Figure 6 for the best transimpedance design. This circuit topology was then implemented using two different analog-to-digital conversion chips

(Figure 7). The ADC1412D [8] and the LTC2284 [9]. Both are 14-bit 105 MSample/s chips. Camera development was performed with the ADC1412D, but this chip was deprecated by the manufacturer mid-project. The LTC2284 was the closest existing drop-in replacement we could find at a reasonable price point. Bode plots for the two designs are shown in Figure 8. Analog bandpass was measured to be about 15 MHz, a very conservative choice to maximize gain.

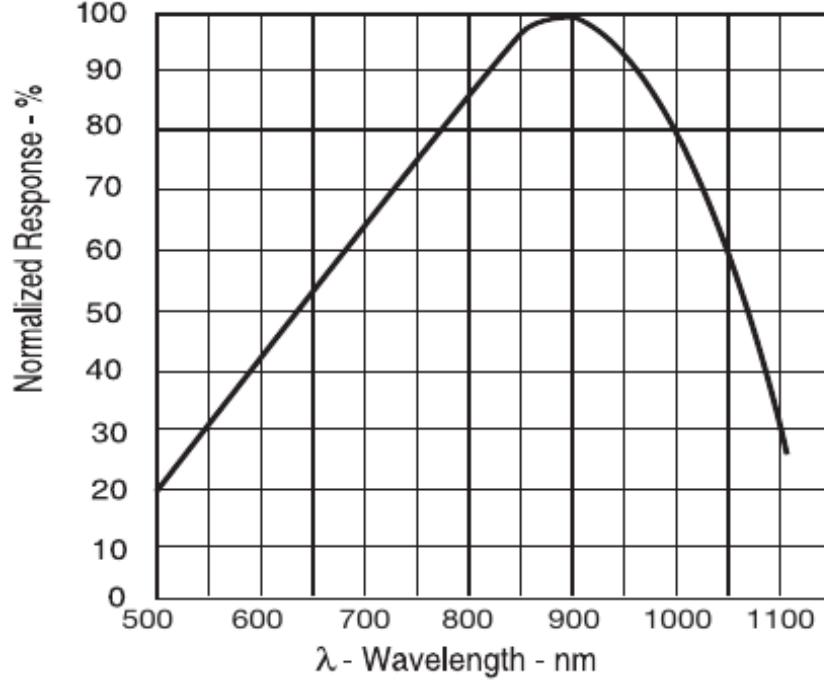


Figure 5 Light wavelength response for the selected photodiode is shown. Junction capacitance is 5 pF and the 10-90% rise time is 5 ns which is sufficient for a 10ns (100MS/s) sample window. [7]

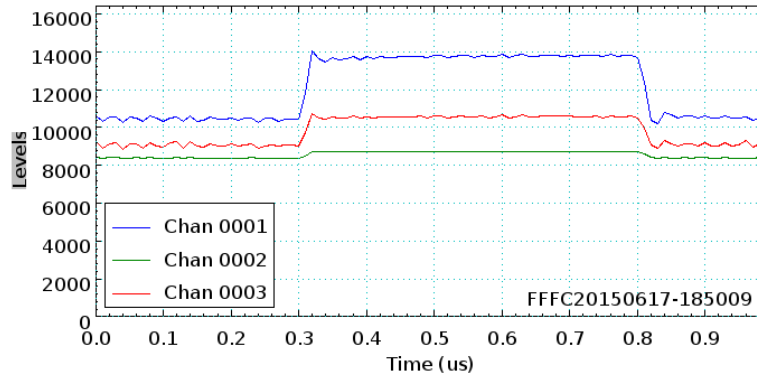


Figure 6 Three circuit topologies were evaluated in Revision 9. Performance using 1MHz square wave test signals is shown for the best design. This design was the basis for the basic 1024 pixel camera unit. This data was acquired with our digital back end camera control software.

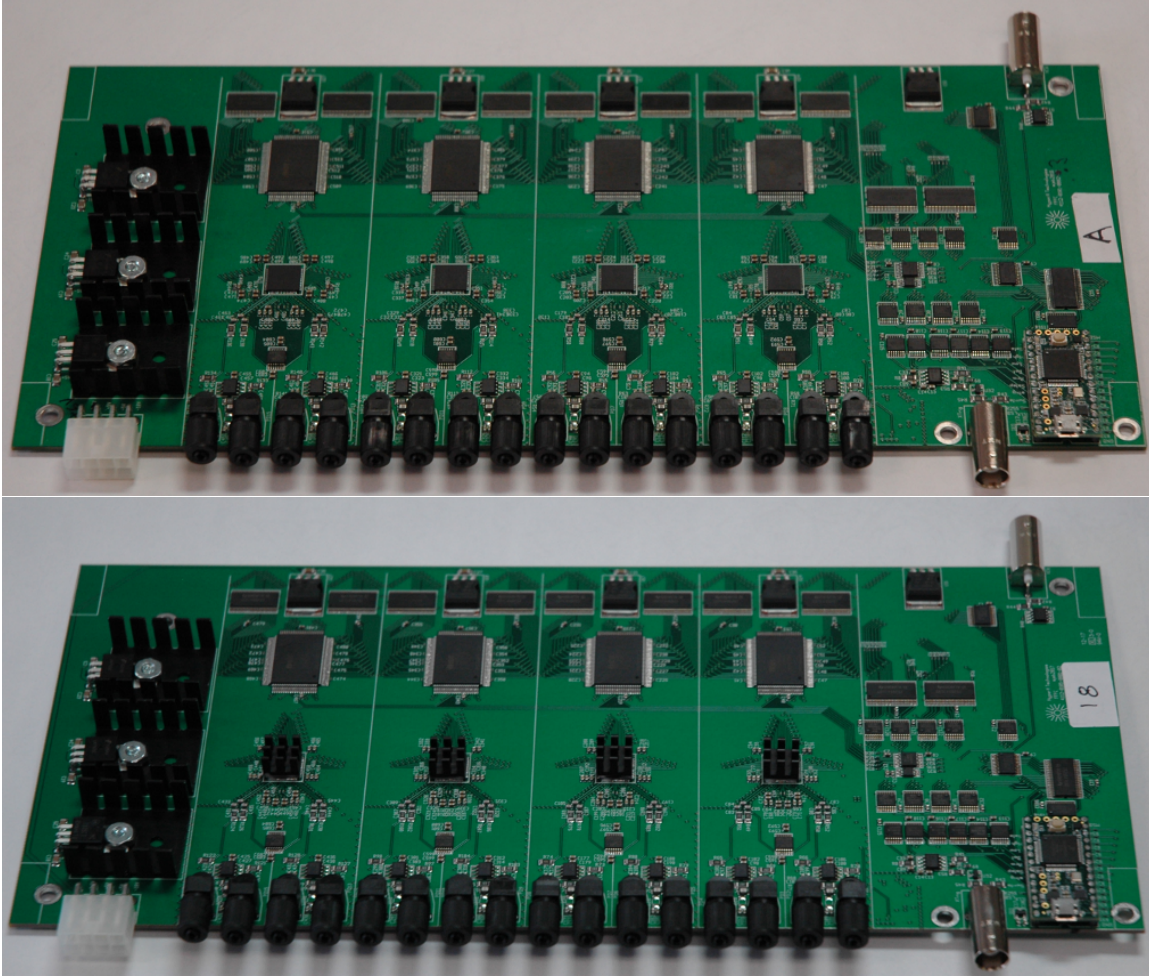


Figure 7 *HyperV’s iterative board design has yielded a board with 16 photodiode channels and uses 6 board layers. Each board has its own embedded controller. This circuit topology was implemented using two different analog-to-digital conversion chips: The ADC1412D (top) and the LTC2284 (bottom).*

Initial designs placed the digitizer voltage input window at $+0/-2V$. However, since photodiode signals are unlikely to produce negative signals, this effectively threw away half the digitizer levels. We discovered that it was possible to adjust the input voltage window bounds with only minor modifications to the existing circuit [10]. This allowed us to build a programmable DC bias which can move the input voltage bounds of all channels up or down as desired for a given experiment, a feature users of our cameras had desired. A prototype of this new feature was added using a 12-bit digital-to-analog converter to the final version of the hardware. Adding this new feature required additional software modifications, but the improved camera function via recovered dynamic range was worth this additional development.

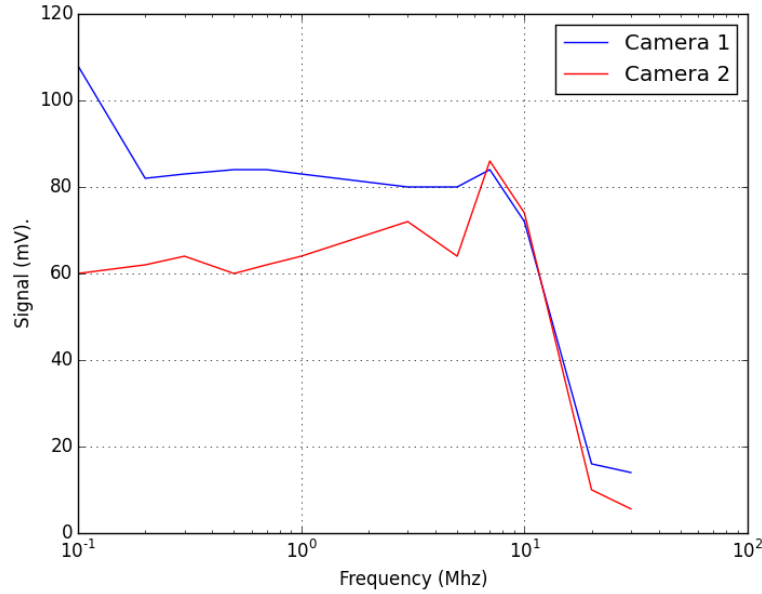


Figure 8 Photodiode circuit topology was implemented using two different analog-to-digital conversion chips. Bode plots for the two designs are shown. Analog bandpass was measured to be about 15MHz, a very conservative choice to maximize gain.

5.3 Cost per Channel

A hardware cost per channel of \$50 was originally targeted in our design. Camera 1 was very close to this at \$53.31. The analog-to-digital conversion chip and PC board assembly costs were the number one and two highest expenses. Camera 2 was more expensive at \$67.10, with the majority of the cost difference between the two designs coming from the added expense of the digitizer. The analog-to-digital conversion chip and PC board assembly costs were again the number one and two highest expenses.

Table 4 Calculated Hardware and Fiber costs per channel for Camera 1 and Camera 2.

Component	Camera 1	Camera 2
ADC Converter	\$13.61	\$24.36
Fiber Optic	\$8.15	\$8.26
Analog Amps	\$3.41	\$3.41
Photodiode	\$2.34	\$2.34
Memory	\$1.13	\$4.16
Channel Support	\$6.80	\$7.01
PCB Board	\$4.94	\$4.82
PCB Assembly	\$12.94	\$12.74
Total	\$53.31	\$67.10

6 Challenges and Resolutions

While the initial plan was to have 128K frames instead of 32K, testing revealed that the discrete 4-bit counter chips which comprise our addresser and counter, while individually rated for high speed data acquisition, each have “all-full” output time delays which make them collectively unsuitable for 100 MHz data acquisition at record lengths of 128,000 or more points. Each chip must cascade the all-full signal in one clock cycle to advance the most significant bit counter, and the collective delay was longer than a clock cycle, never allowing the most significant bits to advance. Rather than slow down the clock speed to allow larger address spaces to work, we opted to reduce the record-length to 32K.

By slightly reducing the size of the memory address space (or the record length) to reduce the number of cascade stages in the addresser, the total time delay in completely updating a TTL addresser can be reduced. The limiting factor is that the counter needs to be able to index over the complete address space so that zero percent pretrigger records can be recorded. Thus by using a 15-bit address space, a 16-bit counter can be employed that only uses three terminal count lines, reducing the total delay of updating the timing units to less than a single clock cycle. This creates record lengths of 32,768 points which is still an excellent record length, but without having to invest in FPGA technology just yet.

The specific details of the rest of the system architecture were determined by how we chose to aggregate the data and transmit it to a control computer. Two designs of camera boards were constructed and bench-tested. Of the 71 NXP-based boards constructed by the external vendor, 19 were found to be faulty. While a few of these faults were obvious manufacturing defects like solder bridges between component leads or the placement of the wrong part at a specific location, many were due to the incorrect or incomplete placement of size 201 resistors. According to our vendor, placing and soldering size 201 parts is quite challenging and carries higher chance of failure, thus reducing production yields. While 201 size resistors have been phased out of future designs, the second camera board, designed concurrently, has many similar issues with size 201 resistors.

Further complications arose when the company making the analog-to-digital conversion chips, NXP, sold off its digital signal processing division in the middle of our project. This led to the deprecation of practically all of the ADC1X12D family of digital signal processors which our board designs were based on. Thus the second camera was constructed using the LTC2xxx family of chips from Linear Technology. This provided almost drop in replacements of similar capability, although at increased price, as noted earlier.

Finally, finding sufficient stocks of chips to avoid lead times of 10 weeks or more when assembly boards necessitated using part families instead of the specifically selected parts. The Camera 1 board was designed and bench tested with 14-bit ADC1412D chips, but only 12-bit ADC1212D chips were available in sufficient quantity to make 71 boards, and similarly for Camera 2.

Early attempts to trigger two boards simultaneously met with mixed results due to the design of the trigger circuit. This was evaluated by observing a strobe light triggered by a photodiode. The result was a random time shift introduced between signals on different boards. Since the initial external trigger design used a follower to drive a TTL OR gate that would notify the control logic when a trigger was received, we suspected this arose from variations of the threshold for activation in the TTL OR gate, in addition to the slope of the

trigger signal created by the strobe light. A new trigger circuit based on a 555 timer was designed and has largely corrected these timing issues.

To reduce noise in collected signals, a low pass filter was added to the photodiode analog input stage. Since the bandpass of the photodiodes is 50 MHz, which is the Nyquist frequency for 100 MHz digitization, any faster analog signals can be discarded.

6.1 Investigating FPGA Controlled Designs

Integrating an FPGA into the board controller would provide a significant increase in controller flexibility and miniaturization. However, upon investigation it was also found to be a significant increase in design and programming complexity. At minimum, an FPGA could be used to replace all of the high speed logic and timing control presently performed with discrete components. At maximum, almost the entire Teensy micro-controller and control board apparatus, and clock control could be contained in an FPGA of sufficient power, almost completely eliminating any board surface area required for board control. In both cases the necessary gate arrangements had to be programmed in VHDL, in addition to altering the circuit to use an FPGA. However, since changing the micro-controller would require rewriting the board control software, we only examined the FPGA solution which makes use of the present Teensy controller, thus minimizing the design perturbation.

The Cyclone IV E FPGA was selected because this is a fairly modern low cost component available in 144 pin packages as well as ball grid arrays. The number of features and gates are expected to be sufficient for the tasks required, while not inflating cost with additional features not leveraged by the current design. Altera, the makers of the Cyclone IV, also provide a freeware version of their compiler for small implementations like this, and the Cyclone IV also has a number of web resources for learning its functionality and integration.

A circuit board using a Cyclone IV was designed and shown in Figure 9. A draft of the VHDL code necessary to power the FPGA was written. However, before code verification was completed and the FPGA design finalized, we figured out how to generate a 32K point address space using TTL logic. A strobe light pulse recorded with 14-bit hardware and a 32K point record length is shown in Figure 10. This was deemed sufficient performance to complete the desired 1024-pixel camera for this Phase 2 project without further investigations into FPGA technology for now.

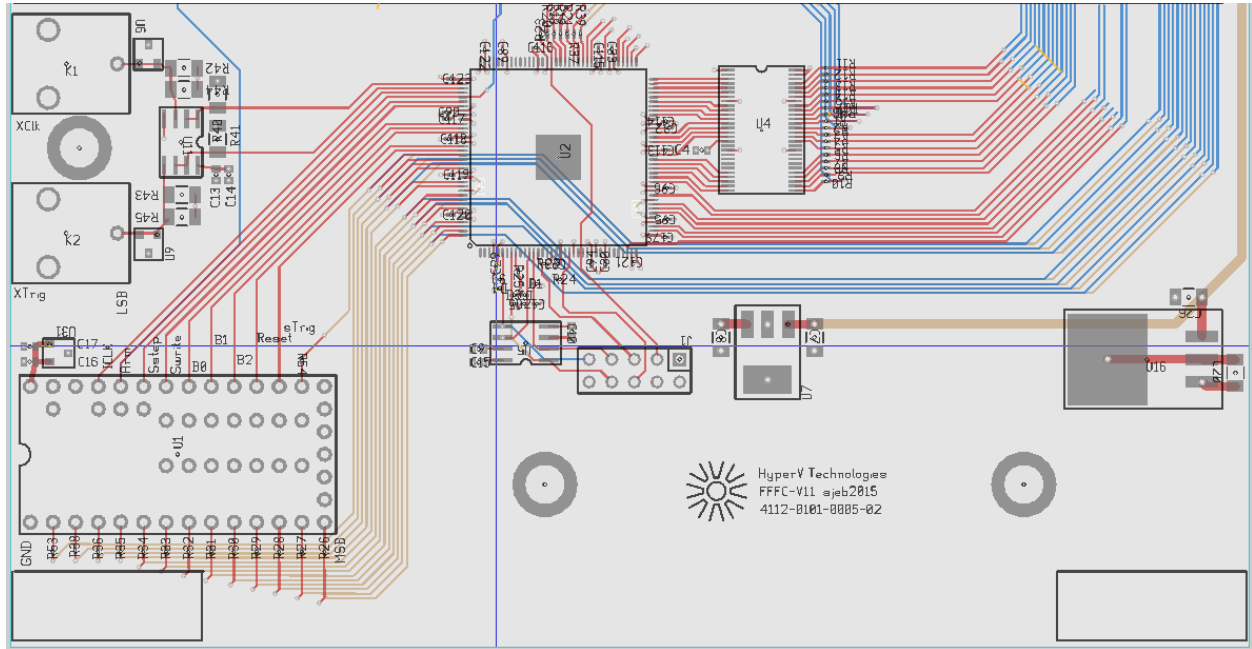


Figure 9 An FPGA-controlled board was designed. The FPGA greatly reduces circuit complexity while even adding additional features. Further gains could be made by integrating the Teensy functionality into the FPGA tasks.

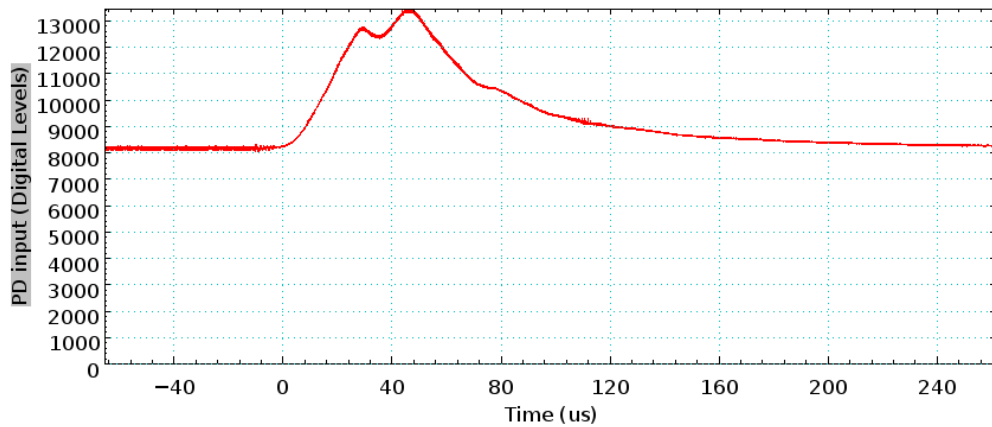


Figure 10 A strobe light pulse recorded with 14-bit hardware. By using a 15-bit address space, a 16-bit counter can be employed that uses only three terminal count lines, reducing the total delay of updating the timing units to less than a clock cycle. This creates record lengths of 32,768 points which is still an excellent record length, without further investigations in FPGA technology for now.

7 Driver Software Design

The camera control software developed in Phase 1 was overhauled and extended to operate the Phase 2 camera system (Figure 11). While many of the higher level camera functions could be preserved, the board level control had to be completely rebuilt, since instead of interfacing to each channel directly, the code would now be servicing micro-controllers over a USB network. The camera driver software was designed in three layers. The lowest layer focuses on interacting with the micro-controller, building a serial bridge between the Python application running on the computer and the embedded application running on each board's micro-controller. The next level of software construction deals with the camera at the board level, specifically the tasks of arming, acquiring, and retrieving information from each board using the serial link built by the lowest level. The final layer is the overall camera control. This layer is a manager capable of launching commands over the array of camera boards and waiting for the status of these commands to be reported back. As many as 64 boards needed to be employed to create a 1024 pixel array, but as many as 127 USB devices (including hubs) can be connected to some computers allowing for increased pixel counts. Thus efforts to maximize serial bus use via parallelization were maximized. Camera shots were expected to have about 50 to 59 Megabytes of data for download depending on the bit depth. For expedited readout of data, two readout methods were developed: one for 14-bit and one for 12-bit. A 6-bit character format was used to further increase data speeds. In hexadecimal, 14 bits is four characters *8FFF*, and 12 bits is three characters *FFF*. By using ASCII codes 32 to 96 to create 6-bit numbers, data sizes are reduced to 3 characters for 14 bits, and 2 characters for 12 bits. This control software has been ported to Linux, Mac, and Windows operating systems.

Software Driver Overview

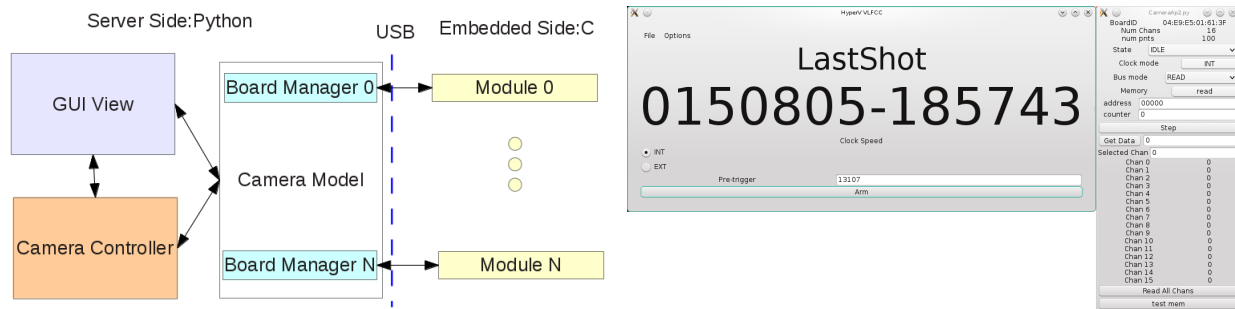


Figure 11 The camera driver software (Left) is designed in three layers. The lowest layer deals directly with interacting with the micro-controller, building a serial bridge between the Python application running on the computer and the embedded application running on each board's micro-controller. The next level is the camera board level that deals with the specifics of arming, acquiring, and retrieving information from each board using the serial link. The final layer is the overall camera control. A high level interface was constructed, as well as a board level interface for diagnostic purposes (Right).

7.1 Optics and Fiber optics

For camera optics, we decided to use a fixed focal length of 60 cm. This was chosen as it is the distance between the window of the HyperV large vacuum chamber and the location of the plasma jet from one of the HyperV plasma accelerators. A single lens solution was developed for the imaging optics, using a 10 cm diameter 200 mm focal length lens. Image aberrations are expected to be much smaller than the 1 mm size of the fiber, so imaging is not be affected.

The mechanical mounting is shown in Figure 12. The mount was simple and robust, consisting of an aluminum tube with two collars to attach the lens and the fiber collection head respectively.

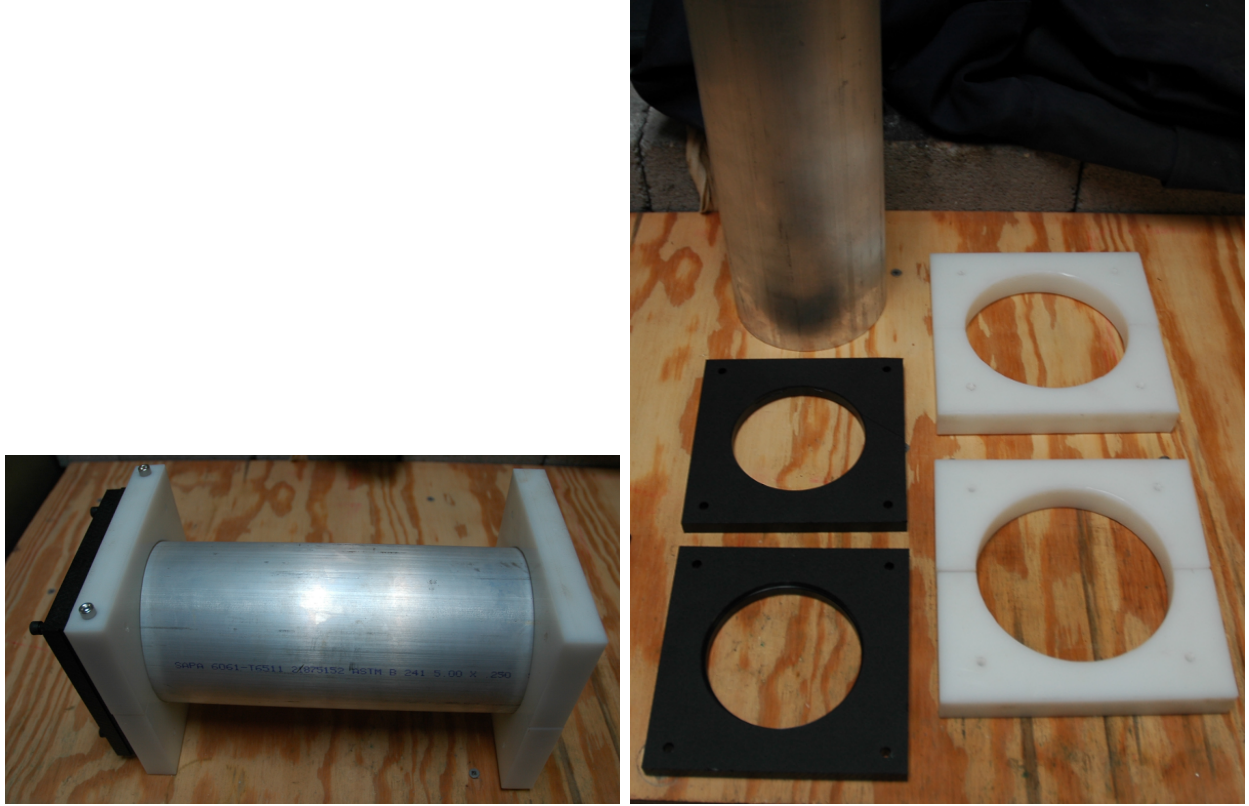


Figure 12 *Optics mounting tube assembled and disassemble. A single lens solution was developed for the imaging optics, using a 10 cm diameter 200 mm focal length lens.*

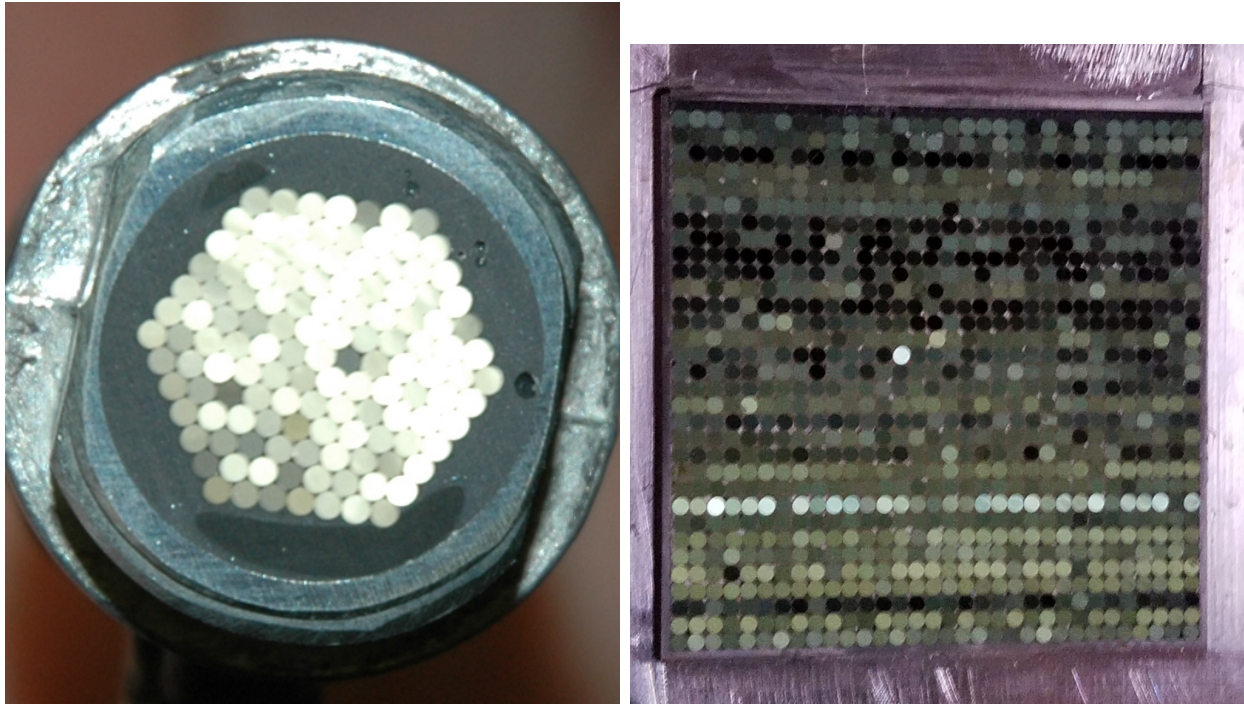


Figure 13 *Experiments were conducted on the construction of a fiber collection head for the camera to see if it could be manufactured in-house. Early results using short sections of fiber and small fiber bundles (127 pixels) were promising (Left), but did not scale well to both larger numbers of fibers and longer fiber lengths. A vendor was used to construct a 32x32 pixel grid (Right) for the prototype array.*

Experiments were conducted on the construction of a fiber collection head for the camera to see if it could be manufactured in-house. Early results using short sections of fiber and small fiber bundles (127 pixels) shown in Figure 13 (left), were promising, but did not scale well to both larger numbers of fibers and longer fiber lengths. Increasing the number of fibers increased the amount of wastage (approximately as many fibers as were in the bundle were wasted), which becomes punitively expensive at large fiber counts. In addition we found that the long fiber tails made assembly very difficult, as the fibers fouled quickly and readily despite efforts to keep them straight. For these reasons, we elected to defer these manufacturing problems and designed a fiber assembly with a vendor, Fiberoptic Systems of Simi Valley, California. A 32 x 32 array of 1024 1mm diameter fiber pixels was constructed, shown Figure 13 (Right).

7.2 Fiber Location and Calibration

One of the key issues in collecting an image using this camera design was accurately locating the position of fibers at the image plane of the optical train. Tracing the fibers individually is possible but does not scale at all well to larger fiber assemblies. We investigated several techniques to locate and calibrate these fibers.

The initial approach to solving this problem was to use a 0.5 mW solid state laser swept across the face of the collection head by a rotating mirror. The laser was spread into a

line using a cylindrical lens and was bounced off an eight sided mirror (from a supermarket checkout scanner) rotating at approximately 5000 rpm. This sweeps a line of laser light across the face of the fibers at about 81 m/s in the configuration we used. From the time of appearance of the laser light on the detector we can back out the x (or y) position of the fiber. Turning the head by 90 degrees and repeating the process allows us to get the y (or x) position, giving us the full (x,y) position coordinates of the fibers. Using amplified photo-detectors (Thorlabs PDA36A) we were able to obtain timing information to calculate the sweep speed. However, when we tried this method with the fiber head, using the Phase 1 camera electronics as a detector, we were not able to extract a useful signal. The Phase 1 camera uses the same photodiodes as the current camera, so we expect that we will get no useful signal using the scanned laser system. It is worth noting that when we tried this method using an amplified silicon photomultiplier we were able to get a usable signal, suggesting that future cameras might use SiPM's for detection of lower light signals.

The next method involved calibrating the AC gain of each fiber, shown in Figure 14 (next page), and then imaging a gradient in each direction to determine their x and y position. Both of these methods had the added benefit of possibly precisely determining each fiber's position, allowing for more accurate interpolation of images taken with imperfect fiber grids to be constructed later. We have found that a Xenon strobe is sufficient to generate a strong signal on the photodiodes. This strobe was used throughout development to test signal strength and detector sensitivity, so we know that a sufficiently strong flash lamp can produce good bench test signals. A 24 in diameter integrating sphere was constructed to convert strobe light flashes into uniform illumination of the imaging grid. A black and white gradient was imaged onto a transparency for location of camera pixels. However, gradient measurements of fiber location contained too much uncertainty in position from noise, and failed to yield usable grid calibrations.

Our final calibration plan, shown in Figure 15 was tedious but accurate and successful. We constructed a mask that would leave one column or row exposed to illumination. We then mounted the fiber grid under a bright lamp so that the mask could be scooted across the grid face in the x and y directions. We then set out the fiber bundles to be sorted. A row was illuminated and the 32 fibers lit the brightest were bundled together and marked as that row number. All 32 rows were sorted and labeled this way. Then the mask was turned 90 degrees and a column was illuminated. The brightest fiber in each bundle was then labeled as that column number. Thus in 64 moves of the mask, the coarse x and y location of each fiber was determined. this process took about 80 person-hours but could be expedited with a piece of software.

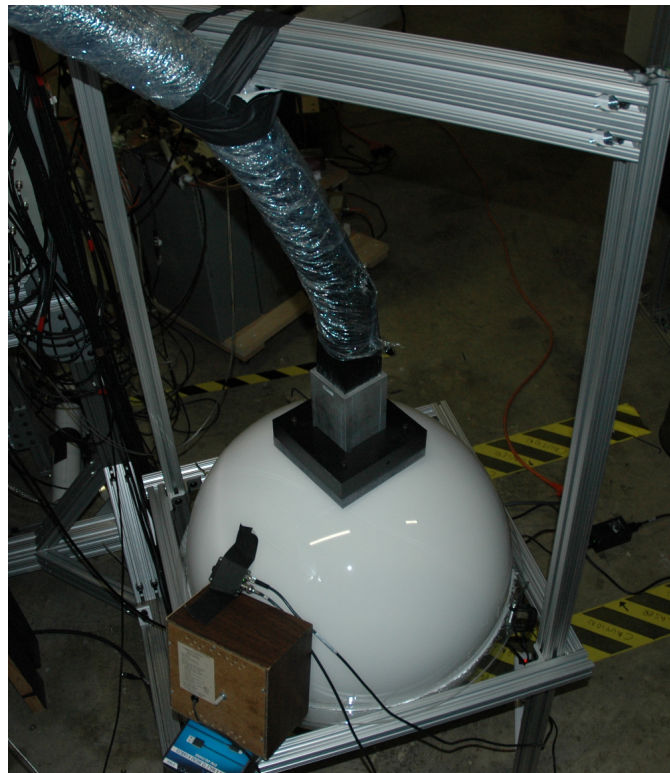
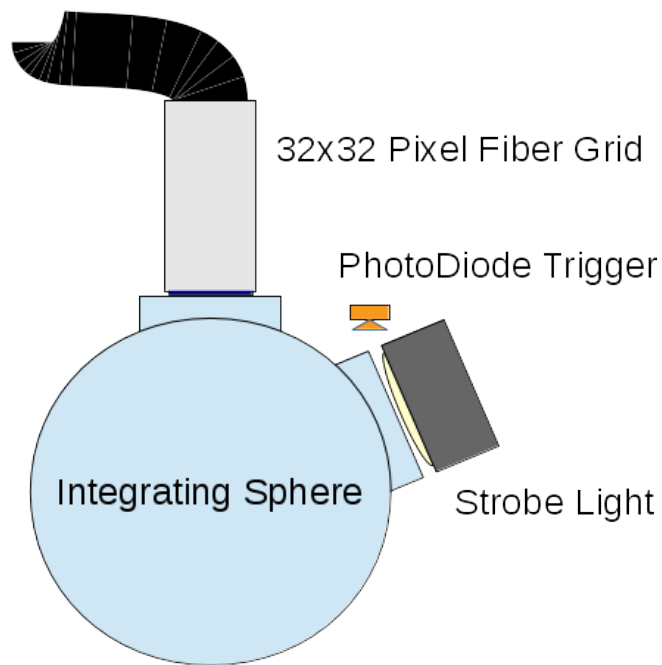


Figure 14 Calibration of the AC gain of each fiber was performed with a strobe light. A 24 in diameter integrating sphere was constructed to convert strobe light flashes into uniform illumination of the imaging grid.

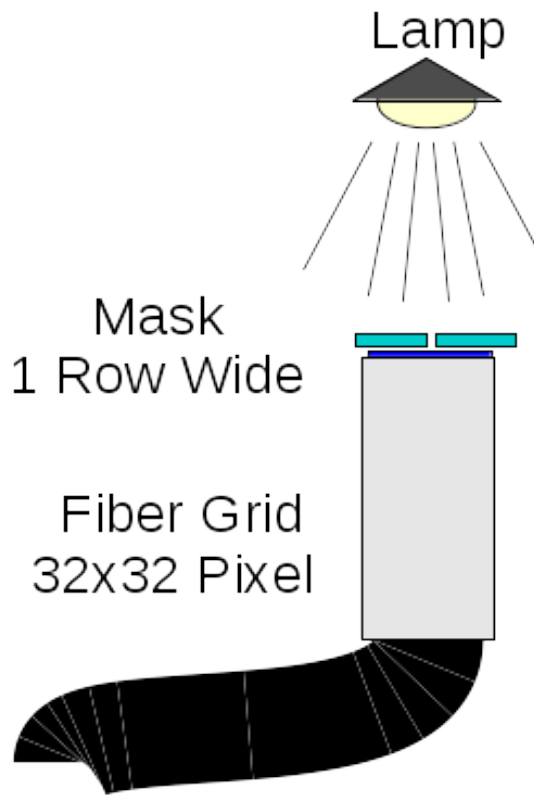


Figure 15 We constructed a mask that would leave one column or row exposed to illumination (Left). We then mounted the fiber grid under a bright lamp so that the mask could be scooted across the grid face in the x and y directions. We then set out the fiber bundles to be sorted (Right). A row was illuminated and the 32 fibers lit the brightest were bundled together and marked as that row number. All 32 rows were sorted and labeled this way. Then the mask was turned 90 degrees and a column was illuminated. The brightest fiber in each bundle was then labeled as that column number. Thus in 64 moves of the mask, the course x and y location of each fiber was determined.

These fibers were then connected to the rack-mounted photodiode boards. Power issues only allowed 63 boards to be powered simultaneously, so 16 pixels were left disconnected. Fiber grid rows connected to a pair of boards. The first board received the first 16 pixels in order and the next board received the next 16 pixels in order, and so on. When the camera software records the data, it makes a list of the hardware address of the boards in the order that their channels were collected. Thus by knowing which boards the fibers were plugged in to, the images collected could be reconstructed in software. Connecting 1008 fibers took about 24 person-hours. When the fibers had been collected, the integrating sphere was used with the strobe lamp to measure and normalize the AC gain of all 1008 channels.

7.3 Test Imaging of a High Speed Fan

Finally, as an all up test of the camera imaging systems, the FFFC camera was used to image a 5500 RPM computer fan. An Evercool 40mm Case/CPU Fan was mounted directly to the face of the fiber imaging grid. This fan has 11 blades and spins at 5500 RPM. Given the camera’s total record length of $T \mu s$ and a computer fan of N blades moving at k rpm’s, the expected number of fan blades observed per shot $g(T)$ is $TNk/60$. This fan was set in motion and illuminated by a Nikon camera flash placed about half a meter in front of the fan and imaging grid, as shown in Figure 16. Travel of about 0.33 fan blades per shot time frame was expected, ensuring that some time dependent optical signals would be produced on the fiber imaging face. A photodiode module was used to trigger the camera off the Nikon flash.

A 32,768 frame image sequence was recorded (Figure 17) of the fan under rotation at 100 Megaframes/second. the 32x32 pixel grid has 12 bits of resolution. Two images from the sequence are shown in Figure 17. Not only is the silhouette of the fan visible but also the direction of the fan’s rotation is observable, marked by the top fan blade crossing the support post and the lower left hand fan blade leaving the support post and creating a space for illumination.

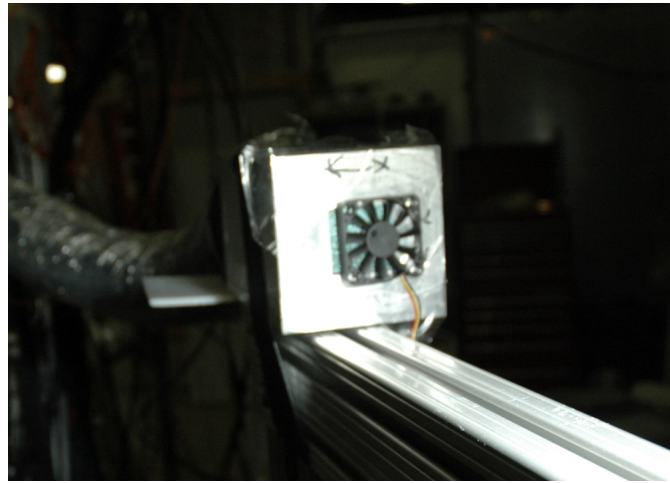
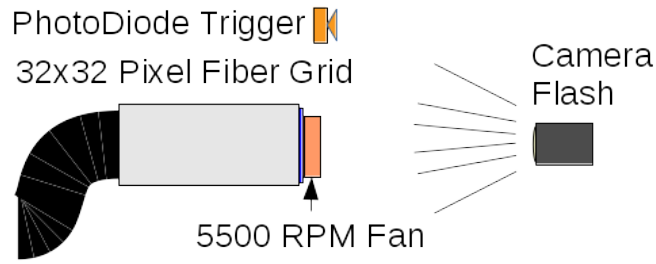


Figure 16 the FFFC camera was used to image a 5500 RPM computer fan illuminated by a Nikon camera flash. This fan has 11 blades. About .33 fan blades crossing per shot were expected.

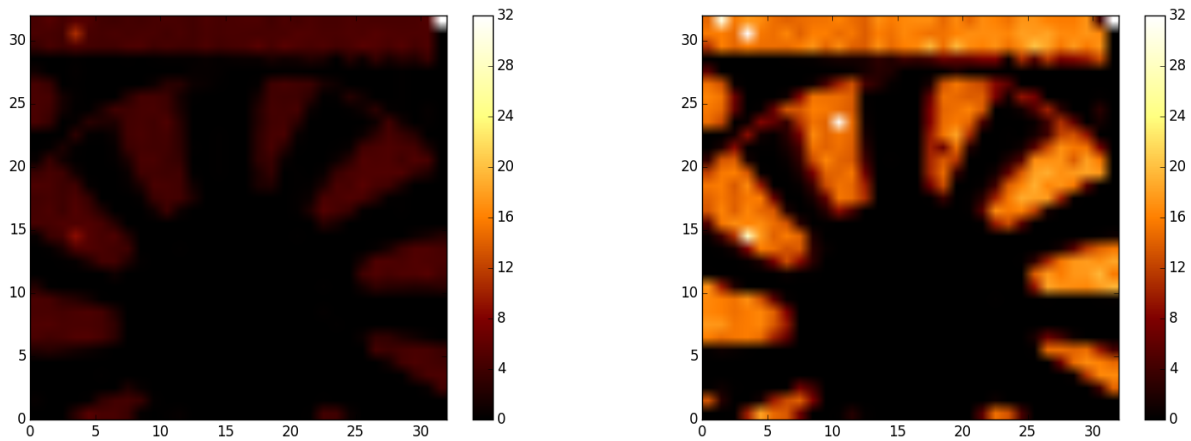


Figure 17 A 32768 frame image sequence was recorded of the fan under rotation at 100 Megaframes/second. Left is time $10\mu\text{s}$ right is time $160\mu\text{s}$. Not only is the silhouette of the fan visible but also the direction of the fan's rotation is observable, marked by the top fan blade crossing the support post and the lower left hand fan blade leaving the support post and creating a space for illumination.

8 1008 Pixel Experimental Results

A 1008 pixel full-scale prototype camera was constructed, calibrated and deployed on the HyperV Plasma Jet Railgun Accelerator facility shown below in Figure 18.

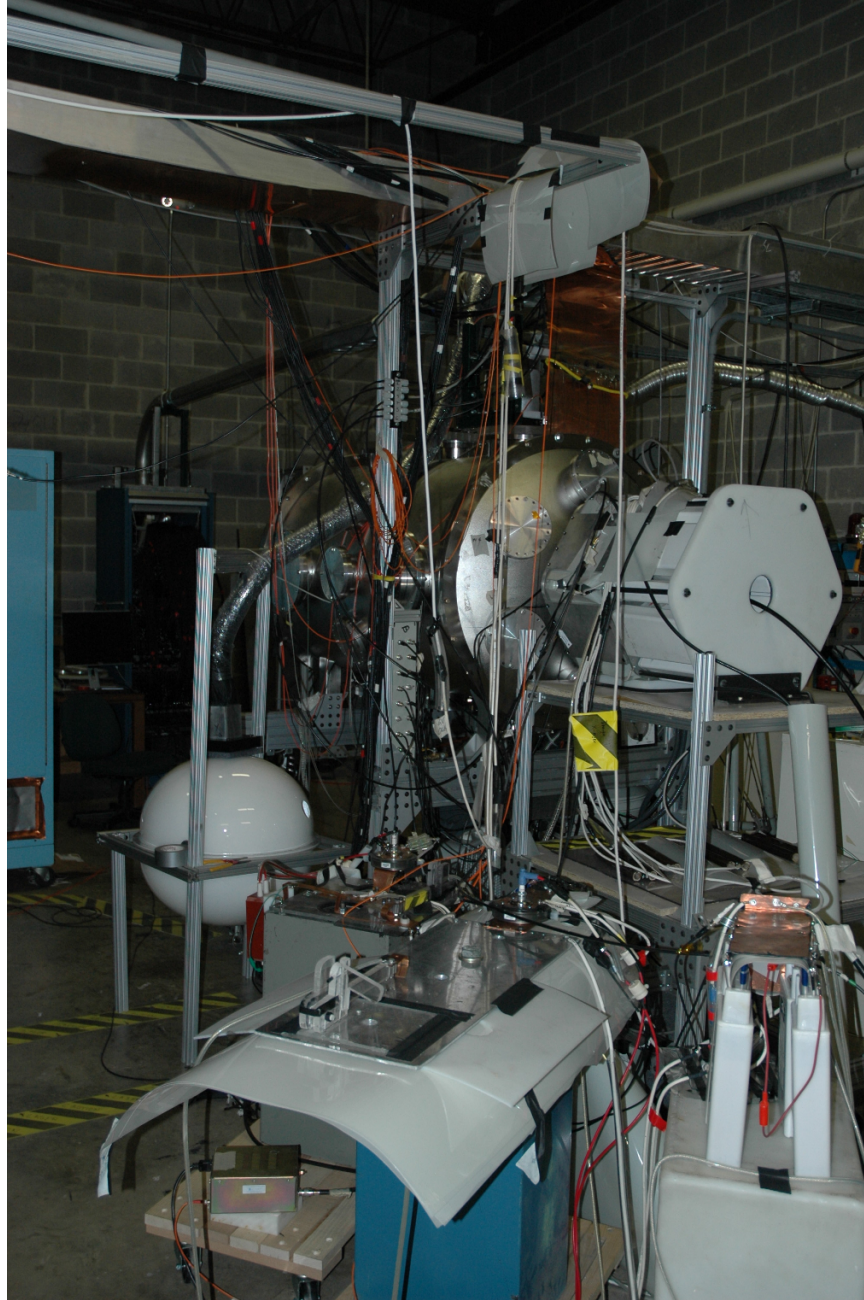


Figure 18 *A 1008 pixel full scale prototype camera shown deployed on the HyperV Plasma Jet Railgun Accelerator at HyperV. Preliminary plasma jet experiments showed that plasma emission light levels were saturating pixels for the amount of gain in this full-scale camera. Thus neutral density filters were employed to reduce optical signals below saturation. The camera imaging head is mounted to the top of the chamber. The camera electronics rack is on the left against the back wall. The plasma gun is mounted on the front end of the vacuum tank.*

This camera uses the Camera1 ADC1412D chip board design shown previously in Figure 7 (top). The camera electronics rack was placed as far away from the pulse power systems of the plasma accelerator as the fiberoptic cables would allow. This placed the electronics rack at the far back wall, as shown below in Figure 19.

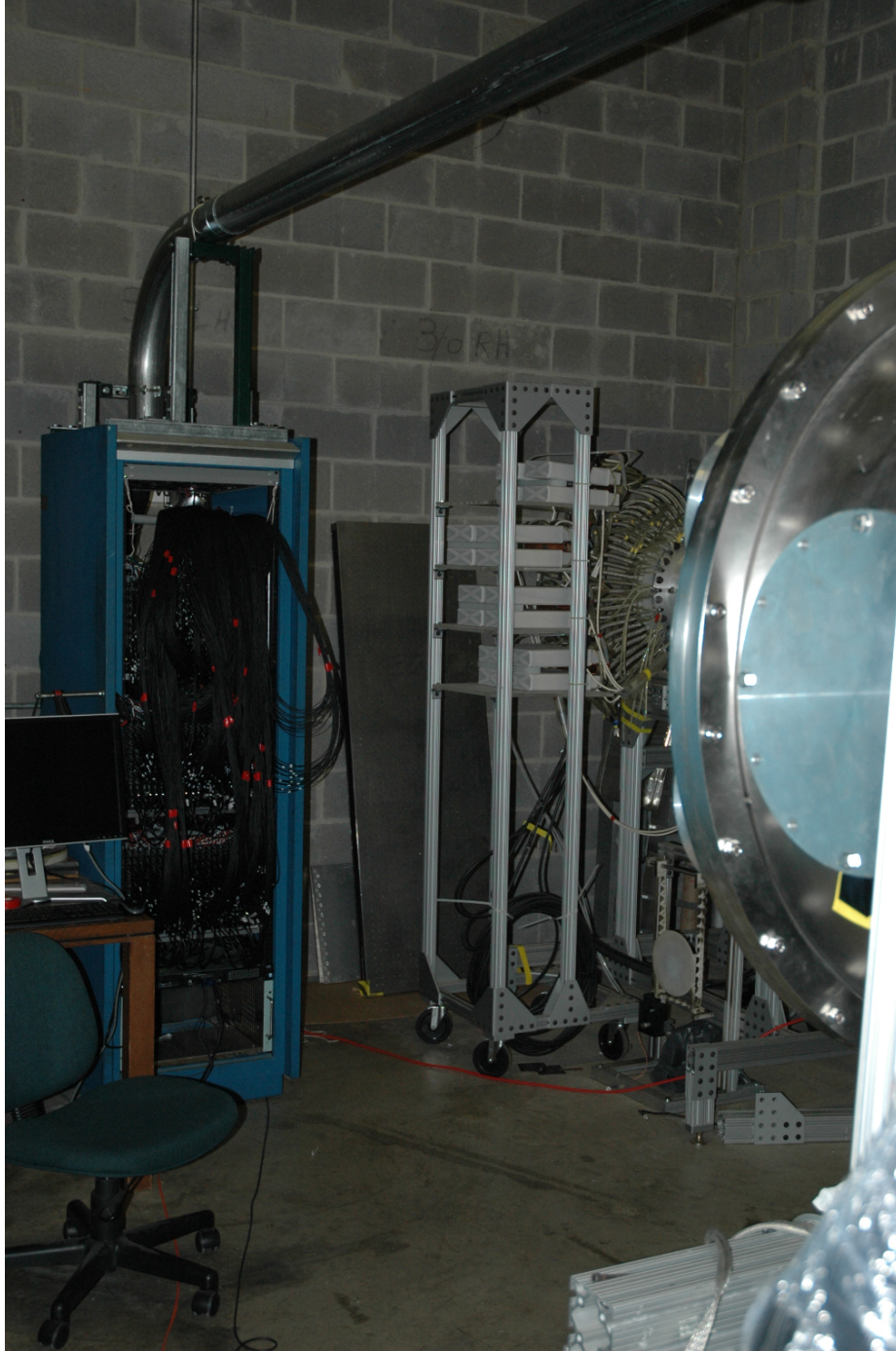


Figure 19 *A 1008 pixel full scale prototype camera was constructed, calibrated and deployed on the HyperV Plasma Jet Railgun Accelerator at HyperV (Figure 21). This camera used the Camera1 ADC1412D chip board design.*

The fiber imaging grid was mounted over the chamber to view the transit of plasma passing the imaging plane (Figure 20). A set of collection optics was used to image visible plasma emission on to the fiber imaging grid. These collection optics were mounted on the first window looking down into the chamber about 35 cm from the nose of the plasma accelerator(see Figure 21 for the experimental setup). Final alignment of the fiber grid and optics showed our focal plane to be above the center of expected ejected plasma by about 5 cm, due to additional components. The focus of our FFFC camera optics was corrected by removing the excess length from the aluminum support tube. The interior of the tube was also lined with a mat black material to decrease wall reflections. Preliminary plasma jet experiments showed that plasma emission light levels were saturating pixels for the amount of gain in this full-scale camera. Thus, neutral density filters were employed to reduce optical signals below saturation.



Figure 20 *A set of collection optics was used to image visible plasma emission on to the 32 x 32 fiber imaging grid. These collection optics were mounted on the first window looking down into the chamber about 35 cm from the nose of the plasma accelerator.*

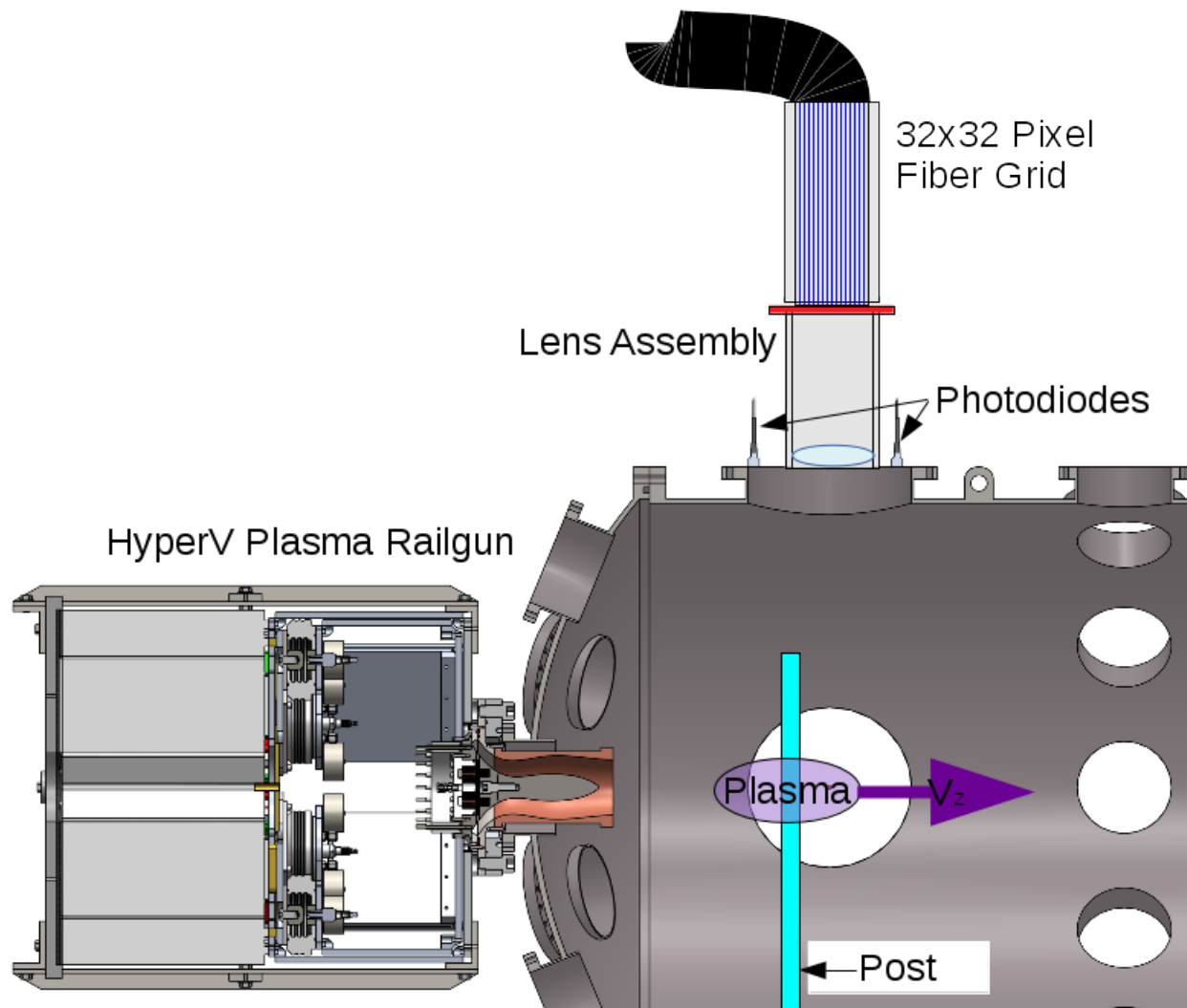


Figure 21 A diagram of camera head installation on the HyperV Plasma Jet Railgun Accelerator HyperV. collection optics were mounted on the first window looking down into the chamber about 35 cm from the nose of the plasma accelerator.

The view of the camera is approximated in Figure 22. Alignment was biased slightly off the center-line in order to increase the distance from center to enable viewing structure in the plasma plume. Experiments were conducted with unobstructed jet propagation and collision of jets against two different diameters of posts. A number of clean up shots were taken before and between camera shots to keep plasma jet performance optimal.

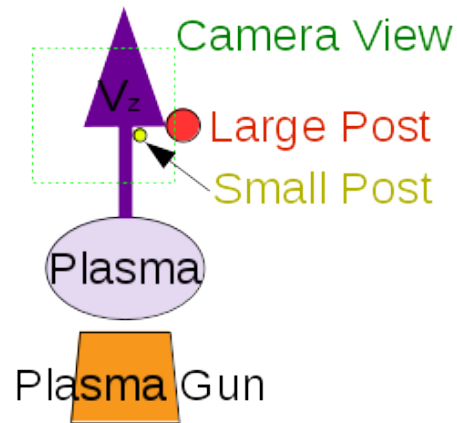


Figure 22 Camera view alignment was biased slightly off the center-line in order to increase the distance from center for viewing plasma structures. Experiments were conducted with unobstructed jet propagation and collision of jets against two diameters of posts.

8.1 Plasma Jets

Shots were taken with the FFFC camera to observe unobstructed plasma jets transiting the camera view. Both 0.9 and 0.3 density neutral density filters were used to attenuate light to acceptable levels. Each shot gathered 32K frames at 10ns intervals of the plasma jet propagation. Figure 23 shows 9 frames selected at 100ns intervals of a single shot. While the 32 x 32 resolution is relatively coarse, structure in the jet is visible. A bright plasma feature in this sequence marches unobstructed past the camera view.

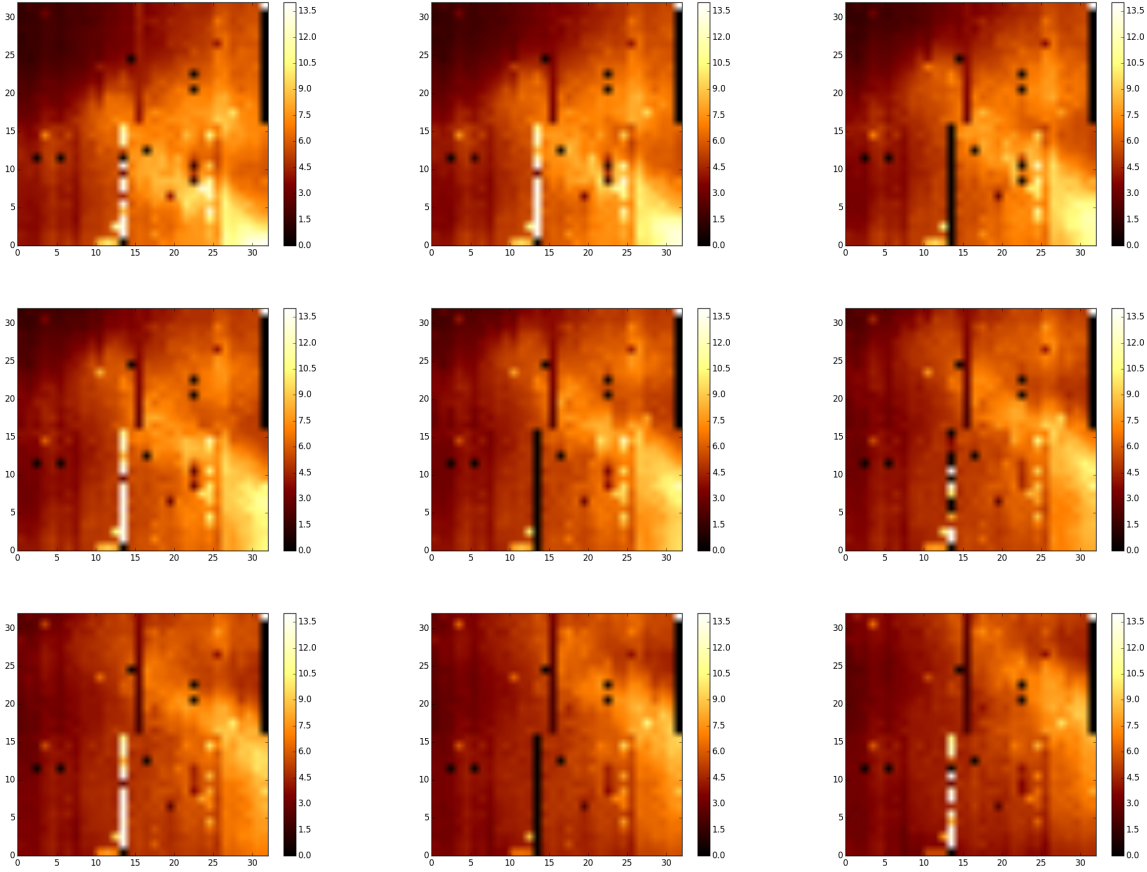


Figure 23 *The FFFC camera was used to observe unobstructed plasma jets transiting the camera view. Nine frames selected at 100ns intervals of a single shot are shown. While the 32 x 32 resolution is coarse, structure in the jet is quite visible.*

Two artifacts were noticed in camera images - dead pixels and missing boards. Gain calibration revealed a number of dead pixels, presumably due to too manufacturing defects or bad parts in the camera boards. These are the isolated black dots. Some of these bad pixels may be correctable. The other artifact is missing boards. While the fiber imaging grid was constructed with 1024 pixels, only 63 boards (1008 pixels) could be powered by the constructed power bus, thus a column of 16 pixels in the upper right hand corner of images are left blank as they have no digitizers. While trigger problems have been largely eliminated by the 555 based improved trigger design, occasionally a board appears to trigger late or

stop acquisition on trigger instead of after the requested time period. The result is a black stripe or a stripe that seems out of phase with the rest of the image. These are intermittent problems, so while they should be correctable, we are still isolating their source.

In addition to XY images of the plasma, streak images of a cross-section of plasma can be plotted. Shown in Figure 24 are the first 16K points of a 32K point image for a 32 pixel column at $x=27$. The brightest plasma transits the camera view between 32 and 44 μs .

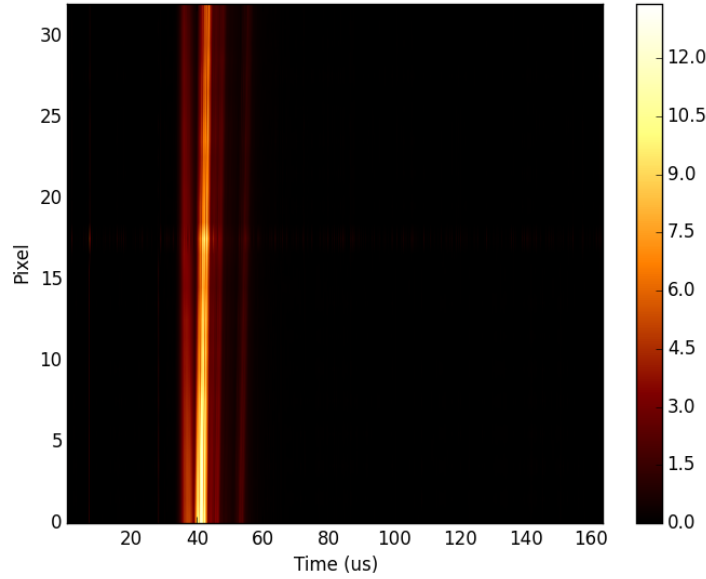


Figure 24 A streak image at $x=27$ of an unobstructed plasma jet transiting the camera view. The first 16K points of a 32K point record are shown. The brightest plasma transits the camera view between 32 and 44 μs .

8.2 Large Post Collisions

Test shots were taken with a 5 cm diameter steel post obstructing plasma jet propagation in order to forcibly introduce additional structure in the camera view. Two 0.9 density neutral density filters were used to filter light down to acceptable levels because of the heating of the plasma colliding with the post. Each shot gathered 32K frames at 10ns intervals of the plasma jet propagation. Nine frames selected at 400 ns intervals of a single shot are shown in Figure 25. The post is located just off to the right of the camera view. The plasma jet enters the field of view, piles up a “bow wave” on the large post, just out of view. Later, a wave of bright trailing plasma also strikes the large post.

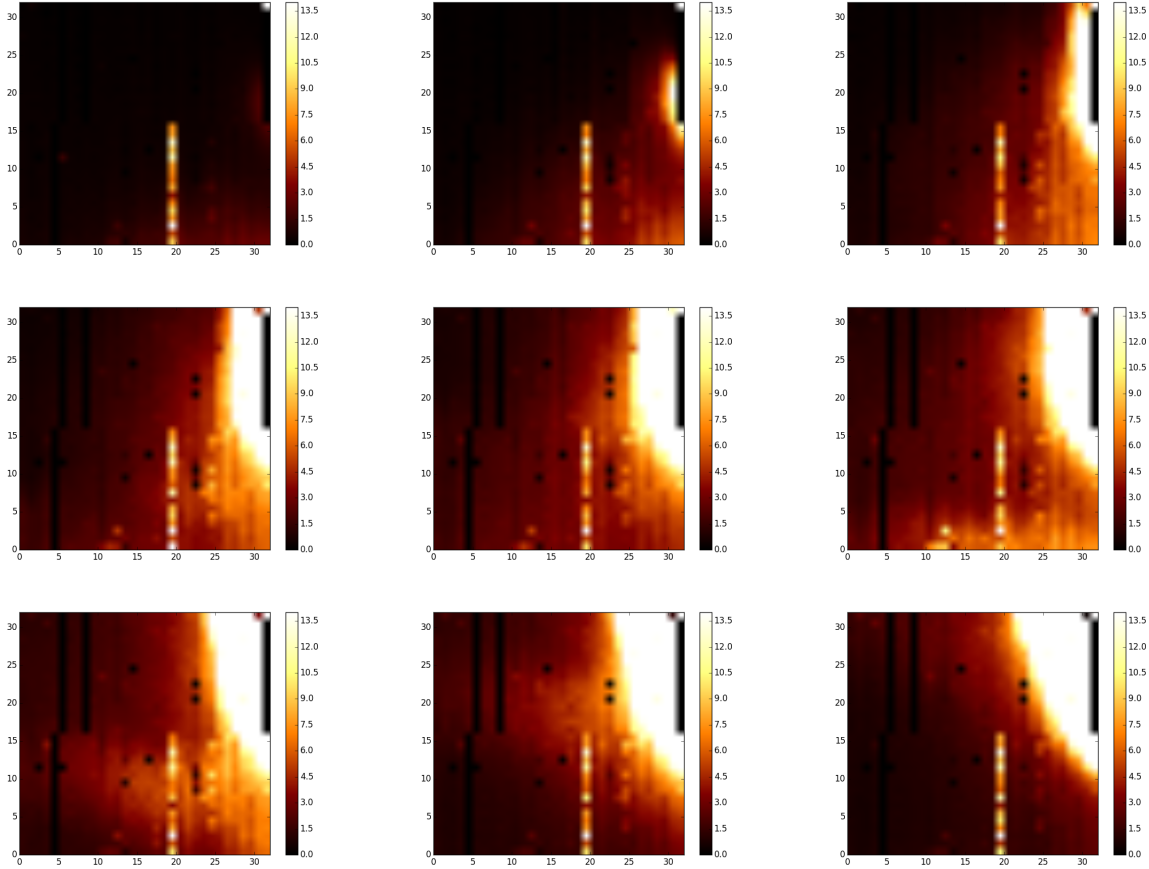


Figure 25 *Shots were taken with a 5 cm diameter steel post obstructing plasma jet propagation. The post is located just off to the right of the camera view. The plasma jet enters the field of view, piles up a “bow wave” on the large post, just out of view. Later, a wave of bright trailing plasma also strikes the large post.*

8.3 Small Post Collisions

Test shots were also taken with a smaller 1.27 cm diameter steel post obstructing plasma jet propagation, again to forcibly introduce additional structure in the camera view. Two 0.9 density neutral density filters were used to filter light down to acceptable levels because of the heating of the plasma colliding with the post. Each shot gathered 32K frames at 10ns intervals of the plasma jet propagation. Nine frames selected at 500 ns intervals of a single shot are shown in Figure 25. The post is located right of center of the camera view to resolve the “bow wave” of the plasma against the post and most of one side of the trailing tail. The plasma jet enters the field of view, piles up a “bow wave” on the small post, and plasma flow can be seen around the side of the post. A wave of bright trailing plasma also strikes the small post late in the shot.

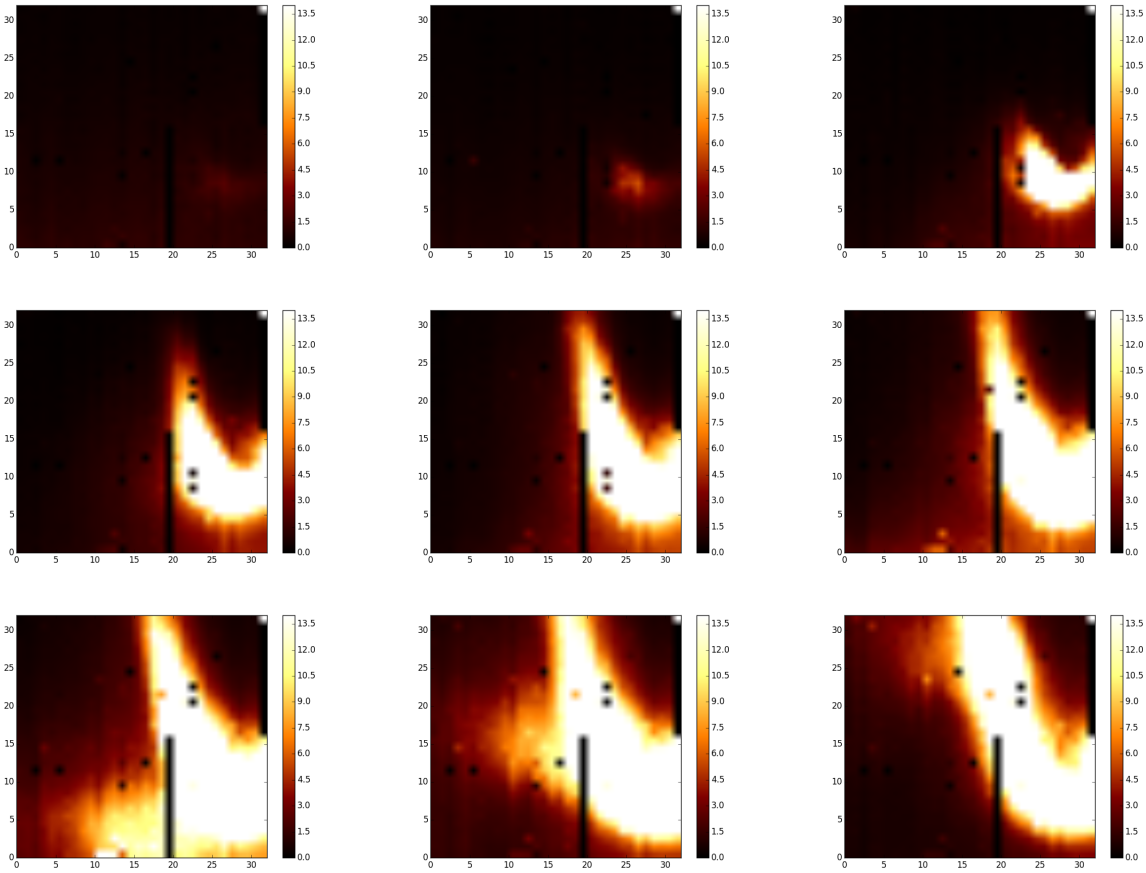


Figure 26 Shots were taken with a smaller 1.27 cm steel post obstructed plasma jet propagation. The post is located right of center of the the camera view to resolve the “bow wave” of the plasma against the post and most of one side of the trailing tail. The plasma jet enters the field of view, piles up a “bow wave” on the small post, and you can see the plasma flow around the side of the post. A wave of bright trailing plasma also strikes the small post late in the shot.

9 Test Pixel Deployment Sites

The focus of the second program track was to deploy prototype channels to select institutions as part of an unfunded collaboration, in order to target camera capabilities to community needs. Since the camera is comprised of arrays of identical pixels, the performance of the 1024-pixel assembly on an experiment can be gauged with the deployment of a few test pixels. Thus, HyperV has sought various programs to receive and evaluate units of a few test pixels as part of an unfunded collaboration of our Phase 2 efforts. Deployments to two programs were made: the Plasma Liner Experiment (PLX) at Los Alamos National Laboratory (LANL) [4], and the Compact Toroid Injection Experiment (CTIX) at the University of California at Davis [6].

Table 5 *Test Site Evaluators*

PI	Institution
Dr. David Hwang	University of California at Davis
Dr. Scott Hsu	Los Alamos National Laboratory

9.1 Work with UC-Davis Test Site

A board of 16 channels based on the Camera1 design was deployed to CTIX. While CTIX has not yet been able to integrate these photodiode detectors into their experiment, CTIX is already a user of our high speed spectroscopy test pixels recently deployed to UC-Davis as part of our DOE SBIR Phase 1 development for high speed low light imaging. Two boards of 16 pixels of Silicon photomultiplier channels employing software and embedded system architecture, built on the design of our camera photodiode channels developed for this program, were deployed to UC-Davis in January 2016. Since these spectra boards use a similar core design to the photodiode unit we provided and similar software the installation process yielded much useful information. Since the boards only required a 5V TTL trigger, integration with existing triggering systems was straightforward. Simultaneity of board acquisition was sometimes a challenge due to the lack of master trigger units in this particular installation, however, master trigger boards had already been developed for the 1024-pixel camera in anticipation of this. Deploying to UC-Davis forced us to make the driver software compatible with Windows as well as Linux, which was readily accomplished in Python. After supporting Windows, adding Python support for Macintosh was trivial. CTIX also requested an alternative data file format which was easily added. It was suggested to us that we build an online repository of driver codes so that software improvements and feature requests can be made available to end users. Python also supports installation packages so that one-click turnkey software packages might be constructable, which would help make systems more user friendly.

9.2 Work with LANL Test Site

The PLX- α project at Los Alamos made use of a prototype version of a HyperV camera board as a high-speed plasma diagnostic. A key part of the experiments at PLX involved firing six

plasma guns at the same time, with as near to identical plasma density and velocity as they could generate. Both jet optical emission profiles and jet velocity can be measured using just two photodiodes per gun. The detector board provided 16 channels of fiber-coupled light detection sampled at 100 MHz. Two fibers were run from the HyperV camera board to a staggered view at the exit of each gun, to monitor the light emission of the plasma as it was fired. An illustrative photograph of the mounting on a seventh as-yet-uninstalled gun is shown in Figure 27. By using the known distance separation between the two fiber views, we are able to deduce the velocity of the plasma jet by analysis of the time delay between the correlated signals.

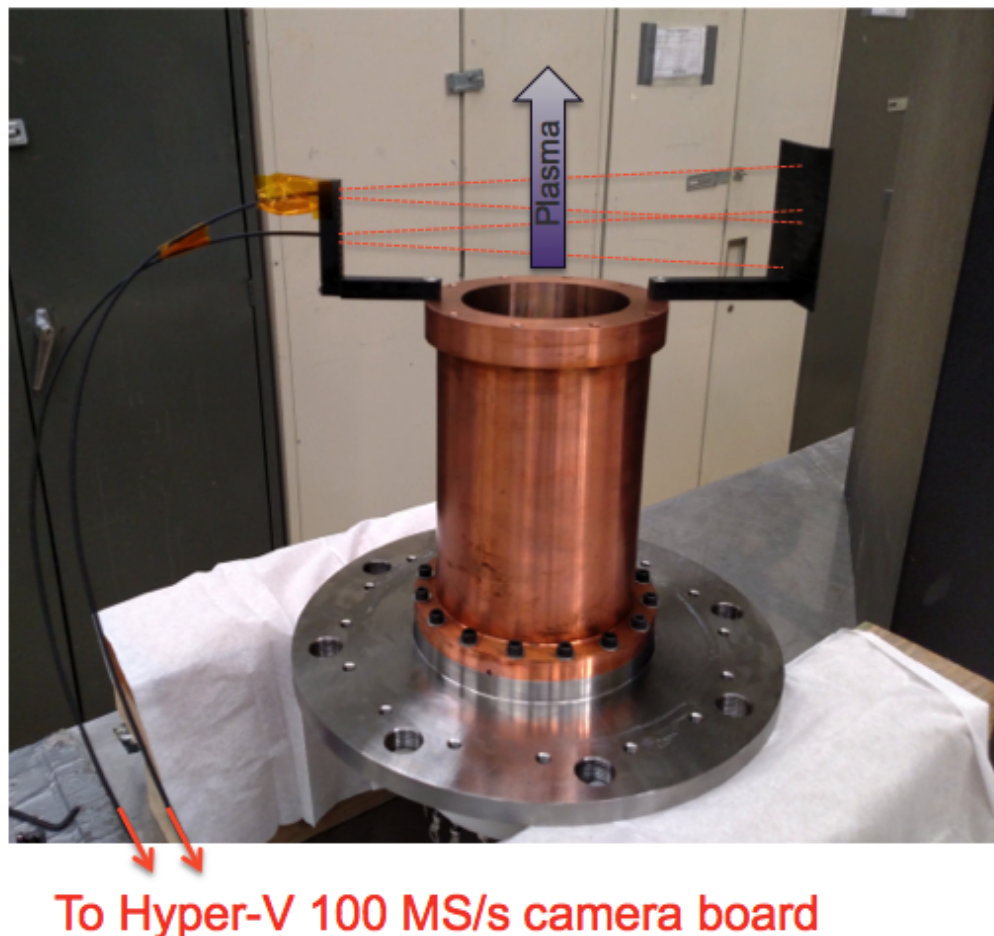


Figure 27 *Diagram of fiber light collection views mounted on gun at LANL.*

LANL rated the camera board as performing “very well”. It yielded a high volume of quality data as shown in the next section. Indeed, in many instances the light emission data proved invaluable in diagnosing differences in jet timing and velocity, and guided the adjustment of gun parameters to compensate. The only operational issue with the camera board was that since it had the old trigger circuit, it only successfully triggered on some shots, but not others. It was eventually discovered that if the board was left in the armed

state for upwards of 1 minute before a shot, it triggered successfully every time. HyperV has already incorporated an improved trigger reception circuit into the newest version of the board which should fully eliminate this issue. Because PLX is Labview-based, we worked with them to port the Camera controller code to Labview. However, because the code was still under development, it was simpler to just run the Python application as a stand-alone module.

10 LANL Experimental results

Some typical data collected with the camera board is shown below in Figure 28. Approximately 300 shots of similar data have been collected to date, providing valuable insight into the gun performance. Figure 29 shows plasma jet velocity across many shots, derived from an analysis of the camera board signals.

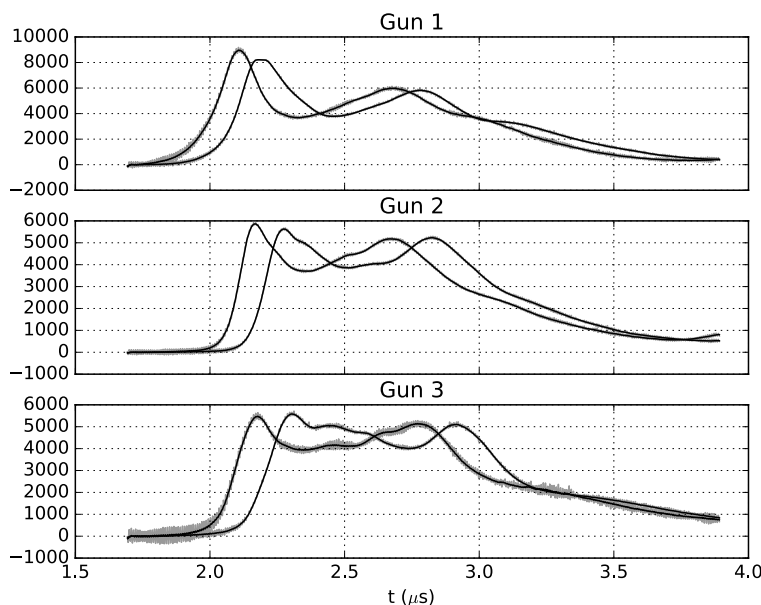


Figure 28 *Time traces of light signals from plasma guns collected with camera board.*

LANL requested a few features for their next camera board. They would like a more reliable trigger, which should already be addressed in the final board version. They would have liked the board provided in a turnkey box so they can plug it in and use it. User-variable gain per channel would be a nice option to consider but not necessarily for PLX experiments. Finally, while the present signal-to-noise levels were sufficient, they would like still more noise immunity because “less noise is always good”. However, they were able to filter signals in digital post processing.

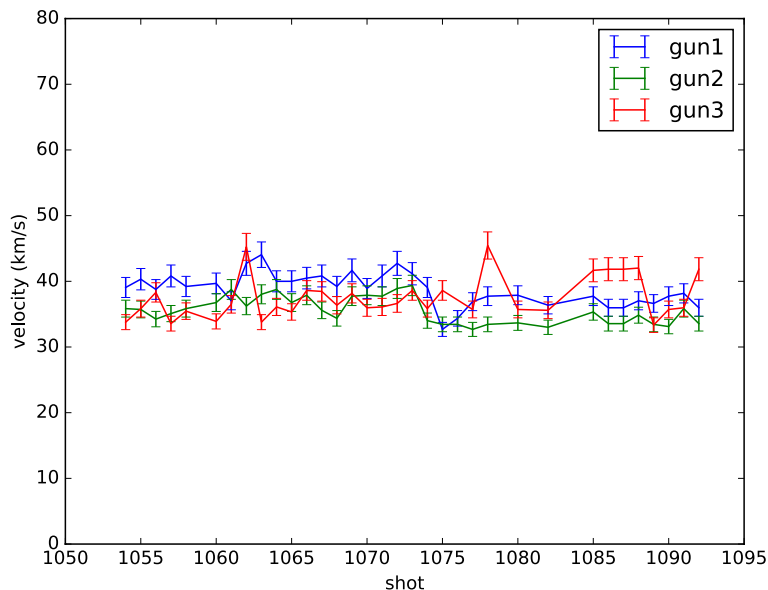


Figure 29 *Plasma jet velocity across many shots, from analysis of light emission data*

11 Intellectual Property

A provisional patent application on the novel features of the camera was drafted and filed in late 2015, followed by a full patent application [11] submitted in late 2016. The patent claims not just the camera in the form in which we are constructing it, but also a set of variants which greatly expand the scope of camera capabilities. These include: the use of silicon photo-multipliers in place of photodiodes, use of optical gain at either the collection optics end (e.g. a image intensifier) or the detection end of the fibers, using the fibers themselves as a means of optical gain by using doped fibers pumped by a laser which allows for gain at a single wavelength, the use of optical filtering either directly at the collection optics or the detection end (which allows different filters for each fiber), and the use of an X-ray pinhole camera for the optics and an X-ray scintillator in front of the imaging head.

12 Summary

HyperV Technologies Corp. has successfully designed, built and experimentally demonstrated a full scale 1024 pixel 100 MegaFrames/s fiber coupled camera with 12 or 14 bits, and record lengths of 32K frames, exceeding our original performance objectives. This high-pixel-count, fiber optically-coupled, imaging diagnostic can be used for investigating fast, bright plasma events. In Phase 1 of this effort, a 100 pixel fiber-coupled fast streak camera for imaging plasma jet profiles was constructed and successfully demonstrated. The resulting response from outside plasma physics researchers emphasized development of increased pixel performance as a higher priority over increasing pixel count. In this Phase 2 effort, HyperV therefore focused on increasing the sample rate and bit-depth of the photodiode pixel de-

signed in Phase 1, while still maintaining a long record length and holding the cost per channel **to levels which allowed up to 1024 pixels to be constructed**. Cost per channel was \$53.31, very close to our original target of \$50 per channel. The system consists of an imaging “camera head” coupled to a photodiode bank with an array of optical fibers. The output of these fast photodiodes is then digitized at 100 Megaframes per second and stored in record lengths of 32,768 samples with bit depths of 12 to 14 bits per pixel. Longer record lengths are possible with additional memory. A prototype imaging system with up to 1024 pixels was designed and constructed and used to successfully take movies of very fast moving plasma jets as a demonstration of the camera performance capabilities. Some faulty electrical components on one of the 64 circuit boards resulted in only 1008 functional channels out of 1024 on this first generation prototype system. We experimentally observed backlit high speed fan blades in initial camera testing and then followed that with full movies and streak images of free flowing high speed plasma jets (at 30-50 km/s). Jet structure and jet collisions onto metal pillars in the path of the plasma jets were recorded in a single shot. This new fast imaging system is an attractive alternative to conventional fast framing cameras for applications and experiments where imaging events using existing techniques are inefficient or impossible. The development of HyperV’s new diagnostic was split into two tracks: a next generation camera track, in which HyperV built, tested, and demonstrated a prototype 1024 channel camera at its own facility, and a second plasma community beta test track, where selected plasma physics programs received small systems of a few test pixels to evaluate the expected performance of a full scale camera on their experiments. These evaluations were performed as part of an unfunded collaboration with researchers at Los Alamos National Laboratory and the University of California at Davis. We also deployed modules of 16 test pixels to both Los Alamos National Laboratory and to the University of California at Davis for evaluation purposes, with positive feedback from both regarding camera performance and usefulness.

Imaging information on the evolution and propagation of fast, bright plasma events that previously had to be aggregated over many shots, can now be recorded in a single shot, albeit at modest spatial resolution. This not only allows shot-to-shot variant dynamics like turbulence and turbulent mixing to be resolved, but also dramatically reduces the resources required to collect this information, especially in large devices where shots are at a premium such as studying ELM mode growth and disruptions in tokamaks. With our prototype camera, ELM mode growth could be imaged and compared between shots. The ability to accurately measure optical emission profiles at high time resolution also provides insight into plasma jet propagation, turbulence, mixing, and time evolution of plasma events and instabilities in general. Fast imaging of bright events could also be used to investigate fast exothermic reactions, and with use of backlighter techniques, observe changes in materials or fluids. Adding optical band pass filtering to this diagnostic increases this camera’s flexibility and utility.

In conclusion, research groups are continually in search of imaging solutions with increased frame-rate, bit-depth, and record length. For events which are not necessarily repeatable from shot-to-shot, or for dynamic events in devices too large to accumulate event evolution over many shots, HyperV’s high-time-resolution, deep-record-length plasma imaging system has a substantial advantage over present single shot and burst shot imaging systems and we are now attempting to commercialize this new technology.

13 Acknowledgments

The authors would like to thank Francis Thio and Curtis Bolton at DOE for their support of this project. The authors would also like to thank the PLX- α group at Los Alamos National Laboratory and the CTIX group at the University of California at Davis. A thank you to Scott Hsu, Kevin Yates, Sam Langendorf, Jackie Vaughan, and John Dunn for all their hard work installing and running the HyperV photodiode channels on the PLX experiment. A thank you to Professor David Hwang, Robert Horton, Russ Evans, and Ruth Klauser for all their hard work on the HyperV spectrometer and photodiode installations at CTIX. The authors would also like to thank the Department of Energy for taking an interest in and support of this new plasma imaging technology. We would also like to thank the team at Dawnbreaker for all their invaluable assistance. This work was supported by the U.S. DOE SBIR Phase 2 Grant DE-SC0009492.

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