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Protection of Renewable-dominated Microgrids: Challenges and Potential Solutions

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Protection of Renewable-dominated Microgrids: Challenges and Potential Solutions

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Abstract

keywords: Microgrid Protection, Impedance Relay, Signal Processing-based Fault Detection, Networked Microgrids, Communication-Assisted Protection

In this report we address the challenge of designing efficient protection system for inverter-dominated microgrids. These microgrids are characterised with limited fault current capacity as a result of current-limiting protection functions of inverters. Typically, inverters limit their fault contribution in sub-cycle time frame to as low as 1.1 per unit. As a result, overcurrent protection could fail completely to detect faults in inverter-dominated microgrids. As part of this project a detailed literature survey of existing and proposed microgrid protection schemes were conducted. The survey concluded that there is a gap in the available microgrid protection methods. The only credible protection solution available in literature for low-fault inverter-dominated microgrids is the differential protection scheme which represents a robust transmission-grade protection solution but at a very high cost. Two non-overcurrent protection schemes were investigated as part of this project; impedance-based protection and

transient-based protection. Impedance-based protection depends on monitoring impedance trajectories at feeder relays to detect faults. Two communication-based impedance-based protection schemes were developed. the first scheme utilizes directional elements and pilot signals to locate the fault. The second scheme depends on a Central Protection Unit that communicates with all feeder relays to locate the fault based on directional flags received from feeder relays. The later approach could potentially be adapted to protect networked microgrids and dynamic topology microgrids. Transient-based protection relies on analyzing high frequency transients to detect and locate faults. This approach is very promising but its implementation in the filed faces several challenges. For example, high frequency transients due to faults can be confused with transients due to other events such as capacitor switching. Additionally, while detecting faults by analyzing transients could be doable, locating faults based on analyzing transients is still an open question.

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Executive Summary

Microgrids continue to be an important tool to improve power grid resilience and reliability. As such, and as the size of microgrids continues to grow, it is becoming crucial to develop efficient protection schemes to selectively clear faults within the microgrid by tripping the least possible part and avoid collapsing the whole microgrid for all internal or external faults. Microgrids with significant inverter-interfaced generation are particularly challenging since fault currents could be very limited and traditional overcurrent protection could fail completely to pick up the fault in the first place. Development of efficient non-overcurrent based protection schemes is a prerequisite for significantly increasing the penetration of renewable generation in microgrids. Currently, lack of efficient protection schemes is impeding the deployment of networked microgrids and other advanced DS operation functions such as splitting distribution systems (DS) into microgrids and automatic reconfiguration. More broadly, as the penetration of inverter-interfaced DERs increases in the distribution system, existing overcurrent protection schemes will fail to work efficiently. Therefore, developing efficient microgrid protection schemes will also be beneficial for protecting distribution systems with very high penetration of inverter-interfaced.

The overall objective of this project is to investigate the challenges facing efficient microgrid protection design and to develop protection schemes for variety of microgrid configurations including radial, mesh and dynamic topology microgrids. A detailed literature survey of existing and proposed microgrid protection schemes concluded that there is a gap in the available microgrid protection methods. The only credible protection solution available in literature for low-fault inverter-dominated microgrids is the differential protection scheme which represents a robust transmission-grade protection solution but at a very high cost. Therefore, there is a need to develop microgrid-specific protection schemes which are non-overcurrent based to ensure efficient operation for low-fault microgrids but also are not element-based to minimize the associated cost and ensure applicability in the field. Based on this conclusion, two non-overcurrent protection schemes were investigated as part of this project; impedance-based protection and transient-based protection.

1 Introduction

Since the introduction of the microgrid concept in [4], it was realized that designing efficient protection schemes for microgrids would be challenging and would require advancing the state of the art of protective relaying. The main challenge facing the development of *standardized* microgrid protection originates from the fact that microgrids differ in their topology, generation mix, feeder sizes and fault interruption devices types and locations. Additionally, microgrids could have radial or meshed topologies.

Even for the relatively simple case of radial microgrids, the design of protection schemes could be challenging for multiple reasons. First, fault current levels could change drastically between grid-connected and islanded modes of operation which makes it very difficult, or even impossible, to maintain overcurrent protection coordination in both cases. Second, in the islanded mode of operation, fault currents could change significantly with generation dispatch which complicates protection coordination design. Third, for microgrids with significant inverter-interfaced generation, renewable generation for example, fault currents could be very limited as a result of inverter current-limiting protection functions which typically limit fault contribution in sub-cycle time frame to as low as 1.1 per unit. For this particular case, overcurrent protection could fail completely to pick up the fault in the first place.

In addition to the above challenges, meshed microgrids represent another altitude of problems for efficient protection system design. From one side, distribution-grade overcurrent protection schemes are not suitable for meshed microgrids since overcurrent protection coordination is very hard to attain. On the other side, using transmission-grade protection schemes would require significant investments in installing fault interrupting devices on each feeder segment of the microgrid and that is not typically justified based on the amount of load served by the microgrid.

Development of efficient non-overcurrent based protection schemes is a prerequisite for significantly increasing the penetration of renewable generation in microgrids. Currently, lack of efficient protection schemes is impeding the deployment of networked microgrids and other advanced DS operation functions such as splitting distribution systems (DS) into microgrids and automatic reconfiguration. More broadly, as the penetration of inverter-interfaced DERs increases in the distribution system, existing overcurrent protection schemes will fail to work efficiently. Therefore, developing efficient microgrid protection schemes will also be beneficial for protecting distribution systems with very high penetration of inverter-interfaced.
The goal of this project is to study protection schemes for inverter-dominated microgrids. A detailed literature survey of existing and proposed microgrid protection schemes were conducted. The survey concluded that there is a gap in the available microgrid protection methods. The only credible protection solution available in literature for low-fault inverter-dominated microgrids is the differential protection scheme which represents a robust transmission-grade protection solution but at a very high cost. Therefore, there is a need to develop microgrid-specific protection schemes which are non-overcurrent based to ensure efficient operation for low-fault microgrids but also are not element-based to minimize the associated cost and ensure applicability in the field. Based on this conclusion, two non-

overcurrent protection schemes were investigated as part of this project; impedance-based protection and transient-based protection.

In this project we showed that a potential solution for detecting faults in low-fault microgrids is monitoring impedance trajectories at feeder relays instead of monitoring the current. Two communication-based impedance-based protection schemes were developed. the first scheme utilizes directional elements and pilot signals to locate the fault. The second scheme depends on a Central Protection Unit that communicates with all feeder relays to locate the fault based on directional flags received from feeder relays. The later approach could potentially be adapted to protect networked microgrids and dynamic topology microgrids.

Transient-based protection relies on analyzing high frequency transients to detect and locate faults. This approach is very promising but its implementation in the filed faces several challenges. For example, high frequency transients due to faults can be confused with transients due to other events such as capacitor switching. Additionally, while detecting faults by analyzing transients could be doable, locating faults based on analyzing transients is still an open question.

2 Microgrid Protection Literature Survey

2.1 Literature Survey

Since the introduction of the microgrid concept in [4], it was realized that designing efficient protection schemes for microgrids would be challenging and would require advancing the state of the art of protective relaying. The main challenge facing the development of standardized microgrid protection originates from the fact that microgrids differ in their topology, generation mix, feeder sizes and fault interruption devices types and locations. Extensive research has been directed toward designing efficient protection schemes for microgrids.
Adaptive overcurrent protection schemes were discussed in several works such as [5, 6, 7]. These schemes consist of a central protection unit that communicates with all feeder relays and all DGs. By continually monitoring the status of all DGs and their potential fault current contributions, the central protection unit could run relay coordination studies online and update the settings of all feeder relays to adjust to the real-time conditions, including mode of operation, of the microgrid. Fig. 1 shows a conceptual diagram for the adaptive overcurrent protection concept. Adaptive overcurrent protection could provide a suitable protection solution for microgrids in islanded and grid-connected modes of operation. However, application of adaptive overcurrent protection schemes for inverter-dominated microgrids is very challenging since fault currents could be too limited to be picked up by overcurrent protection in the first place particularly in the islanded mode of operation.

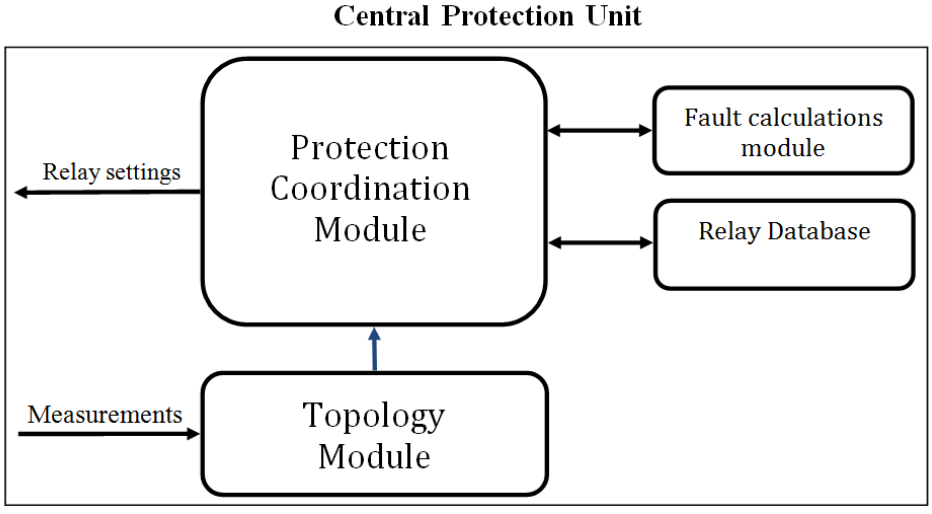


Figure 1: Conceptual representation of a microgrid central protection unit

Several non-overcurrent protection schemes were introduced for inverter-dominated low fault current microgrids. A voltage based protection schemes was discussed in [8]. The method is based on the fact that during faults, voltage levels dips across the microgrid. However, discriminating between faults and other normal-operation events based on voltage levels, such as capacitor tripping, is hard to achieve. Additionally, in a typical microgrid, the magnitude of voltage dip during faults would be the same in different locations due to small feeder lengths; therefore, determining fault location based on voltage magnitude

could be very difficult. Reference [9] used voltage-based protection in combination with directional elements to develop protection scheme for low fault low voltage radial microgrids. Communication-assisted voltage-based protection for radial medium-voltage microgrids was proposed in [10].

A differential protection scheme for low-fault microgrids was proposed in [1]. That scheme is based on installing fault interrupting devices and differential relays at both ends of each feeder segment of the microgrid. Additionally, the scheme requires communication channel for each protection zone and it rely on synchronized measurement of currents at both ends of each line segment. Fig. 2 shows a depiction of the differential protection scheme proposed in [1]. That scheme could clearly provide a robust protection solution for low-fault microgrids in both modes of operation. However, the cost of such scheme could be prohibitively high given two breakers must be installed at both ends of each microgrid feeder segment. Therefore, unless the particular application of a microgrid justify the cost, it is hard to see that scheme used widely for typical microgrids. A differential-based sequence component protection scheme was proposed in [11] which assumes protection zone granularity similar to [1] but it requires more processing time and more extensive communication infrastructure without any improvement in protection robustness.

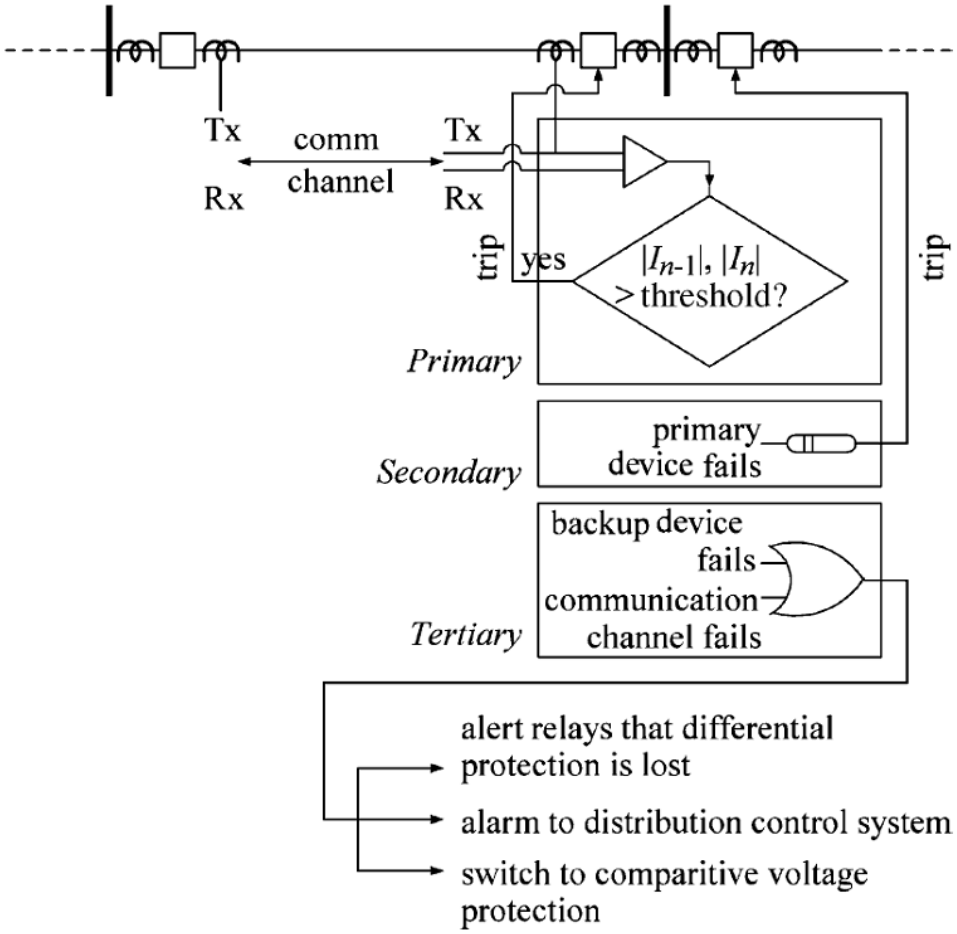


Figure 2: Conceptual representation of the differential scheme for microgrids [1].

The application of traditional distance protection for microgrids, and generally for distribution systems, was discussed in [12]. However, distance protection is not typically efficient when applied to tapped feeders since it will cause the relay to underreach and thus complicates coordination between different relays.
Several protection methods based on transient behaviour of faults was discussed in literature. In [13], a travelling wave based protection scheme was presented. The scheme is based on measuring timing and polarity of the initial waves at both side of the protected line after the occurrence of the fault. It is not clear what is the triggering event which the relays will use to start measuring the incident wave travelling time. Additionally, for a typical microgrid it is very hard to discriminate between incident waves travelling timing to different locations due to the relatively small feeders lengths compared with travelling waves speed. Moreover, the method require protection zone granularity similar to differential protection proposed in [1], however, differential protection is way more robust. Protection schemes based on wavelet analysis of fault currents was presented in [14] and [15]. These papers only discussed faults at the terminals of DGs and there is no discussion about how the scheme will detect feeder faults midway between DGs. Additionally, as for other transient based methods, there is no general proof that the transient signature used in the proposed protection is universal and does not depend on the microgrid configuration or generation dispatch.

On the other hand, dynamic topology microgrids, sometimes also called networked microgrids, represent a new paradigm for microgrid and distribution systems operation [16]. By allowing the dynamic formation of microgrids in real-time based on actual system conditions and load generation balancing, dynamic topology microgrids could significantly improve the self-healing capability of the system especially after major disturbances which would result in enhanced system resilience [17] [18]. However, the development of suitable protection systems for networked microgrids is a prerequisite for its widespread applications. Changing the topology of microgrid in real-time represent a major challenge for the design of microgrid protection systems.

2.2 Conclusions

Based on the literature survey, it is clear that the main protection solutions available for microgrids are overcurrent-based protection and differential protection. While overcurrent protection is relatively inexpensive and is widely available in the distribution system, it is not particularly suitable for low-fault renewable-rich microgrids. On the other hand, differential protection provides a very robust protection solution but at a very high cost which could be prohibitively expensive for many microgrids applications. Therefore, there is a need to fill the gap between low-cost low-reliability schemes like overcurrent protection and high-cost high reliability schemes like differential protection. This approach is depicted in Fig 3

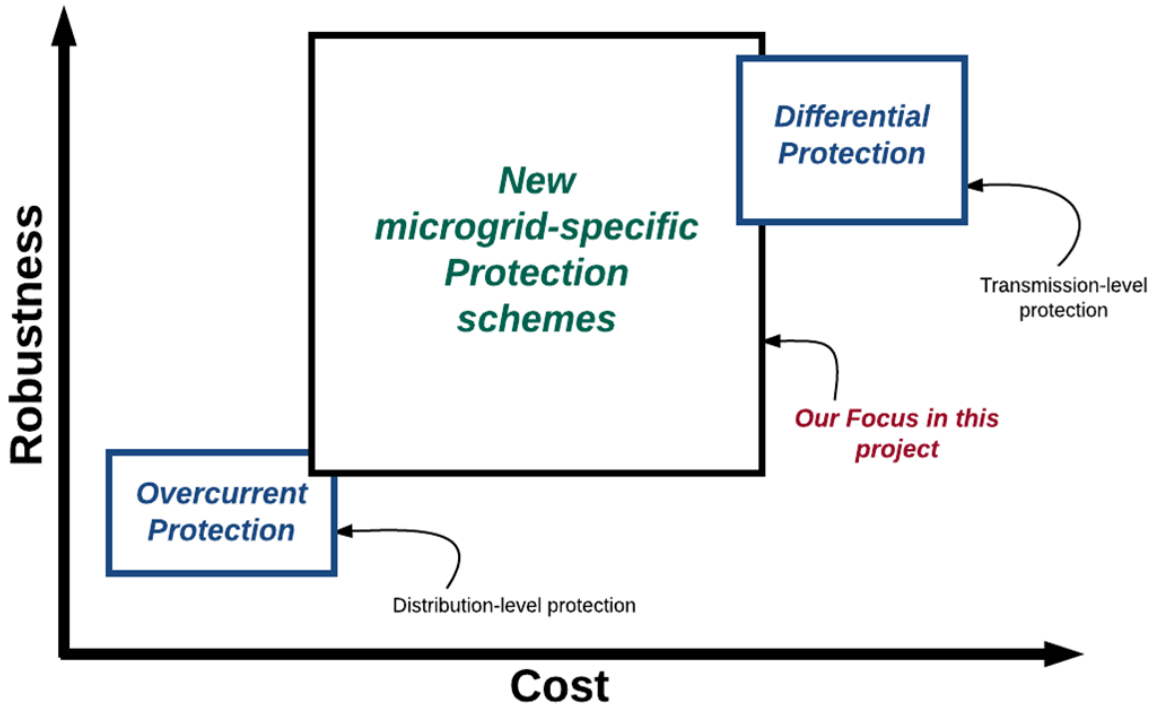


Figure 3: Microgrid Protection Gap

3 Impedance-based Protection Scheme for Inverter-dominated Microgrids

In this section, we will discuss impedance-based protection as an alternative to overcurrent protection for low-fault inverter-dominated microgrids.

3.1 General Microgrid Protection Zones

In order to design a rather general protection scheme for Microgrids that does not depend on locations of fault interrupting devices, we define microgrid protection zones as: *a part of the microgrid bordered by a set of fault interrupting devices*. Figure 4 shows examples of microgrid protection zones. If a fault was to occur in a certain protection zone, the *least disruptive way* to clear the fault would be to open all fault interrupting devices surrounding that particular zone - we will call them the *set of fault interrupting devices of that particular zone*. In other words, for protection purposes any microgrid could be split into a group of protection zones and there is a one-to-one mapping that maps every protection zone to a unique set of fault interrupting devices.

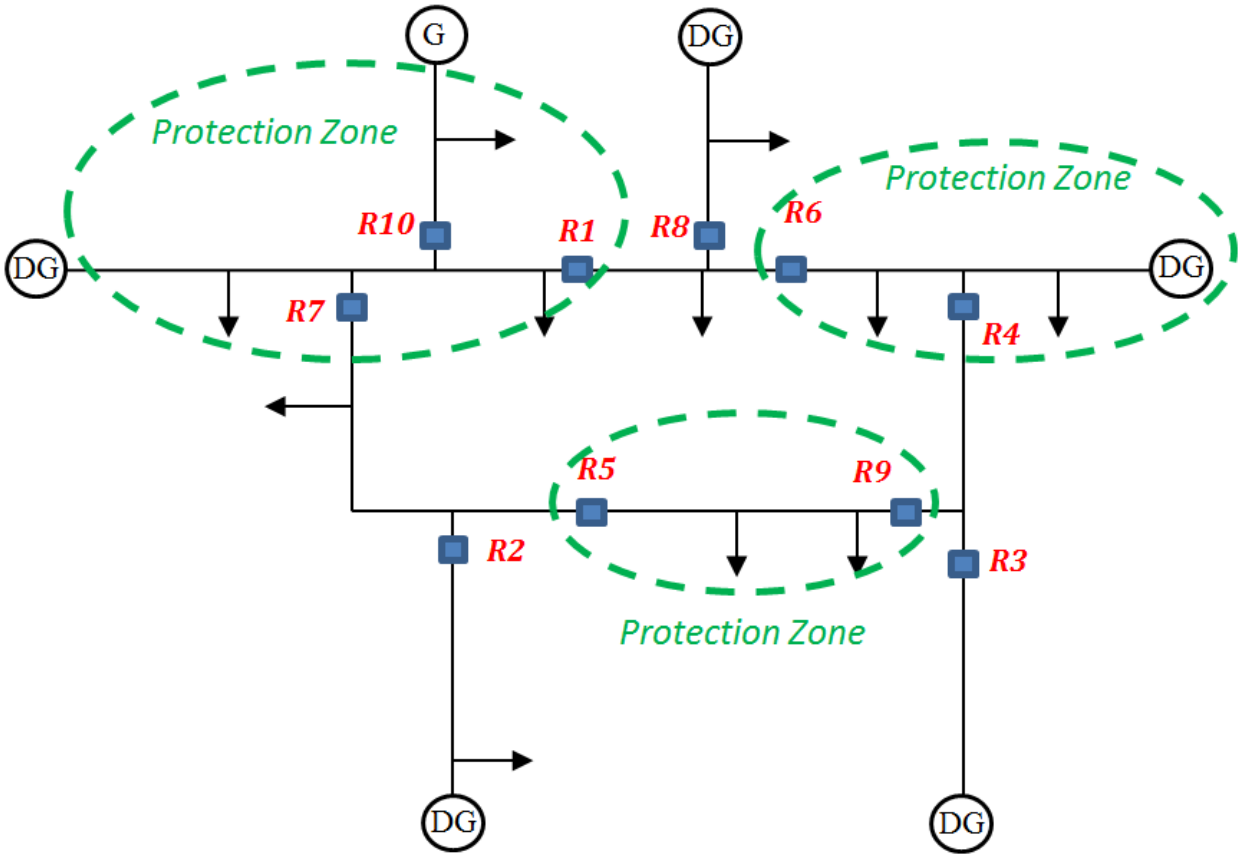


Figure 4: General Microgrid Protection Zones

Formally, let ZO_i be a zone of a microgrid, then there exist a mapping $\mathcal{M}(ZO_i)$ such

that:

$$\mathcal{M}(ZO_i) = S_i \tag{1}$$

where S_i is a set containing fault interrupting devices of ZO_i. This mapping is easily constructed from the topology of the microgrid and could be updated to reflect dynamic topology as will be discussed in section 3.3.2. Additionally, each fault interrupting device is a member of *at most* two sets of fault interrupting devices associated with two different protection zones. However, if we define a direction variable $d_j \in \{0, 1\}$ for every fault interrupting device j, then we could define a one-to-one mapping $\mathcal{T}(ZO_i)$ such that:

$$\mathcal{T}(j, d_j) = S_i \tag{2}$$

Again this mapping could be constructed from the topology of the microgrid and could be updated to reflect the dynamic topology. The direction variable d_j could be assigned arbitrarily to distinguish between the two protection zones; 0 for forward zones and 1 for backward zone. The actual realization of the direction variable d_j in real-time will be determined based on a directional element in the relay as will be discussed in section 3.3.

3.2 Inverter-dominated Microgrids fault detection

It is important to notice that the low fault current contribution of inverters is mainly due to the inverter controller actions and not because of network impedance. As a matter of fact, the impedance of the microgrid, as defined by the impedance bus matrix for instance, would change due to the presence of the fault regardless of the attributes of the electrical source. However, the presence of the fault would not result in high fault current from the inverter-interfaced source, the way it typically would for a conventional source, due to the control actions of the inverter. As a result, the voltage at the terminals of the inverter would typically decrease more than it would for a conventional source. Based on that, a better way to detect faults in low-fault microgrids is by monitoring impedance changes instead of current changes. In this section we will develop impedance-based protection schemes to detect faults by monitoring impedance changes at different locations in the microgrid. During design stage, short circuit studies would be conducted to determine impedance threshold values that indicates faults for different feeder relays. A fault is declared by a relay whenever its measured impedance falls below its impedance threshold value.

3.3 Impedance-based Microgrid Protection schemes

Although monitoring the change in impedance could be a reliable way to detect the occurrence of faults in low-fault microgrids, locating faults can be more complicated depending on the microgrid particulars. From one hand, feeder lengths of typical microgrids are relatively small, thus the impedance seen by different relays, not necessarily only the closest relay to the fault, could drop below their threshold values. Moreover, since microgrids come in different configurations, have tapped feeders and with no standard locations for fault interrupting devices, it is hard to use traditional distance protection to coordinate between impedance-relays based on their measured impedance values.
For those microgrids where coordination between impedance relays based on the measured

impedance is not feasible for the above mentioned reasons, we propose the use of communication-assisted directional elements in conjunction with impedance-elements to reliably detect and locate faults in low-fault inverter-dominated microgrids. Two communication-assisted impedance-based protection schemes are described in this section:

1. Impedance-based Pilot Protection Scheme.
2. Impedance-based Central Protection Scheme.

3.3.1 Impedance-based Pilot Protection Scheme

This protection scheme is based on communication between adjacent relays, or in general between relays of the same protection zone, to locate the fault. Each feeder relay will be equipped with an impedance element to detect fault occurrence and a directional element to determine the direction of the fault. Different pilot protection logic could be used to determine the location of the fault. For example, a pilot protection logic based on permissive and blocking signals could be implemented as follows:

1. Any relay that detects a fault will:
    - send a block signal to its reverse zone breakers.
    - send a permissive signal to its forward zone breaker.
2. Any relay that receives a permissive signal will:
    - if it has detected a fault and the signal is from one of its reverse zone breakers, ignore the signal.
    - if it has detected a fault and the signal is from one of its forward zone breakers, issue a trip signal to the breaker (fault is located in the forward zone).
    - if it has not detected, send back a permissive signal and issue a trip signal to the breaker (fault is located in the zone shared by the breaker which sent the original permissive signal).

In essence, the criteria for tripping is the fulfilment of one of the following two conditions:

1. Fault detection no blocking signal and, optionally, receiving permissive signal.
2. No fault detection, no blocking signal and receiving a permissive signal.

Note that in the above pilot protection logic, the blocking signal increase the security of the scheme but it could also work well based on permissive signals only.
To illustrate the basic operation of the proposed scheme, consider Fig 5. Assume a fault occurred on the line segment between $B1$ and $B2$. Additionally, assume that impedance-elements at all three relays ,$B1, B2$ and $B3$, detected a drop in their measured impedances below the detection threshold and thus declared a fault. Directional elements of the three relays will identify the direction of the fault as shown in Fig 5.

Based on the pilot protection logic mentioned above, relay $B1$ will send a permissive signal to relay $B2$ and a block signal to its reverse zone relays (not shown in Fig 5), relay

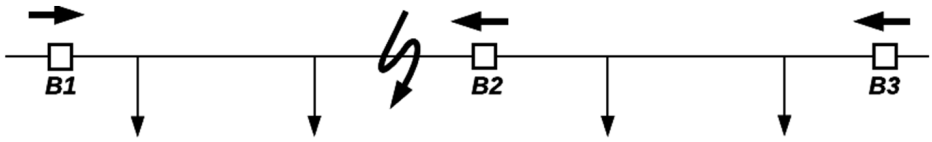


Figure 5: Impedance-based pilot protection scheme illustration

$B2$ will send a permissive signal to relay $B1$ and a blocking signal to relay $B3$ and, similarly, relay $B3$ will send a permissive signal to relay $B2$ and a block signal to its reverse zone relays (not shown in Fig 5). As a result, relays $B1$ and $B2$, having detected the fault and received permissive signals, will trip their associated breakers to clear the fault.

In general, all relays of the same protection zone will have to be able to communicate with each other. For example, for the part of the microgrid depicted in Fig 6, assume that $B7$ was the only relay that detected the fault $F1$ based on drop of the measured impedance at $B7$. According to the above pilot logic, $B7$ should send permissive signals to $B1, B2, B4$ and $B8$. This task could be achieved based on peer communication by sending the permissive signal from $B7$ to $B2$ and requesting that $B2$ transfer the permissive signal to $B4$ and so on. It is important to notice, however, that while microgrid configurations like the one depicted in Fig 6 is quite complicated from protection perspective, they are rather uncommon in practice today.

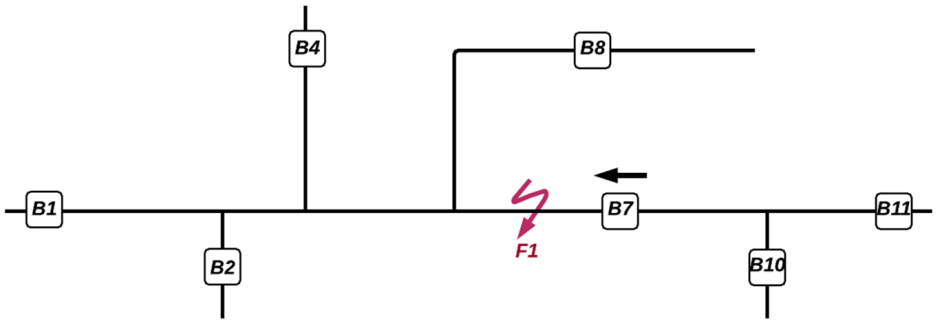


Figure 6: Impedance-based pilot protection scheme illustration

3.3.2 Impedance-based Central Protection Scheme

The pilot protection scheme presented in section 3.3.1 is suitable for use for fixed topology microgrids. As the topology of the microgrid change there would be a need to adjust the pilot protection scheme by redefining the protection zones and potentially reprogram communication channels. To overcome this issue for dynamic topology microgrids, also called networked microgrids, a protection system based on a central protection unit is proposed in this section. The proposed scheme is based on two main steps:

1. Determine the faulty zone based on directional elements readings of feeder relays which detected the fault.

2. Trip all fault interrupting devices of the identified faulty zone.

In this scheme, all feeder relays communicate with a Central Protection Unit (CPU). Upon detecting a drop of impedance below a certain threshold, a feeder relay will send a fault flag to the CPU along with direction flag indicating whether the fault was detected in the forward or reverse zones.

The CPU represents the heart of the proposed protection scheme and is responsible for:

1. Process any topology change in the microgrid and update the mappings, $\mathcal{M}(ZO_i)$ and $\mathcal{T}(j, d_j)$ as discussed in section 3.1, equations 1 and 2.

2. Communicate with feeder relays to receive fault and direction flags.

3. Process the received fault and direction flags and use the protection zones mappings to locate the faulty zone.

4. Issue tripping signals to fault interrupting device of the faulty zone to clear the fault.

Fig. 7 shows a functional diagram for the proposed CPU.

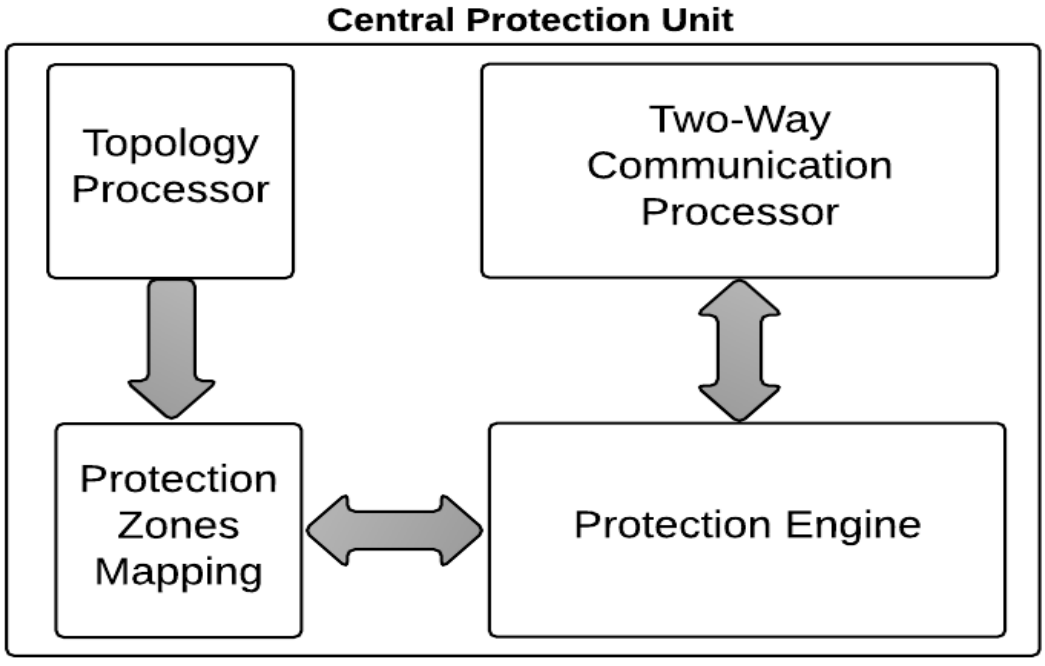


Figure 7: Proposed Central Protection Unit for Dynamic Topology Microgrid

The topology processor is responsible for tracking any topology change in the microgrid. This could be done manually by having the operator who execute the reconfiguration of the microgrid update the topology in the CPU as well. Alternatively, in a fully automated

microgrid, signals received from automatic switches could be used to update the topology automatically in the CPU. Topology processor would only be required for the protection of dynamic topology microgrid. There are several ways to implement the fault interrupting devices mappings. One way is to use lookup tables in the CPU. For example, for the microgrid depicted in Fig 8, the mappings $\mathcal{M}(ZO_i)$ and $\mathcal{T}(j, d_j)$ are represented by Tables 1 and 2. Automatic updating of the mapping tables could be achieved by utilizing input from the topology processor.

Once the CPU receives fault and direction flags from at least one feeder relay, a fault is declared. Then, the CPU will process the received flags to determine the faulty zone. The faulty zone will be *the one and only one zone in the microgrid where all of its fault interrupting devices either declare a fault in its direction or does not detect the fault at all.* Ultimately, the CPU will issue tripping signals to fault interrupting devices of the faulty protection zone.

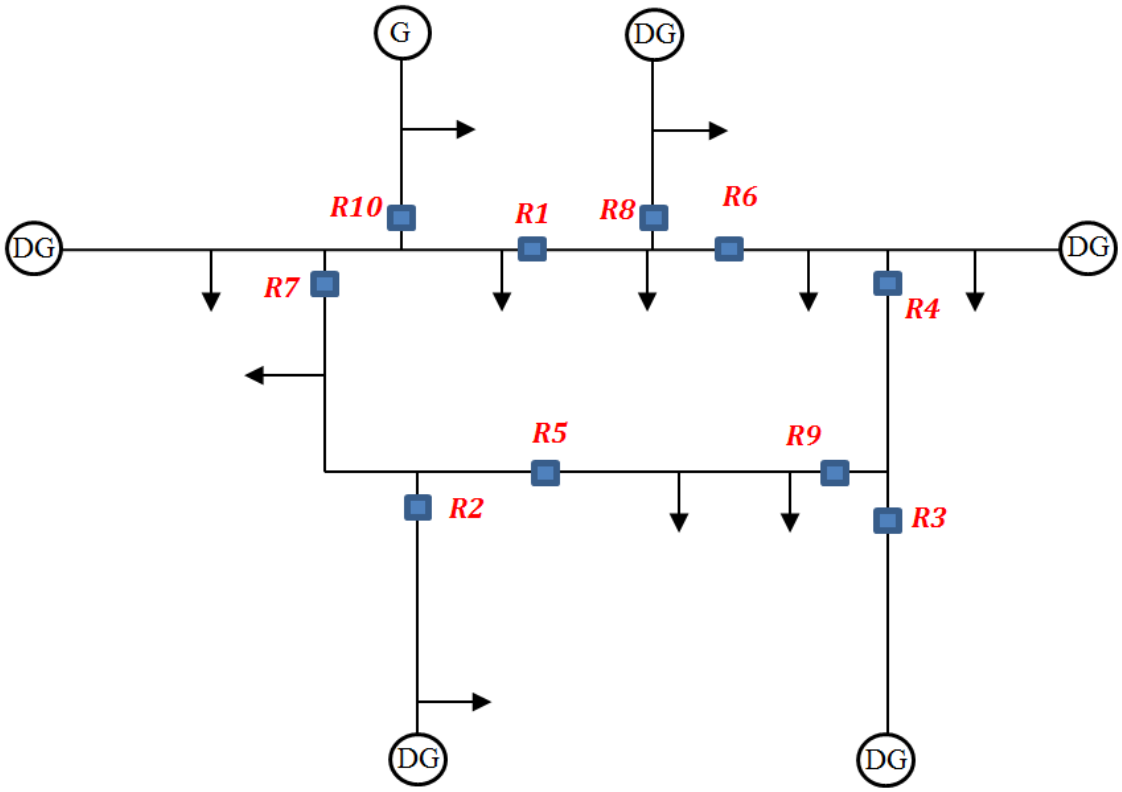


Figure 8: A General Topology Microgrid

Table 1: Lookup Table implementation for mapping $\mathcal{M}(ZO_i)$

Protection Zone	**Fault Interrupting Devices Set**
1	$\{R1,R7,R10\}$
2	$\{R2,R5,R7\}$
3	$\{R5,R9\}$
4	$\{R3,R4,R9\}$
5	$\{R1,R6,R8\}$
6	$\{R4,R6\}$

Table 2: Lookup Table implementation for mapping $\mathcal{T}(j, d_j)$

Fault Interrupting Device	**Direction Flag**	**Protection Zone**
R1	0	1
R1	1	5
R2	0	2
R3	0	4
R4	0	4
R4	1	6
R5	0	2
R5	1	3
R6	0	5
R6	1	6
R7	0	1
R7	1	2
R8	0	5
R9	0	3
R9	1	4
R10	0	1

3.4 Impedance-based Protection Implementation Issues

In this section we will discuss different aspects related to the implementation of the proposed protection scheme, namely, Impedance Relays design, role of communications, fault interruption speed and weak infeed issues.

3.4.1 Feeder Impedance Relays

Each fault interrupting device in the protected microgrid is assumed to be equipped with an impedance relay. The vast literature and extensive existing experience in designing distance relays for transmission systems could be utilized in designing the proposed impedance relay. In the particular design implemented in this study, we assume that the impedance relay is composed of three impedance elements for phase faults and three impedance elements for ground faults. The three phase relays are configured using delta-connected PTs and delta-connected CTs [2]. The three ground relays are configured based on the residual compensation scheme as shown in Fig.9 and the turns ratio is given by:

$$\frac{N_2}{N_1} = \frac{1}{3}(\frac{Z_{L0}}{Z_{L1}} - 1) \tag{3}$$

where Z_{L0} and Z_{L1} are the zero and positive sequence impedance of the protected feeder, respectively. Note that, unlike traditional transmission distance relays, the proposed scheme does not depend on the value of the measured impedance as a basis for coordination between relays. Therefore, accurate measurements of the impedance between the relay and the fault is not crucial for the success of the proposed protection scheme.

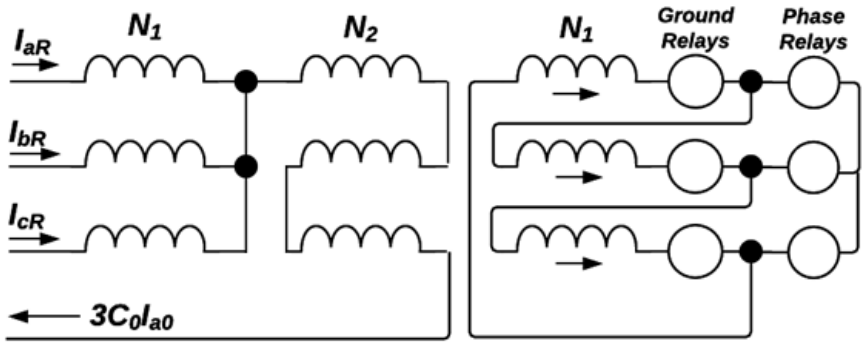


Figure 9: Residual Compensation scheme for ground impedance elements and the delta connection for phase elements CTs, [2]

Additionally, each fault interrupting device in the protected microgrid is assumed to be equipped with a directional element. Again, the particular design of the directional element does not impact the proposed protection scheme and therefore any directional element design could be used based on the particulars of the protected microgrid [19]. For this study we have used a simple directional element utilizing line voltages as the polarizing quantity for phase relays and zero sequence voltage, as obtained from an open-delta scheme, as polarizing quantity for ground relays. During design stage, impedance threshold value will be determined

for each feeder impedance relay based on short circuit studies. During operation, a relay will declare a fault if its measured impedance is less than its impedance threshold value.

3.4.2 Communications

Communication is needed only if coordination between impedance elements is deemed not possible based on the measured impedance values as discussed in 3.3. However, only low bandwidth communications is required since only permissive and blocking signals will be transferred between relays in the pilot scheme and only fault and direction flags are required to be communicated in the central unit protection scheme. The proposed scheme could be designed to "peggy-back" on any communication infrastructure that already exist in the microgrid. Unlike the schemes described in [1, 10, 13], the proposed impedance-based protection schemes does not require relay measurements to be synchronized regardless of the distances between relays and the Central Protection Unit.

3.4.3 Fault Interruption Speed

One of the concerns for any communication-assisted protection scheme is the speed of fault interruption. Even though the two proposed communication-assisted protection schemes are instantaneous, they relies on receiving signals over communication channels. Therefore, there is an inherent time delay in fault clearing. However, given the small distances of a typical microgrid, excessive time delays during communications is not likely. Additionally, for fault current levels expected in inverter-dominated microgrids, even an inverse-time overcurrent relay, if it at all detects the fault, would take few cycles to pick up. Ultimately, the trade-off between cost and reliability, in terms of speed of fault interruption, should determine the communication medium to be used to implement the proposed schemes. Alternatively, the proposed schemes could be implemented as a backup protection for traditional overcurrent protection. In that case, the overcurrent protection would provide fast fault interruption during grid-connected mode of operation and the proposed impedance-based scheme would protect against low fault current situations.

3.4.4 Weak Infeed Issues

The weak infeed problem is a well-known issue in transmission distance protection literature [20]. This problem could happen when there is no fault current source behind the distance relay or even in some cases when the fault current source behind the distance relay is so weak to supply sufficient fault current to operate the relay or to activate overcurrent starting scheme for some types of switched distance relays [21]. Weak infeed was particularly problematic for electromechanical relays where a minimum current is needed to produce enough torque to operate the relay. The widespread use of numerical and microprocessor based relays with high sensitivity for current measurement has to a good extend diminished the severity of the weak infeed problem for the case of weak sources. Different pilot based schemes are typically used to overcome the weak infeed problem in transmission protection particulary for the case of open generator breaker behind the relay. Implementation of the proposed impedance-based schemes using numerical relays should largely provide immunity against weak infeed issues for the islanded mode of operation.

The case of a fault on the grid during grid-connected mode should be carefully considered. For a very weak microgrid connected to a relatively strong distribution feeder, the fault current contribution from the microgrid could be difficult to detect. That case could be covered by an undervoltage element combined with a directional element at the PCC of the microgrid or by a transfer trip signal from the utility breaker.

3.5 Simulation Results

The proposed impedance-based protection schemes were tested on two microgrids with different topologies: a radial microgrid based on an actual microgrid design and a hypothetical meshed microgrid. MATLAB/SimPowerSystems was used to run all time-domain simulations. Inverter-interfaced generators are modelled as current-controlled inverters with a real/reactive-power control outer loop in the $dq-$frame. Inverters are modelled using averaged three phase voltage-source converter models as depicted in Fig. 10, see [3] for modelling details.

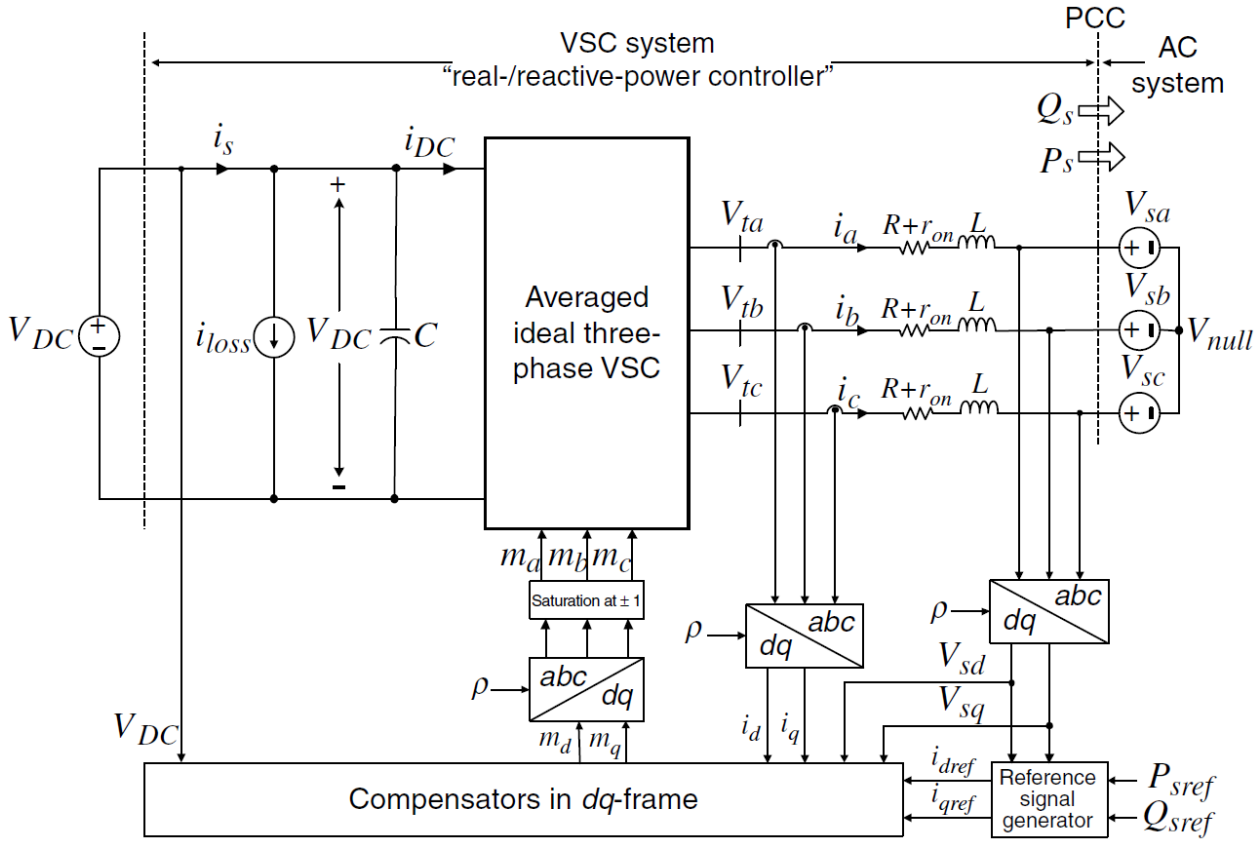


Figure 10: Inverter and controller modelling [3]

3.5.1 *Case* 1: Radial Microgrid

For this case, the proposed protection scheme was tested on the radial microgrid shown in Fig. 11 [22]. Feeders are modelled using 336ACSR with positive sequence impedance of $0.27974+j0.6388\ \Omega/mile$ and zero sequence impedance of $0.57118+j1.80198\ \Omega/mile$. Feeder lengths are shown in Fig. 11. Impedance relays are designed as discussed in section 3.4.1. Fault detection impedance threshold for all relays is set as a circle centered at the origin with a radius of 10 Ω. This circle is shown on the impedance trajectory plots for reference.
Four fault scenarios are presented in this section. For each scenario, a fault is applied at $t = 0.3sec$ and removed at $t = 0.45sec$. Fig. 12 shows the impedances measured by different relays prior to applying any fault to the microgrid.
Impedance trajectories for fault $F1$, are shown in Fig. 13. It is clear from these figures that relays $R2, R3$ and $R4$ detected the fault. For this particular microgrid, $R2$ is designed such that it will trip for any fault in its downstream zone since that is the only zone downstream of $R2$. Following the pilot protection logic of section 3.3.1, $R3$ and $R4$ would have to wait for a permissive signal before tripping. However, since in this particular case the fault will be cleared by $R2$ instantaneously, $R3$ and $R4$ will see there impedance trajectory change and their fault detection flags will reset automatically and hence no communication is needed. Simulation results for faults $F2$ and $F3$ are shown in Figs. 14 and 15. These two faults are cleared by relays $R1$ and $R3$ respectively in a similar fashion as $F1$ was cleared by $R2$ without a need for communications.

Fault $F4$ was simulated with the microgrid operating in grid-connected and islanded modes of operation. Figure 16 and 17 show the impedance trajectories for both cases. It is clear from these figures that all relays have detected the fault in both modes of operation, except obviously $R4$ in the islanded mode. For this fault, by following the pilot protection logic of section 3.3.1, all the four relays will eventually receive permissive signals and trip to clear the fault.

It is also interesting to notice that, fault $F4$ could be cleared if all relays are programmed to trip after a suitable delay if the fault could still be detected. The intentional delay will, for example, prevent $R3$ and $R4$ from tripping for $F1$ to allow $R2$ to clear the fault. Thus an intentional delay could provide a suitable way to discriminate between faults for this particular microgrid. As a result, for this particular microgrid, all faults could be cleared without the need for communications. In conclusion, while communications is needed in general to implement the impedance-based protection scheme, there are cases where good coordination between relays could be achieved without the need for communications based on the particular design of the microgrid under study.

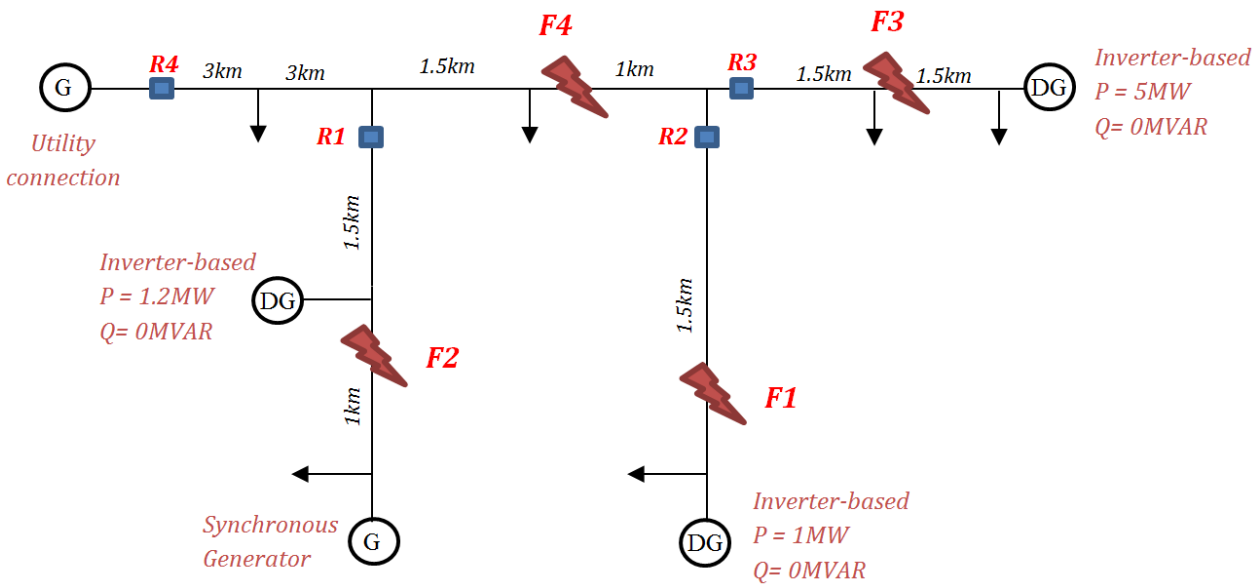


Figure 11: Microgrid used for $Case1$ study

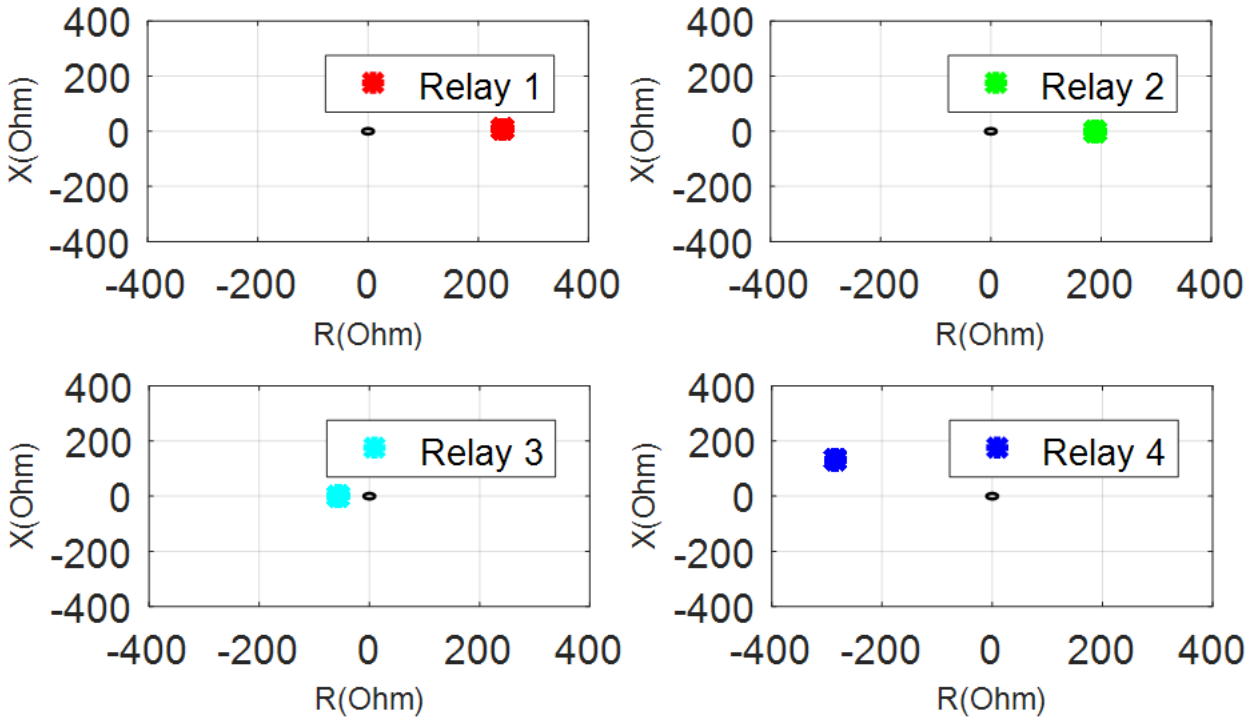


Figure 12: Impedance measured by all relays prior to applying any fault

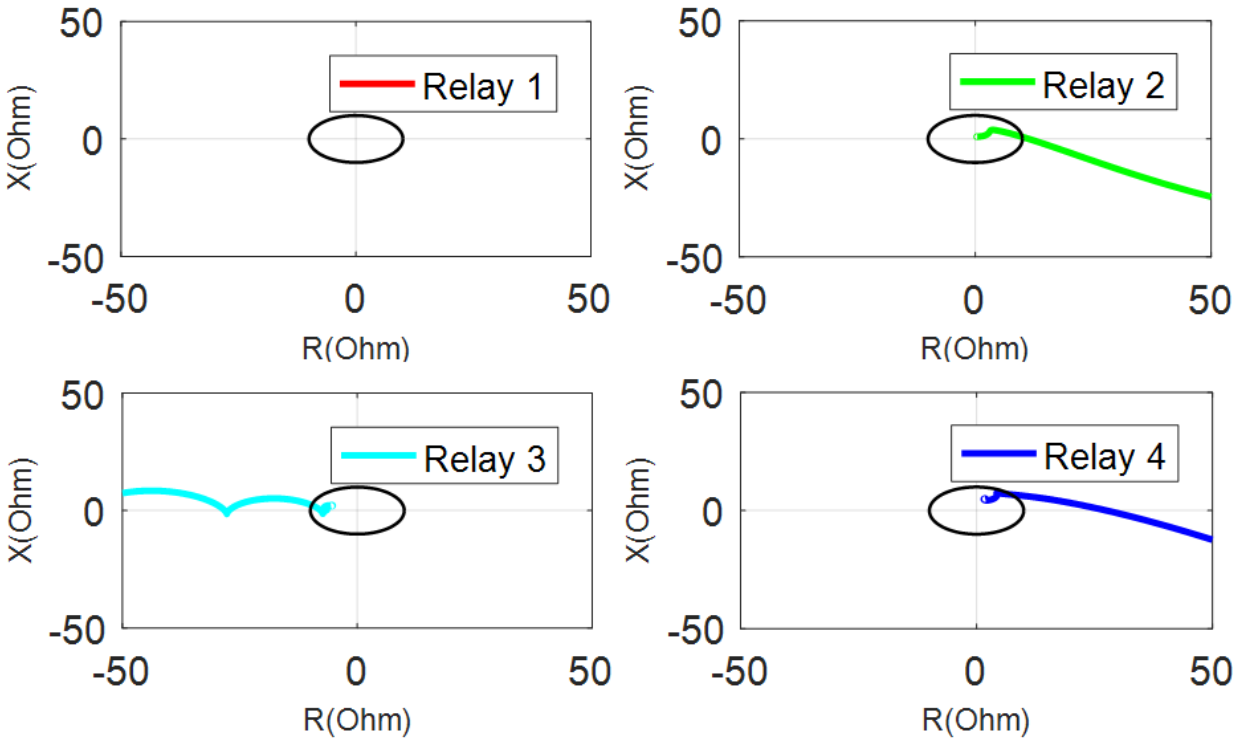


Figure 13: Impedance trajectories during a three phase to ground fault at $F1$

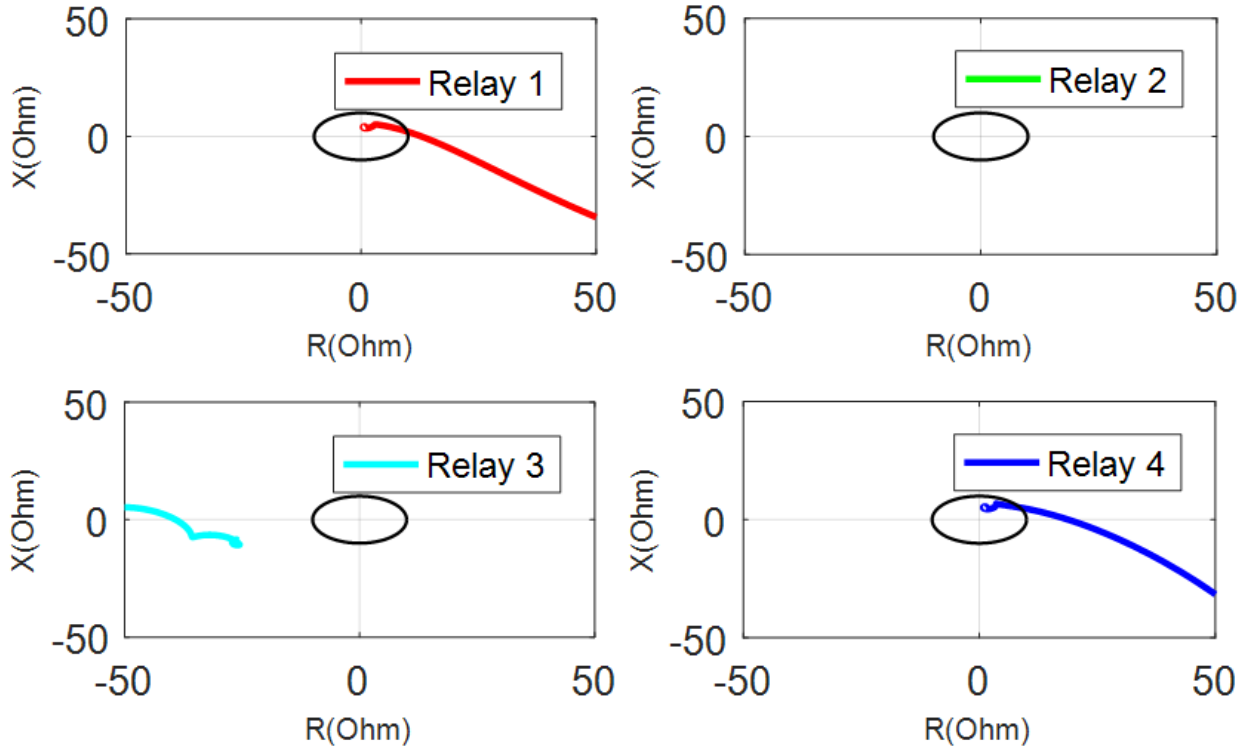


Figure 14: Impedance trajectories during a phase A to ground fault at $F2$

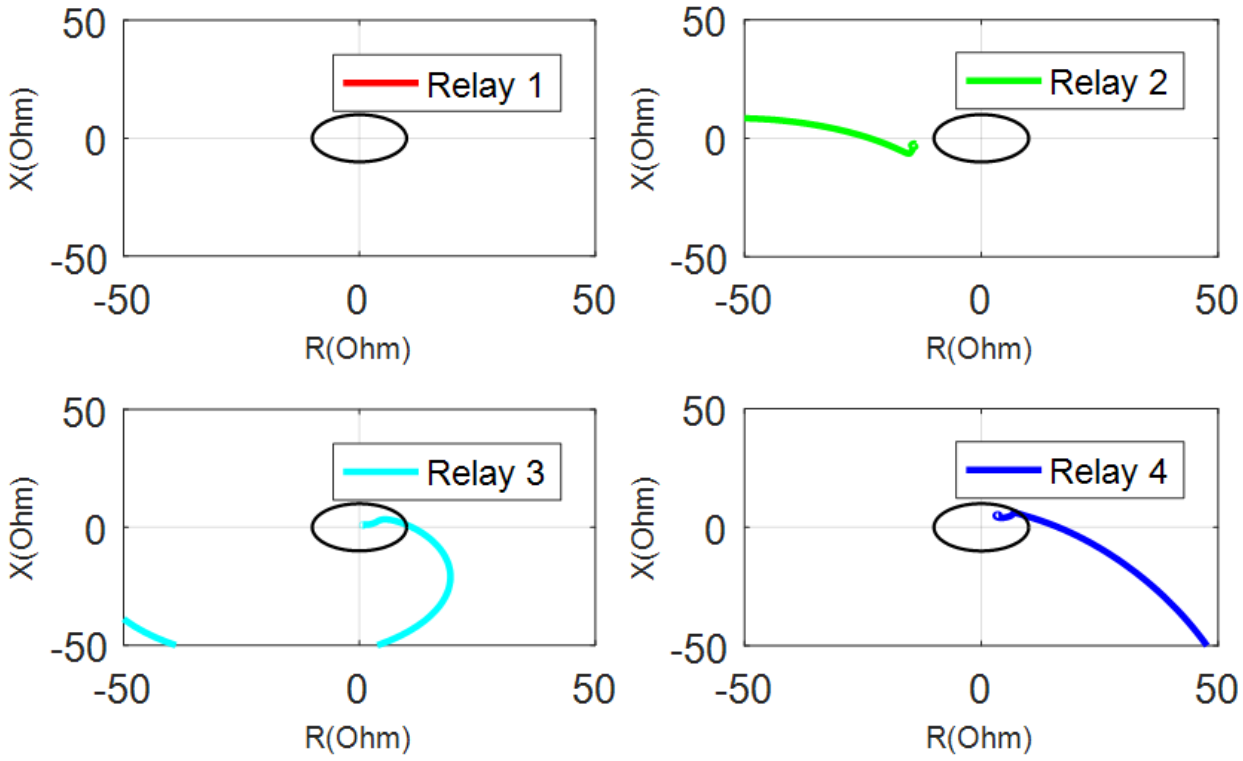


Figure 15: Impedance trajectories during a phase A to B to ground fault at $F3$

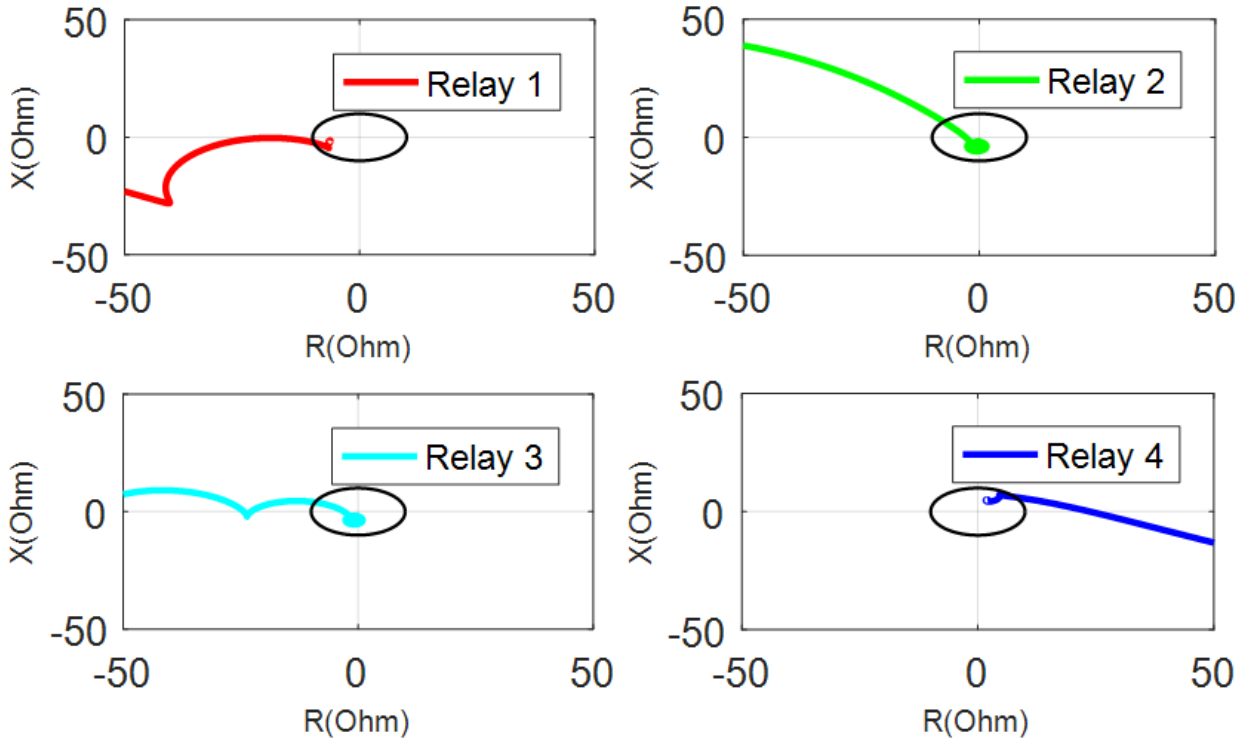


Figure 16: Impedance trajectories during a three phase to ground fault at $F4$ under grid-connected mode of operation

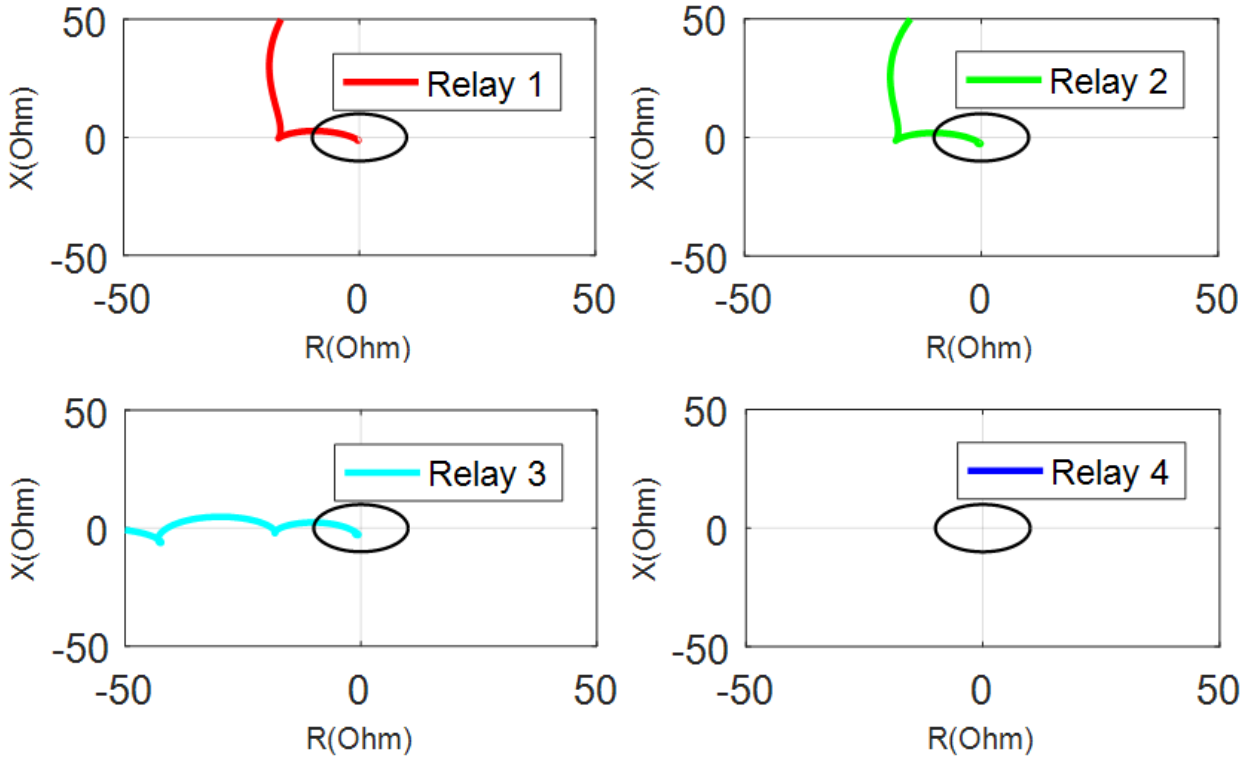


Figure 17: Impedance trajectories during a three phase to ground fault $F4$ under islanded mode of operation

3.5.2 *Case* 2: Meshed Microgrid

For this case, the proposed protection scheme was tested on the islanded meshed microgrid shown in Fig. 18. Feeders are modelled using 336ACSR with positive sequence impedance of $0.27974 + j0.6388\ \Omega/mile$ and zero sequence impedance of $0.57118 + j1.80198\ \Omega/mile$. Feeder lengths are shown in Fig. 18. Fault detection impedance threshold for all relays is set as a circle centered at the origin with a radius of 15 Ω. This circle is shown on the impedance trajectory plots for reference.
For this microgrid, we use the impedance-based central protection scheme discussed in section 3.3.2. Tables 1 and 2 shows the topology mappings for the study microgrid. Note that for Relays $R2, R3, R8$ and $R10$, a fault in their reverse zone, direction flag is 1, will trigger an instantaneous trip. Simulation results for four different faults are presented in this section. For each scenario, a fault is applied at $t = 0.3sec$ and removed at $t = 0.45sec$. Fig. 19 shows the impedances measured by all relays prior to applying any fault to the microgrid. Impedance trajectories for faults $F1, F2, F3$ and $F4$ are shown in Figs. 20 to 23, respectively. For each fault, the Central Protection Unit will receive fault and direction flags from the relays which detected the fault. Based on these flags the fault will be located and appropriate relays will be commanded to trip. To illustrate this process consider fault $F1$. Table 3 shows the relays which picked up the fault along with their direction flags. Also shown is the corresponding protection zone based on the direction flags as determined from Table 2. Using Table 3 and Table 1, the Central Protection Unit will determine that the fault is in zone 1 since this is the only zone in the microgrid that has all of its relays either detected a fault in its direction or did not detect a fault at all. Finally, relays $R1, R7$ and $R10$ will be commanded to trip to clear the fault.

Table 3: Relays that picked up fault $F1$ along with their direction flags and corresponding protection zones

Fault Interrupting Device	**Direction Flag**	**Protection Zone**
R1	0	1
R2	0	2
R3	0	4
R4	0	4
R5	0	2
R7	0	1
R8	0	5
R9	0	3
R10	0	1

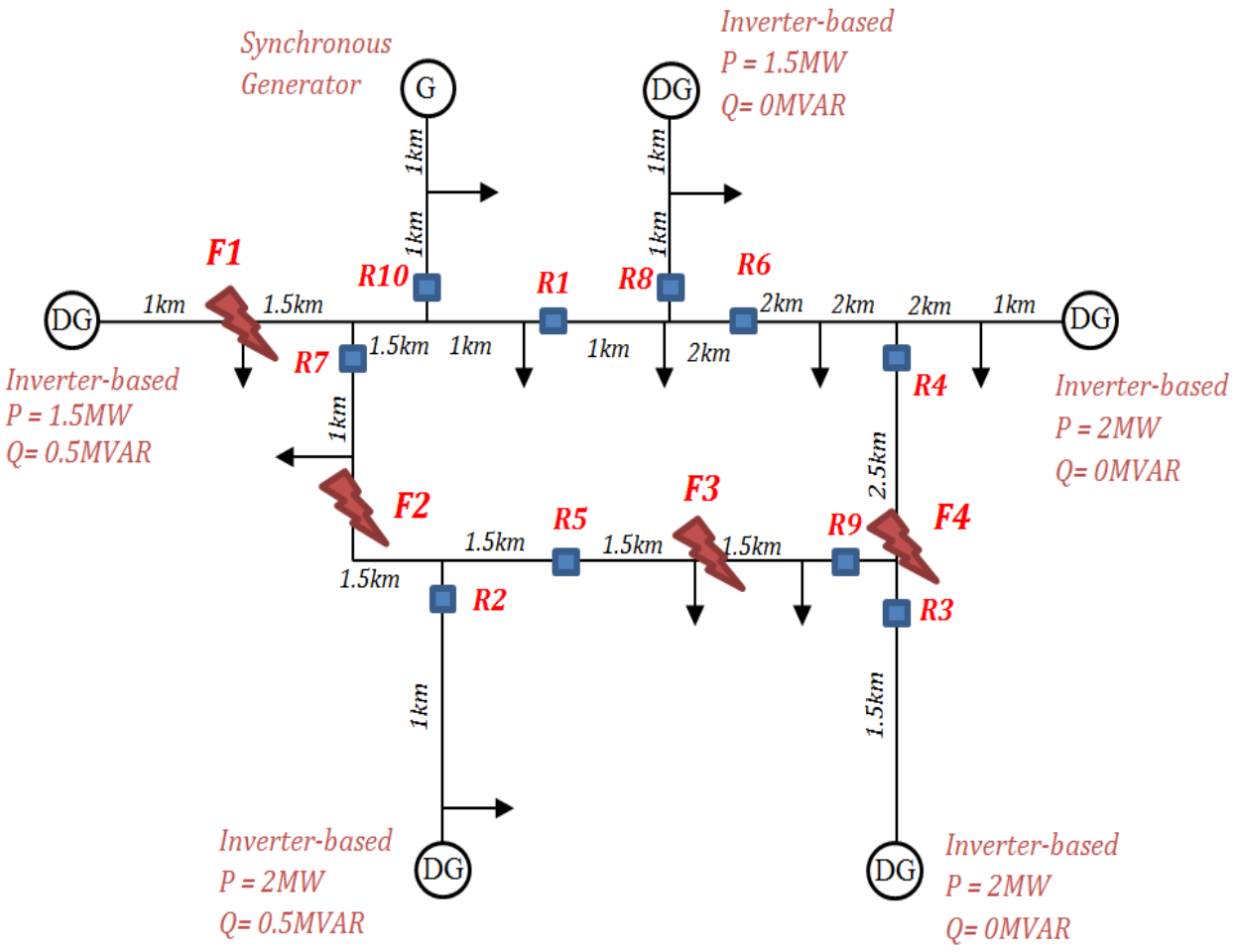


Figure 18: Microgrid used for *Case*2 study

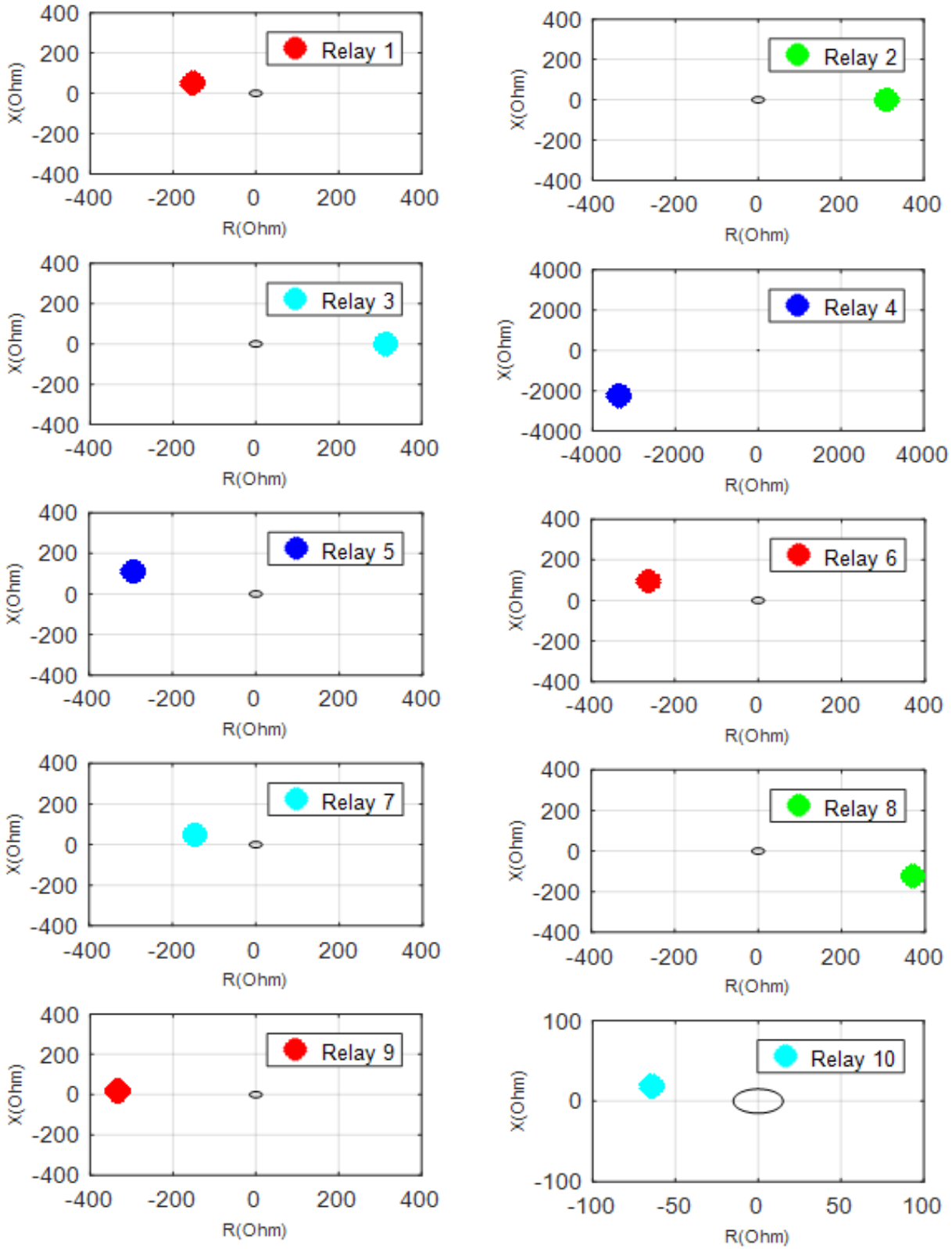


Figure 19: Impedance measured by different relays prior to applying any fault

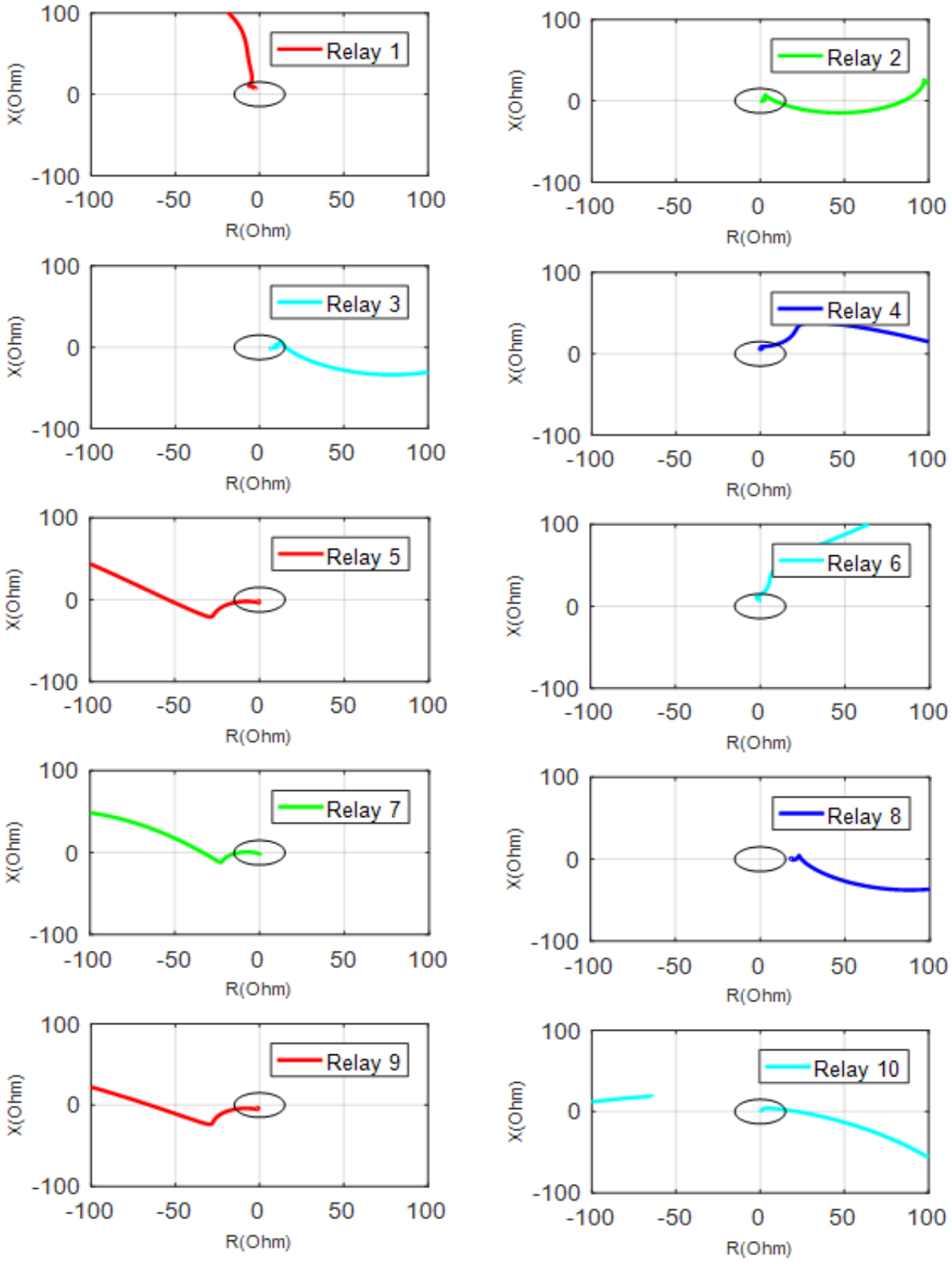


Figure 20: Impedance trajectories for $F1$ case

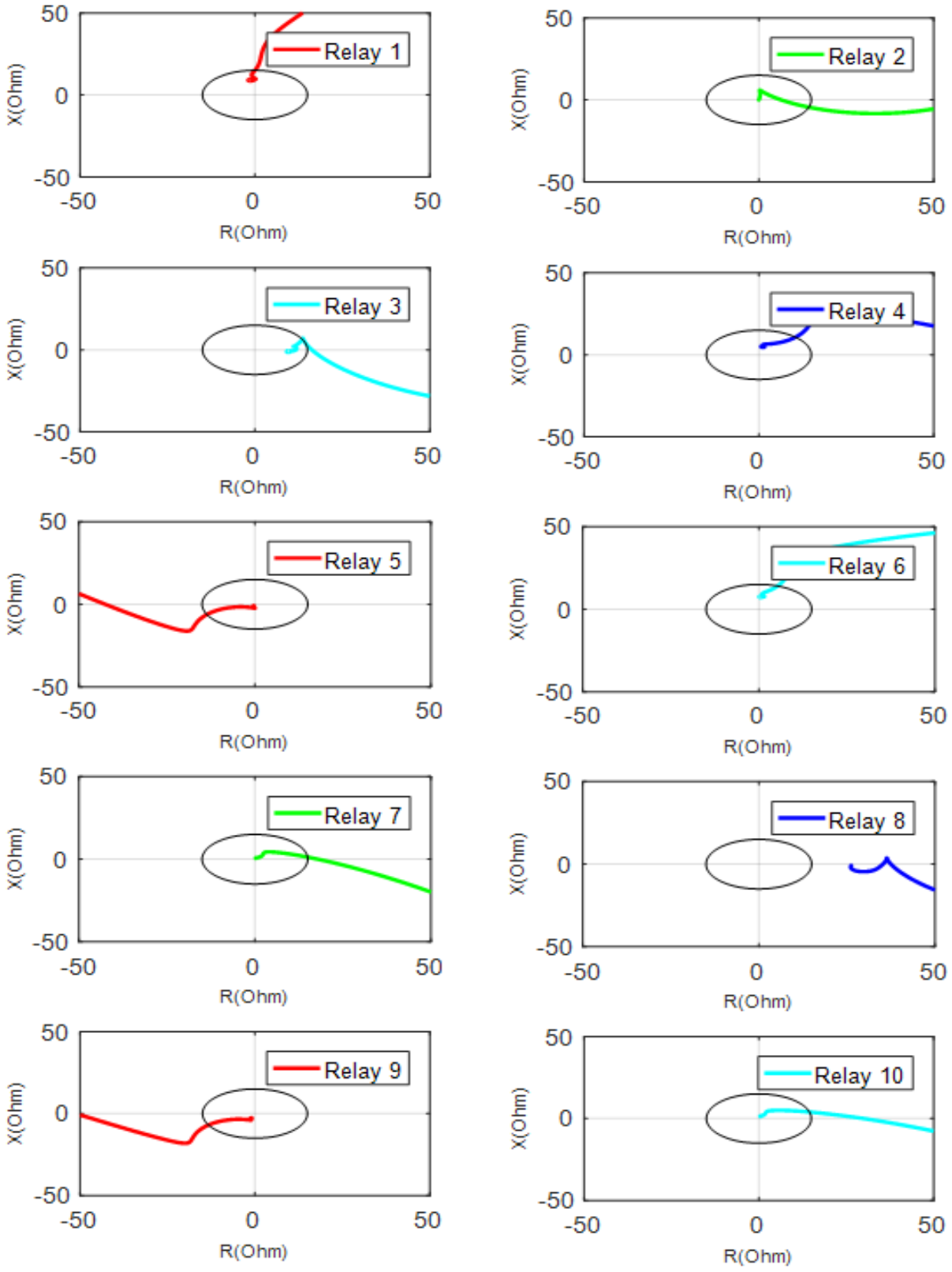


Figure 21: Impedance trajectories for $F2$ case

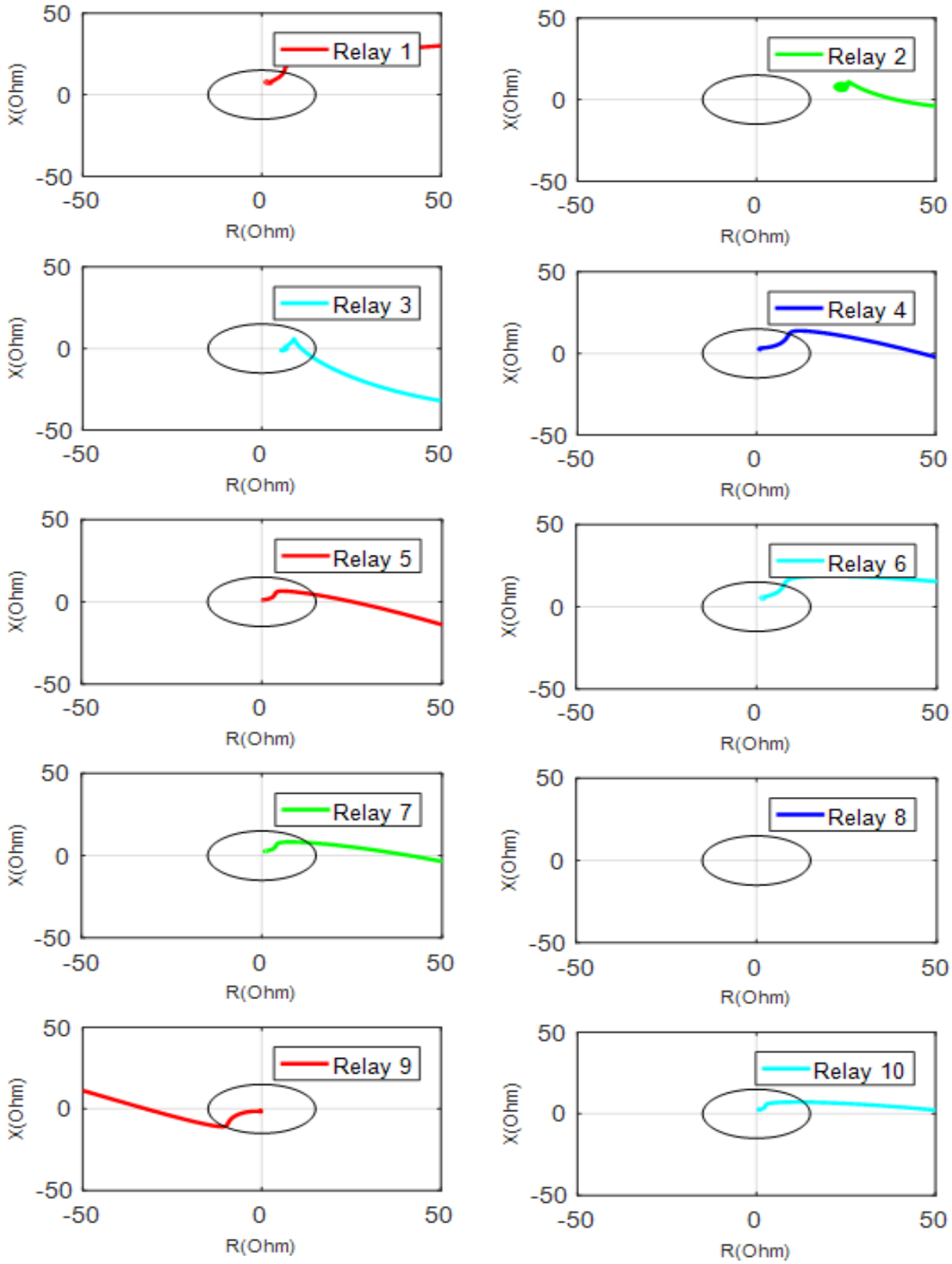


Figure 22: Impedance trajectories for $F3$ case

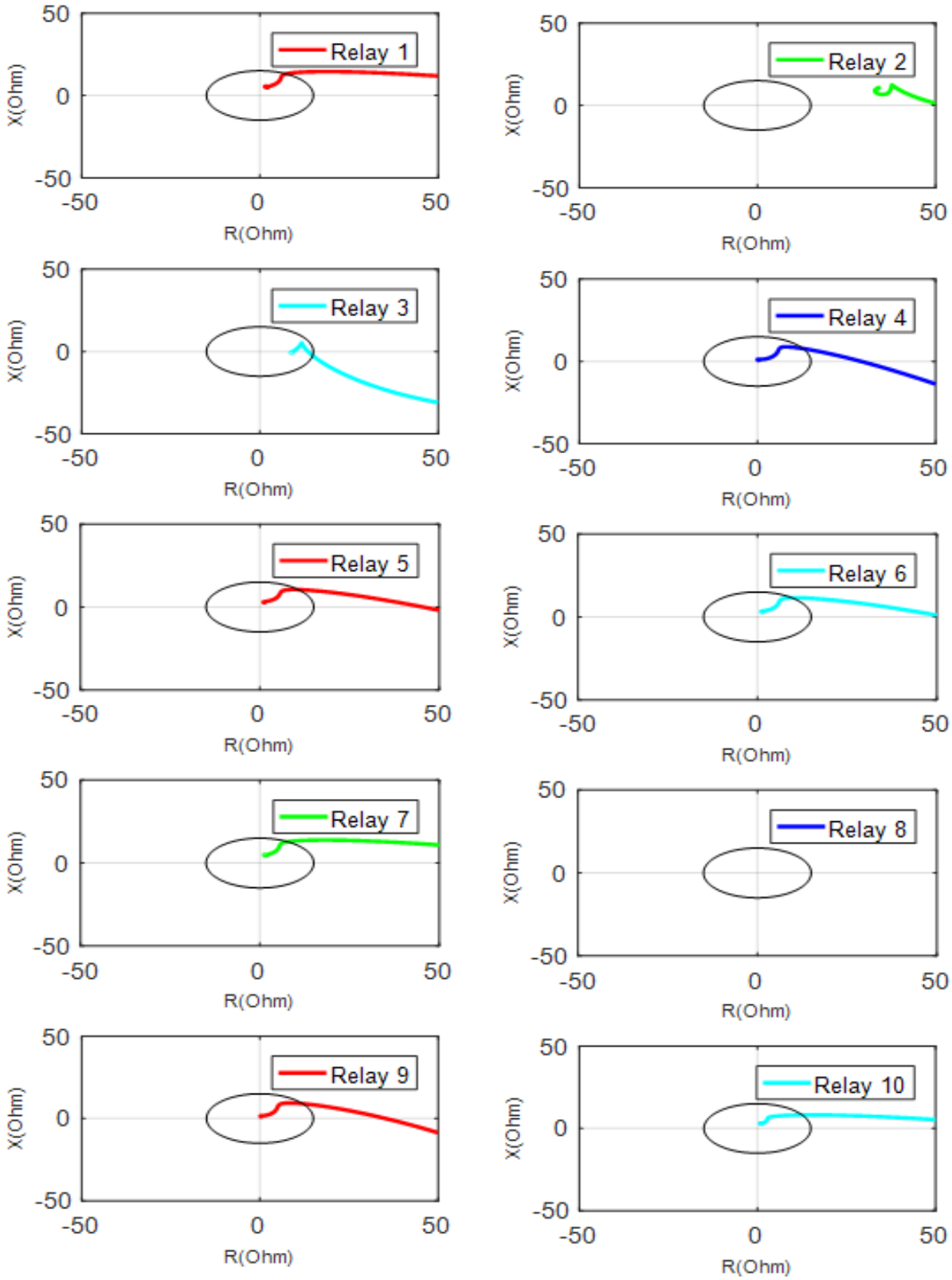


Figure 23: Impedance trajectories for $F4$ case

3.6 Conclusions

In this section impedance-based protection was discussed as a viable alternative to traditional overcurrent protection for low-fault inverter-dominated microgrids with general configuration and potentially with dynamic topology. Two communication-assisted protection schemes were proposed: impedance-based pilot protection scheme and impedance-based Central Protection scheme. The proposed schemes could be applied to any microgrid regardless of the number and locations of fault interrupting devices. Additionally, these schemes only require low-band width communication and, unlike other schemes proposed in literature, they do not rely on synchronized measurements. While the proposed schemes depend on communications in general, it is possible in some cases, based on the particular configuration of the microgrid under study, to design the coordination between feeder impedance relays based solely on measured impedance values as was demonstrated in section 3.5.1. The proposed schemes are less expensive than differential protection and at the same time are more reliable than overcurrent protection thus represent viable alternatives that could potentially fill the microgrid protection gap depicted in Fig. 3. Moreover, the ability of the proposed scheme to protect dynamic topology microgrids would help overcome a significant hurdle facing the widespread application of networked microgrids.

4 Transient-based Protection for Low Fault Microgrids

In this section we will analyze the response of a grid tied inverter to different types of faults in the grid and investigate methods for detection of faults at the output of the inverter.

4.1 Three phase Grid Connected Inverter

The three phase photovoltaic (PV) inverters are generally deployed in large scale installations and are tied to the grid. The rated output of commercially available three phase inverters are normally 208 or 480 V. So, we have designed the inverter to result in a line to line voltage of 480 V. We consider a single stage topology. The detailed specifications of the inverter are summarized in Table 4. These specifications are adopted from [23] and are based on a commercial GE grid-connected inverter platform.

Inverter Parameter	**Value**	**Unit**	**Description**
V_{dc}	900	V	dc source voltage
F_S	8000	Hz	Switching Frequency
V_{LL}	480	V	Line-to-line Voltage
P	100	kW	Rated power
pf	1		Power factor

Table 4: Specifications of the Inverter

As the output from the PV modules can be modeled as a dc source, the input to the inverter is modeled as an ideal dc voltage source. PV characteristics are not modeled, since they are not essential to the scope of this study. The dc source is connected to a controlled bridge circuit consisting of inverter generally consists of a dc bus feeding three pairs of power electronic switches (normally Insulated Gate Bipolar Transistors (IGBTs)). Each IGBT is accompanied by a free wheeling diode to allow flow of current in reverse direction. The switching pattern of the power electronic switches are controlled through pulse width modulation (PWM), to generate required AC power. The current and voltage waveform at the output of bridge switches, are further conditioned by a filter circuit, to reduce harmonic distortions and improve power quality. The inverter output filter can either be a simple inductive (L) filter, inductive & capacitive (LC) filter or a LCL filter. In our inverter model, we use a LC filter, due to its wide spread acceptance [3]. An inverter can either operate in standalone mode feeding a set of loads or can be connected to the utility grid. In the grid connected mode the inverter feeds power to the grid, according to commands set by the user. The inverter is normally tied to the grid through a $\Delta - YG$ transformer.

4.1.1 Control Block Diagram

The inverter can either be voltage controlled or current controlled. In a grid connected inverter, current control enables quick response to change in real and reactive power demand [24]. Thus, most PV inverters are current controlled. We use a constant current control

strategy for the inverter simulated in this report. The inverter is implemented in PSCAD and is modeled based on a NREL report [24]. The basic block diagram of the inverter with control modules is shown in Fig. 24.

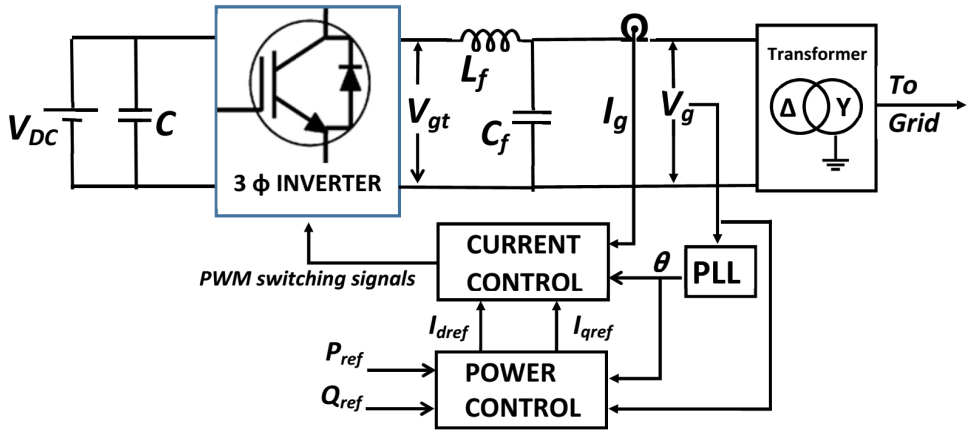


Figure 24: The inverter block diagram with controls

The control objectives are :

- The voltage and current waveforms out of the inverter should be clean (less distortions).
- The Real and reactive power output should follow instructed command values.
- The output current of the inverter should not exceed 110% of the rated current, during faults or grid disturbances.

In constant current control, the inverter output currents are regulated with respect to the specified current references. The magnitude and phase of inverter output currents can be precisely controlled to have a command over the real power (P) and reactive power (Q) output. The inverter controls can be designed either in stationary (a,b,c) or rotational (dq) frame of reference. The control in rotational frame of reference yields better performance due to the conversion of control signals to dc quantities [25], in contrast to the sinusoidal quantities. So, simple proportional Integral (PI) controller can be effectively used to achieve control actions. In addition, the real and reactive power commands can be directly interpreted in the *dq* frame of reference.

4.1.1.1 Phase locked loop (PLL) The grid synchronization for the inverter is achieved through a *dq* phase locked loop (PLL). The block diagram for the PLL is shown in Fig. 25. The PLL locks at the grid frequency by driving the quadrature component of the voltage (V_{gq}) to zero, through a PI controller. The PLL provide the angle reference for calculating the Park transformation to convert between synchronous and rotational frames of reference.

4.1.1.2 Power Control The power control block is responsible for generating reference currents based on the specified commands for real and reactive power. As mentioned earlier, the control is carried out in a rotating frame of reference.

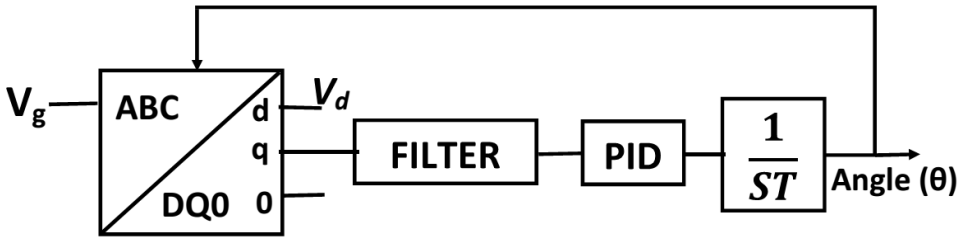


Figure 25: The dq PLL circuit

The expression for complex power delivered by the inverter onto the grid can be written as [26]:

$$S = (V_{gd}I_{gd} + V_{gq}I_{gq}) + j(V_{gq}I_{gd} - V_{gd}I_{gq}) \tag{4}$$

$$= P + jQ \tag{5}$$

where, V_{gd} and V_{gq} are the d and q components of three phase voltage (V_g), at the grid. I_{gd} and I_{gq} are the d and q components of three phase output current (I_g). P and Q denote the real and reactive power.

If the d axis of V_g is aligned with d axis of inverter terminal voltage V_{gt} then $V_{gd} = V_g$ and $V_{gq} = 0$. This is achieved through grid synchronization with PLL. Please observe in Figurefig:pllthat the dq PLL drives V_{gq} to zero. Therefore, real and reactive powers can be expressed as [27]:

$$P = v_{gd}I_{gd} \tag{6}$$

$$Q = -v_{gd}I_{gq} \tag{7}$$

The reference currents in dq axis, I_{dref} and I_{qref} can be directly calculated from the reference

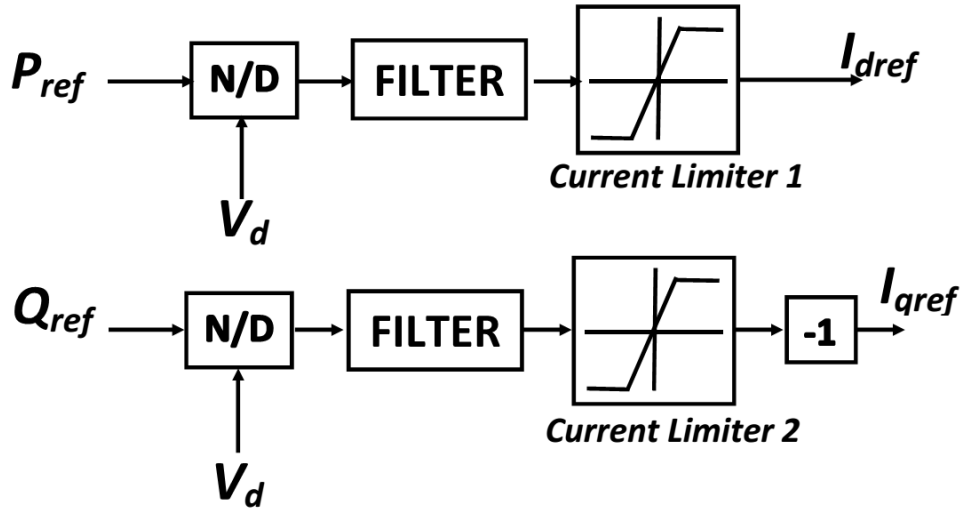


Figure 26: The Power control circuit

powers P_{ref} and Q_{ref} according to equations (6) & (7). The power control block in Fig. 26

carries out this operation. The calculated reference currents are filtered to remove the noisy variations and smoothen them. The reference currents must not exceed the maximum current limit specified for the inverter. The current limiter block takes care of it by specifying hard limits of minimum and maximum values for I_{dref} and I_{qref}. The calculation of the limiting values are explained in Section 4.1.1.4. The commanded real and reactive powers can be achieved by regulating the the reference currents I_{dref} and I_{qref}, respectively.

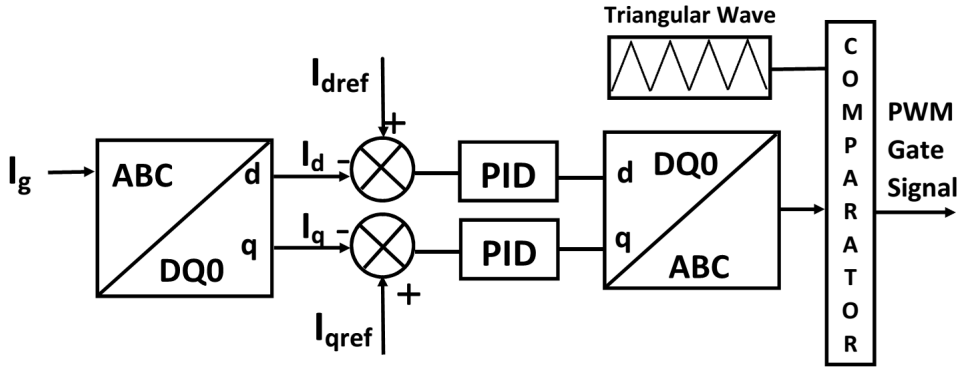


Figure 27: The current controlled PWM circuit

4.1.1.3 Current Control The Current Control module shown in Fig. 27 is responsible for tuning inverter output currents (I_d & I_q) in order to match the reference currents. The error between actual output and reference current values are minimized by the PI controllers. The control over I_d & I_q are achieved by altering the switching pattern of the IGBTs through PWM signal. The PWM signal is generated by comparing the output of the PI compensated error signal in synchronized reference frame with a normalized triangular wave. The frequency of the triangular wave corresponds to switching frequency of the inverter.

4.1.1.4 Current Limiting Action The power electronic circuit inside the inverter have limited current carrying capacity and must be protected against any increase of current due to external disturbances. Although the maximum current limit is decided by the current carrying capacity of the IGBTs, a value of 1.1 pu is adopted by many available commercial inverters. The current limiting is achieved by specifying hard limits over the direct and quadrature components of the reference currents. The current limiting action can have two possible modes of operation: (1) P-priority and (2) Q-priority. In P-prority mode, the range of real current component I_{dmax} is maximized and the remaining current carrying capability is used for determining reactive component I_{qref}. For Q-priority, The controller maximizes the range of reactive component I_{qmax} and uses the remaining capability for reactive current I_{dref}. We have implemented the P-priority mode of operation in the inverter. The current limiting scheme is shown in Fig. 28. The abnormalities in voltage is monitored through a abnormal voltage range detection circuit shown in Fig. 29. The output flag V_{dip} is set to '1', whenever voltage exceeds 1.3 pu or drops below 0.7 pu [24]. During normal conditions, $V_{dip} = 0$, the limit of reactive current component I_{qref} lies in between $+i_{max}$ and $-I_{max}$. The

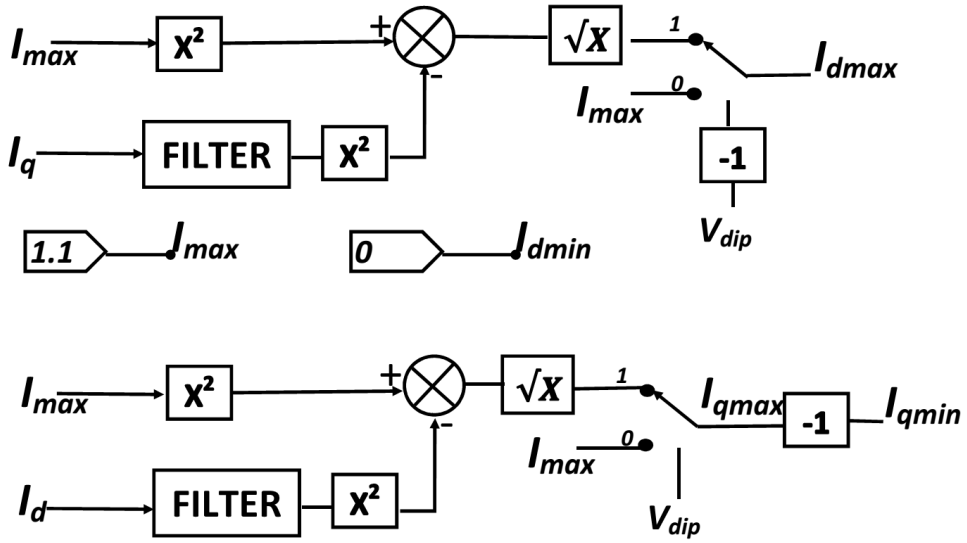


Figure 28: The current limiter circuit

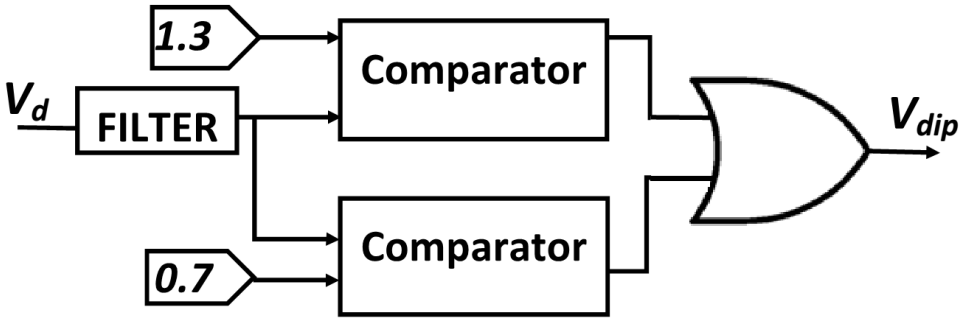


Figure 29: The abnormal voltage range detection circuit

maximum value of active current component (I_{dref}) is set according to (8).

$$I_{dmax} = \sqrt{I_{max}^2 - I_{qref}^2} \tag{8}$$

However the current limits are not reached or limiter has no effect on output, as the inverter follows the commanded active and reactive power.

The current limiter gets into action when the output voltage (V_g) drops below the specified value because of faults or other disturbances in the grid. so, V_{dip} is set to 1. With decrease of V_g, I_{dref} increases but can reach only until the specified limiting value I_{dmax}. The maximum limit of I_{qref} is calculated as $I_{qmax} = \sqrt{I_{max}^2 - I_{dref}^2}$ and minimum value is set as $I_{qmin} = -I_{qmax}$.

4.1.2 Performance Evaluation of the Inverter

The designed inverter was connected to a 4.16 kV ideal source as shown in Figure 30. The parameters of the test setup are summarized in Table 5.

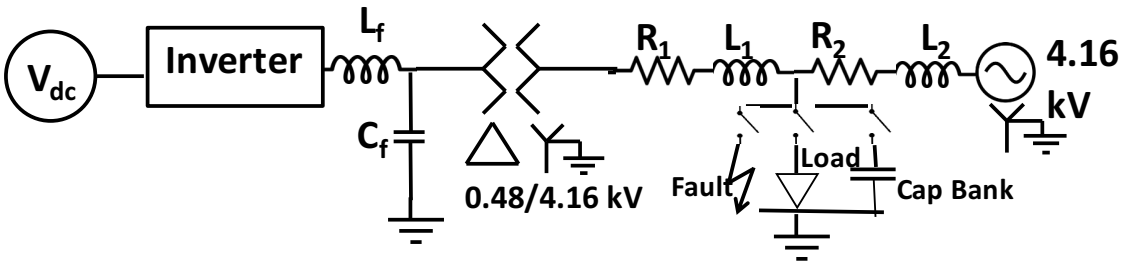


Figure 30: Test setup showing the inverter connected to an ideal AC source

4.1.3 Command over Real and Reactive Power

To test the ability of inverter to follow commanded power values test cases were created by varying the power to 100%, 50% and 10% of the rated value at power factor angles of 0^o,30^o,60^o and 90^o. The implemented inverter circuit could effectively track the desired commands.

Parameter	**Value**	**Unit**	**Description**
L_f	2.6	mH	Filter Inductance
C_f	20	μF	Filter Capacitance
R_1	1.2	Ohm	Line Resistance
L_1	2	mH	Line inductance
R_2	1.2	Ohm	Line Resistance
L_2	2	mH	Line inductance
Load	50	kVA, 0.8 lag	Load
Cap Bank	100	kVar	Capacitor Bank

Table 5: Data of the Inverter

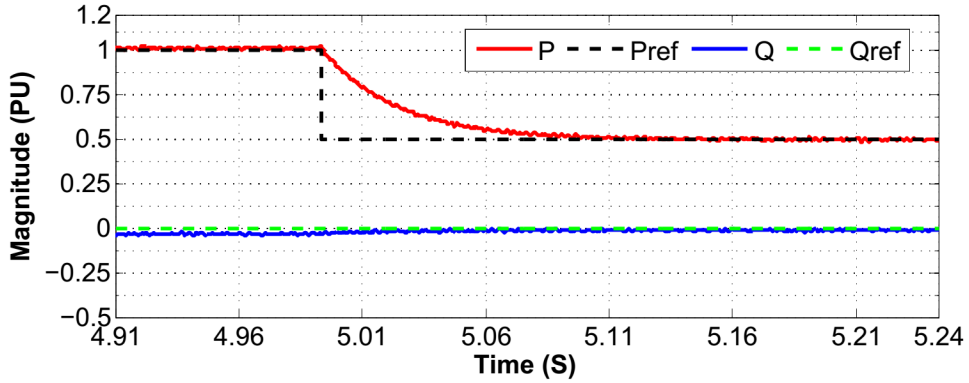
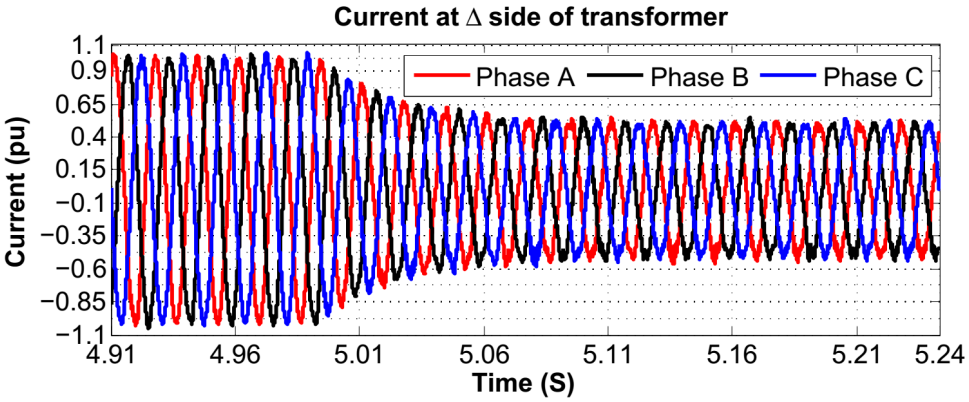
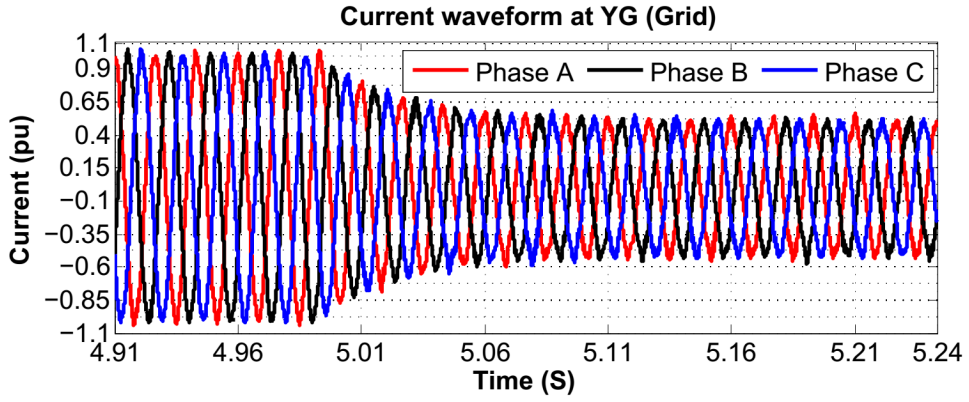


Figure 31: The reference and actual active and reactive power of the inverter output during a command to change from 100% to 50% of rated power at upf

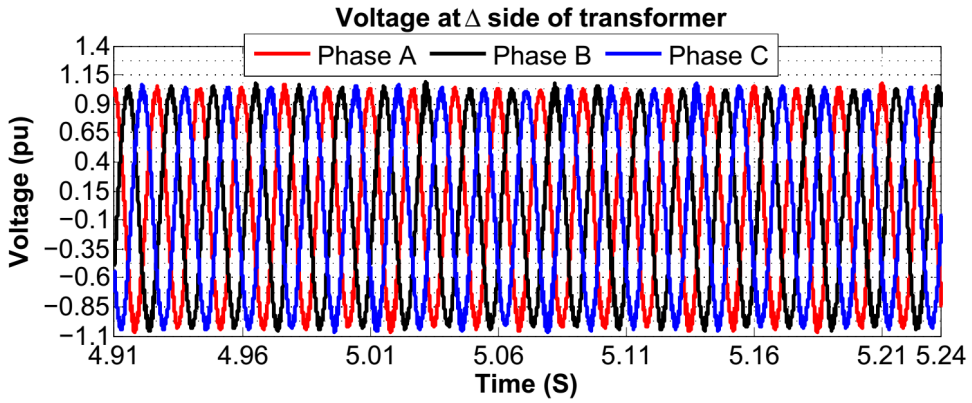


(a)

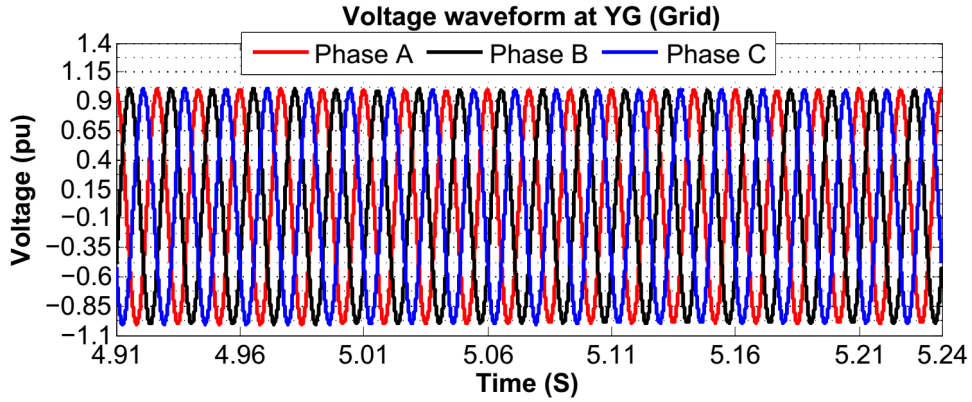


(b)

Figure 32: Current waveform at (a) delta side and (b) YG (grid) side of the coupling transformer during a real power command to change from 100% to 50% of rated power at upf



(a)



(b)

Figure 33: Voltage waveform at (a) delta side and (b) YG (grid) side of the coupling transformer during a command to change from 100% to 50% of rated power at upf

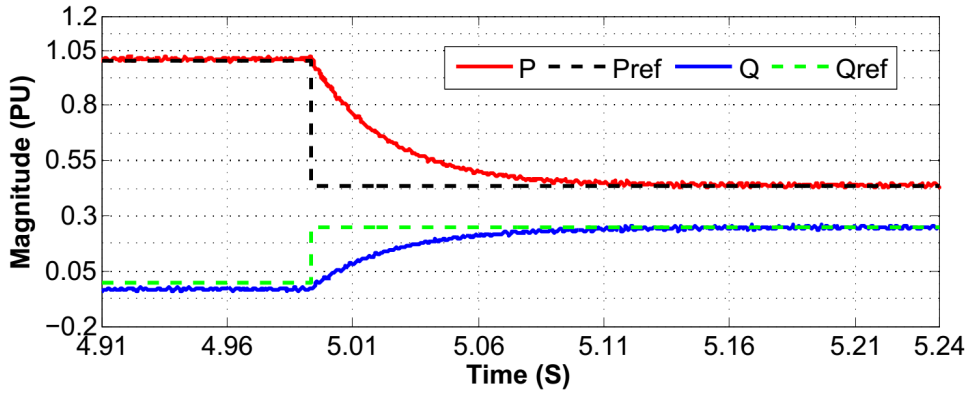
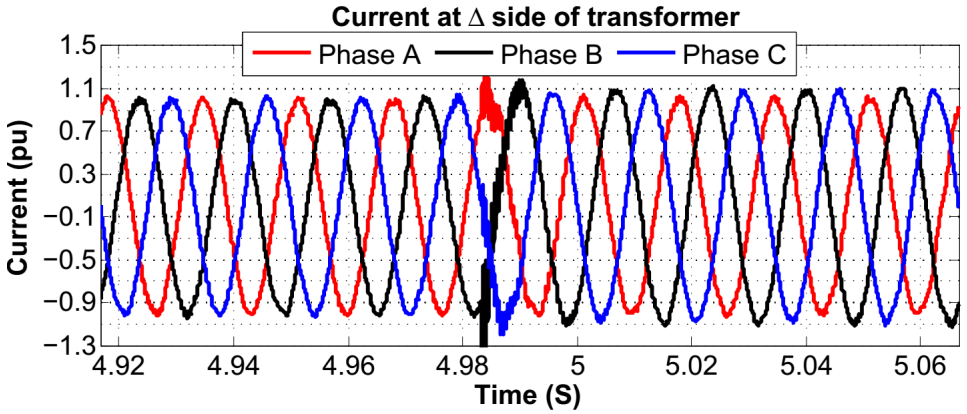
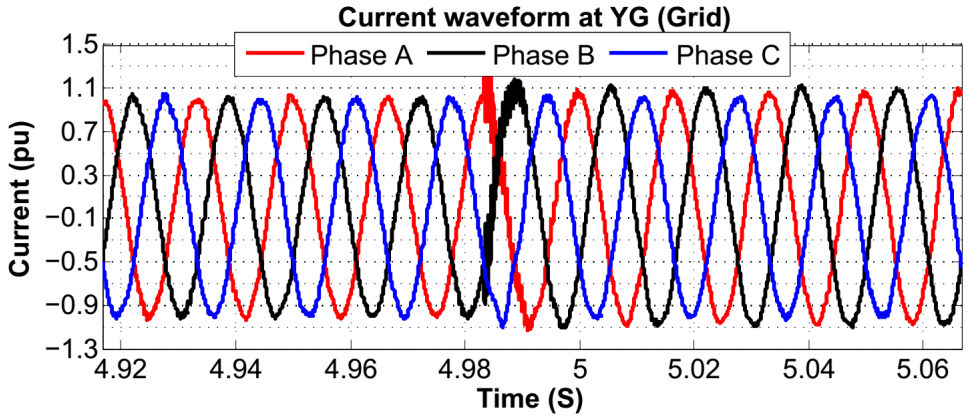


Figure 34: The reference and actual active and reactive power of the inverter output during a command to change from 100% at unity pf to 50% of rated power at 0.867 pf

Figure 31 shows the output power delivered by the inverter in response to change in reference active and reactive power from 100% of the rated value to 50% of the rated value at unity power factor (upf). The currents at delta and Y-grounded side of the coupling transformer are shown in Figure 32. The voltage waveforms at delta and Y-grounded side of the coupling transformer are presented in Figure 33. The actual power output and the commanded active and reactive power is shown in Figure 34. Note from figures that the inverter responds promptly to the change in active and reactive power commands. The voltage and current waveforms at both delta and YG side of the coupling transformer can also be observed to be free from distortions. Another case with change in reference active and reactive power from 100% of the rated value at upf to 50% of the rated value at 0.867 power factor (pf) is shown in Figure 34. It can be observed that the inverter is capable of adapting to change in commanded active and reactive powers. So, the inverter satisfies the first control objective. Although more sophisticated controls can be used to increase the response time of the inverter to change in commands, it is out of the scope of this study.

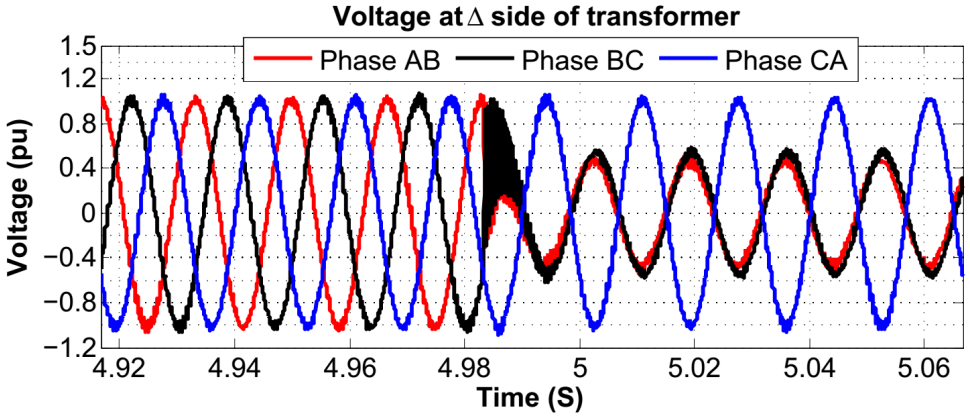


(a)

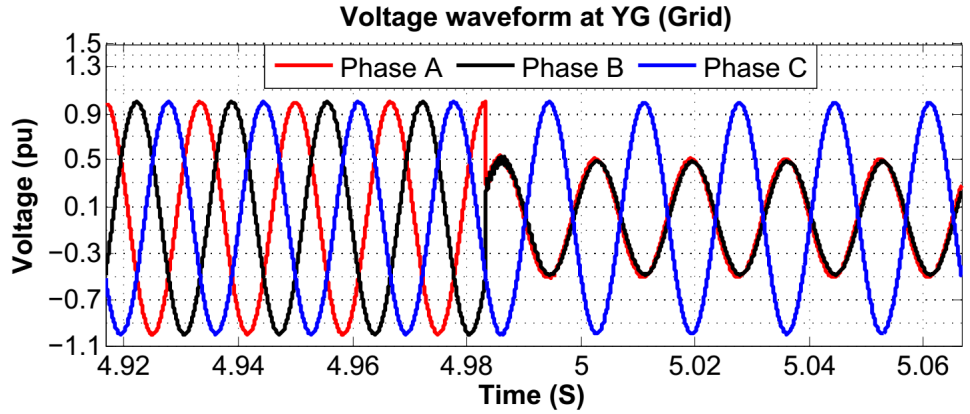


(b)

Figure 35: Current waveform at (a) delta side and (b) YG (grid) side of the coupling transformer for an two phase (AB) fault



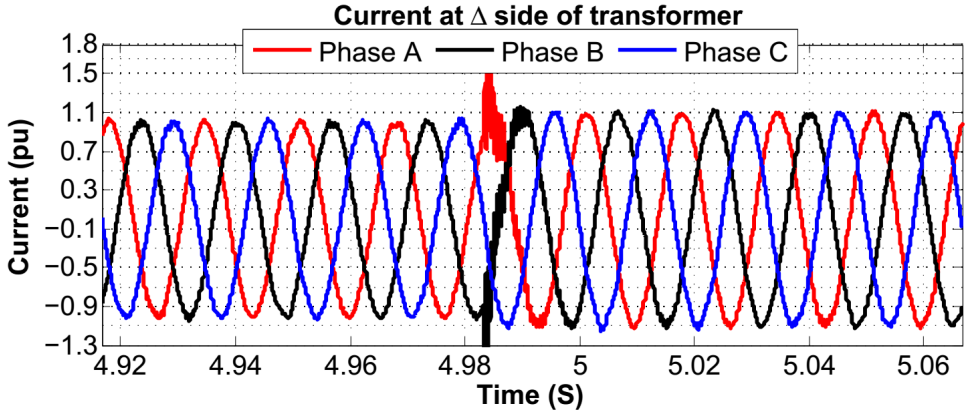
(a)



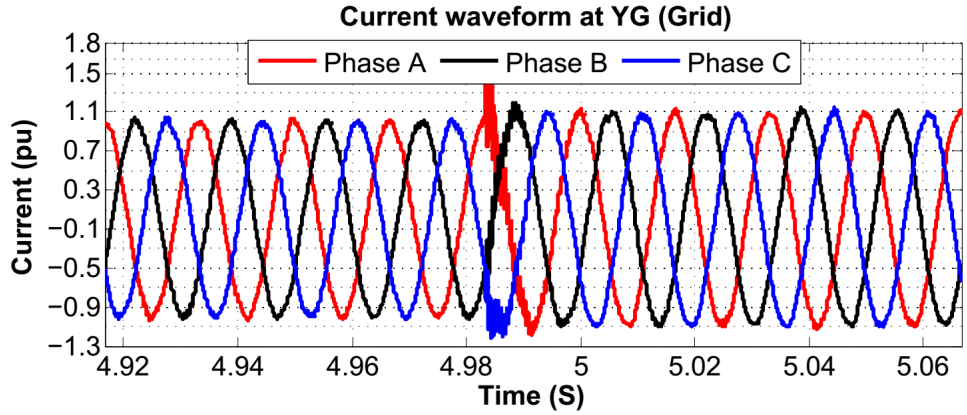
(b)

Figure 36: Voltage waveform at (a) delta side and (b) YG (grid) side of the coupling transformer for an AB fault

4.1.3.1 Current limits during faults Various fault cases were created in the grid side of the test set-up shown in Figure 30. Figure 35 and 36 show the delta side current, grid side current, delta side voltage, grid side voltage waveforms for a Phase A to B fault. The fault resistance was taken as 0.1 Ohm. The fault starts at 4.9833 S (at the peak of the grid side Phase A voltage waveform). Observe in Figure 36, the Phase A and B voltages go below 0.5 pu, due to the fault. So, the inverter output current must increase to maintain the delivery of commanded power. It can be seen that the delta side and grid side currents increase after the fault, but are curtailed at 1.1 pu. This occurs due to the current limiting action of the inverter. Another demonstration of the current limiting action of the inverter is presented in Figure 37 and Figure 38. In this case, a three phase to ground fault with fault resistance of 0.05 Ohm is considered. It can be seen in Figure 38 that all the three phase voltages drop below 0.2 pu. But the currents, as shown in Figure 37, doesn't go beyond the limiting value. Please note that at the point of inception of fault, the current was observed to shoot up beyond the limit of 1.1 pu for a short transient duration, while the control actions reinforce the limits on the current.



(a)

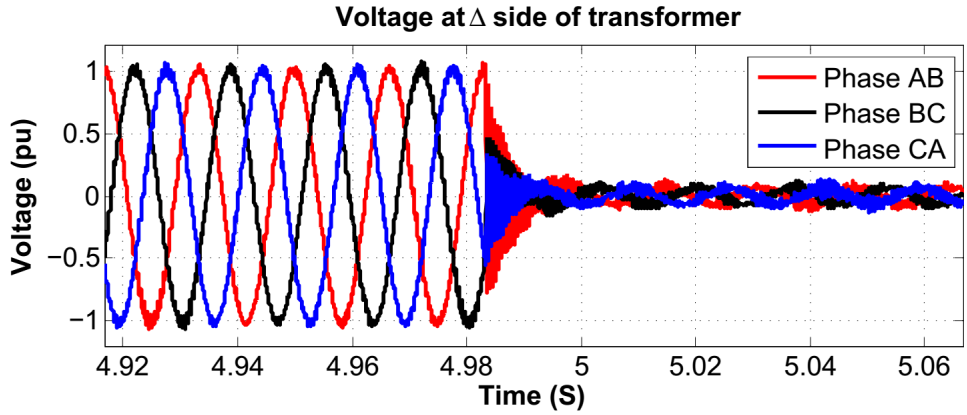


(b)

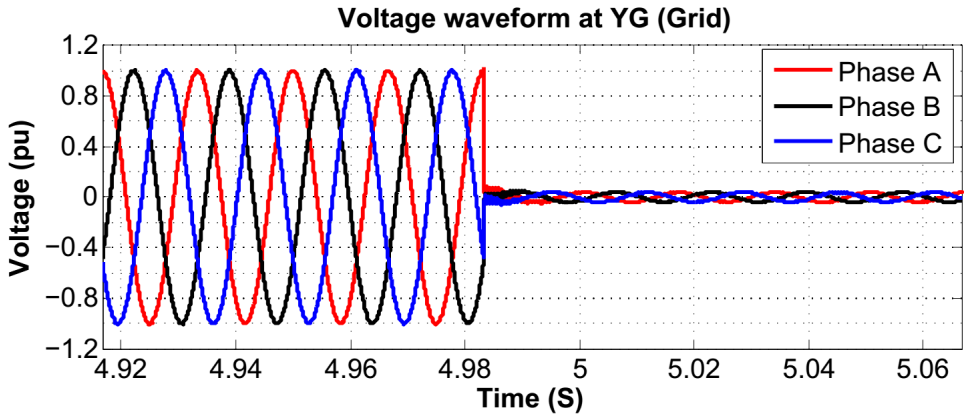
Figure 37: Current waveform at (a) delta side and (b) YG (grid) side of the coupling transformer for a 3-phase to ground fault

4.1.4 Transient signature upon inception of faults

Observe in Figure 35 - 38, short duration transient are present in both the voltage and current waveforms, except for grid side voltage, upon inception of fault. The strength of the transient is more prominent in the delta side of the transformer in comparison to the Y-grounded side. Although in the figures shown, the transients can be seen in both the delta and YG side currents, a relatively lighter transient at the delta side may get lost after passing through the coupling transformer. Cases demonstrating this are discussed in section 4.1.5 & section 4.3. The transients in the voltage at delta side are more prominent than the transient in the currents at delta side. Also observe that the voltage transients completely disappear at the Y-grounded side voltage. Based on this analysis, the delta side voltage and currents bear transients at the inception of fault, and these transients can be monitored to devise an alternative approach for fault detection. The cause of this transient can be attributed to the *filter capacitor* (C_f) at the output of the inverter bridge circuit. This can be verified from Figure 39, which shows the current waveforms before capacitive filtering. Note that the



(a)



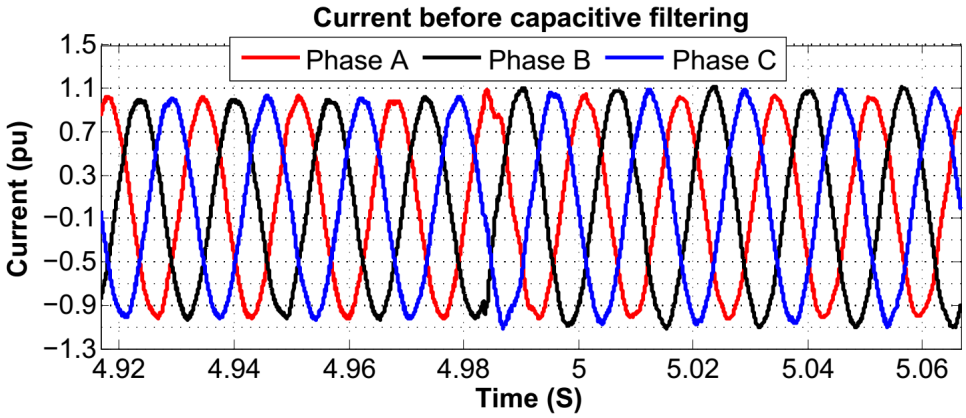
(b)

Figure 38: Voltage waveform at YG (grid) side of the coupling transformer for a 3-phase to ground fault

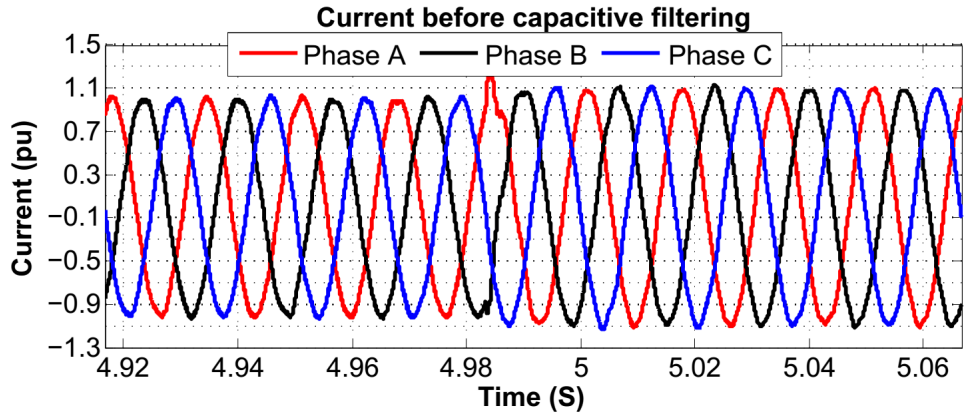
transient is not present in the current waveform before being subjected to filtering.

4.1.5 Effect of fault inception angle on Transient Signature

The transient signature may also depend on the fault inception angle. To verify this, we have simulated four single phase to ground (Phase A to ground) fault cases with inception angles at $0^o, 30^o, 45^o$ and 90^o or peak, with respect to Phase A voltage. The delata side voltage & current and YG side voltage & currents are shown in Figure 40-43. Observe Figure 40, showing the delta side currents. It can be observed that, fault inception at zero instantaneous voltage of any phase results in very light or no transient signature at that phase. The prominence of the transient increases with inception angle changing to $30^o, 45^o$ and becomes most prominent at 90^o or peak. Similar behavior can also be observed in case of delta side voltages shown in Figure 42. Observe the grid side (Y-grounded) currents in Figure 41, the current shoots up due to the contribution of zero sequence component and no transient signatures are observed. In case of grid side voltages depicted in Figure 43,



(a)



(b)

Figure 39: Current waveforms at delta side of the coupling transformer before filtering for (a) AB fault (c) ABCG fault

no transient signatures are observed. The absence of transient at zero inception angle for a single phase fault will limit the capability of transient based fault detection. However, for two phase and three phase faults,even if one of the phase lie at zero instantaneous voltage, the other phases will correspond to a different inception angle and will bear transient signature. waveforms at delta as well as Y-grounded side are shown in Figure 41-43.

4.2 Transient based event detection

4.2.1 Fast variant of Discrete S-Transform (FDST)

Time frequency transforms are used to extract time varying spectral information of non-stationary signals. Since we had earlier used time-frequency analysis for assessing the harmonic and inter-harmonic content, the same approach can be extended to segregate the high frequency transient signature. A brief description of the approach is discussed below.

The S-Transform (ST)[28] is a linear Time Frequency transform. The frequency compo-

nents in ST are spaced uniformly, separated by a fixed spectral resolution. Unlike wavelets, the Fourier amplitude and phase can be directly observed from the spectrum inferred by ST. We use an improved fast variant of discrete S-Transform (FDST)[29] to compute time frequency representation.

Let $x(n)$ ($n \in [0, N-1]$) be a value in a voltage or current waveform with N recorded samples, with a sampling frequency of F_s Hz.

The frequency domain expression for FDST of a sampled signal $x(n)$ is expressed as :

$$S_d(n,k) = \begin{cases} \frac{1}{N}\sum_{k'=0}^{N-1}(X(k') \times W((k'-n),k))e^{\frac{j2\pi kk'}{N}}, \\ \qquad\qquad \text{if } k' = k \text{ and } X(k') \geq \mu \\ 0 \qquad \text{Otherwise,} \end{cases} \tag{9}$$

where $n = 0, 1, \cdots, (N-1)$ denotes the index of the original sample at time t (in s), thus $n = t.F_s$. And $k = 0, 1, \cdots, N/2$ denotes the index of the sample in the frequency domain for $f \in [0, F_s/2]$ in Hz. $X(k')$ is the Discrete Fourier Transform (DFT) of $x(n)$ and $W(k', k)$ is the DFT of the time domain generalized Gaussian window function $w(n, k)$. $w(n, k)$ satisfies $\sum_{-\infty}^{\infty} w(n, k) = 1$ and is expressed as (10) [29]:

$$w(n,k) = \frac{1}{\sigma(k)2\pi} e^{-(\frac{n}{2F_s\sigma(k)})^2} \tag{10}$$

where, $\sigma(k) = \frac{\eta}{\alpha+\beta|\frac{k.F_s}{N}|^\gamma}$, subject to $\eta \leq \sqrt{\alpha^2+\beta^2}$; η, ν and β are parameters which can be appropriately adjusted to enhance energy concentration of the TFR. Here, it is to be noted that the enhancement of TFR energy increases the compactness of the time localized spectral variation, resulting in accurate TF decomposition.

The parameter μ is a threshold that defines the significance of the frequency components in time frequency representation (TFR). μ is fixed based on the noise associated with the input signal. If the signal to noise ratio (SNR) of the acquired signal normalized with respect to the base value is specified in *db* as SNR_{dB}, then μ value is chosen as $\mu = \frac{1}{\sqrt{10^{SNR_{dB}/10}}}$. Alternatively, the value of μ can also be fixed as $\mu = \sigma_\nu$, Where μ_ν^2 is the variance of noise associated with the signal. Therefore, FDST not only reduces the computations but also offers inherent noise rejection while calculating the TFR. In real world situations where the noise power can't be determined; μ can be chosen as the minimum intensity level above which the spectral components need to be analyzed, for a specific application. We keep $\mu = 0$,$\eta = 1$,$\alpha = 0.01$, $\beta = 1$ and $\gamma = 1$ for the simulations presented in this report.

4.2.2 Monitoring with FDST

We propose a framework shown in Figure 44, utilizing FDST for monitoring. The analog input signals captured by voltage and current transducers are subjected to a low pass anti-aliasing filter, which band limits the input signal in accordance to the Nyquist rate defined by the sampling frequency. The sample and hold analog to digital converter block samples the band limited analog signal to result in discrete time samples.

For harmonics monitoring, IEC 61000-4-7 standard appendix B[30] recommends measuring frequencies in the range of 2-9 kHz with a frequency resolution of 5 Hz. We monitor with

a frequency resolution of 5 Hz, and choose the sampling frequency as 50 kHz, which is well above the Nyquist rate to measure components in the range of 2-9 kHz. In accordance with IEEE standard 519-2014 [31] the measurement window was kept 12 cycles, or approximately 200 ms for the 60 Hz power system, for estimating harmonics. This ensures that the spectral resolution or spacing between any two consecutive frequency bins or samples is 5 Hz. We employ a zero crossing detection technique to encapsulate one complete cycle of data, where we use first order backward derivative and observe sign change of slope to detect zero crossing [32]. The time varying magnitudes and phases of harmonic, sub-harmonic, interharmonic and supraharmonics components are then extracted from the TFR.

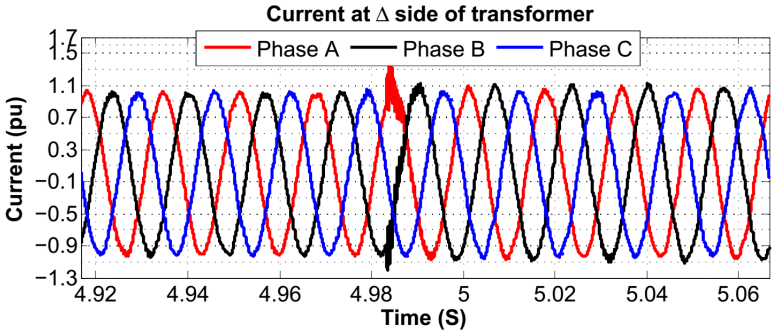
We extend the capability of the FDST based monitoring framework beyond the estimation of harmonics and interharmonics components and propose to use it for transient based fault detection.

4.2.3 Transient envelope extraction

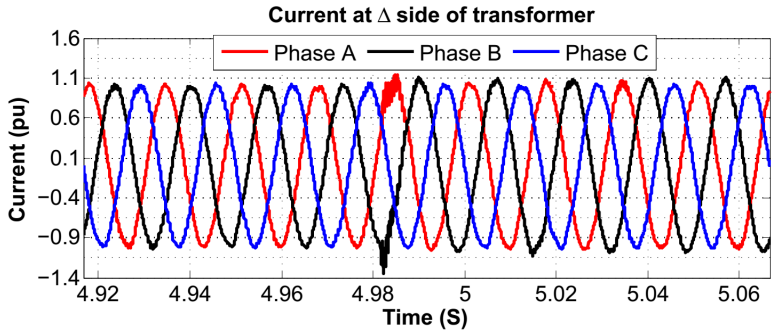
For transient detection, the measurement window slides by one cycle. The FDST is computed over the 12 cycles and the results are stored. The FDST result is a matrix with $S_d(n,k)$ with each row corresponds to a specific time and each column correspond to a frequency. We compute the envelope of the transient according to (11)

$$TR_{env}(n) = max\{|S_d(n,k)|\}, \quad \forall\ k \geq (\frac{N * f_l}{F_s}) \text{ and } k \leq \frac{N}{2} \tag{11}$$

where, $TR_{env}(n)$ denotes the transient envelope magnitude at time sample n over all the frequencies above f_l Hz. We keep $f_l = 500$ Hz for the simulations in this paper. The value of 500 Hz was chosen on the basis of analysis carried out in this study, as the filter capacitance result in transients with higher order frequency. In order to detect occurrence of a fault, a threshold value (ρ) is specified. Then a metric called as average transient magnitude is computed by avaraging all the values of $TR_{env}(n) \geq \rho$, over the measurement window.



(a)



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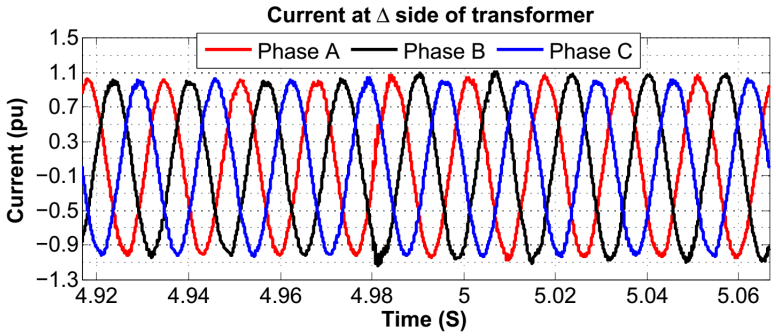
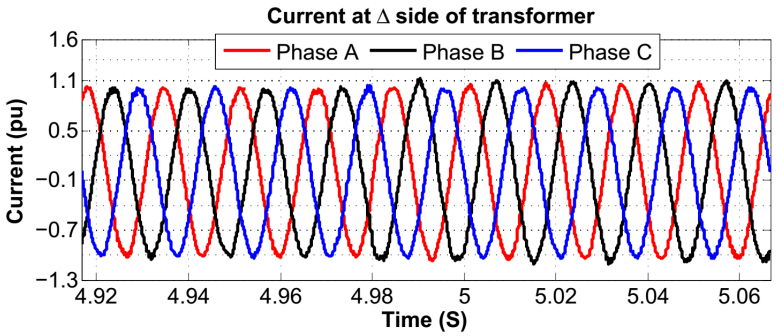
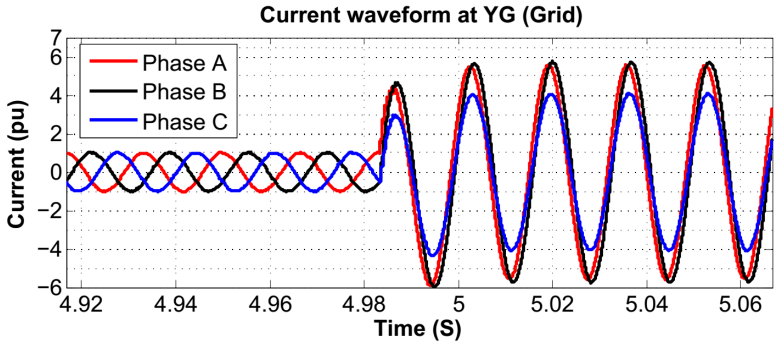


(c)

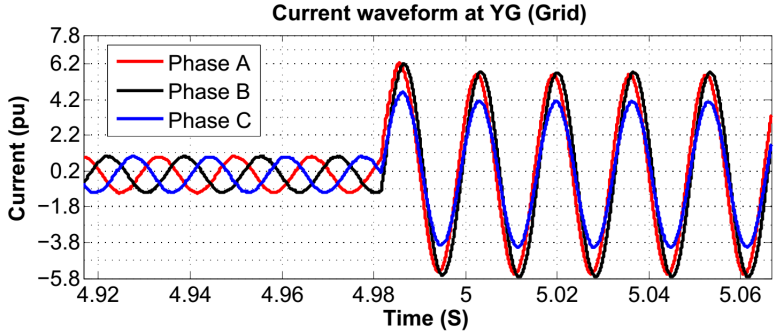


(d)

Figure 40: Current waveform at delta side of the coupling transformer for AG fault with inception angle with respect to Phase A voltage at (a) peak (b) 60^o (c) 30^o (d) 0^o



(a)



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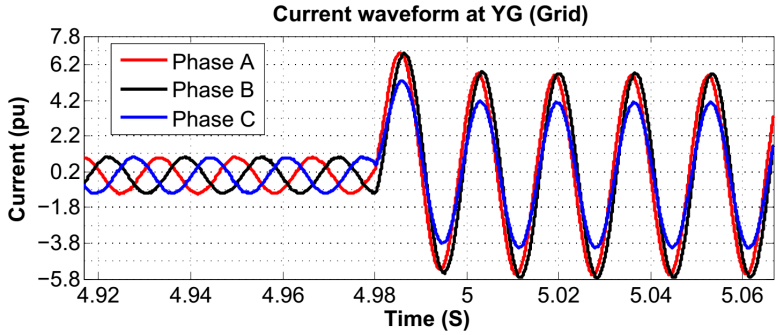

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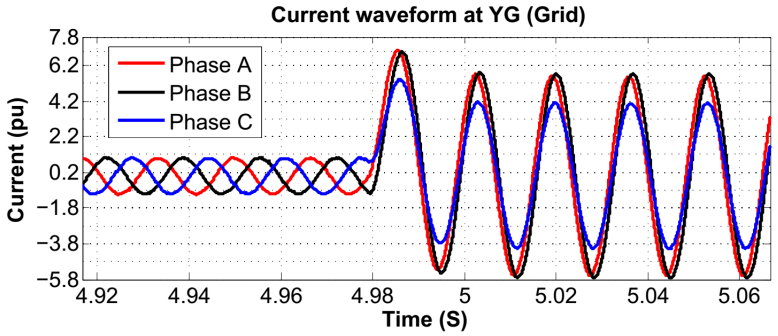
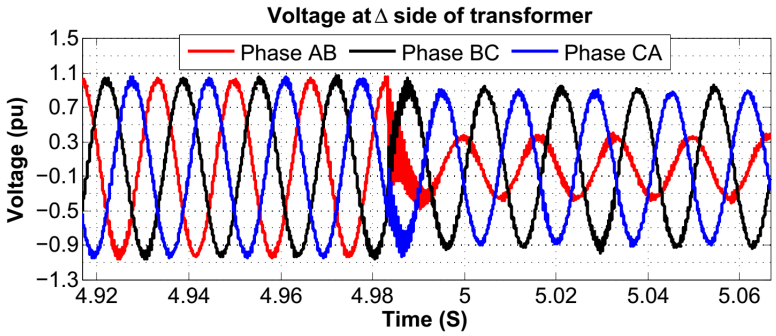
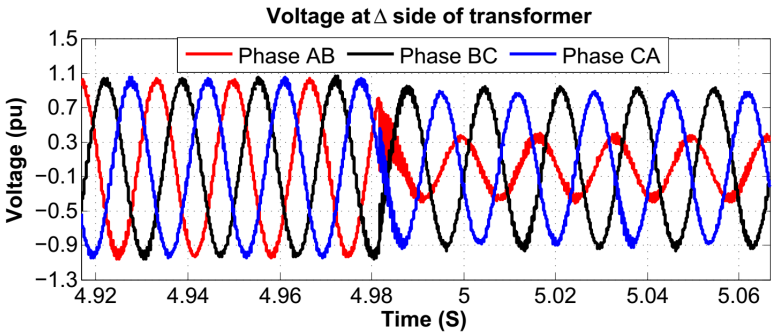


(d)

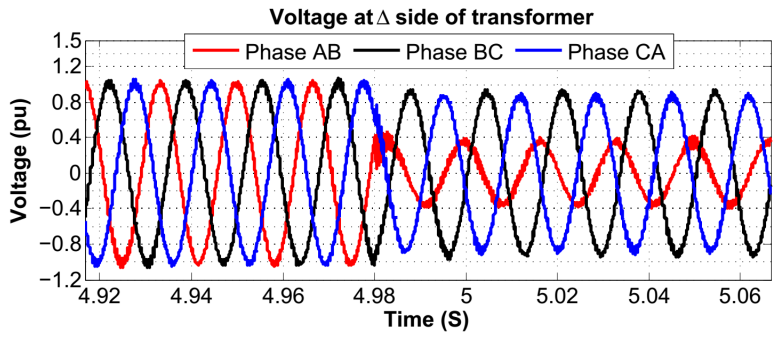
Figure 41: Current waveform at YG (grid) side of the coupling transformer for AG fault with inception angle with respect to Phase A voltage at (a) peak (b) 60^o (c) 30^o (d) 0^o



(a)



(b)



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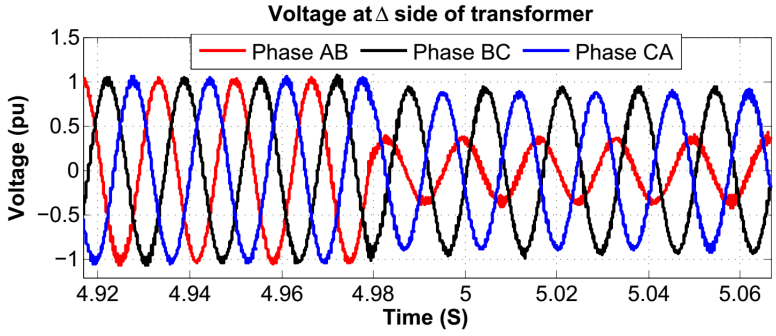
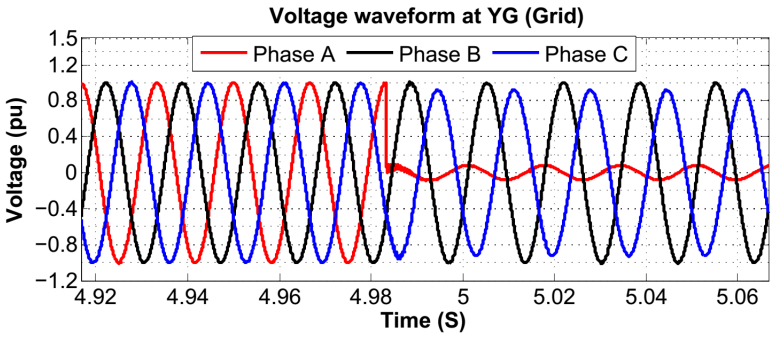
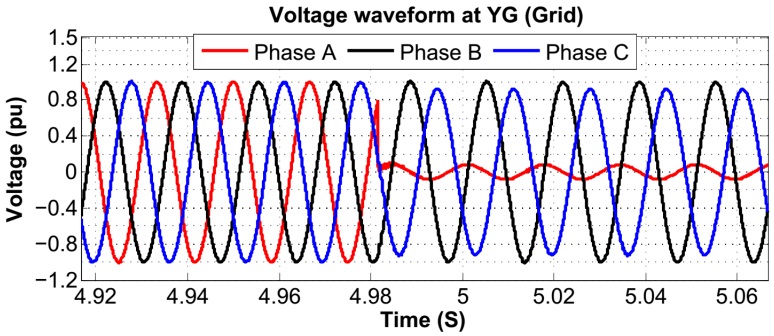


(d)

Figure 42: Voltage waveform at delta side of the coupling transformer for AG fault with inception angle with respect to Phase A voltage at (a) peak (b) 60^o (c) 30^o (d) 0^o



(a)



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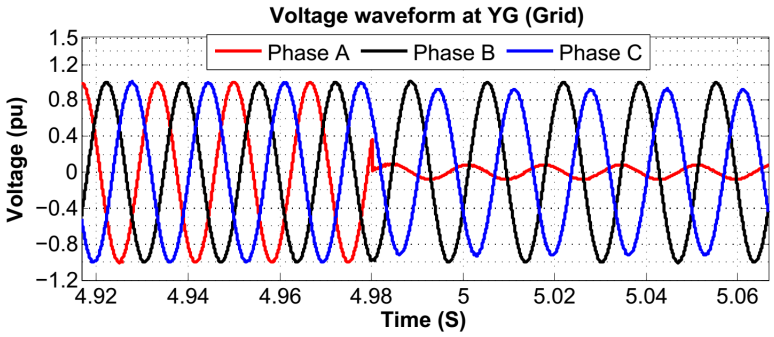

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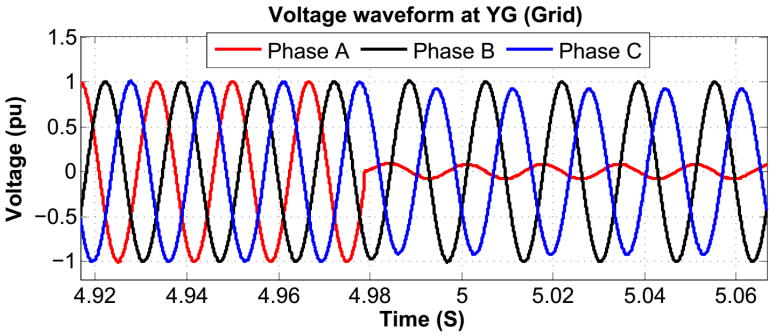


(d)

Figure 43: Voltage waveform at YG (grid) side of the coupling transformer for AG fault with inception angle with respect to Phase A voltage at (a) peak (b) 60^o (c) 30^o (d) 0^o

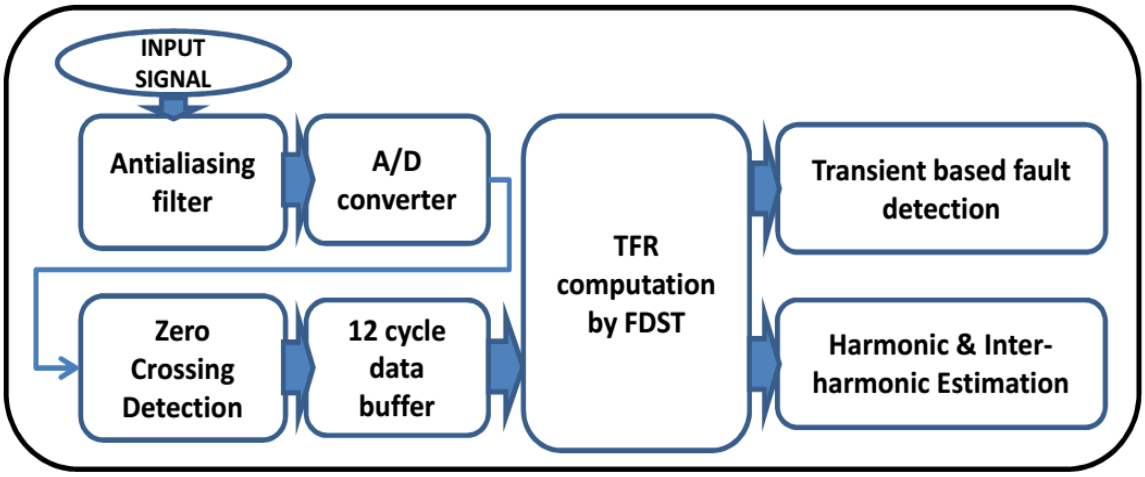


Figure 44: Block diagram of the monitoring framework

4.3 Simulation, Results and discussion

4.3.1 Simulated System

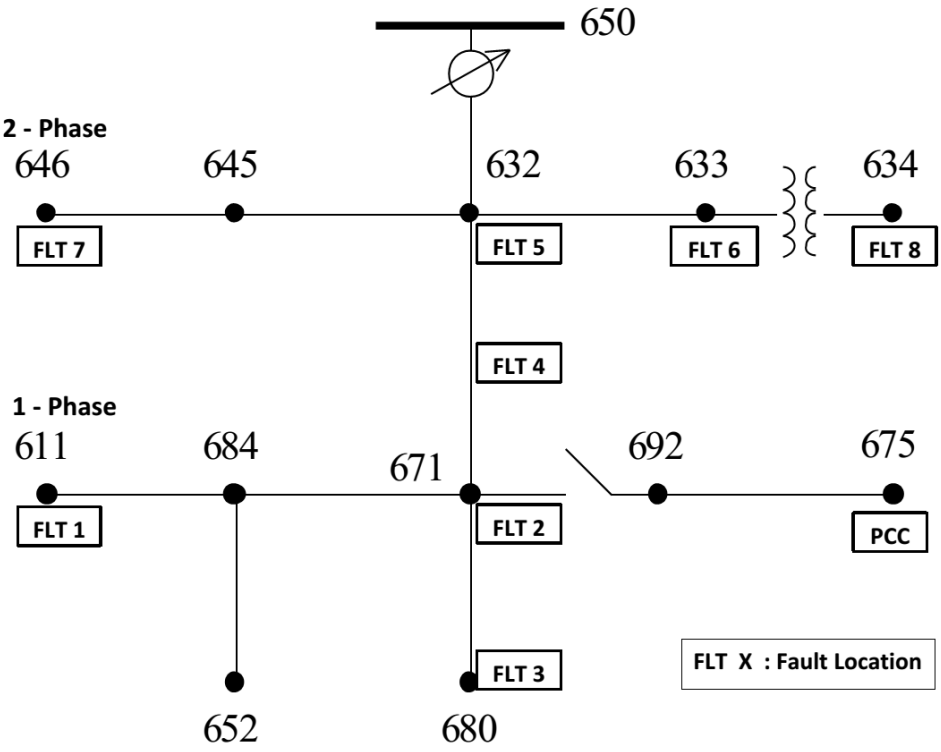


Figure 45: IEEE 13 node distribution system test feeder showing fault location and PCC.

The 100 kW three phase inverter described in section 4.1 was connected to the 13-node 4.16 kV distribution grid shown in Figure 45 at node 675 through a $480V/4.16kV$ $Delta/YG$ transformer. The primary (delta) side of the transformer was connected to the inverter output terminals. Observe that inverter itself does not provide a ground reference, but the transformer secondary is a zero sequence source. Node 650 is the substation source which is modeled as a grounded 4.16 kV source with $0.01 + j0.8$ Ω Thevenin impedance. Various types of faults were simulated at different buses of the system. The fault locations on the test feeder are marked in Figure 45. Different types of faults at different location, and cases of capacitor switchings were simulated in this test system.

Figure 46 - 47 shows the output current and voltage at the delta side and YG side of the transformer for a line-to-line (B-to-C) fault at node 646, with fault resistance of 0.5 Ω. The fault is created at 6 s and lasts for 0.1 s duration. Observe in Figure 46 that the current limiter is operating correctly. The sequence currents at the delta side (inverter) and YG side (grid) are shown in Figure 48 to emphasize that inverter produces no zero sequence currents and negligible negative sequence currents, which is according to design. Zero sequence currents on the YG side show that the test system has significant unbalance. This zero sequence current does not change after fault because of the nature of the fault. The positive sequence current on Δ sides is limited due to the current limiter, which also restricts the grid side

positive sequence current. Thus, the inverter performance is shown to be according to design when connected to the test distribution system.

4.3.2 Detection of Fault

Voltages and currents shown in Figure 46 - 47 indicate that faults introduce transients in the voltages and currents on the inverter side. It can also be seen that there is a significant voltage dip during faults. It is also expected that the zero sequence current on the YG side will significantly increase for all fault involving ground. Therefore a fault detection criterion based on each of these observations is conceived and tested, as described in the following subsections.

4.3.2.1 Detection with Transient signature

Looking at Figure 46, short duration transients can be observed in the delta side currents and voltages at the instant when the fault occurs (at 6 s), in all the three phases (most prominently in phase C). In order to detect the occurrence of fault, we attempt to quantify these transient signatures. Note that the YG side current and voltage waveforms carry no or very light transient signature, which conforms with the observations in Section 4.1.4.

The time-frequency representation of the current and voltage signals at the inverter terminals were calculated through FDST algorithm explained in 9. The intensity profile of dominant frequency components above 500 Hz was extracted as mentioned in Section 4.2.3, which captures the transient profile or envelope of the transient. The average intensity throughout the duration of transient is used as an indicator for occurrence of fault. Figure 49 shows the envelope of the extracted transient signature from the inverter output currents (shown in Figure 46) for the BC fault at node 646.

Total of 78 different fault cases were simulated at various locations and fault resistances. Figure 50 shows plots of the transient envelopes calculated from the current and voltage waveforms at the Δ side of the inverter for all the simulated faults. Based on this figure, a threshold value of $\rho = 0.05$ units for current and $\rho = 0.08$ units for voltage are taken as thresholds for detection of fault. Table 6 indicates the faults that could be detected by either current or voltage transient signatures. A Y in the *I Transients* column indicates that the fault could be detected from Current Transient signature. Similarly, Y in the *V Transients* column indicates that the fault could be detected from Voltage Transient signature. The average transient intensity for each case and each phase are summarized in Columns $5-7$ for current waveforms and in columns $9-11$, for voltages. For the fault cases that could be detected, the maximum and minimum value of the average transient intensity for transients in any of the phase was found to be 0.1583 and 0.0524 for current, and 0.2429 and 0.0802 for voltage respectively.

Out of the 78 cases 11 fault cases correspond to various faults created at node 634. This bus is connected to the grid via a $500kVA$, $480V/4.16kV$, YG/YG transformer. Because of isolation of the transformer the faults at 611 does not result in any transient signature for any type of fault. This is another limitation of transient based detection.

Out of the remaining 67 cases, the total number of different fault types detected by current/voltage transients are summarized in Table 7. In total 56 out of total 67 faults could be detected by current transient based detection and 57 out of total 67 faults could

be detected by voltage transient based detection. It can be observed from Table 6, that the **transient based technique can identify all the line-to-line and three phase faults**. The results for current or voltage transients are similar, however the voltage transient based detection may perform slightly better.

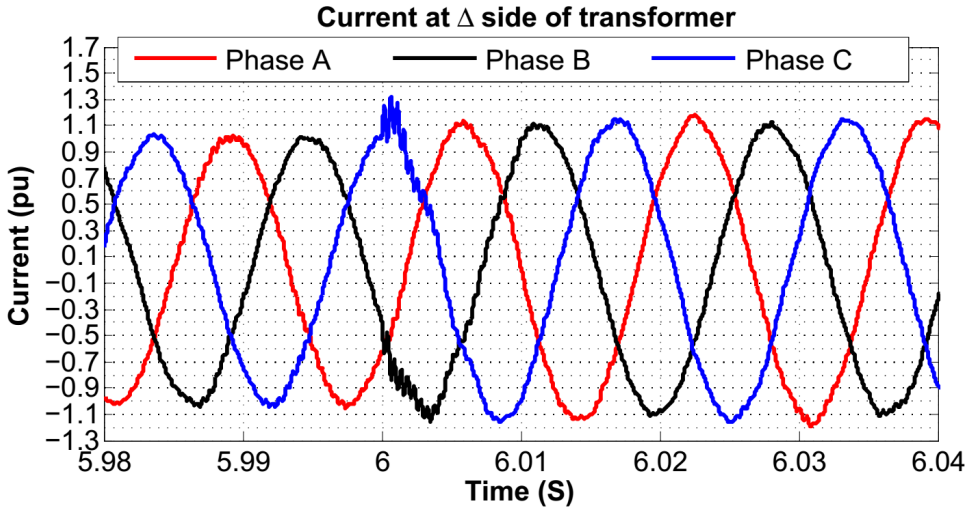
The effect of the fault inception angle for single phase faults are discussed in Section 4.1.5. Since in this simulation the fault inception time of 6 s lies very near to the zero crossing point of Phase A voltage waveform, observe in Table 6 that out of 9 phase A to ground faults, 7 don't get detected by either current or voltage transients. However, out of 8 Phase B to ground faults, 7 got detected, as the fault inception angle for phase B is different.

Until now we focused on transients in the inverter output voltage and current, which were caused by the filter capacitor dumping its energy due to sudden decrease in voltage in case of fault. This is because we are interested in detecting fault at the PCC of renewable generation. However, it is worth analyzing transients at other bus voltages in the system due to faults. This is because, fault currents contributed by inverter-interfaced sources may be too small to detect fault even at other system buses. This problem can be the worst for an islanded microgrid. Faults typically result in voltage transients, due to sudden change in current imposed on a (usually) inductive circuit, and the dynamics with the line capacitance.

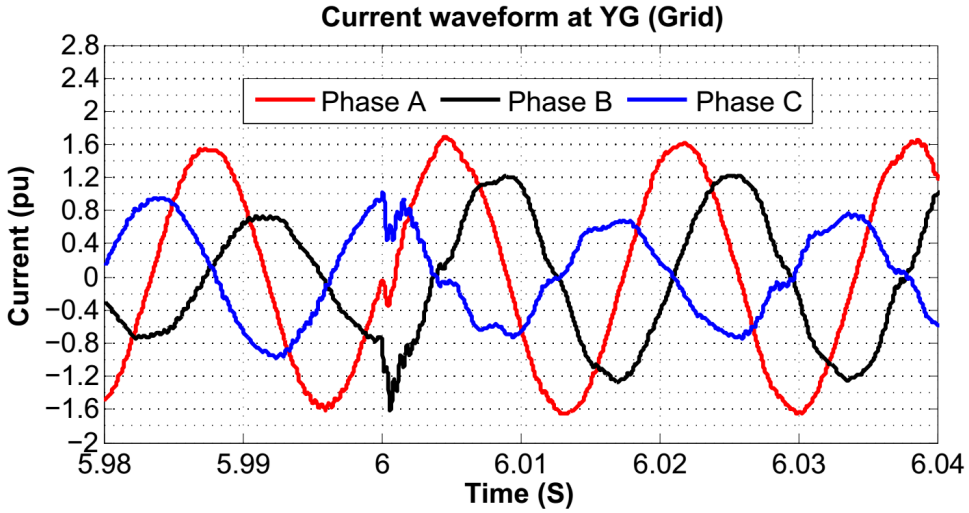
A B-C fault was created on feeder 632-671, and the voltages at node 671 were recorded. These are shown in Figure 51. Contrary to expectations, the inception of fault is not accompanied by significant transients in the voltage waveforms. This can be attributed to the highly resistive nature and short feeder-sections of this particular test feeder, which probably results in strong damping. *More studies are needed for this case to further explore this assumption.*

4.3.3 Sequence component based detection

As explained in Section 4.3.2.1, not all the faults resulted in transient signature. Figure 52 - 53 show the inverter output currents on the delta side, line voltages at delta side, and phase voltages at YG or grid side, for a phase-A-to-ground fault with fault resistance of 0.5Ω, at node 633. The fault occurs at 6 s, but no transient signature can be observed in inverter output current waveforms. The transient based fault detection fails in this case.

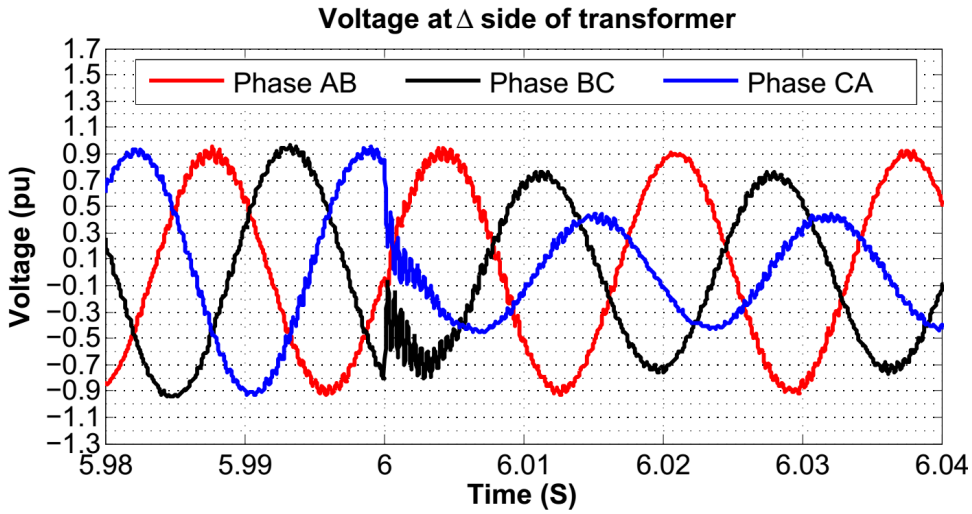


(a)

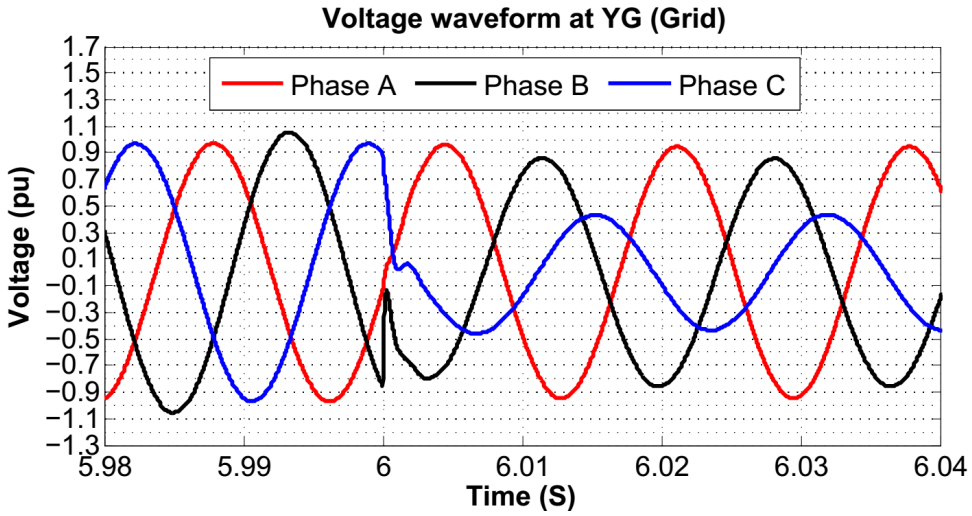


(b)

Figure 46: Current waveform at (a) delta side and (b) YG (grid) side of the coupling transformer for BC fault at node 646.

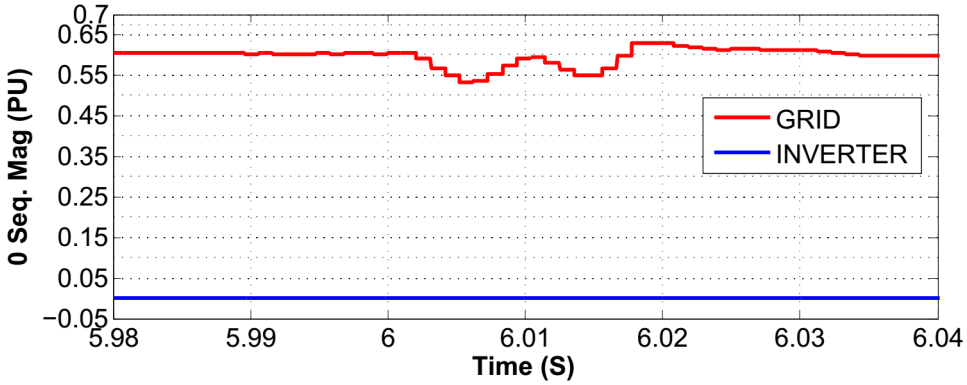


(a)

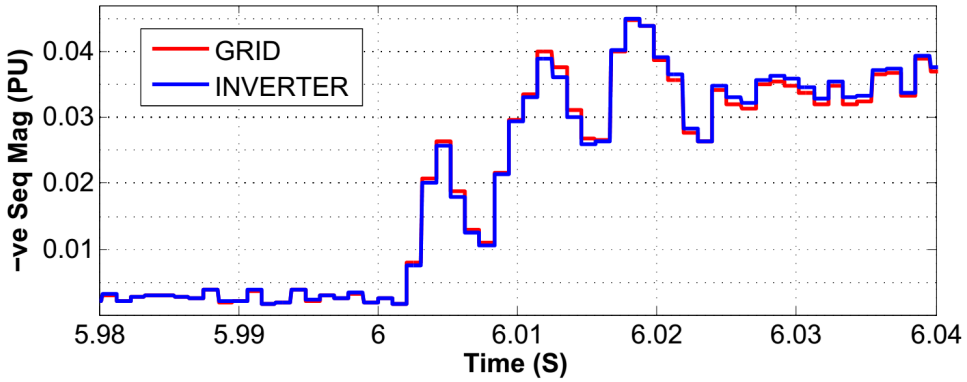


(b)

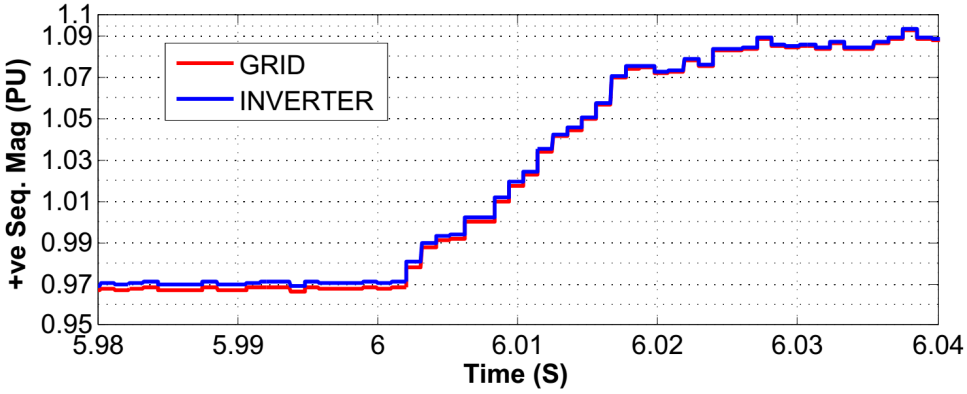
Figure 47: Voltage waveform at (a) delta side and (b) YG (grid) side of the coupling transformer for BC fault at node 646.



(a)



(b)



(c)

Figure 48: (a) Zero, (b) Negative and (c)Positive Sequence components of the currents at YG (grid) side of the coupling transformer for BC fault at node 646

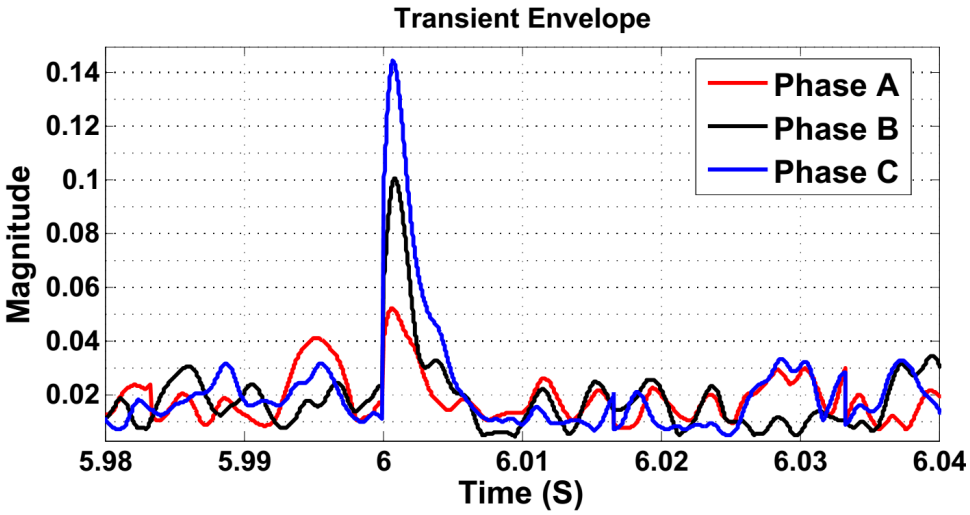
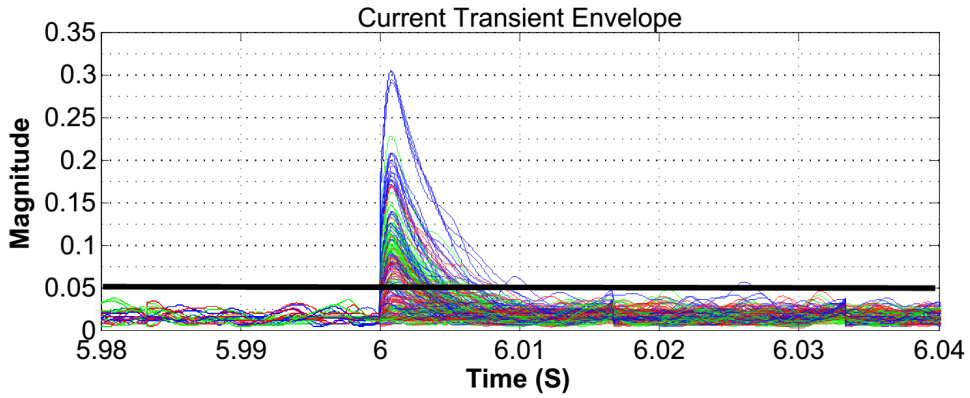
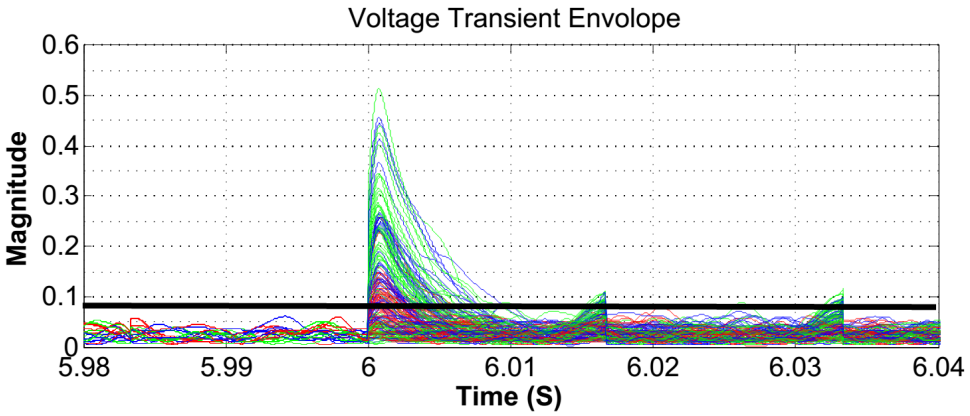


Figure 49: Envelope of transient signature for BC fault at node 646



(a)



(b)

Figure 50: Transient Envelope of the (a) Current and (b) Voltage waveforms at delta side of the coupling transformer for all the faults. The thick black line represents the threshold.

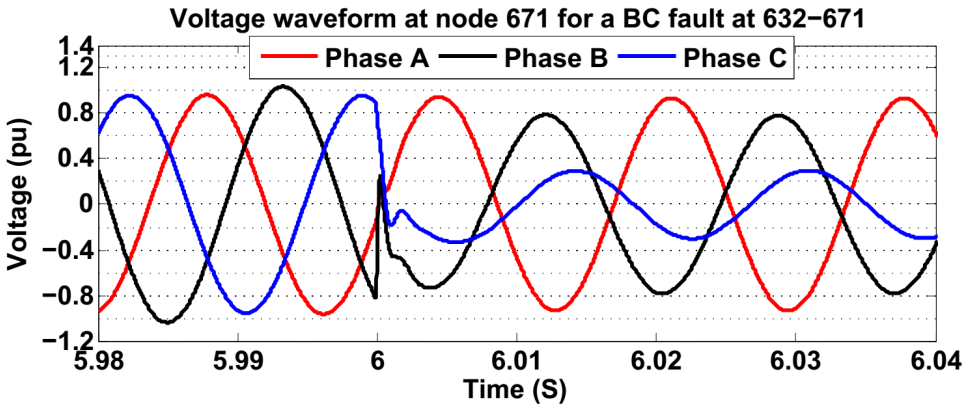
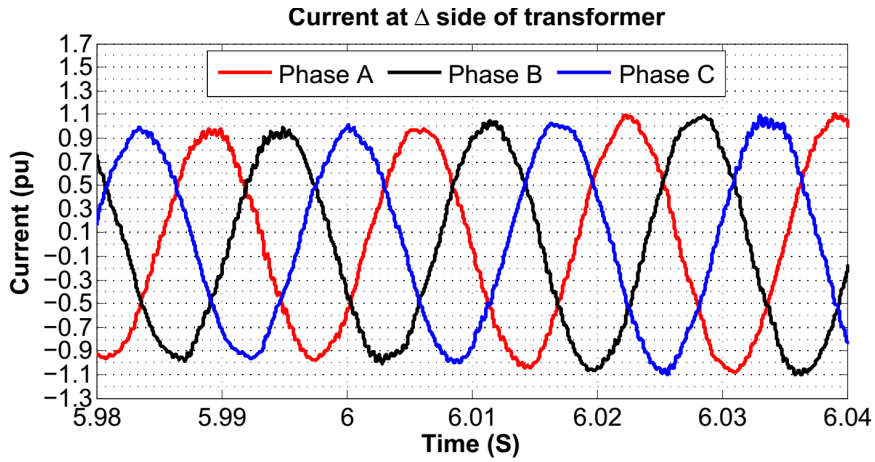
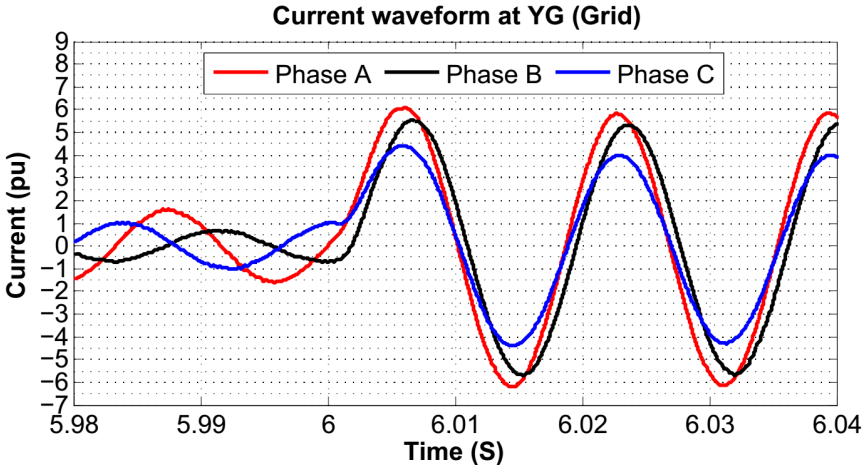


Figure 51: Voltages at node 671 for a B-C fault on feeder 632-671.

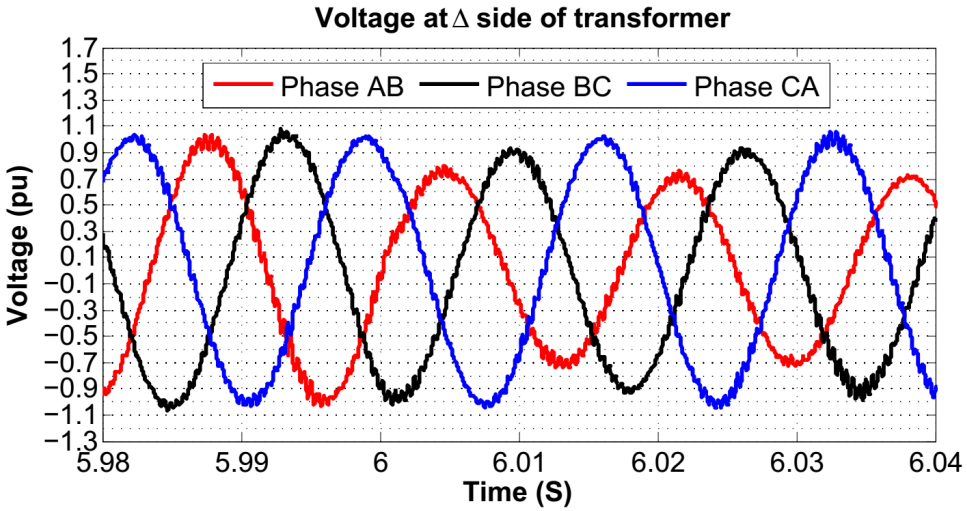


(a)

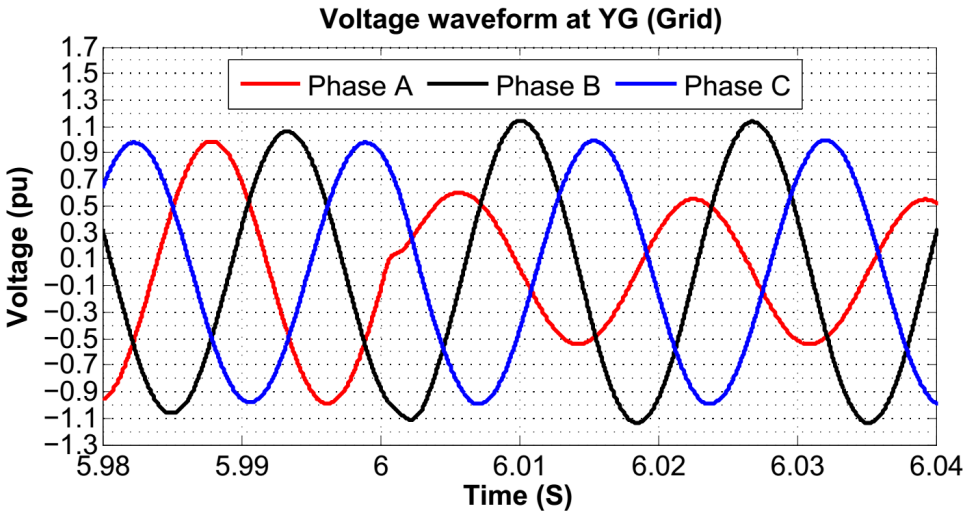


(b)

Figure 52: Current waveform at (a) delta side (b) YG (grid) side of the coupling transformer for AG fault at node 633.



(a)



(b)

Figure 53: Voltage waveform at (a) delta side, (b) YG (grid) side of the coupling transformer for AG fault at node 633.

The sequence components of current waveform at the grid side of inverter are shown in Figure 54. Again, the figure shows that the inverter is able to limit the positive sequence current, and does not inject any significant negative sequence current. However, since the YG winding is a zero sequence source, zero sequence component of the grid side current shoots up significantly during the fault (observe it is non-zero before fault due to the unbalance in the circuit), and results in much higher line currents on the grid side as well. This rise in zero sequence current was observed for all unbalanced ground faults. The minimum and maximum values of this rise were observed to be 4.4799 times and 12.85 times the steady state value respectively, considering all unbalanced grounded faults. Therefore, ground overcurrent relay with the conventional 200% threshold could detect all the line-to-ground and line-line-ground faults. *Transient and zero sequence based detection could detect all faults between themselves.*

4.3.4 Undervoltage based detection

It was also considered worthwhile to use voltage dip in the grid side as an indicator for fault. All faults resulted in significant voltage drop at the YG side of transformer. Voltage dip attains a minimum value of 0.1812 pu and maximum value of 0.7596 pu in any one of the phases, while considering all the 78 faults. Thus, an under voltage threshold of 0.8 pu can detect all the faults.

Table 6 lists all the fault cases simulated, and the fault detection technique that could identify each of them. A Y in columns 8 or $12-14$ indicates a success and N indicates failure. A summary of number of faults detected by each technique is presented in Table 7.

Sl. No	**Type of Fault**	**Location**	**Resistance (Ohm)**	I Trans. A	I Trans. B	I Trans. C	**I Transients**	V Trans. A	V Trans. B	V Trans. C	**V Transients**	**Zero Sequence**	**Voltage Dip**
1	ab	634	0.002	0	0	0	N	0	0	0	N	N	Y
2	ab	671	1	0	0.088	0.067	Y	0.121	0.135	0	Y	N	Y
3	ab	632	0.5	0	0.082	0.067	Y	0.102	0.114	0	Y	N	Y
4	ab	632-671	0.5	0	0.074	0.057	Y	0.114	0.133	0	Y	N	Y
5	ab	633	0.5	0	0.065	0	Y	0.095	0.098	0	Y	N	Y
6	ab	671	0.5	0	0.086	0.069	Y	0.124	0.14	0	Y	N	Y
7	ab	680	0.5	0	0.076	0.051	Y	0.107	0.116	0	Y	N	Y
8	abc	634	0.002	0	0	0	N	0	0	0	N	N	Y
9	abc	632	0.5	0.064	0.098	0.129	Y	0	0.139	0.135	Y	N	Y
10	abc	632-671	0.5	0.068	0.081	0.116	Y	0.083	0.152	0.143	Y	N	Y
11	abc	633	0.5	0	0.08	0.095	Y	0	0.128	0.129	Y	N	Y
12	abc	671	0.5	0.096	0.093	0.152	Y	0	0.18	0.194	Y	N	Y
13	abc	680	0.5	0.068	0.074	0.116	Y	0	0.143	0.151	Y	N	Y

14	abcg	634	0.002	0	0	0	N	0	0	0	N	N	Y
15	abcg	680	1	0.067	0.07	0.104	Y	0	0.153	0.151	Y	N	Y
16	abcg	632	0.5	0.066	0.089	0.122	Y	0	0.13	0.138	Y	N	Y
17	abcg	632-671	0.5	0.062	0.079	0.084	Y	0	0.16	0.175	Y	N	Y
18	abcg	633	0.5	0	0.084	0.098	Y	0	0.167	0.129	Y	N	Y
19	abcg	671	0.5	0.105	0.09	0.158	Y	0	0.192	0.243	Y	N	Y
20	abcg	680	0.5	0.069	0.074	0.114	Y	0	0.158	0.164	Y	N	Y
21	abg	634	0.002	0	0	0	N	0	0	0	N	Y	Y
22	abg	671	1	0	0.07	0.082	Y	0.089	0.138	0.107	Y	Y	Y
23	abg	632	0.5	0	0.09	0.084	Y	0.092	0.132	0.085	Y	Y	Y
24	abg	632-671	0.5	0	0.077	0.069	Y	0.11	0.157	0.091	Y	Y	Y
25	abg	633	0.5	0	0.081	0.064	Y	0.105	0.132	0	Y	Y	Y
26	abg	671	0.5	0	0.085	0.095	Y	0.093	0.158	0.112	Y	Y	Y
27	abg	680	0.5	0	0.078	0.07	Y	0.089	0.133	0.082	Y	Y	Y
28	ac	634	0.002	0	0	0	N	0	0	0	N	N	Y
29	ac	632	0.5	0.072	0	0	Y	0.116	0	0.1	Y	N	Y
30	ac	632-671	0.5	0.071	0.054	0	Y	0.11	0	0.105	Y	N	Y
31	ac	633	0.5	0.053	0	0	Y	0.084	0	0	Y	N	Y
32	ac	671	0.5	0.11	0.08	0.065	Y	0.159	0	0.163	Y	N	Y
33	ac	680	0.5	0.075	0.055	0	Y	0.119	0	0.11	Y	N	Y
34	acg	634	0.002	0	0	0	N	0	0	0	N	Y	Y
35	acg	632	0.5	0.068	0	0.053	Y	0.099	0	0.111	Y	Y	Y
36	acg	632-671	0.5	0.071	0	0.054	Y	0.096	0	0.108	Y	Y	Y
37	acg	633	0.5	0.053	0	0	Y	0.08	0	0	Y	Y	Y
38	acg	671	0.5	0.111	0.056	0.08	Y	0.152	0	0.175	Y	Y	Y
39	acg	680	0.5	0.076	0.053	0	Y	0.116	0	0.108	Y	Y	Y
40	ag	634	0.002	0	0	0	N	0	0	0	N	Y	Y
41	ag	611	0.002	0.073	0	0.068	Y	0.091	0	0.131	Y	Y	Y
42	ag	680	1	0	0	0	N	0	0	0	N	Y	Y
43	ag	632	0.5	0	0	0	N	0	0	0	N	Y	Y
44	ag	632-671	0.5	0	0	0	N	0	0	0	N	Y	Y
45	ag	633	0.5	0	0	0	N	0	0	0	N	Y	Y
46	ag	611	0.5	0.066	0	0.061	Y	0.085	0	0.115	Y	Y	Y
47	ag	671	0.5	0	0	0	N	0	0	0	N	Y	Y
48	ag	680	0.5	0	0	0	N	0	0	0	N	Y	Y
49	bc	634	0.002	0	0	0	N	0	0	0	N	N	Y
50	bc	632	0.5	0.057	0.101	0.128	Y	0	0.142	0.13	Y	N	Y
51	bc	632-671	0.5	0.06	0.083	0.105	Y	0.093	0.164	0.145	Y	N	Y

52	bc	633	0.5	0	0.087	0.09	Y	0.082	0.156	0.114	Y	N	Y
53	bc	646	0.5	0	0.072	0.088	Y	0	0.142	0.123	Y	N	Y
54	bc	671	0.5	0.065	0.134	0.146	Y	0.121	0.213	0.168	Y	N	Y
55	bc	680	0.5	0.059	0.088	0.121	Y	0.086	0.173	0.16	Y	N	Y
56	bcg	634	0.002	0	0	0	N	0	0	0	N	Y	Y
57	bcg	632	0.5	0.06	0.104	0.118	Y	0	0.182	0.153	Y	Y	Y
58	bcg	632	0.5	0.06	0.082	0.11	Y	0.086	0.189	0.175	Y	Y	Y
59	bcg	633	0.5	0	0.086	0.099	Y	0.081	0.166	0.128	Y	Y	Y
60	bcg	646	0.5	0	0.068	0.089	Y	0	0.144	0.122	Y	Y	Y
61	bcg	671	0.5	0.095	0.093	0.15	Y	0	0.211	0.228	Y	Y	Y
62	bcg	680	0.5	0.058	0.093	0.119	Y	0	0.19	0.162	Y	Y	Y
63	bg	634	0.002	0	0	0	N	0	0	0	N	Y	Y
64	bg	646	1	0	0.057	0.055	Y	0	0.101	0	Y	Y	Y
65	bg	632	0.5	0	0.084	0.083	Y	0.092	0.131	0.086	Y	Y	Y
66	bg	632-671	0.5	0	0.074	0.07	Y	0.099	0.148	0.093	Y	Y	Y
67	bg	633	0.5	0	0.076	0.065	Y	0.096	0.126	0	Y	Y	Y
68	bg	646	0.5	0	0.055	0.052	Y	0	0.099	0	Y	Y	Y
69	bg	671	0.5	0	0.082	0.094	Y	0.093	0.152	0.112	Y	Y	Y
70	bg	680	0.5	0	0.076	0.072	Y	0.087	0.135	0.085	Y	Y	Y
71	cg	634	0.002	0	0	0	N	0	0	0	N	Y	Y
72	cg	646	1	0	0	0	N	0	0	0	N	Y	Y
73	cg	632	0.5	0	0	0	N	0	0	0.087	Y	Y	Y
74	cg	632-671	0.5	0.052	0	0	Y	0	0	0.089	Y	Y	Y
75	cg	633	0.5	0	0	0	N	0	0	0	N	Y	Y
76	cg	646	0.5	0	0	0	N	0	0	0	N	Y	Y
77	cg	671	0.5	0.081	0	0.069	Y	0.107	0	0.136	Y	Y	Y
78	cg	680	0.5	0	0	0	N	0	0	0	N	Y	Y

Table 6: Faults detected by different detection techniques

Type of Fault	Total Simulated Cases	Detected with Current Transients	Detected with Voltage Transients	Zero Sequence Relays	Voltage Threshold
LG	25	11	12	**25**	**25**
LLG	20	**17**	**17**	**20**	**20**
LLLG	7	**6**	**6**	0	**7**
LL	20	**17**	**17**	0	**20**
LLL	6	**5**	**5**	0	**6**
All	78	56	57	45	**78**

Table 7: Summary of number of faults detected by different techniques

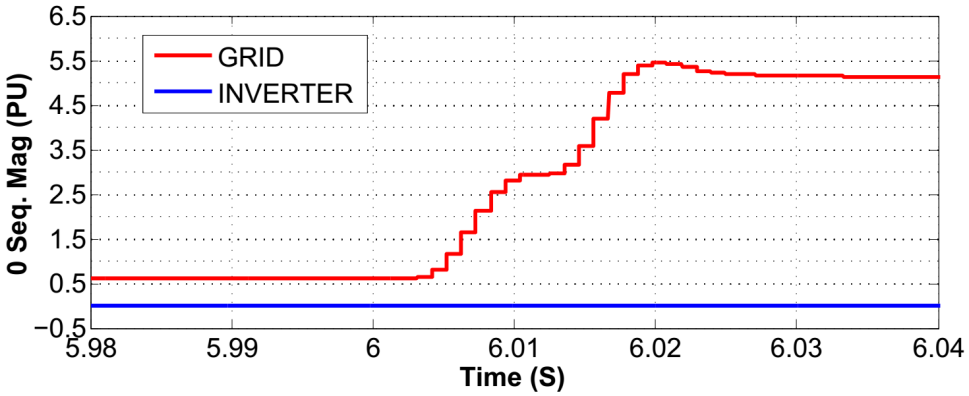
Sl. No	Type of Switching	Angle (degrees)	Location	I Trans. A	I Trans. B	I Trans. C	I Transients	V Trans. A	V Trans. B	V Trans. C	V Transients
1	ON	0	675	0.134	0.108	0.149	Y	0.092	0.234	0.267	Y
2	ON	90	675	0.174	0.178	0	Y	0.322	0.202	0.177	Y
3	ON	30	675	0.062	0.155	0.174	Y	0.143	0.309	0.228	Y
4	ON	0	611	0	0	0	N	0	0	0	N
5	ON	90	611	0	0	0	N	0	0	0	N
6	ON	60	611	0	0	0	N	0	0	0	N
7	OFF	0	675	0	0	0	N	0	0	0	N
8	OFF	90	675	0	0	0	N	0	0	0	N
9	OFF	0	611	0	0	0	N	0	0	0	N
10	OFF	90	611	0	0	0	N	0	0	0	N

Table 8: Faults detected by different detection techniques

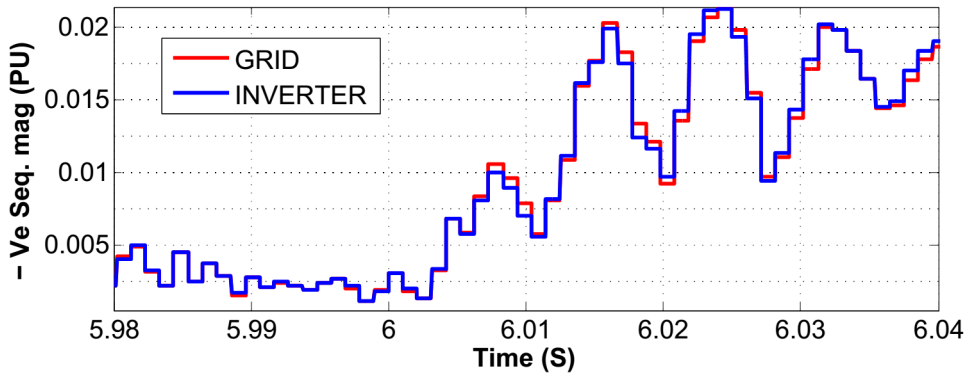
4.3.5 Sensitivity to capacitor switching

Although transient based technique can detect faults, they may exhibit sensitivity towards other events like capacitor switching. In order to verify this, 10 capacitor switching cases were created by switching ON and OFF the capacitor bank at node 675 and 611. The results of the detection are summarized in Table 8. None of the cases with capacitor switching at 611 (both ON and OFF) got detected with transients. In addition, capacitor switching OFF cases at node 675 didn't get detected. However, three capacitor switching ON cases were picked up by both current and voltage transients, obviously due to the proximity of node 675 to the PCC. The current and voltage transient envelopes for all the case are shown in Figure 55. It can be observed that signature of transients in case of capacitor switching is similar to that of fault, making them difficult to segregate from faults.This is a limitation of transient based protection.

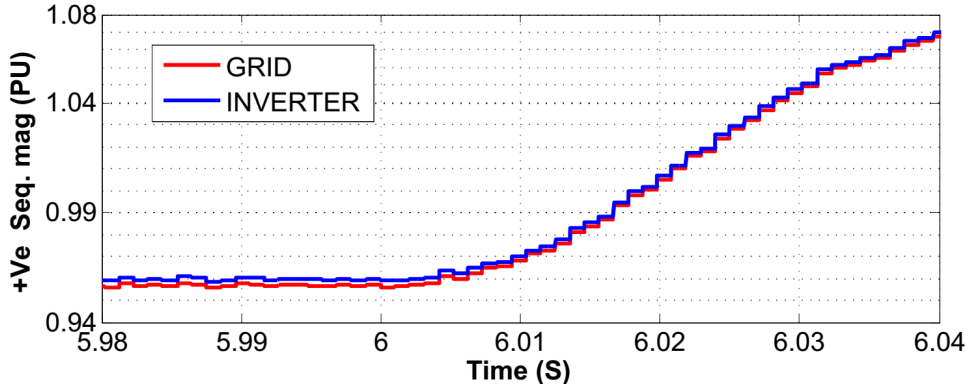
However, this can be easily remedied by monitoring the currents drawn by capacitors. The capacitor inrush current that rides the system fundamental current to cause confusion at the Δ side of PCC, is in itself devoid of the fundamental current. This is a well-known feature that is used by overcurrent relays protecting capacitor banks to distinguish between capacitor inrush and faults. A simple DFT of the capacitor current therefore can resolve this problem. Of course if we solely depend on the *local* information at the PCC, the confusion between some capacitor inrush cases and faults cannot be overcome. To illustrate this rationale, current through the capacitor at bus 675 for a Capacitor switching ON event is shown in Figure 56. Observe that, at 6 s, when the capacitor is switched on, the inrush current shoots up multiple folds (7 folds in the case shown) before settling down to steady state. Notice the absence of fundamental component during the inrush period.



(a)

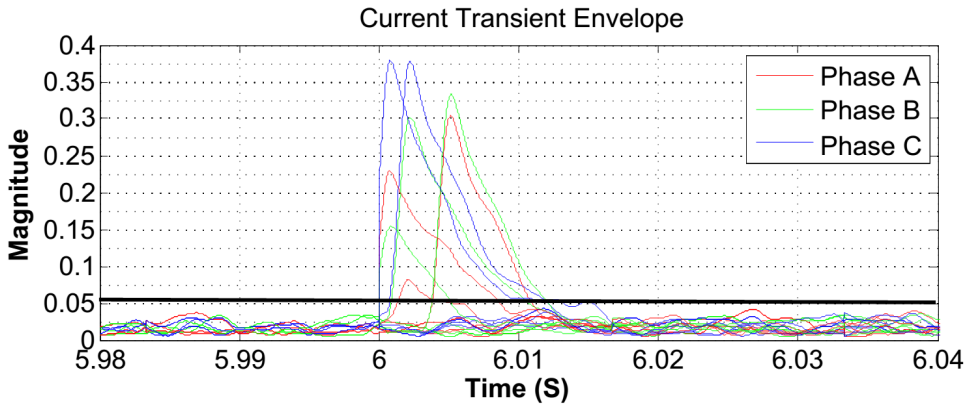


(b)

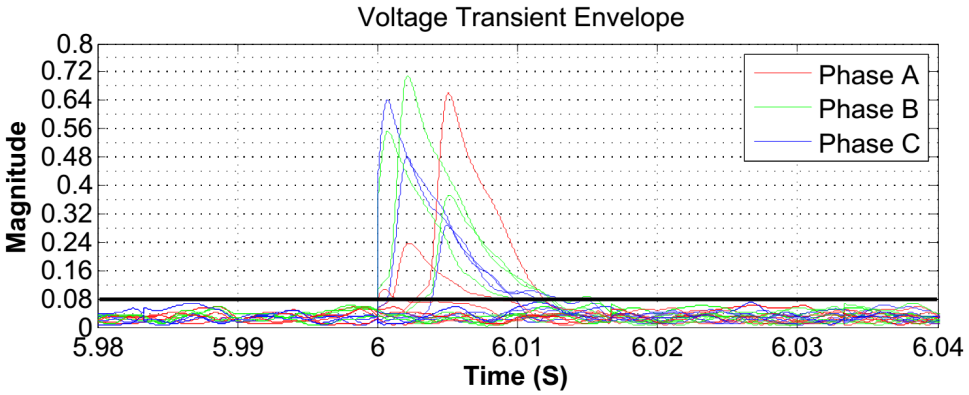


(c)

Figure 54: Sequence components of the voltages at YG (grid) side of the coupling transformer for AG fault at node 633



(a)



(b)

Figure 55: Transient Envelope of (a) the current waveforms, and (b) the voltage waveforms at delta side of the coupling transformer for capacitor switching events

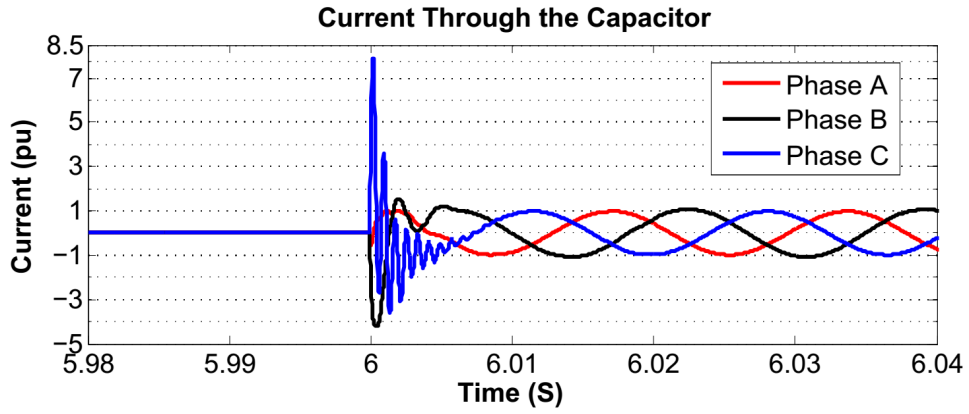


Figure 56: Current drawn by capacitor bank at bus 675 during switching ON.

4.4 Conclusion

In this section, a three-phase inverter was modeled in details and implemented in time domain. This inverter was connected to a 13-node IEEE test distribution feeder for fault analysis in order to derive insights into protection. The effectiveness of transient based fault detection technique relies on the transient signature. Some faults, particularly single phase to ground faults, do not give rise to significant transient signature, masking their detection by transient based technique. Another limitation of transient based technique is their sensitiveness towards capacitor switching, which could be circumvented by monitoring the current drawn by the capacitor. All the unbalanced ground faults can be detected by a zero sequence relay at the PCC due to the YG connection of transformer secondary. The detection based on undervoltage on any of the phase was found to work for all the faults. This shows that a combination of these three approaches should provide reliable fault detection at the inverter terminals. For detecting faults at any bus of the system, same criteria should work, however, contrary to expectations, faults did not create significant transients in bus voltages. This may be due to the specific nature of the test system, and needs more investigation. The next phase of work will focus on the behavior of grid during faults when multiple inverters are connected. This is nontrivial because the individual controls of these inverters may create instability. Reduced short circuit models may need to be developed, validated, and implemented based on the insight gained into the inverter performance. In addition, the next phase will also look at islanded microgrids, where source current is absent during faults. After this modeling and the ensuing results, reliable protection methods will be designed and tested.

5 Conclusions

The overall objective of this project is to investigate the challenges facing efficient microgrid protection design and to develop protection schemes for variety of microgrid configurations including radial, mesh and dynamic topology microgrids. It was shown as part of this project that there is a gap in the available microgrid protection methods. The only credible protection solution available in literature for low-fault inverter-dominated microgrids is the differential protection scheme which represents a robust transmission-grade protection solution but at a very high cost. Therefore, there is a need to develop microgrid-specific protection schemes which are non-overcurrent based to ensure efficient operation for low-fault microgrids but also are not element-based to minimize the associated cost and ensure applicability in the field. Based on this conclusion, two non-overcurrent protection schemes were investigated as part of this project; impedance-based protection and transient-based protection.

Future work includes analysis of microgrid protection design under heavy inverter-interfaced DERs and further development of non-overcurrent protection schemes. On the analysis front, we will investigate the impact of high penetration of DERs on the operation of fundamental protection system elements. In particular, we will investigate the performance of directional and impedance elements under high penetration of DERs and study the interactions between inverter-dominated microgrid protection and the hosting DS protection. The performance of inverter-dominated microgrid protection for faults on the utility side could be challenging due to the limited fault current of the microgrid. Moreover, we will continue the development of non-overcurrent protection schemes particularly; impedance-based protection and communication-assisted protection. Hardware-in-the-loop tests will be conducted for the proposed impedance-based protection scheme to validate the performance of the scheme under different microgrid configurations. Development of communication-assisted protection schemes for microgrids will be carried out potentially by analyzing transient-signatures of faults.

References

[1] E. Sortomme, S. S. Venkata, and J. Mitra, "Microgrid protection using communication-assisted digital relays," *IEEE Transactions on Power Delivery*, vol. 25, no. 4, pp. 2789–2796, 2010.

[2] P. M. Anderson, *Power System Protection*. Wiley-IEEE Press, 1999.

[3] A. Yazdani and R. Iravani, *Voltage-sourced converters in power systems: modeling, control, and applications*. John Wiley & Sons, 2010.

[4] R. H. Lasseter, "Microgrids," in *Power Engineering Society Winter Meeting, 2002. IEEE*, vol. 1, pp. 305–308 vol.1, 2002.

[5] T. Ustun, C. Ozansoy, and A. Ustun, "Fault current coefficient and time delay assignment for microgrid protection system with central protection unit," *Power Systems, IEEE Transactions on*, vol. 28, pp. 598–606, May 2013.

[6] T. Ustun, C. Ozansoy, and A. Zayegh, "Modeling of a centralized microgrid protection system and distributed energy resources according to iec 61850-7-420," *Power Systems, IEEE Transactions on*, vol. 27, pp. 1560–1567, Aug 2012.

[7] H. Laaksonen, D. Ishchenko, and A. Oudalov, "Adaptive protection and microgrid control design for hailuoto island," *IEEE Transactions on Smart Grid*, vol. 5, pp. 1486–1493, May 2014.

[8] H. Al-Nasseri, M. A. Redfern, and F. Li, "A voltage based protection for micro-grids containing power electronic converters," in *2006 IEEE Power Engineering Society General Meeting*, pp. 7 pp.–, 2006.

[9] M. Zamani, T. Sidhu, and A. Yazdani, "A protection strategy and microprocessor-based relay for low-voltage microgrids," *Power Delivery, IEEE Transactions on*, vol. 26, pp. 1873–1883, July 2011.

[10] M. A. Zamani, A. Yazdani, and T. S. Sidhu, "A communication-assisted protection strategy for inverter-based medium-voltage microgrids," *IEEE Transactions on Smart Grid*, vol. 3, pp. 2088–2099, Dec 2012.

[11] E. Casagrande, W. L. Woon, H. H. Zeineldin, and D. Svetinovic, "A differential sequence component protection scheme for microgrids with inverter-based distributed generators," *IEEE Transactions on Smart Grid*, vol. 5, pp. 29–37, Jan 2014.

[12] M. Dewadasa, A. Ghosh, G. Ledwich, and M. Wishart, "Fault isolation in distributed generation connected distribution networks," *IET Generation, Transmission Distribution*, vol. 5, pp. 1053–1061, October 2011.

[13] X. Li, A. Dyśko, and G. M. Burt, "Traveling wave-based protection scheme for inverter-dominated microgrid using mathematical morphology," *IEEE Transactions on Smart Grid*, vol. 5, pp. 2211–2218, Sept 2014.

[14] S. Saleh and R. Ahshan, "Digital multi-relay protection for micro-grid systems," in *Industry Applications Society Annual Meeting (IAS), 2012 IEEE*, pp. 1–8, Oct 2012.

[15] S. Saleh, "Signature-coordinated digital multirelay protection for microgrid systems," *Power Electronics, IEEE Transactions on*, vol. 29, pp. 4614–4623, Sept 2014.

[16] M. E. Nassar and M. M. A. Salama, "Adaptive self-adequate microgrids using dynamic boundaries," *IEEE Transactions on Smart Grid*, vol. 7, pp. 105–113, Jan 2016.

[17] Z. Wang and J. Wang, "Self-healing resilient distribution systems based on sectionalization into microgrids," *IEEE Transactions on Power Systems*, vol. 30, pp. 3139–3149, Nov 2015.

[18] C. Chen, J. Wang, F. Qiu, and D. Zhao, "Resilient distribution system by microgrids formation after natural disasters," *IEEE Transactions on Smart Grid*, vol. 7, pp. 958–966, March 2016.

[19] K. Zimmerman and D. Costello, "Fundamentals and improvements for directional relays," in *Protective Relay Engineers, 2010 63rd Annual Conference for*, pp. 1–12, March 2010.

[20] J. L. Blackburn, *Protective Relaying: Principles and Applications*. CRC Press, 2006.

[21] *Alstom Grid, Network Protection and Automation Guide*. 2011.

[22] S. Brahma, J. Trejo, and J. Stamp, "Insight into microgrid protection," in *Innovative Smart Grid Technologies Conference Europe (ISGT-Europe), 2014 IEEE PES*, pp. 1–6, Oct 2014.

[23] Z. Ye, R. Walling, L. Garces, R. Zhou, L. Li, and T. Wang, "Study and development of anti-islanding control for grid-connected inverters," *National Renewable Energy Laboratory*, 2004.

[24] E. Muljadi, M. Singh, and V. Gevorgian, *User Guide for PV Dynamic Model Simulation Written on PSCAD Platform*. National Renewable Energy Laboratory, 2014.

[25] N. R. Zargari and G. Joos, "Performance investigation of a current-controlled voltage-regulated pwm rectifier in rotating and stationary frames," *IEEE Transactions on Industrial Electronics*, vol. 42, pp. 396–401, Aug 1995.

[26] M. Chaudhary, *PhD Dissertation: Investigating Short Circuit Models for Wind Turbine Generators*. New Mexico State University, 2013.

[27] M. Prodanovic and T. C. Green, "Control and filter design of three-phase inverters for high power quality grid connection," *IEEE transactions on Power Electronics*, vol. 18, no. 1, pp. 373–380, 2003.

[28] R. G. Stockwell, L. Mansinha, and R. Lowe, "Localization of the complex spectrum: the S transform," *IEEE Transactions on Signal Processing*, vol. 44, no. 4, pp. 998–1001, 1996.

[29] M. Biswal and P. Dash, "Estimation of time-varying power quality indices with an adaptive window-based fast generalised s-transform," *IET Science, Measurement & Technology*, vol. 6, no. 4, pp. 189–197, 2012.

[30] "General guide on harmonics and interharmonics measurements for power supply systems and equipment connected thereto," *IEC 61000-4-7 Std*, 2002.

[31] "IEEE recommended practice and requirements for harmonic control in electric power systems," *IEEE Std 519-2014 (Revision of IEEE Std 519-1992)*, pp. 1–29, June 2014.

[32] R. Wall, "Simple methods for detecting zero crossing," in *Proceedings of The 29th Annual Conference of the IEEE Industrial Electronics Society Paper*, vol. 291, p. 1, 2003.

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