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Single-electron-occupation metal-oxide-semiconductor quantum dots formed from efficient poly-silicon gate layout

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Abstract

We introduce a silicon metal-oxide-semiconductor quantum dot structure that achieves dot-reservoir tunnel coupling control without a dedicated barrier gate. The elementary structure consists of two accumulation gates separated spatially by a gap, one gate accumulating a reservoir and the other a quantum dot. Control of the tunnel rate between the dot and the reservoir across the gap is demonstrated in the single electron regime by varying the reservoir accumulation gate voltage while compensating with the dot accumulation gate voltage. The method is then applied to a quantum dot connected in series to source and drain reservoirs, enabling transport down to the single electron regime. Finally, tuning of the valley splitting with the dot accumulation gate voltage is observed. This split accumulation gate structure creates silicon quantum dots of similar characteristics to other realizations but with less electrodes, in a single gate stack subtractive fabrication process that is fully compatible with silicon foundry manufacturing.

INTRODUCTION

Spin qubits in semiconductor quantum dots (QD) are strong contenders for quantum computing [LossDiVincenzo1998]. Silicon is emerging as a favored material for this application because of its long spin coherence [Tyryshkin2003, Witzel2010, Abe2010, Maune2012, Wu2014, Kawakami2014, Veldhorst2014] and the foundational resources of the microelectronics industry, which offers the potential to accelerate the development of many QD quantum processors [Vandersypen2016]. There has been rapid progress in lithographic Si QD fabrication and performance over the last five years [Eng2016, Kawakami2014, Veldhorst2014, Zajac2015, Takeda2016]. However, challenges in reproducibility, lithographic location of the QD and optimization of multi-QD arrays has represented a challenge for multi-qubit demonstrations using Si QDs [Borselli2011b, Nordberg2009, Thorbeck2012, Veldhorst2015]. A reliable Si QD platform, sufficient to extend beyond two-qubit coupling demonstrations [Veldhorst2015] is an immediate challenge for the silicon quantum computing community.

Three properties that are commonly necessary for a reliable QD design are: (1) a *well-isolated two-level energy subspace*; (2) *well-controlled dot-reservoir tunnel barriers* (i.e. tunable in the few-electron regime); and (3) *extensible fabrication* (e.g. tiled layout, and repeatable with respect to critical parameters). For Si QD implementations, qubits are predominantly pursued as lithographically gated structures on either a strained-Si (sSi)/SiGe or metal-oxide-semiconductor (MOS) stack. Either implementation faces challenges related to one or several of the aforementioned properties. For example, up to nine QDs in a linear array have been fabricated in sSi/SiGe with repeatable parameters (i.e., charging and orbital energy, lever arm) [Zajac2016]. However, for electrons in Si, the conduction band valley splitting can be small. Erratic valley splittings in neighboring QDs have been reported in the sSi/SiGe system [Borselli2011, Zajac2015] compromising the formation of a well-isolated two-level energy subspace. In contrast, anecdotal reports of tunable valley splitting in MOS suggest that this system might provide both reliable and tunable valley splitting [Yang2013, Gamble2016]. Unfortunately, the larger disorder potential of the more imperfect MOS interface [Nordberg2009, Thorbeck2012] and the relatively large effective mass in Si increases susceptibility to unintentional localization [Veldhorst2015, Thorbeck2012]. Doubts persist about achieving successful multi-QD networks in MOS, despite the utilization of a predominant local accumulation design [Lim2009] that favors an additive, multi-metal-level process flow in an attempt to completely control the surface potential around the QD, resulting in strongly confined electrons [Yang2013, Zajac2015].

In this study, we present: (1) a MOS QD design that successfully produces single electron occupation with tunable valley splitting; (2) provides a wide range of tunnel coupling tuning of the dot-reservoir tunnel barrier in the few electron regime and (3) uses an efficient single-layer, subtractive [WolfTauber], poly-silicon gated process flow. Polysilicon gates promise the potential for reduced charge noise [Zimmerman2014], reduced stress [Thorbeck2015], improved reliability [Yu1979] and overall less challenging processing than Al gates [WolfTauber]. A further observation of this efficient design concept is that orthogonal tunnel barrier control (i.e. well-decoupled from dot occupation control) can be achieved without a dedicated barrier gate. It is sufficient to form a gap in the metal layer and tune the barrier with the reservoir accumulation and QD accumulation gates. The response of the tunnel rate to voltage tuning is of similar magnitude as designs with a dedicated barrier gate. The design concept is validated in two different layouts. Each layout is measured in a different laboratory providing an additional level of confidence in the repeatability of the design concept in achieving the three critical properties for QDs.

DEVICES AND METHODOLOGY

The devices are fabricated using the Sandia National Laboratories MOS quantum dot fabrication technology [Tracy2009]. The gate stack consists of a float zone substrate, 35 nm gate oxide and a degenerately As-doped polysilicon gate (shown in Fig 1a). The nanostructure is defined in the polysilicon gate stack by electron-beam lithography and dry etching. Contacts to ohmics and the poly-silicon gates are made with Al through vias in the field oxide. A forming gas anneal is done as a last step to reduce interface defect densities. Additional details on the fabrication process can be found in Appendix A. The gate oxide properties have been characterized in a Hall bar fabricated on the same wafer as the samples. Peak mobility, critical density [Tracy2009, Borselli2011b], scattering charge density [DasSarma2013, Tracy2009], interface roughness and interface correlation length [Mazzoni1999] were measured for the wafers used for each of the devices and are indicated in Table 1 of Appendix B.

The basic element of the devices is a split accumulation gate, designated AD and AR in Fig 1a. Application of positive voltages on AR and AD forms a reservoir and a quantum dot, respectively, at the Si/SiO_2 interface, in a similar fashion to well-established local enhancement devices [Lim2009, Borselli2014, Veldhorst2014, Zajac2016]. The electrons accumulated under AR originate from an Ohmic contact located several microns away to prevent disorder in the doped region from affecting the active area. The spatial gap between AD and AR creates a natural tunnel barrier between the dot and the reservoir, with tunnel rate Γ. We argue that in a split accumulation gate design, the reservoir accumulation gate AR can control the dot-reservoir tunnel rate Γ efficiently, when compensated by the dot accumulation gate AD to keep the dot chemical potential, μ_{dot}, fixed. This is in contrast with the more predominant method for dot-reservoir tunnel rate control in local accumulation designs, for which a dedicated barrier gate is placed directly on top of the tunnel barrier, overlapping with AD and AR to minimize dot size (compensation is also needed here to maintain dot occupation). By using AR for Γ tuning, the dedicated barrier gate becomes superfluous, allowing a single layer, no lift-off fabrication process.

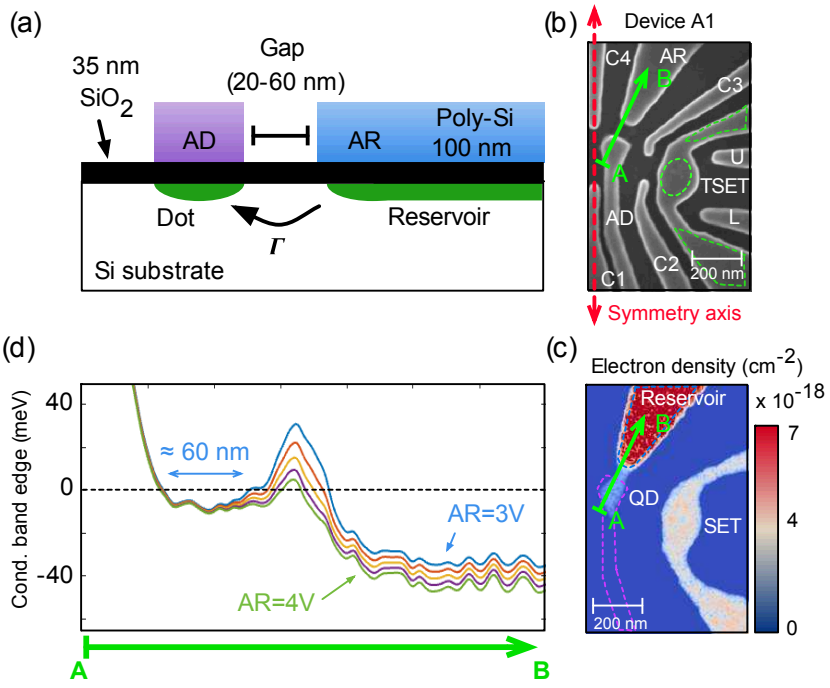

Figure 1: (a) Schematics of the elementary structure for the minimalist local accumulation layout. The transverse cut corresponds to the A-B axis indicated by the green arrow in (b). (b) False-color scanning electron micrograph (SEM) of single-lead device A1, a double quantum dot operated in single-dot mode by using only the right half. The MOS structure is composed of a single poly-silicon gate stack 100 nm thick, a 35 nm SiO_2 gate oxide and a 10 000 Ohm-cm n-type silicon wafer. AR is the reservoir accumulation gate, and AD is the dot accumulation gate. C1, C2, C3, and C4 are confinement gates, necessary in this entirely 2D (planar) structure to create a circular dot, as the extension of AD away from the leads must be depleted. The gate TSET accumulates electrons to form the SET, and U and L help define its source and drain barriers. A mirror structure, including gates AD', AR', C2', C3', TSET', U', and L', is located on the other side of the symmetry axis (see Fig 5 in Appendix B), but is kept inactivated for most measurements. (c) Simulated density, representing approximately 20 electrons in the dot. The voltages applied to the gates in this regime are indicated in Table 2, Appendix B. (d) Simulated conduction band edge profile along the green arrow A-B from Fig 1c, for V_{AR} varying from 3 to 4V with 0.25 V increments, with other parameters kept constant. Traces are smoothed to minimize granularity from the meshing process.

We present results gathered from three distinct devices based on the split gate design: labeled A1, A2 and B. A detailed account of the characteristics of the three devices is presented in Table 1, Appendix B. Devices A1 and A2 are double quantum dots in a single-lead configuration (i.e., only one reservoir is connected to each dot) that we operate in the single-dot regime, by activating only one half of the device (see Fig 1b). No transport measurements are performed on A1 and A2, and all data is acquired through charge sensing. Devices A1 and A2 have the same layout, with differences in scale only (see Table 1 and Fig 5 in Appendix B). Device B (Fig 3a) is a single quantum dot device in a double-lead configuration (the dot is connected to two reservoirs), allowing both transport and charge sensing measurements. Devices A1 and A2 measurements are performed using the proximal SET as a charge sensor with standard lock-in technique, at 16.4 Hz and 19 Hz respectively, with a source-drain bias of 100 μV applied to the SET channel. Single shot measurements on device A1 are realized through RF reflectometry, using a carrier wave of 180 MHz and a 326 kHz bandwidth

[Muller2012]. For device B, measurements also rely on standard lock-in technique at 492.6 Hz, with a source-drain bias of 50 μV rms applied to the SET channel for charge sensing, and to the QD channel for transport.

Experiments are performed in two distinct laboratories, Université de Sherbrooke (devices A1 and A2) and Sandia National Laboratories (device B), in dilution refrigerators sustaining electronic temperature of 125 mK and 160 mK, respectively. In the limited testing of standard measurements, the samples are found to be robust to thermal cycles (i.e., little threshold shift) and no devices were visually altered by the long-distance shipping (e.g., damage from electrostatic discharge was not observed). The devices are also electrically stable, with the drift of the quantum dot chemical potential in device B characterized as approximately 5.3 ± 0.5 μeV standard deviation over a 150 hour period.

To illustrate the operation of the split accumulation gate, we have performed Thomas-Fermi numerical simulations [Gao2013] of a single-lead device (device A1, Fig. 1b) using the corresponding three-dimensional MOS structure and operating gate voltages as input parameters. Figure 1c shows the simulated electron density at the substrate-oxide interface when the device is experimentally set in a ~20 electrons regime. A reservoir is formed under AR gate, and a quantum dot under the tip of AD gate, separated by a region of slightly lower density in between, which constitutes a tunnel barrier. Tunnel barrier control using the reservoir gate voltage, V_{AR}, is suggested by simulations of the potential along the dot-reservoir axis (Fig 1d). Indeed, as a function of V_{AR}, the profiles present a tunnel barrier of varying height and width between the dot and reservoir. Variation in V_{AR} shifts the conduction band edge directly. The effect is most pronounced under AR and gradually diminishes when approaching the bottom of the quantum dot well under AD. The simulation highlights that the reservoir gate alone can strongly influence the tunnel barrier height with relatively small shift in the potential of the QD.

In practice, varying the voltage on two electrodes is necessary to achieve the few-electron regime with measurable tunnel rates. While one gate will affect mostly the dot occupation, another will act more strongly on the tunnel rate. The two electrode voltages are chosen to compensate one another so that a relatively constant tunnel rate is maintained while the QD occupation is reduced (or vice-versa). Therefore, a sufficient orthogonality between tuning of the tunnel rate and control of the dot occupancy is imperative to maximize the operation range of the device [Ciorga2000]. This operation principle, which we refer to as *tuning orthogonality*, is demonstrated next for the split gate, without an electrode specifically dedicated to barrier tuning.

RESULTS AND ANALYSIS

Figure 2a presents a charge stability diagram obtained by sweeping the AR and AD gate voltages (V_{AR} and V_{AD} respectively) on a single-lead device. The quantum dot occupancy can be tuned down to the single electron regime as indicated by the absence of further transitions on the bottom left of the diagram, and confirmed with spin filling from magnetospectroscopy. The effect of V_{AR} on the tunnel rate Γ is initially visible through the

charge transitions, which go from a “smooth” appearance at high $V_{AR,}$ when Γ is high compared to the measurement rate, to a speckled appearance at low V_{AR}, when Γ is of the order of the measurement rate or lower [Thalakulam2010].

Another feature of this stability diagram is the curvature visible in the dot transitions, which we believe originates from the gradual decreases of the AR gate capacitance to the dot, $C_{AR\text{-}dot}$, as the reservoir fills up with electrons. To illustrate this effect, we extract the capacitance ratio $C_{AR\text{-}dot}/C_{AD\text{-}dot}$ =-1/*m* [GrabertDevoret1992] from the slope *m* of the transitions in the stability diagram (Fig 2a), as shown in the inset of Fig 2a. This leads us to argue that the accumulation of charges in the reservoir contributes to the tuning orthogonality of the split gate structure by effectively reducing the AR-dot lever arm at higher V_{AR}. A similar dependence of the capacitance ratio is also observed in numerical simulations, but the agreement is only qualitative, due in part to the limitations of the semi-classical simulation and the slight differences between the simulated and measured devices.

To quantify the capability of the split gate to provide well-controlled tunnel barriers, we examine the dot-reservoir tunnel rate Γ along the N=0$\rightarrow$N=1 charge transition, as V_{AR} is compensated with V_{AD} (Fig. 2b). Two data sets are combined,diamond and filled circles respectively, to include a larger span of tunnel rates. The data sets were taken at different voltages applied to a surrounding gate, resulting in a 1.5 decade offset in tunnel rates. This offset is subtracted (hollow circles) revealing an exponential dependence of Γ with V_{AR} [Borselli2015, Maclean2007]. This result indicates that the tunnel rate can be tuned over several orders of magnitudes with AR while maintaining single charge occupation in the QD.

From the slope of the exponential fit, we extract a gate response of $\Delta\Gamma_{AR,AD}$ = 5.9 $\pm$ 0.7 decade/V_{AR}, defined as the variation in dot-reservoir tunnel rate induced by a change of one Volt on gate AR, when compensated by gate AD to keep the dot chemical potential fixed. We can remove the device geometry specific capacitance by converting voltage change to change in chemical potential of the QD, $\Delta\mu_{dot}$. We use the definition: $\beta_{AR,AD}=\Delta\Gamma_{AR,AD}/\Delta\mu_{dot}$. Because this quantity doesn’t explicitly depend on the gate voltages, it allows us to make a coarse order of magnitude comparison between QD geometries. Indeed, there are a variety of differences in dimensions between layouts of QD designs, which leads to different lever arms and makes a direct comparison of tunnel barrier responses difficult.

For device A1, the above analysis leads to $\beta_{AR,AD} \approx 0.9 \pm 0.3$ decade/mV, using the gate lever arm $\alpha_{AR}\approx$0.007 meV/mV. We note that the chemical potential of the QD does not actually shift because there is a second gate compensating the chemical potential shift from the first. Therefore, care must be taken in interpreting this ratio: it does not represent the effect of a single gate on the tunnel rate rather the interplay of two gates acting in opposite direction on the two quantities, with unequal contributions. Details on the assumptions leading to the metric β and its limitations can be found in Appendix C. The quantity $\beta_{1,2}$ can be estimated for other designs in the literature in the same way, for any pair of gates

1 and 2 used to tune the tunnel rate and compensate for change in the dot occupation, respectively. We estimate $\beta_{BG,AD}=1.1 \pm 0.3$ decade/mV for the case of a dedicated barrier gate BG compensated by the dot accumulation gate AD equivalent in a Si/SiGe device [Zajac2015]. Details on the calculations are provided in Appendix C. These observations lead to the conclusion that the minimalist layout for split accumulation gate devices we propose allows control of the tunnel rate and dot occupation with a similar performance to the dedicated barrier gate devices, within the uncertainty of the measurements.

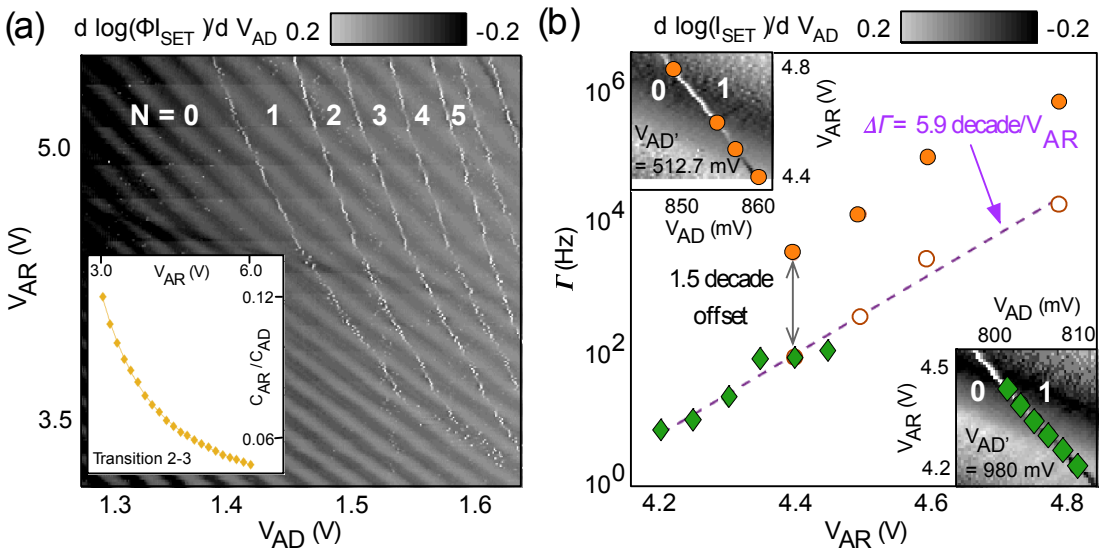

Figure 2: (a) Stability diagram of AD vs AR in the few-electron regime for the single-lead device A2. The data was processed through a 5th order Butterworth digital filter and a Hilbert transform to extract the phase of the signal and minimize the appearance of the background from the SET's Coulomb oscillations. Charge occupation N in the dot is indicated for each region between the transitions. Bottom left inset: capacitance ratio $C_{AR\text{-}dot}/C_{AD\text{-}dot}$ as a function of V_{AR} extracted from the 2-3 charge transition's slope. Best fit to the data is a sum of two exponential functions. (b) Reservoir-dot tunnel rate as a function of V_{AR} for the N=0→N=1 transition in device A1 (Fig 1b). The green (diamonds) data points are obtained via full counting statistics of single-shot traces [Gustavsson2009] while the orange (circles) data points are extracted from pulse spectroscopy [Elzerman2004]. Hollow orange points are the orange points translated by $\Delta\Gamma$=1.5 decade, the offset needed to get the same tunnel rate at V_{AR} =4.4V in both data sets. The dotted violet line is an exponential fit to green and hollow orange data points. Top left inset: zoom on the region of the stability diagram corresponding to the orange data points, with the left dot accumulation gate AD' (not shown) at 512.7 mV. Bottom right inset: Zoom on the region of the stability diagram corresponding to the green data points, with $V_{AD'}$=980 mV.

A second device, Fig. 3a, shows a two-lead split gate design, device B, that supports transport down to the last electron, Fig. 3b. Transport is through a QD under gate AD with source and drain reservoirs under gates AR_1 and AR_2. A mirrored structure can be operated as a SET charge sensor, correlating the transport transitions with charge sensed measurements (Fig 3c). The slight curvature in the transitions is ascribed to a similar screening effect as in the single lead devices (A1 and A2). The tunnel rate also ranges from the life-time broadened regime at high V_{AR}, corresponding to a ~3 GHz tunnel rate [Zajac2015, DeFranceschi2001] to slower than can be detected by the charge sensor, ~8 Hz.

Both V_{AR1} and V_{AR2} are adjusted simultaneously to symmetrize the tunnel barriers on the source and drain side of the QD, giving rise to the Coulomb diamonds diagram in Fig 3d. There is a notable difference in voltage ranges applied on AR_1 and AR_2 in this regime. Asymmetry in the voltages applied on the neighboring gates on the left and right side of the device could contribute to this (see Table 3 in Appendix B for applied voltages), as could the fact that the AD-AR gap dimensions are different on the left and right sides. Limited studies on gap size, not shown, show a dependence of the device behavior supporting this speculation, but completely establishing this dependence was out of the scope of this work.

The addition energy of the last electron and the first orbital energy can be extracted from the Coulomb diamonds from Fig. 3d and are approximately 11 and 3 meV, respectively. A classical capacitance between the QD and the AD gate of 2.3 aF is extracted (e.g., $C=e/\Delta V_{AD}$ with ΔV_{AD} the voltage needed to go from the 0-1 charge transition to the 1-2 transition in the stability diagram Fig 3c). The classical capacitance can be associated with a circular 2D QD below the gate and can be used to estimate a QD radius of 27 nm, using $\varepsilon = 3.9$ for the SiO_2 and neglecting small errors due to the electron offset from the SiO_2 interface and depletion of the polysilicon. The orbital energy also provides an estimate of QD size. Following Zajac et al. [Zajac2015], we can extract an effective length of a confining 2D box ($\pi r^2 = L^2$) and using $E_{orb} = \frac{3\hbar^2\pi^2}{2m^*L^2} = 3$ meV, we obtain a similar dot size, $r = 25$ nm, using $m^* = 0.19\ m_e$. The estimated dot size and energies are similar to the ones obtained in multi-metal layer devices [Zajac2015, Angus2007].

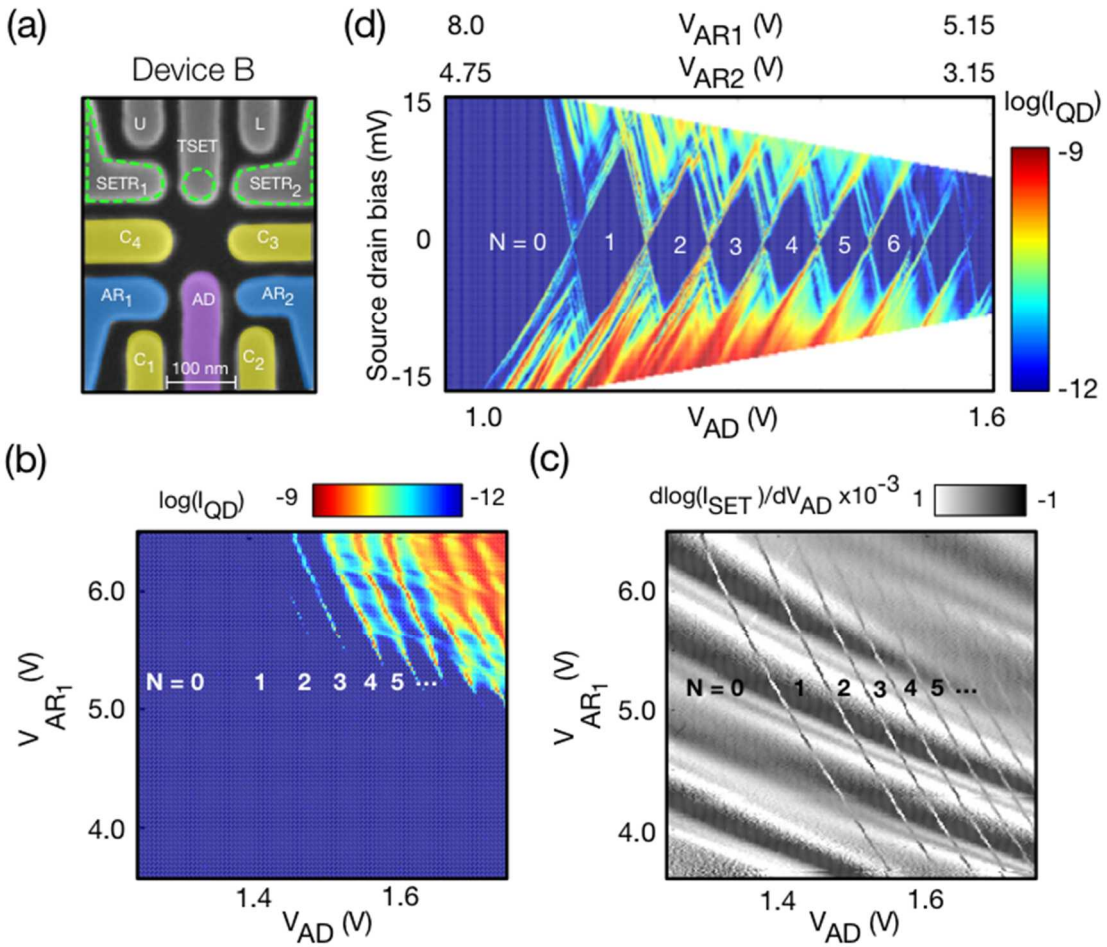

Figure 3: (a) SEM of a two-leads single quantum dot device, device B. C1 and C2 are confinement gates, AD is the dot accumulation gate, and AR_1 and AR_2 are the source and drain reservoirs accumulation gates, respectively. A mirror structure above is operated as a SET for charge sensing. (b) Stability diagram in transport of AD vs AR_1. Current is measured between the source and drain, across the quantum dot under AD, with a 50 μV_{rms} source-drain excitation. (c) Stability diagram in charge sensing corresponding to the transport diagram in (b). (d) Coulomb diamond measurement.

Sufficient separation of the lowest energy manifold from higher energy states is a critical requirement for spin qubits. We examine the singlet-triplet energy splitting and spin filling in our silicon QDs using magnetospectroscopy [Borselli2011, Zajac2015]. The first 4 transitions from device B are shown as a function of magnetic field, at V_{AD}=1.8 V, in Fig 4a. The first transition shows a shift in chemical potential consistent with a lowering of energy due to increasing Zeeman splitting. The inflection point at $B=B_{ST}$ in the $N=1 \rightarrow N=2$ charge transition indicates the magnetic field at which the singlet-triplet (ST) transition occurs in the quantum dot [Yang2013, Culcer2010]. The magnetospectroscopy for the 3rd transition has an inflection at the same B-field as the 2nd transition. This is consistent with a simple model for which there are two valleys and the 2nd valley is loaded with 3rd electron as spin down. The inflection point again marks the crossing of the spin up of the lower valley with the spin down of the upper valley. The 4th electron then loads always up also suggesting that the next orbital energy is well offset from this lower manifold, which is indeed consistent with the order of 3 meV estimate from the Coulomb diamonds. This

filling also indicates a relatively small Coulomb repulsion relative to orbital energy spacing [HadaEto2003].

The magnetospectroscopy measurements are repeated for different V_{AD}, compensating with the confinement gate C1 to maintain charge occupation. We estimate the single particle valley splitting from $E_{vs}=g\mu_B B_{st}$, assuming g=2, for devices A2 and B (Fig 4b). For device B, we extract a linear tunability with the accumulation gate voltage of 231±15 μeV/V, the range corresponding to a 95% confidence interval on the fit. Roughly approximating the vertical electric field as $\Delta F_z=\Delta V_{AD}/t_{ox}$, where t_{ox} is the gate oxide thickness, 35 nm here, we convert this tunability to 8.1±0.6 μeVm/MV. The linear trend is qualitatively consistent with theory and recent observations [Gamble2016, Yang2013]. For device A2, although the measurements were too noisy to extract a convincing tunability fit, all data points are located into the confidence interval for device B tunability. We note that differences in valley splittings between devices A2 and B would be expected from variations in electrostatic environments (e.g., gate layout and dimensions, distribution of voltages to reach single electron occupation and threshold voltages) and in interface roughness, approximately 20% different between the two samples [Gamble2016]. Considering the clear linear trend for the data of device B and the amplitude of the tunability, evidence supports the claim that our minimalist layout allows tuning of the valley splitting in a range suitable for spin qubit applications (i.e., a well isolated two level system can be achieved).

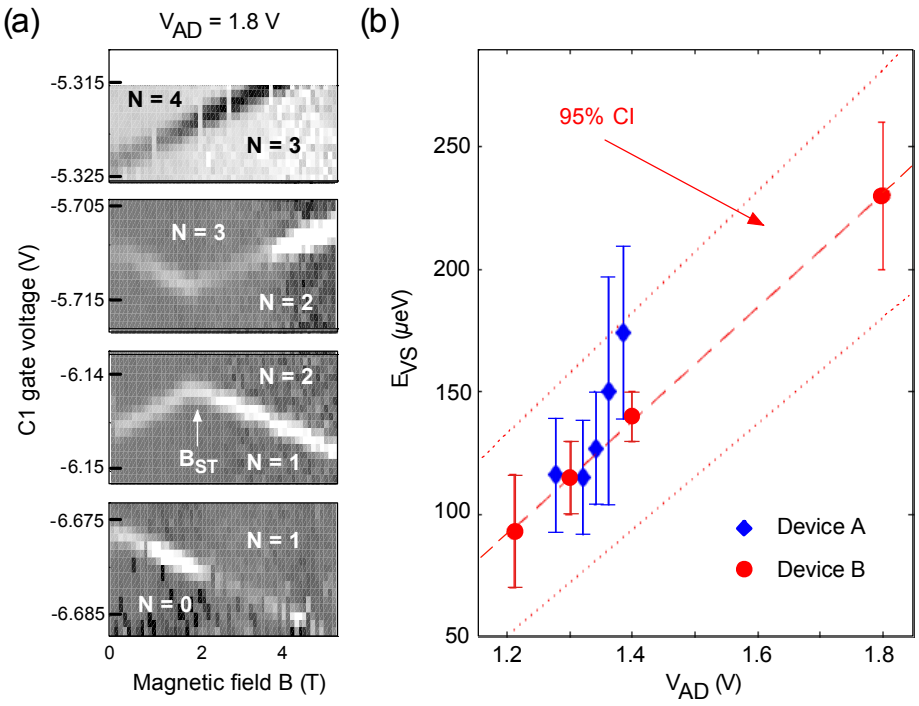

Figure 4: (a) In-plane magnetospectroscopy measurements for device B, for transitions N=0→N=1, 1→2, 2→3, and 3→4, from a stability diagram similar to Fig 3c, at V_{AD}=1.8 V. A lever arm of 31±4 ueV/mV is inferred assuming g=2.0, within 15% of the lever arm extracted from Coulomb peak width temperature dependence [Beenakker1991]. B_{ST} indicates the magnetic field at which the singlet-triplet transition occurs.

(b) Extracted valley splitting E_{VS} as a function of the dot accumulation gate voltage V_{AD}. The diamonds (blue) data points are for device A2 (single-lead, similar to Fig 1b), and the circles (red) data points are for device B (two-leads, Fig 3a). Valley splitting for both devices are obtained from the extracted B_{ST} at the kink in the 1-2 charge transition at each V_{AD}, assuming g=2 for the lever arms, and using $E_{vs}=g\mu_B B_{st}$. Dashed red line indicates the fit for the valley splitting tunability of device B, and the 95% confidence range (CI) is indicated by the red filled region.

CONCLUSION

In summary, we presented an efficient split gate layout for silicon MOS quantum dots that (1) forms a well-isolated two-level energy subspace, (2) provides dot-reservoir tunnel barriers that are sufficiently tunable in the few electrons regime, and (3) favors extensible and reliable fabrication.

Quantum dots with charging energies up to 11 meV and orbital energy of 3 meV are observed, corresponding to a ≈25 nm radius, demonstrating strongly confined electrons in a silicon single gate stack architecture. Furthermore, the valley splitting is linearly tunable with the vertical electric field in both the single and double-lead designs (8.1±0.6 μeVm/MV) and is measured over a range of ≈75 – 250 μeV.

Using the reservoir accumulation gate to control the tunnel rate between the dot and the reservoir, we demonstrate orthogonal tuning of the tunnel rate and dot occupation without a dedicated barrier gate. The orthogonality of the tunnel barrier control and the dot occupation is quantified by the tuning orthogonality $\beta_{AR,AD} \approx 0.9$ decade/mV, yielding a comparable performance to devices with dedicated barrier gate.

The demonstration of sufficient tuning orthogonality enables the use of a minimalist gate layout for QDs, which offers the potential for higher yield through (1) using fewer electrode layers; (2) using subtractive processing; (3) leveraging more fully compatible silicon foundry processes and (4) potentially avoiding complications of metal electrodes recently identified (e.g., stress and noise). Furthermore, the split gate architecture we presented here represents a potential avenue to implement large array of quantum dots all connected to their own reservoir. Such a geometry could simplify initialization of multiple quantum dots [Zajac2016] and allow simultaneous addressable single spin readout of multiple quantum dots, with one less gate per unit cell. It could be a way to mitigate the latching effect observed in linear arrays of quantum dots with only one source and one drain reservoir [Yang2014, Bogan2016], and eliminate the need for charge shuttling in readout procedures [Baart2016].

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APPENDIX A: SAMPLES FABRICATION

The fabrication is composed of two phases. The first phase is run in a 0.35 micron CMOS silicon foundry, and the second phase is performed in another fabrication area that provides more flexibility in processing, particularly the e-beam lithography used for the nanofabrication. Three different devices are presented in this work. We will describe the process flow for devices A1 and A2. Significant differences in the structure are noted for device B.

Phase 1 (silicon foundry): The initial material stack is fabricated using a 0.35 micron silicon foundry process at Sandia National Labs. The starting material is a 150 mm diameter float zone <100> n-type silicon wafer with a room temperature resistivity of 10,000 ohm-cm. Device B used a p-type float zone substrate with a 99.95% ^{28}Si enriched epitaxy layer instead. A thermal oxide is grown at 900°C with dichloroethene (DCE) followed by a 30 min, 900°C N_2 anneal. This oxide forms a 35 nm thermal SiO_2 and the SiO_2/Si interface is where the surface quantum dots form in the device. The next layer deposited is a 100 nm amorphous silicon layer followed by a $5x10^{15}$ cm^{-2}, 10 keV Arsenic implant at 0 degree tilt. Device B used a 200 nm layer and the implant energy was 35 keV with the same dose. The amorphous layers are crystallized later in the process flow to form a degenerately doped poly-silicon electrode. This poly-silicon layer conducts at low temperature, and will eventually form the enhancement electrodes of the nanostructure. In the silicon foundry, the poly-Si is patterned and etched into large scale region, a "construction zone" often order of 100 µm x 100 µm, that will later be patterned using e-beam lithography to form the nanostructure. After etching, Ohmic implants are formed using optical lithography and implantation of arsenic at 100 keV and density of $3x10^{15}$ cm^{-2}. An oxidation anneal of 900°C for 13 min and an N_2 soak at 900°C for 30 min follows the implant step and serves the multiple purposes of crystallizing, activating and uniformly diffusing the dopants in the poly-Si while also forming a SiO_2 layer (10-25 nm)

on the surface of the poly-Si. This SiO_2 layer, on top of the poly-Si, forms the first part of the hard mask layer used for the nanostructure etch in the construction zone. The second part of the hard mask is a 20 nm Si_3N_4 layer (35 nm for device B). An 800 nm thick field oxide is subsequently deposited using low pressure chemical vapor deposition (CVD), tetraethoxysilane (TEOS) or high density plasma CVD for device B. The field oxide is planarized using chemical mechanical polishing (CMP) leaving approximately 500 nm over the silicon and 300 nm over the poly-Si. Exact thicknesses are determined using ellipsometry after the CMP step. Vias are etched to the conducting poly-Si and n^+ Ohmics at the silicon surface. The vias are filled with Ti/TiN/W/TiN. The W is a good, high contrast alignment marker for subsequent e-beam lithography steps. Then large, approximate 100 µm x 100 µm windows aligned to the construction zones are etched in the field oxide to expose the underlying hardmask and poly-Si construction zone for nanostructure patterning. The last processing step for the devices in the silicon foundry was a 450°C forming gas anneal for 90 min.

Phase 2 (separate nano-micro fabrication facility): The wafers are removed from the silicon foundry and subsequently diced into smaller parts. For this particular work, the mask layout led to 10 mm x 11 mm die. The die used in this work had four construction zones each. For the nanostructures in this work, we pattern the structure using electron beam lithography and a thinned ZEP resist. The pattern is transferred with a two-step etch process. First the SiN and SiO_2 hard mask layers are etched with a CF_4 dry etch and O_2 clean then strips the resist in-situ. The second etch step is to form the poly-Si electrodes, which is done with an HBr dry etch in the same chamber. The poly-Si etch is monitored using end-point detection in a large scale etch feature away from the active regions of the device. Wet acetone and dry O_2 cleans are used to strip the residual resist after the poly-silicon nanostructure formation. A lift-off process is used for aluminum formation of bond pads to contact the Ohmics and poly-silicon electrodes. The last step is a 400°C, 30 minute forming gas anneal. The Al bond pads were deposited after the wet strips of the tungsten vias. For device B, after polysilicon etch, a second e-beam lithography and implant step was done to place donors near the QD region. The device was sent out for implant, $4x10^{11}$ cm^{-2} Phosphorus at 45 keV. After the implant step, the photoresist was stripped with acetone and then the metal and residual organics were stripped from the surface using peroxide and RCA cleans. The device was subsequently metallized using an Al lift-off process similar to devices A1 and A2.

APPENDIX B: DEVICES CHARACTERISTICS AND EXPERIMENTAL PARAMETERS

We describe in details the devices characteristics in Table 1, as well as the experimental parameters for all measurements shown, in Table 2 for devices A1 and A2, and in Table 3 for device B. Figure 5 shows the complete gate layout for device A2.

Device	A1	A2	B
Reservoirs	Single-lead	Single-lead	Double-lead
Device dimensions	AD-C2: 60 nm, AD-AR: 50 nm	AD-C2: 25 nm, AD-AR: 30 nm	AD-C2: 30 nm, AD-AR: 20 nm
Mobility (cm^2/(V.s))	4560	4560	11 600
Interface roughness (A)	2.4	2.4	1.8
Critical density (cm^-2)	6.0x10^11	6.0x10^11	1.6x10^11
Scattering charge density (cm^-2)	7.6x10^10	7.6x10^10	5.2x10^10
Interface correlation length (A)	26	26	22
Wafer type	10 000 Ω-cm n	10 000 Ω-cm n	10 000 Ω-cm p*
Polysilicon gate stack	100 nm	100 nm	200 nm
Silicon gate oxide	35 nm	35 nm	35 nm

*Device B contains a 99.95% ^{28}Si enriched epitaxy layer.

Table 1: Measured devices characteristics. Devices A1 and A2 present the same layout, differing only in the spacing between the gates and the width of the gates (A2 gates are more closely packed than A1 gates). For comparison, we label the devices by the distance between gates AD and C2, and the distance between AD and AR tips (see Fig 1b).

	Fig 1c	Fig 2a	Fig 2b, top inset	Fig 2b, bottom inset	Fig 4b
Device	A1	A2	A1	A1	A2
AD	1.75 V	1.25 to 1.65 V	0.840 to 0.870 V	0.790 to 0.820 V	1.25 to 1.40 V
AR	3.0 to 6.0 V	3.0 to 6.0 V	4.4 to 4.9 V	4.2 to 4.5 V	6.5 V
C1	-1.0 V	-3.0 V	-1.0 V	-1.0 V	-1.0 V
C2	-3.0 V	-1.4 V	-3.0 V	-3.0 V	-3.0 V
C3	-1.0 V	-1.4 V	-1.0 V	-1.0 V	-1.0 V
C4	-1.0 V	-1.0 V	-1.0 V	-1.0 V	-1.0 V
TSET	2.59 V	2.0 V	2.45 V	2.59 V	2.0 V
U	-1.32 V	-1.4 V	-3.19 V	-2.32 V	-1.4 V
L	-2.06 V	-1.4 V	-1.75 V	-2.06 V	-1.4 V
AD’	0.980 V	0 V	0.5127 V	0.980 V	0 V
AR’	7.0 V	0 V	7.0 V	7.0 V	0 V
C2’	-3.0 V	0 V	-1.0 V	-1.0 V	0 V
C3’	-1.0 V	0 V	-1.0 V	-1.0 V	0 V
TSET’	0 V	0 V	0 V	0 V	0 V
U’	0 V	0 V	0 V	0 V	0 V
L’	0 V	0 V	0 V	0 V	0 V
Measure	Thomas-Fermi numerical simulations.	Charge sensing, f_{LI}=16.4 Hz, V_{SD}=100 μV.	Pulse spectroscopy, measured by charge sensing, f_{LI}=19 Hz, V_{SD}=100 μV.	Single-shot measured by RF reflectometry, carrier wave f=180 MHz, bandwidth of 326 kHz.	Charge sensing, f_{LI}=16.4 Hz, V_{SD}=100 μV.

Table 2: Experimental parameters for various data sets of the main text, for devices A1 and A2.

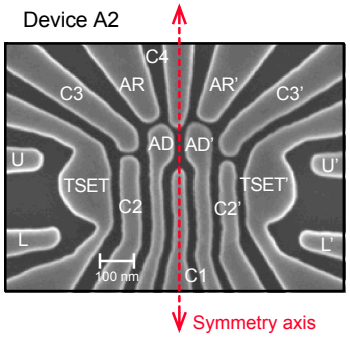

Fig 5: SEM of single-lead device A2. The device has a symmetry axis between the two quantum dots. Experiments on device A2 involved the formation of a single quantum dot, on the left side of the device only (under AD).

Measurement	Fig 3b and 3c	Fig 3d	Fig 4a	Fig 4b
Device	B	B	B	B
AD	1.2 to 1.8 V	0.9 to 1.6 V	1.8 V	1.21 to 1.8 V
AR1	3.0 to 7.0 V	5.15 to 8.0 V	5.0 V	5.0 V
AR2	3.5 V	3.15 to 4.75 V	3.0 V	3 to 3.1 V
C1	-2.7 V	-1.5 V	-6.7 to -5.3 V	-6.7 to -0.76 V
C2	-4.0 V	-3.0 V	-3.0 V	-3.0 V
C3	-0.26 V	0 V	-0.26 V	-0.26 V
C4	-4.2 V	-4.2 V	-4.2 V	-4.2 V
TSET	2.61 V	0 V	2.53 V	2.53 V
SETR1	2.5 V	0 V	2.5 V	2.5 V
SETR2	2.5 V	0 V	2.5 V	2.5 V
U	-1.5 V	0 V	-4.8 V	-4.8 V
L	-4.8 V	0 V	-0.92 V	-0.92 to -1.26 V
Details of the measurement	Charge sensing and transport, f_{LI}=492.6 Hz, V_{SD}=50 µV rms.	Transport, f_{LI}=492.6 Hz, V_{SD}=100 µV.	Charge sensing, f_{LI}=492.6 Hz, V_{SD}=120 µV.	Charge sensing, f_{LI}=492.6 Hz, V_{SD}=120 µV.

Table 2: Experimental parameters for various data sets of the main text, for device B.

APPENDIX C: TUNING ORTHOGONALITY

When designing a QD device, it is of interest to provide local control of important device properties, with the surface gate voltages often serving as the control knobs. One oft used parameter is gate lever arm α, which describes the efficacy of a gate voltage on the QD chemical potential level μ. The lever arm is defined as

$$\Delta\mu_i = \alpha_i \Delta V_i, \tag{1}$$

where there is a unique α_i for each gate i. In a similar spirit, a parameter describing the controllability of the QD-lead tunnel rate can be defined as

$$\Delta\Gamma_\mathrm{i} = \beta'_i \Delta V_i. \tag{2}$$

While α is always positive by definition, β' can be positive or negative, depending on if gate i increases or decreases the reservoir-QD tunnel rate with a positive voltage change. For example, gate AR increases the tunnel rate with increasing voltage (Fig. 1d), while gate AD' decreases the tunnel rate with increasing voltage (Fig. 2b). Geometric arguments can typically be made to estimate the sign of β' by considering whether a positive voltage change on a gate is pulling the dot towards or away from the reservoir.

Of particular interest for designing QDs is the ability to tune the tunnel rates to the QD while only imparting a minimal change in the QD chemical potential, which denotes a high degree of tuning orthogonality between the two properties. Good orthogonality facilitates emptying the QD (fewer gate compensations are required to obtain N=1) and tuning the reservoir coupling with minimal effect on the shift in the charge stability diagram (quicker optimization of relaxation and coherence times). For a single gate, the orthogonality between the tunnel rate and the chemical potential tunability is optimized by maximizing the ratio $\frac{\Delta\Gamma_\mathrm{i}}{\Delta\mu_i} = \frac{\beta'_i}{\alpha_i} \equiv \beta_i$. We rewrite this in an analogous form to the lever arm

$$\Delta\Gamma_i = \beta_i \Delta\mu_i. \tag{3}$$

To obtain β_i, one must measure the change in both tunnel rate and chemical potential for a change on the gate voltage ΔV_i. In practice, this is impossible because a change in a single voltage moves the QD level out of resonance with the Fermi level, and a change in tunnel rate cannot be determined. Thus, one must consider the effect of two gate voltages changing and compensating each other such that the QD chemical potential is always in resonance with the Fermi level. Continuing the analogy with the lever arm, we assume that the total change in tunnel rate is simply the sum of the contributions of each gate that has changed. For two gates 1 and 2, this results in

$$\Delta\Gamma_{1,2} = \Delta\Gamma_1 + \Delta\Gamma_2 = \beta_1\alpha_1\Delta V_1 + \beta_2\alpha_2\Delta V_2 \tag{4}$$

As the chemical potential has not changed, we have the additional constraint

$$\Delta\mu_{1,2} = \Delta\mu_1 + \Delta\mu_2 = \alpha_1 \Delta V_1 + \alpha_2 \Delta V_2 = 0 \quad (5)$$

Combining Eq. (4) and (5), we can define the two-gate tunnel rate orthogonality parameter as

$$\beta_{1,2} \equiv \beta_1 - \beta_2 = \frac{\Delta\Gamma_{1,2}}{\Delta\mu_1}, \quad (6)$$

which is directly attainable from the measurements in Figure 2b. From the data, we extract a slope of $\frac{\Delta\Gamma_{AR,AD}}{\Delta V_{AR}} = 5.9 \pm 0.7 \ \frac{\text{decades}}{\text{V}_{\text{AR}}}$, describing the change in tunnel rate induced by a change in both V_{AR} and V_{AD}. With a lever arm $\alpha_{AR} = 0.007$ eV/V, we determine $\beta_{AR,AD} = 0.9 \pm 0.1 \ \frac{\text{decades}}{\text{meV}}$.

This value of $\beta_{1,2}$ for our minimalist split gate architecture, where we omit a dedicated barrier gate and only rely on the reservoir enhancement gate for tunnel barrier tuning, is competitive with other, more complicated, device architectures. For comparison, we extract $\beta_{1,2}$ for a multilayer enhancement mode Si/SiGe device which uses a dedicated barrier gate located directly on top of the tunnel barrier, sandwiched between the reservoir and QD gates [Zajac2015]. Information on the tunnel rates are determined from the stability diagram of the tunnel barrier gate LB1 and the QD gate L1 (Fig. 2a of [Zajac2015]). To more easily compare this data to our device, we relabel LB1→BG and L1→AD. The voltage ranges studied show transition rates ranging from the measurement sample rate (assumed to be at least 10 Hz) to the lifetime broadened regime ($\frac{k_B T_e}{h} = 800$ MHz for a reported electron temperature of $T_e = 40$ mK). This provides two coordinates (Γ, V_{BG}) to estimate the tunnel rate orthogonality, for which we find $\Delta\Gamma_{BG,AD} = \frac{7.9 \text{ decades}}{0.4 \text{ V}_{\text{BG}}} = 19.8 \ \frac{\text{decades}}{\text{V}_{\text{BG}}}$. From the reported lever arms and capacitance ratio for the QD and barrier gates, we determine $\alpha_{BG} = 0.018$ eV/V, and thus $\beta_{BG,AD} = 1.1 \pm 0.3 \frac{\text{decades}}{\text{meV}}$.

The values $\beta_{BG,AD}$ for a device with a dedicated barrier gate and $\beta_{AR,AD}$ for our simpler split gate design are comparable within the error of the measurements. In addition, the definition of $\beta_{1,2}$ lends itself to compare other devices and geometries as well, as $\beta_{1,2}$ is independent of geometry specific information like capacitances. The concept of $\beta_{1,2}$ can also be extended to optimize QD devices for other characteristics which may be useful for qubit operation. For example, on can similarly define a parameter that describes the orthogonality between a double-QD coupling and the double-QD detuning, or a double-QD coupling and the valley splitting.

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