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A CMOS Compatible, Forming Free TaO_x ReRAM

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Resistive random access memory (ReRAM) has become a promising candidate for next-generation high-performance non-volatile memory that operates by electrically tuning resistance states via modulating vacancy concentrations. We demonstrate a wafer-scale process for resistive switching in tantalum oxide that is completely CMOS compatible. The resulting devices are forming-free and with greater than $1x10^5$ cycle endurance.

Introduction

Resistive random access memories (ReRAM), also referred to as memristors, have emerged in the past several years as a leading emerging nonvolatile memory device due to excellent scalability [1] and stackability [2], low energy [3], and high endurance [4]. Furthermore, the analog properties of this device are a potential enabler of neuromorphic computing [5]. Of particular interest are the class of ReRAM based on based on the mechanism named valence change memory (VCM) and fabricated from transition metal oxides (TMOs) such as TaO_x, HfO_x, and TiO_2 [6]. Switching in of VCM ReRAM is the subject of continued research, but is thought to occur as a result of oxygen vacancy motion in a small (50-200 nm) channel created in the TMO region of the device [7]. This particular class of ReRAM has achieved record endurance (10^{12} cycles) [4], sub-nanosecond switching speeds [3], and demonstrated operation in 10x10 nm devices [1]. Note that all of these metrics are for research devices, not integrated with a CMOS process. In fact, two of the significant hurdles to overcome with ReRAM technology are integrating high performance ReRAM devices with a CMOS back end of line (BEOL) processes [8,9] and eliminating the high voltage electroforming step [10]. This work reports on initial results from the wafer-scale integration of a TiN/Ta/TaOx/TiN ReRAM stack using a process compatible with CMOS. These initial results demonstrate that a CMOS integrated process which does not require a high voltage forming step and exhibits performance on par with integrated flash memory.

Experiment

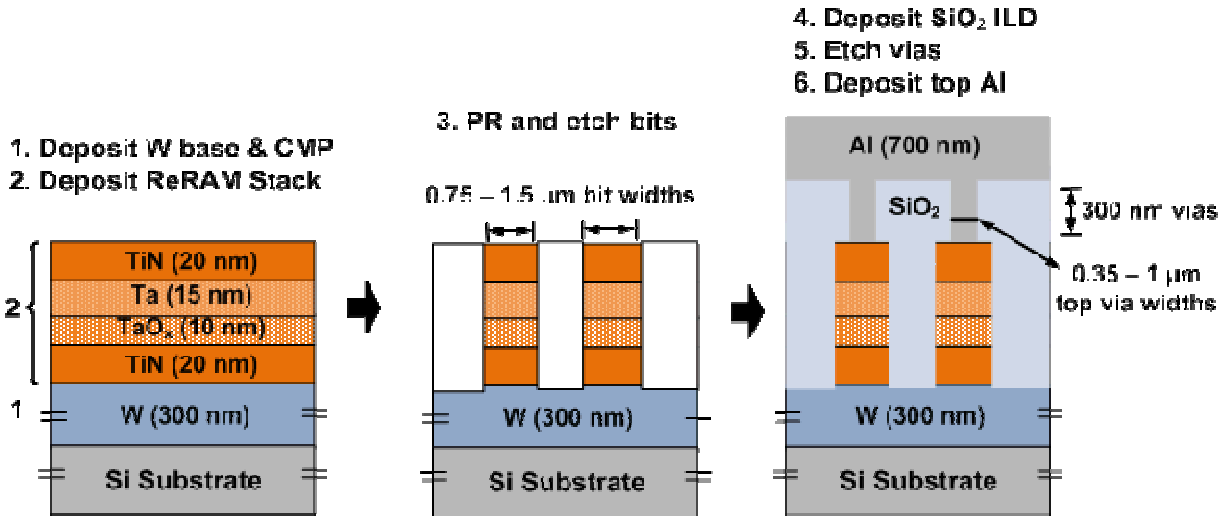

Figure 1. The process flow for fabricating the CMOS compatible ReRAM devices is shown.

The details of the fabrication process are illustrated schematically in Fig. 1. This is a "short loop" process used to evaluate process parameters, and is intentionally simplified from the full BEOL CMOS process which is being integrated with Sandia's in-house CMOS7 BEOL. The process begins with PVD deposition and CMP polishing of a 300 nm Tungsten layer on a standard p-type wafer. Next, the ReRAM stack is deposited using reactive PVD without breaking vacuum. The ReRAM stack consists of (top to bottom) TiN(20nm)/Ta(15nm)/TaO_x(5-15nm)/TiN(20nm). Experiments varying oxygen flow during the reactive PVD deposition of the TaO_x allow optimization of switching behavior. Next, the ReRAM stack bits are dry etched, followed by the CVD deposition of the standard BEOL SiO_2 interlayer dielectric (ILD). The standard ILD SiO_2 recipe reaches 400°C and hence there was concern that the TaO_x film would be damaged, however results below indicate that the film was still functional. Finally, vias were etched above the bits with diameters ranging 0.35 to 1.5 µm and filled with the Al top metal. The best switching performance was obtained from the smallest vias (0.35 and 0.5 µm). In this step, through vias were etched to contact the bottom metal (not shown in Fig. 1). Fig. 2 gives a photomicrograph of a final 32x32 crossbar produced from this process. Fig. 3 shows an SEM cross section of a typical bit with key regions identified and Fig. 4 gives a zoomed-in cross section of the bit area.

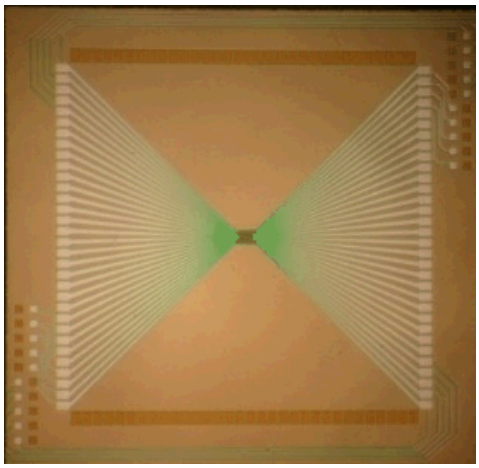

Figure 2. A photomicrograph of a 32x32 array shows the devices and electrodes (left-to-right) and the contacts to the bottom electrodes using through vias (top and bottom periphery).

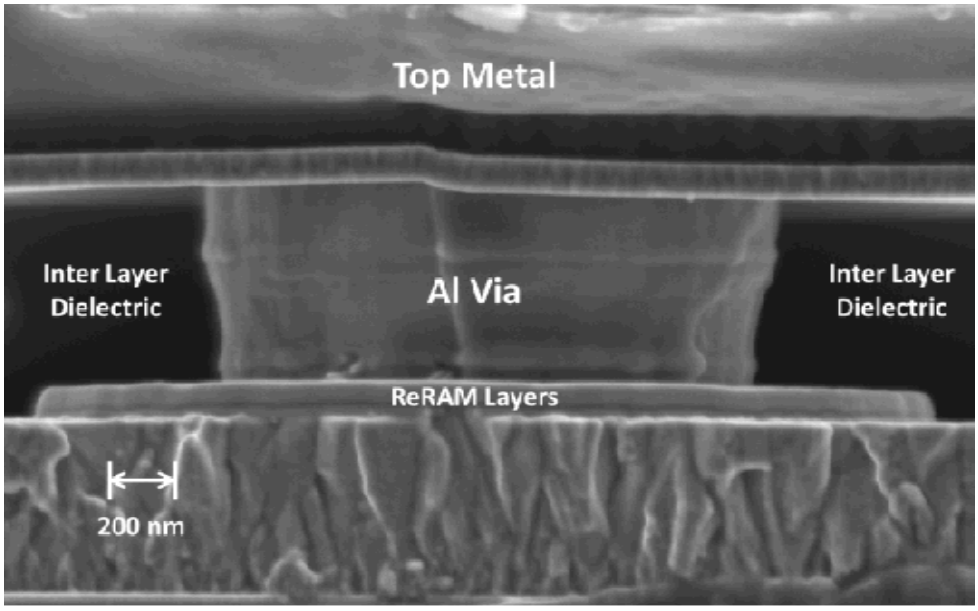

Figure 3. An SEM cross-section shows the device structure, highlighting the vias and metal layers

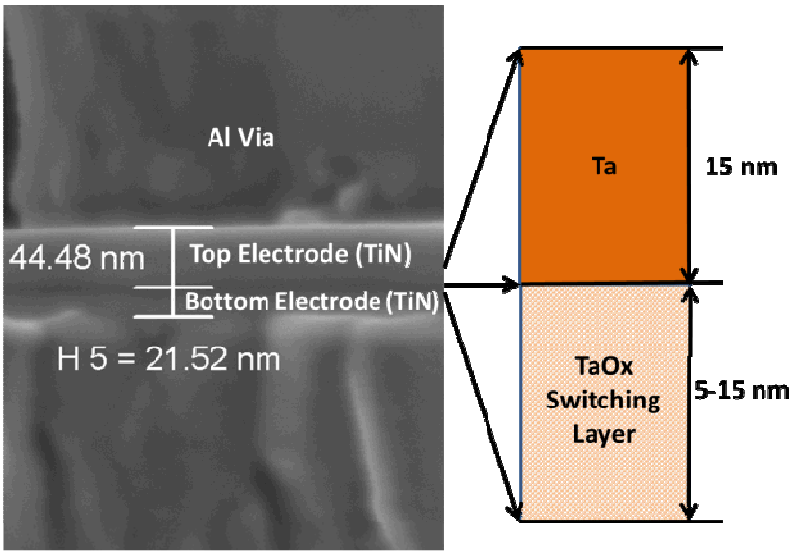

Figure 4. An SEM cross-section shows the device structure, highlighting the ReRAM bit stack.

Results and Discussion

Basic current-voltage (I-V) characterization was performed on a probe station in a dark box, using an Agilent 4156C. I-V hysteresis loops (often associated with a memristor) were used as a method of initial characterization (Fig. 5). The remarkable characteristic of Fig. 5 is that the virgin I-V curve shows a starting resistance only slightly below the ON state (i.e. low resistance). The first application of positive current switches it from nearly ON to ON and then a negative current is used to turn it OFF (i.e. high resistance). The OFF current magnitude is the same as is required for subsequent OFF switching. Hence, the device does not need a high voltage forming step, but simply switches off during the first negative cycle. The reason for this excellent result is a topic of investigation and may be related to specifics of the BEOL processes employed, such as the brief 400°C anneal required for the SiO_2 ILD. This result is a major advancement in our CMOS integration work, as we no longer will require forming voltages above the capability of our standard logic transistors (3.3V).

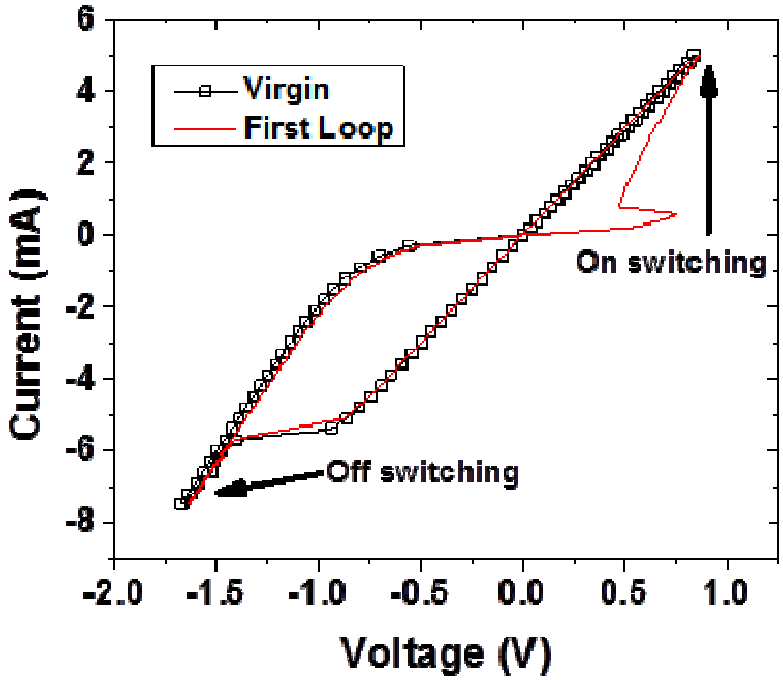

Figure 5. Current-Voltage hysteresis loops show that these devices are forming free. The black squares show that the device starts in a low resistance state and once ON behaves identically to subsequent cycles.

From Fig. 5 it is also apparent that the R_{OFF}/R_{ON} ratio in these devices is within an acceptable range. The device shown in Fig. 5 is representative, having a ratio of approximately 10 within the 100 mV read window but devices often have larger R_{OFF} resulting in significantly larger R_{OFF}/R_{ON} ratio. R_{OFF} in the range of 50-100 kΩ are frequently observed. With continued cycling however, the OFF state resistance that can be achieved becomes progressively smaller. Eventually this decreasing OFF state limits falls below a threshold for state separation, thereby limiting the endurance. This decreasing OFF state resistance with increased cycling was observed in all but one of our CMOS compatible devices but not observed in our research devices even with active oxide layers deposited using the same deposition system. Although endurance of these CMOS compatible ReRAM devices are a long way from the records set using CMOS-incompatible research devices [4], their endurance is already competitive with state-of-the-art FLASH memory.

Endurance was measured using an Agilent 81130A Pulse/Arbitrary Waveform Generator and an Agilent 4156B parameter analyzer. Figs. 6 and 7 show an endurance of over 100k before R_{OFF}/R_{ON} drops below 2 positioning it, even in these early stages of development as a viable replacement for current FLASH technologies. Present work indicates that this endurance can be improved by optimizing the process and switching conditions.

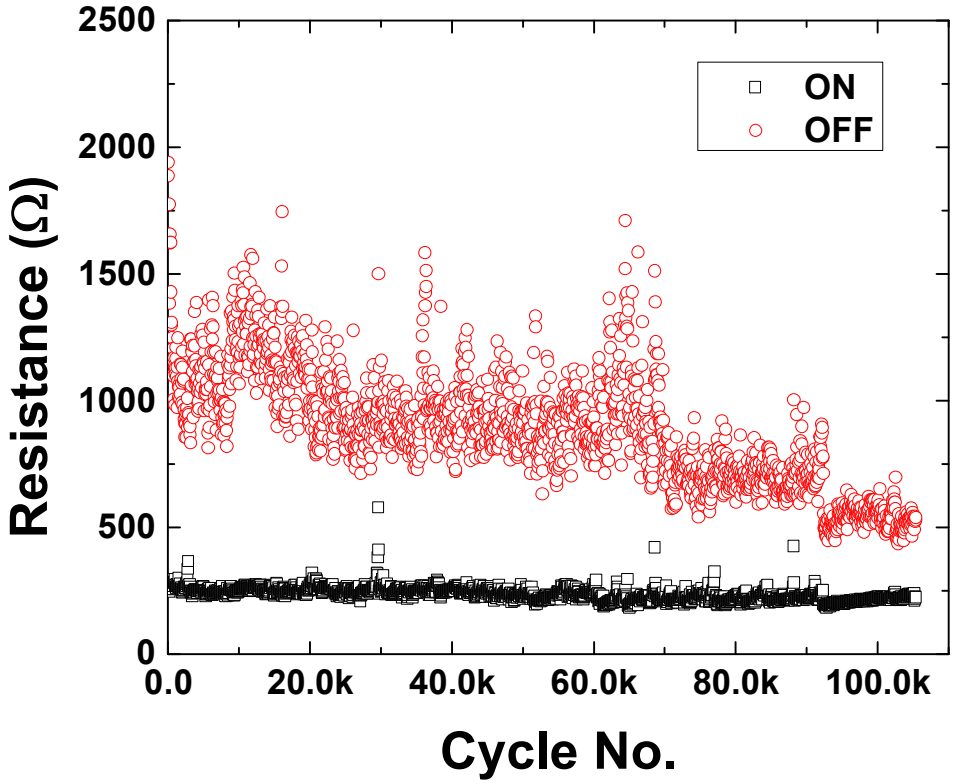

Figure 6. OFF (red circles) and ON (black squares) resistances are shown for 100,000 cycles of a single device.

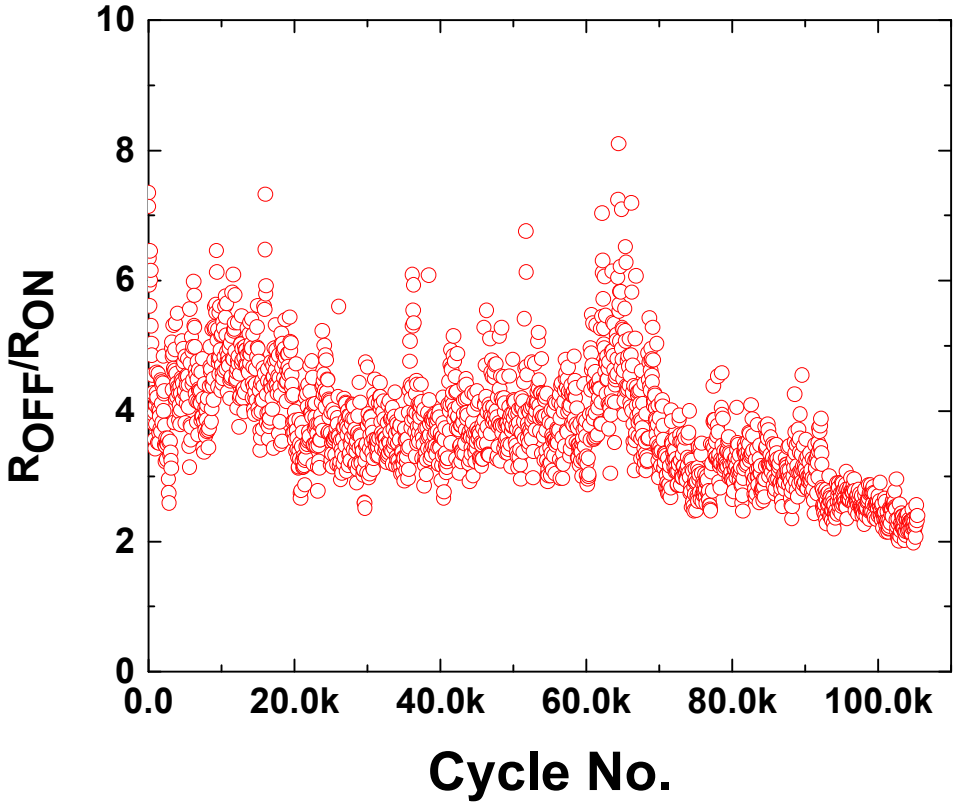

Figure 7. The resistance ratio R_{OFF}/R_{ON} is shown for 100,000 cycles of a single device.

Conclusions

We demonstrate a wafer-scale CMOS compatible process for fabricating tantalum oxide based resistive switches. Further, we show that the devices are forming free thereby reducing the restrictions on drive circuitry and stochastic issues that arise from the electroforming step. The electrical properties of these devices are also promising with the exception of endurance which is orders of magnitude lower than the ReRAM record endurance. The discrepancy is caused by OFF state degredation with repeated cycling but even in the presence of OFF state degredation, endurance is still in excess of 100,000 cycles placing it in the range of state-of-the-art FLASH memory technologies.

Acknowledgments

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