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DC Link Bus Design for High Frequency, High Temperature Converters

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***Abstract* — Advancements in IGBT device performance and reliability have been important for widespread electric vehicle (EV) and hybrid electric vehicle (HEV) adoption. However, further improvements in device performance are now limited by silicon's (Si) inherent material characteristics. New improvements are being realized in converter efficiency and power density with wide bandgap materials, such as silicon-carbide (SiC) and gallium nitride (GaN), which permit faster switching frequencies and higher temperature operation. On the horizon are ultra-wide bandgap materials such as aluminum nitride (AlN) and aluminum gallium nitride (AlGaN) which hold the potential to push the envelope further. As device operating temperatures and switching frequencies increase, however, the balance of the power conversion system becomes more important: DC bus design, filter components and thermal management. This paper considers a typical 6-pulse inverter application common in EV and HEV power systems and provides an alternative, cost-effective solution to the design of a low-impedance DC bus. In contrast to systems that use bus bars with film or electrolytic dc link capacitors, the proposed high-frequency (HF) bus design reduces parasitic resistance and inductance, tolerates higher temperature and is potentially scalable to MHz frequencies. A prototype was built and compared in simulation to the DC bus design documented for the 2010 Toyota Prius.**

Keywords— DC link bus, parasitics, WBG converters, EV, HEV, MLCC, Film, capacitor resonance

I. INTRODUCTION

The DC link of an electric vehicle (EV) or hybrid electric vehicle (HEV) drive system typically includes bulky filter capacitors that have large parasitic losses and inductance. The assembly of these systems are optimized for switching frequencies in the range of 5-10 kHz, the typical operating range of Silicon (Si) IGBTs in EV/HEV applications. Manufacturers are interested in the development of new power electronic drives, with high power density and high specific power, for use in electric and hybrid electric vehicles. These designs will likely exploit new wide bandgap (WBG) semiconductor materials such as silicon carbide (SiC) and gallium nitride (GaN) which are capable of higher voltage, higher switching frequencies and higher temperature operation. However, to enable these higher switching frequencies, the dc link bus must be redesigned to mitigate parasitic inductance so that voltage ripple is minimized even with high-frequency currents.

Electrolytic capacitors, historically used in power electronics due to their low cost and high energy density [1], have a reputation for unreliable long-term operation (electrolyte vaporization leads to increased equivalent series resistance (ESR) that can drastically affect circuit operation [2]), catastrophic failure, and poor current ripple handling. Due to these drawbacks, many power system designers have replaced electrolytic capacitors with film capacitors, as film capacitor manufacturers have improved peak current and energy density to rival electrolytics while decreasing cost.

Typical plastic dielectrics for film capacitors include polypropylene (PP), polyethylene terephthalate (PET), polyethylene naphthalate (PEN), and polyphenylene sulphide (PPS) [3]. Film is attractive because of its self-healing property which ensures a safe failure mode (open circuit) [4]. Each material system has tradeoffs in performance, cost, and temperature dependence; although, the majority of film capacitors utilize biaxially oriented PP films as the dielectric due to its low cost, low resistance [5], and highly consistent manufacturing [6]. It is common for a film or electrolytic capacitor to resonate around 10-15 kHz and be limited to temperatures below 105°C. However, as switching frequencies and operating temperatures of circuits increase due to the incorporation of WBG devices, the necessary filter capacitances decrease, but circuit design for high frequency and high temperature operation becomes necessary.

There is already work in the area of high-voltage, high-temperature packaging [7], optimal module design for higher-current WBG implementations [8], and novel methods for thermal management for WBG-based devices [9]. On the horizon are ultra-wide bandgap materials such as aluminum nitride (AlN) and aluminum gallium nitride (AlGaN). In fact, first-of-their kind devices have already been developed using AlGaN, including an AlGaN diode [10] and transistor [11].

To make the first leap from Si to SiC, the circuit should support >100 kHz switching and high-temperature up to 125°C. We must therefore rethink the DC link bus, improving its performance while preserving economy and manufacturability. The approach should also be potentially scalable to MHz switching in future instantiations.

Herein, we propose a method that replaces bulky DC link capacitors with PCB mounted multi-layer ceramic capacitors (MLCCs), utilizing techniques to minimize the impedance and maximize heat dissipation. MLCCs, composed of alternating layers of sintered ceramic powder with interdigitated metal electrodes, have high operating temperatures, excellent long-

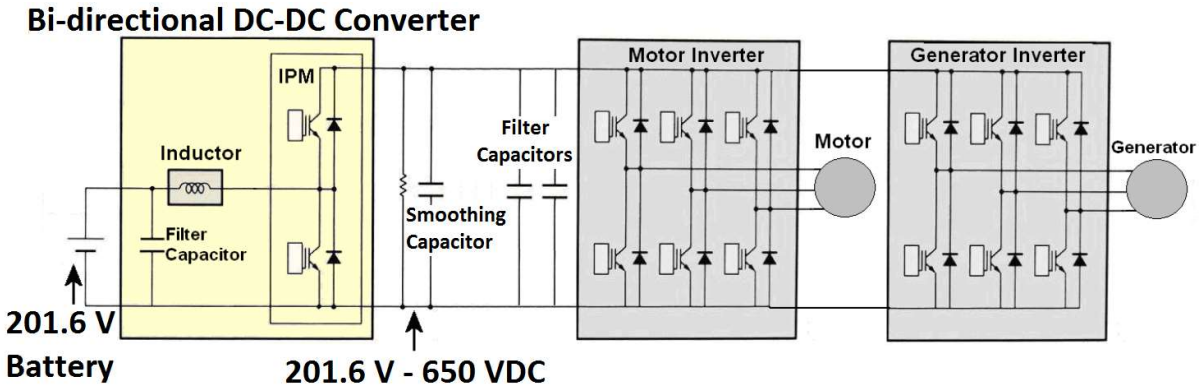

Fig. 1. Circuit diagram of 2010 Prius PCU; from [14]

term reliability, high resonant frequencies (~10 MHz) and high volumetric current densities. These devices have been used extensively in lower power electronics. Unfortunately, due to the cost of precious metals used as the electrode (traditionally a 85% silver/15% palladium alloy), MLCCs have not traditionally been used in higher power circuits. However, new advances in ceramic materials and fabrication techniques are enabling improved operational stability at higher temperature [12] and use of lower cost electrodes [13].

In this work, a low impedance DC bus, having parallel plate current carrying conductors and a DC link capacitor built from a PCB with surface mount MLCCs, is designed, constructed, and characterized. The performance of this high-frequency (HF) bus is then considered in the context of an electric vehicle drive and compared to an implementation based on the system installed in the 2010 Prius. An overview of an EV electric drive system is given in the next section. A model of the DC bus, with capacitors, is given in Section III. Section IV presents a prototype of the HF bus implementation as well as characterization of the bus using impedance measurement. Section V includes simulation of the EV boost converter using an estimated model of the original bus and operating conditions and compares it to the HF bus component at higher frequency. Section VI provides a discussion of control implications given the lower capacitance value. Section VII summarizes the results from this project and outlines future work.

II. Overview of an EV Converter-Inverter System

In this work, the electrical power system of the 2010 Toyota Prius was selected as a baseline due to its popularity and the comprehensiveness to which it has been documented [14]. Fig. 1 shows a circuit diagram of this system, reproduced from [14]. The Power Control Unit (PCU) of the 2010 Prius has a 27 kW bi-directional DC-DC converter used for boosting the battery voltage to ranges between 201.6 V – 650 V and operates at switching frequencies of 5 kHz or 10 kHz. The high voltage (HV) DC link bus connects the high side of the DC-DC converter, the generator inverter (MG1) and the motor inverter (MG2). This configuration allows power transfer between the battery and any combination of the internal combustion engine (ICE), MG1, and MG2. On the HV bus are several capacitors. Two HV film-type filter capacitors are located near the IGBT switches. The HV bus then connects with a separate capacitor module, which has a total of 888 µF of DC link capacitance for smoothing, realized using three parallel 296 µF film capacitors in parallel. There is also a 53.8 kΩ burden resistor, and an additional film type filter capacitor. Component values and dimensional information from [14] as well as online datasheets were used to determine or estimate parameter values for components in Fig. 1.

The model presented herein requires information not included in [14]. In these instances, an effort was made to estimate these values by identifying representative components that provided the needed information. For example, ESR for the 296 µF caps was cited in [14], but since the equivalent series inductance (ESL) for the capacitors was not available, a variety of film capacitors with similar ratings were surveyed. The ESL used for the 296 µF capacitor model was found by averaging values for eight capacitors similar in size. When comparing the averaged ESR of these same capacitors, it matched the data extracted from the actual 2010 Toyota Prius system with an approximate four percent error; 2.4 mΩ (actual) compared to 2.5 mΩ (averaged). The same approach was taken to find ESL values for the LV and HV filter capacitors. See Table I.

Table I: Toyota Prius DC Circuit Parameters, [14]

Component	Value (µF/µH)	Quantity	ESR (mΩ)	ESL (nH)
Filter Capacitor (LV)	315	2	4	20
Input Inductor	112.8	2	2.5 (EST)	NA
Smoothing Capacitor (HV)	296	3	2.4	15 (EST)
Filter Capacitor (HV)	0.562	2	10	18 (EST)
Filter Capacitor (HV)	0.8	1	10	23 (EST)

III. DC Link Circuit Model

A candidate equivalent circuit for the Toyota Prius HV DC link is shown in Fig. 2, wherein the terminals at the left represent an interconnect to the DC-DC converter high side, and the parasitic inductances and equivalent series resistances of the bus and its components are represented. The model is assembled using documented information for the components (ie capacitance, ESR, ESL) as well as the values computed for the bus bars using measured or estimated dimensions. By computing the resistance, capacitance, and inductance in select parts of the bus, a partial element equivalent circuit (PEEC) model may be constructed [15],[16].

In Fig. 2, the value C_x is the capacitance of a given capacitor (in Farads) while r_{cx} and L_{cx} are the ESR (in Ohms) and ESL (in Henries) respectively for that component. For this model, capacitors 3-5 of Fig. 2 comprise the smoothing capacitors of Table I, capacitors 1 and 6 are the first filter capacitor listed, and capacitor 2 is the second filter capacitor listed. The small capacitance between bus bar conductors is given by C_{bbx}, and portions of the bus bar resistance and inductance are given by r_{bbx} and L_{bbx} respectively.

If the total impedance of the DC link (with capacitors) were to be measured as a function of frequency, it would appear capacitive at lower frequencies until the first resonance was reached. After which, the impedance would rise, appearing inductive. As frequencies increase further, additional resonances would occur that depend on parasitic inductances and capacitances. For example, the bus bars of the 2010 Prius (without components) would have an estimated resonant frequency around 100 MHz which requires the PEEC model to have at least 17 groups of parasitic elements (C_{bbx}, L_{bbx}, r_{bbx}) to represent this response with high fidelity [16]. However, since the focus of this work is to manage ripple by minimizing the impedance at switching frequencies (5-100 kHz), only a few elements were used to characterize the bus response.

To model the HV DC link bus bars in the 2010 Prius, bus bar dimensions were determined from values and images presented in [14]. Bus bar widths, lengths, and distance from the wall of the enclosure were determined from images, and inductances were then computed using online tools [17],[18] for computing the inductance or impedance between coplanar conductors near a ground plane. In addition, bus resistance was estimated using these dimensions while accounting for the skin effect [19]. See Table II. Therein, the bus bar resistance is listed for copper at 1 MHz and 80ºC. Since the bus bar capacitance was computed to be very small, these values were neglected. In addition, since the bi-directional DC-DC converter and both drives are co-located with little distance between them, these inductances and resistances were also neglected.

Table II: Estimated DC Link Bus Parameters for 2010 Prius

Parameter	Value
C_{bb1} - C_{bb6}	NA
L_{bb1}, L_{bb2}	NA
r_{bb1}, r_{bb2}	NA
L_{bb3}	130 nH
r_{bb3}	1.9 mΩ
L_{bb4}, L_{bb5}	71 nH
r_{bb4}, r_{bb5}	0.7 mΩ
L_{bb6}	NA
r_{bb6}	NA
L_{bb7}	38 nH
r_{bb7}	1.6 mΩ

IV. New DC Link Bus Design

The goal of this new DC link bus is to create a design that will support WBG-based and UWBG-based power systems being developed to reduce component sizing and real estate in new generations of EV/HEV. The design is comprised of two metal plates and a flat capacitor made from a PC board with surface mount ceramic capacitors. The metal bus plates carry the majority of the DC current; these plates connect to the PCB at several points to provide a low impedance connection for high frequency currents. See illustrations in Fig. 3 and Fig. 4. The flat profile of the assembly is also expected to have favorable thermal benefits.

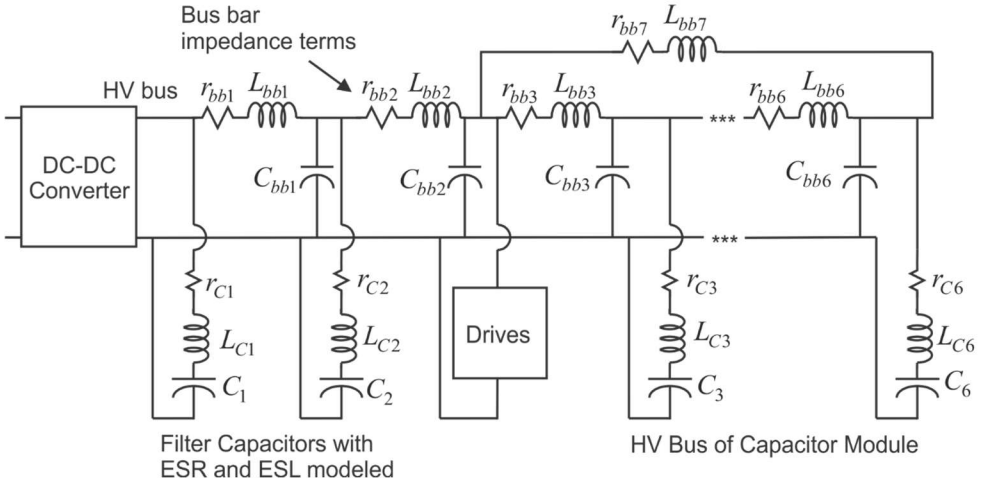

Fig. 2. DC Link equivalent circuit, including equivalent series inductance and resistance of DC link capacitors

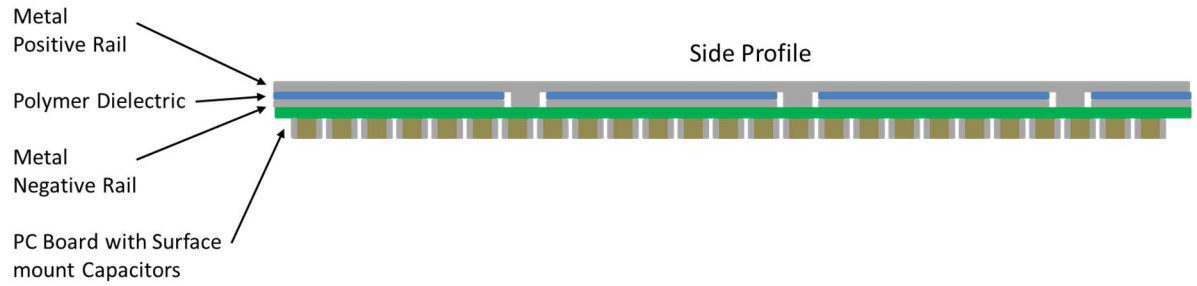

Fig. 3. Profile illustration of capacitor concept: the bulk of DC currents flow in closely-spaced metal plates; plates connect electrically to copper planes of a PC board with ceramic capacitors

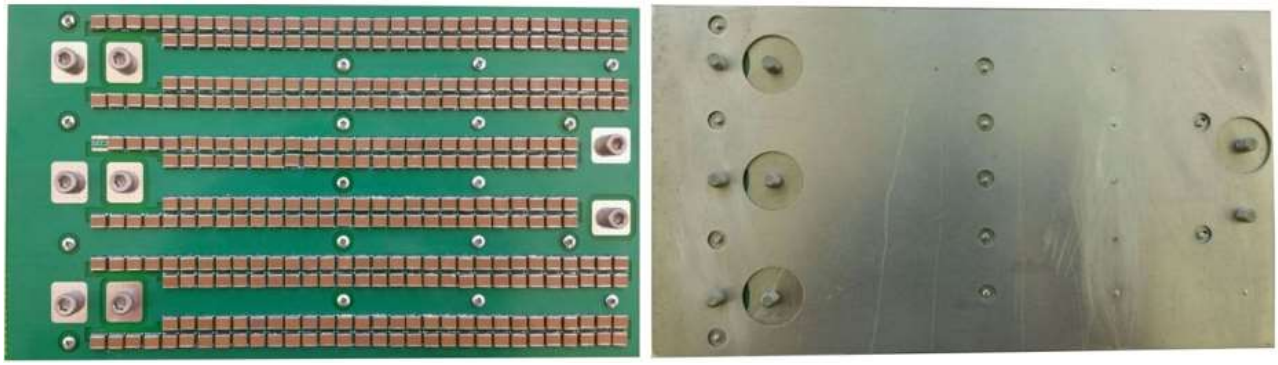

Fig. 4. (Left) Photo of assembled board; (Right) Photo of aluminum plates carry majority of DC current

The minimum DC link capacitance required to achieve the same voltage ripple specification is proportional to the maximum current through the capacitor and inversely proportional to the switching frequency, computed as

$$C_{\min} = \frac{I_{\max} D}{f_s \Delta V_{link}} \quad (1)$$

The target switching frequency is 100 kHz; therefore, the capacitance can be reduced from 888 µF to as little as 44.4 µF: a reduction by a factor of 20.

To reduce cost, assembly should be accomplished easily using high-volume reflow soldering methods on SMD devices. Of the available SMD capacitor options, film capacitors are attractive because they offer higher capacitances; however, due to their low operating temperatures, they must be located in the "cooler regions" of the assembly, reducing gains in system power density. MLCCs allow higher operating temperature and therefore do not impede power density gains. A survey of available parts was performed and it was found that high-voltage MLCCs also offer higher energy density than SMD film capacitors in the 1000 V range. For the prototype presented herein, a Kemet C2225X154KDRACTU 0.15 µF, 1000 V MLCC was used. These components have X7R dielectric and are AEC-Q200 qualified making it suitable for under the hood automotive applications [20].

A. DC Link Bus PCB Layout

The HF bus PCB design (shown in Fig. 4) is 0.062" with 2 layers and has appropriate spacing between voltage potentials. This was important due to the high voltage and current levels that will be seen. Only 296 capacitors were needed at 0.15 µF each to reach the 44.4 µF threshold. The 6" x 11" PCB dimension allowed for 336 capacitors in parallel for a nominal capacitance of 50.4 µF which provides additional capacitance to account for component irregularities and effects from varying voltage and temperature.

Impedance was minimized by reducing the loop inductance using multiple via-in-pads per component [21]. The PCB was fabricated with 2 oz. copper for better heat dissipation and lower ESR. Each of the three pairs of pads on the left connect to a SiC MOSFET half-bridge assembly. The two pads on the right connect to the DC source. Aluminum plates that match the profile of the circuit board act as the primary conductor of DC current; these plates connect to the circuit board positive and negative rails at regular intervals to maintain low impedance at high frequency and provide additional structural support to the assembly. Due to the large number of parallel devices, the individual component current ratings can be low. Each individual capacitor is rated for approximately 300 mA at 100 kHz giving the entire assembly a rating of approximately 100.8 A. The complete HF bus prototype was fabricated for under $700, not including labor. It is difficult to predict the cost at production scale, but in higher volume implementations, this cost would be expected to reduce substantially.

B. Impedance Measurement

The input impedance of the HF bus was measured at two terminals at the edge of the PCB for frequencies between 1 kHz and 10 MHz. These data were then used to generate a representative circuit model of the prototype. Fig. 5 shows the

circuit model, and Table III lists the parameter values for the model. Fig. 6 compares the modeled impedance of the existing 2010 Prius DC bus, the measured impedance of the HF bus, and the modeled impedance of the 2010 Prius HV DC link. Typical ranges for switching frequencies for different existing and speculative semiconductor technologies are also shown in Fig. 6 for reference.

The bus resonance for the modeled 2010 Prius bus occurs around 21 kHz while the HF bus has a resonance around 130 kHz. At 100 kHz, the HF bus has an impedance of 29 mΩ while the 2010 Prius model is 31 mΩ. Thus the proposed design is not only smaller but is expected to have less (or at least comparable) voltage ripple in a 100 kHz application. This could, for example, be important for enabling the use of SiC switches.

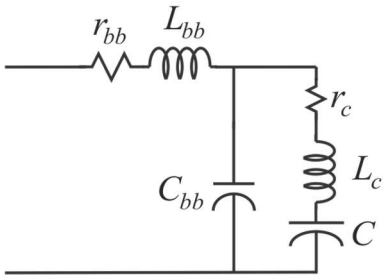

Fig. 5. Circuit Model representing input impedance of HF bus prototype

Table III: Modeled Parameters for HF Bus Prototype

Parameter	Value
r_{bb}	25 mΩ
L_{bb}	30 nH
C_{bb}	4 nF
r_c	0.36 mΩ
L_c	3.0 pH
C	50.4 µF

As future design enhancements are realized, this approach may enable higher frequency operation.

V. Steady State Simulation

The Prius DC-DC converter was modeled and simulated using LTspice to determine an expected range for current ripple and voltage transients. The model included the circuit of Fig. 2 with component and parasitic values listed in Table I and Table II. The low side switch of the DC-DC converter is composed of three parallel IGBTs for current handling purposes. Since switch information was unavailable, the system was modeled using Fairchild FGL40N120AND IGBTs. It is also noted that the higher switching frequency enabled a reduction in the boost converter's input inductor. This is obviously desirable for cost reduction, but, as will be discussed in Section VI, this is likely also necessary for maintaining stable operation. For the HF Bus at 100 kHz switching, a 15 µH input inductor was used in the simulation.

Simulation of the Toyota Prius system indicated some ringing on the HV bus following each switching transient. Fig. 7 shows the bus voltage at C_1 following a switch transition. Therein, the HV bus is at a nominal 650V; following a switch transition, the voltage rings at just over 1 MHz with a 42 V peak-to-peak amplitude. Fig. 8 shows the expected ripple current into the HF bus for a scenario representing operation at 450 V and 75°C. Several scenarios were simulated using the original 2010 Prius model as well as the HF bus model. These results are summarized in Table IV wherein bus voltage ripple and capacitor current ripple are compared for the Prius bus operating at 5 kHz and 10 kHz and for the HF bus at 100 kHz. In the table, $I_{C1,RMS}$ represents the RMS current into either each smoothing capacitor for the Prius Bus or into each MLCC capacitor for the proposed PCB based HF bus. Also, $I_{Ctot,RMS}$ represents the total RMS current into either capacitor assembly. The Prius and HF Bus model were analyzed at nominal HV bus voltages of 250 V, 450 V, and 650 V.

For the HF Bus, custom Spice models were obtained from the manufacturer to compare operation at various voltages and temperatures to ensure acceptable performance at different conditions.

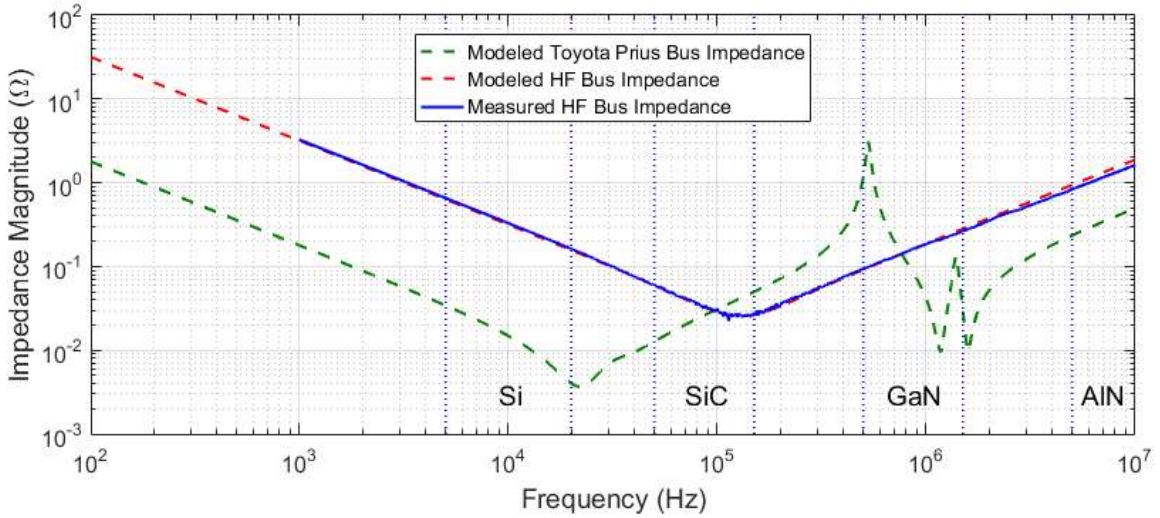

Fig. 6. Magnitude bode plots of existing and proposed DC bus with typical ranges identified for existing and anticipated semiconductor technologies

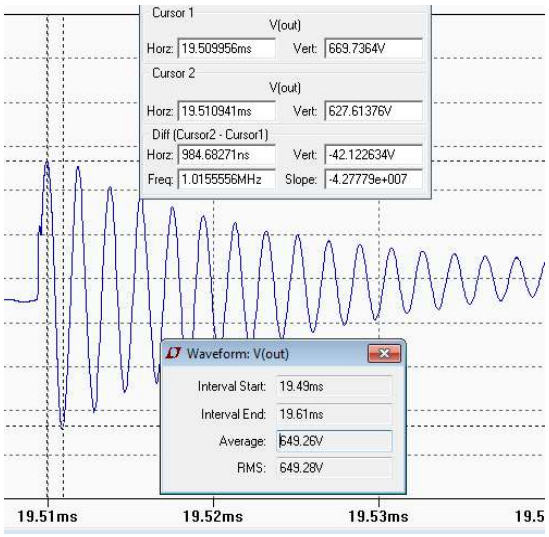

Fig. 7. Simulated ringing of Prius bus voltage (at C_1)

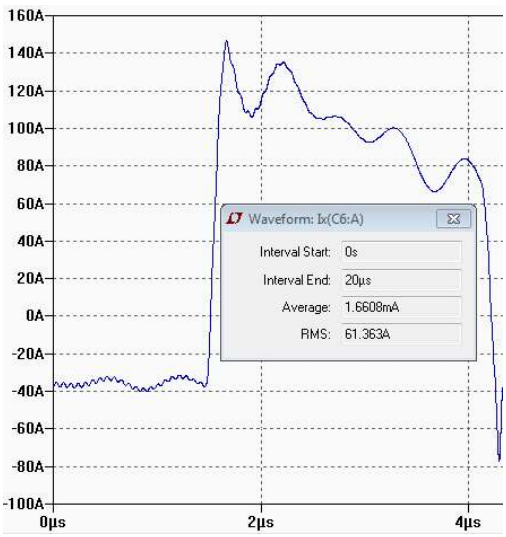

Fig. 8. Simulated ripple current into HF Bus at 75ºC

It should be noted that the capacitance of X7R dielectric does reduce with higher applied bias voltage and was represented for each voltage level in each model. At a given voltage level, the variation in temperature affected the current ripple less than 4 percent between temperature extremes. For the Prius model, a temperature compensated model was not used for the capacitors.

In general, for both systems, the ripple current was found to increase with higher voltages which corresponds to larger duty cycles and is a standard characteristic of boost converters. Capacitor voltage ripple, $\Delta V/V_o$, was measured as the peak-to-peak voltage at the load divided by the average voltage. As stated earlier, a large portion of the voltage ripple is due to high frequency ringing, caused by the bus inductance. In the 250 V case, the HF Bus performed better in voltage ripple (1% vs 3.5%) but slightly worse for the 650 V 75ºC case (5.5% vs 4.4%). For the most part, however, the HF Bus at 100 kHz showed comparable performance (in voltage and current ripple) to the (estimated) Prius implementation.

Table IV – Simulation of DC Bus Performance

Bus Design	f_s (kHz)	Temp (°C)	V_{bias} (V)	$\Delta V/V_o$ (%)	$I_{C1,RMS}$ (A)	$I_{Ctot,RMS}$ (A)
Prius	5	NA	250	4.2	4.1	12.7
	10			3.5	3.5	10.4
	5		450	6.2	13.0	38.9
	10			4.9	12.1	36.2
	5		650	7.5	22.9	68.7
	10			4.4	22.9	68.6
Proposed	100	27	250	1.0	0.036	12.0
			450	3.1	0.107	35.8
			650	5.4	0.183	61.5
		75	250	1.0	0.036	11.9
			450	3.2	0.106	35.77
			650	5.5	0.183	61.5
		125	250	1.0	0.036	12.0
			450	3.2	0.106	35.7
			650	5.3	0.184	61.7

VI. Discussion of Transient Response

The simulation results presented in the previous section consider the system in steady-state and compare the capacitor voltage ripple and RMS capacitor current. However, another important consideration is that of the dynamic response, including stability and disturbance rejection. As the switching frequency goes up with adoption of WBG devices, this enables the passive elements to shrink without increasing ripple; however, this also means that the circuit stores less energy, resulting in larger bus voltage response for a given load transient. Thus, with smaller bus capacitance, the converter controls must be modified to improve disturbance response, which often requires operating at higher gains.

Unfortunately, a boost converter operating in continuous conduction mode is more difficult to stabilize due to the inherent right half plane (RHP) zero, which results in a non-minimum phase response [22],[23]. For a system such as the one illustrated in Fig. 2, the boost converter would regulate the bus voltage supplying the motor and generator drives. The motor and generator drives would act as a constant-power load or constant-power source depending on mode of operation. The small-signal duty-to-output transfer function for a boost converter with constant power load is given by [22]:

$$G_{vd} = \frac{v_{bus}(s)}{d(s)} = \frac{V_{bus}}{1-D} \frac{1 - s\dfrac{L}{(1-D)^2}\dfrac{P_{bus}}{V_{bus}^2}}{s^2\dfrac{LC}{(1-D)^2} - s\left(\dfrac{L}{(1-D)^2}\dfrac{P_{bus}}{V_{bus}^2}\right) + 1} \quad (2)$$

where G_{vd} is the transfer function relating small signal bus voltage to the small signal duty cycle around an operating point

defined at nominal duty cycle D, bus voltage V_{bus} and total bus load P_{bus}. Inspection of (2) indicates that for $P_{bus} > 0$, a RHP zero occurs, and its location is dependent on power level, bus voltage, and inductor value. When acting as a constant power load, $P_{bus} > 0$ also results in a RHP pole pair. To maintain good disturbance rejection and stability, the controller action must be adjusted for faster response. This may include higher gain and/or utilization of a feedforward scheme [22]. In addition, the timescale separation between the RHP zero and the poles should be maintained [23]. This requires the inductor size to be reduced. In this work, for simulation scenarios that included the HF bus and 100 kHz switching, the boost converter inductor value was changed to 15 µH to maintain a factor of 10 separation between RHP zero and RHP poles in a full power scenario. In practice, this would be desirable as it would be a much smaller inductor.

A more thorough study of stability is beyond the scope of this paper but is the subject of a future work that focuses on stabilization of WBG-based converter systems having smaller passive components.

VII. Conclusions and Future Work

This paper describes a high-frequency/low impedance DC link bus design that could be used with WBG-based power systems in power inverters. The approach was investigated in the context of electric vehicle power systems with comparisons made to that of the 2010 Toyota Prius. Based on this study, it is expected that the bus will support WBG devices operating at 100-130 kHz, thus indicating the potential for use with SiC-based inverter systems. It is expected that design enhancements may allow the resonant frequency to be pushed higher, allowing for GaN and eventually even UWBG device implementations.

Since the measured impedance at resonant frequency was approximately 25 mΩ, a large portion of the impedance may have come from solder connections made for testing or other imperfections in the prototype assembly. It is noted however that the prototype was fabricated from parts costing under $700, including the PCB. It is expected that the cost would be further reduced with larger scale production.

Future work will include the integration of the HF bus into an inverter system to further evaluate the approach. Candidate systems include an EV/HEV system or potentially a photovoltaic inverter. Future work will also include additional prototype iterations to improve performance. Development of these prototypes are likely to include high-fidelity multi-physics modeling of the HF bus to enable co-optimization of thermal and electrical properties. This model may aid in determining the optimal dimensions, number of capacitors, and component placement to minimize ESL (and overall impedance) while not exceeding thermal design limits.

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