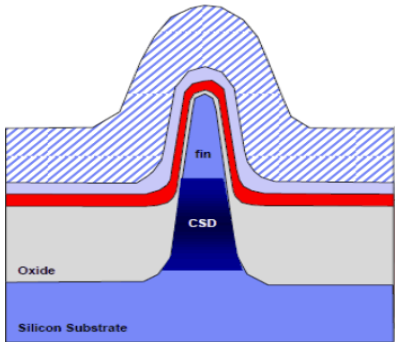
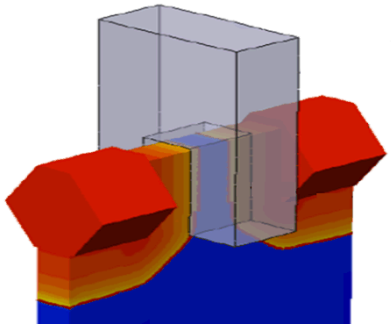
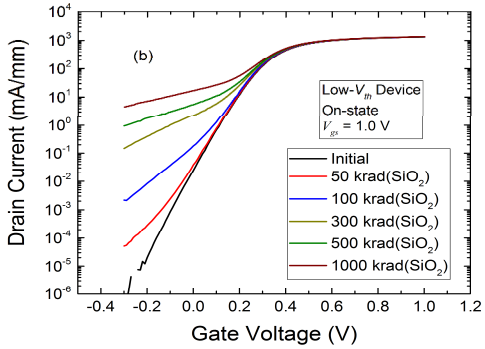
SAND2016-4642C

Exceptional service in the national interest

Sandia National Laboratories







Analysis of TID Process, Geometry, and Bias Condition Dependence of 14-nm FinFETs and Implications for RF and SRAM Performance

. P. King, X. Wu, M. Eller, S. Samavedam, M. R. Shaneyfelt, A. I. Silva, B. L. Draper, W. C. Rice, T. L. Meisenheimer, E. Zhang, K. J. Shetler, T. D. Haeffner, L. W. Massengill

VANDERBILT UNIVERSITY

U.S. DEPARTMENT OF ENERGY

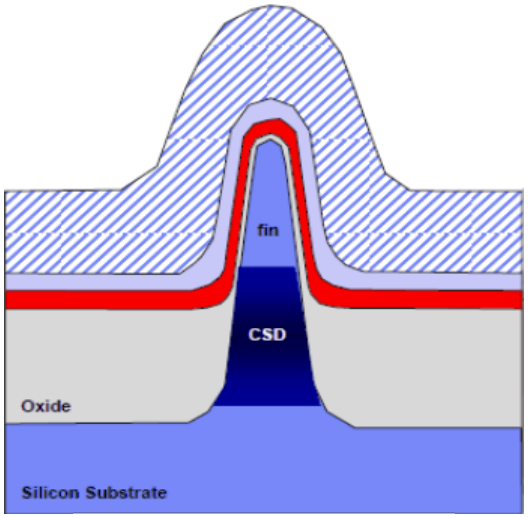
National Nuclear Security Administration

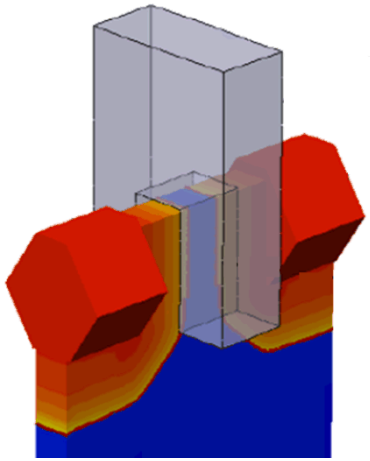
GLOBALFOUNDRIES®

Sandia National Laboratories is a multi-program laboratory managed and operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Corporation, for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000. SAND NO. 2011-XXXXP

Motivation

- Most commercial fabs have migrated to FinFETs below 20-nm gate length feature sizes
- FinFETs exhibit improved electrostatic control of the channel and improved reliability compared to equivalent scaled planar CMOS
- Some work on the TID response of FinFETs has been presented at IRPS, NSREC, and RADECs
- This work presents an in-depth study of current-generation 14-nm commercial FinFET response to TID





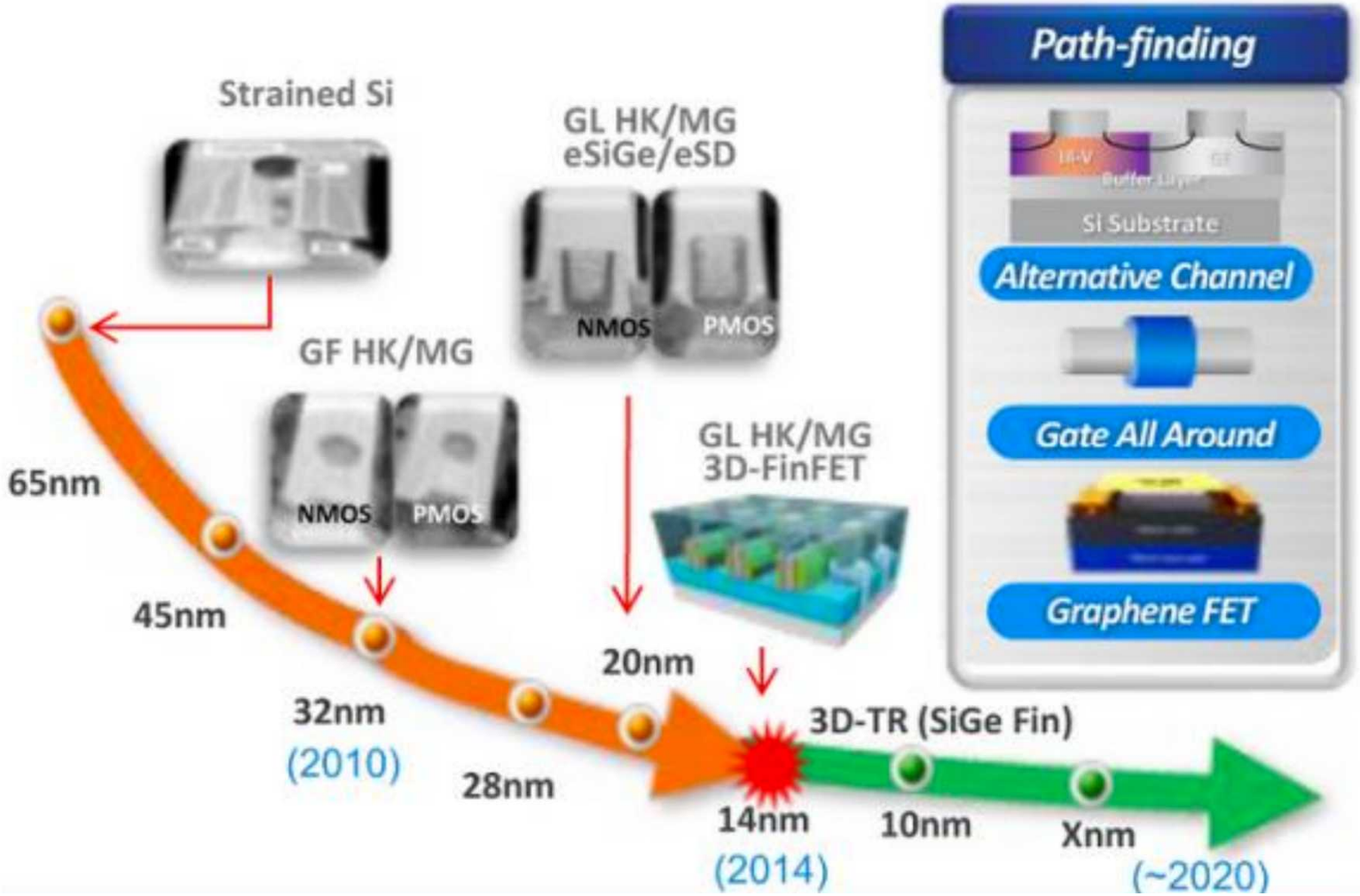
T. Hook, FDSOI Conference, Taiwan, 2013

Outline

Sandia National Laboratories

- Background
- Processing, Performance, Reliability
- Review of SEU and TID on FinFETs to Date
- Description of Test Structures
- Experimental Methods
- Irradiation Bias Condition Dependence
- Response of Low-Vth vs High-Vth Devices
- Results for SRAM Pull-down and Pass-gate Transistors
- Conclusion

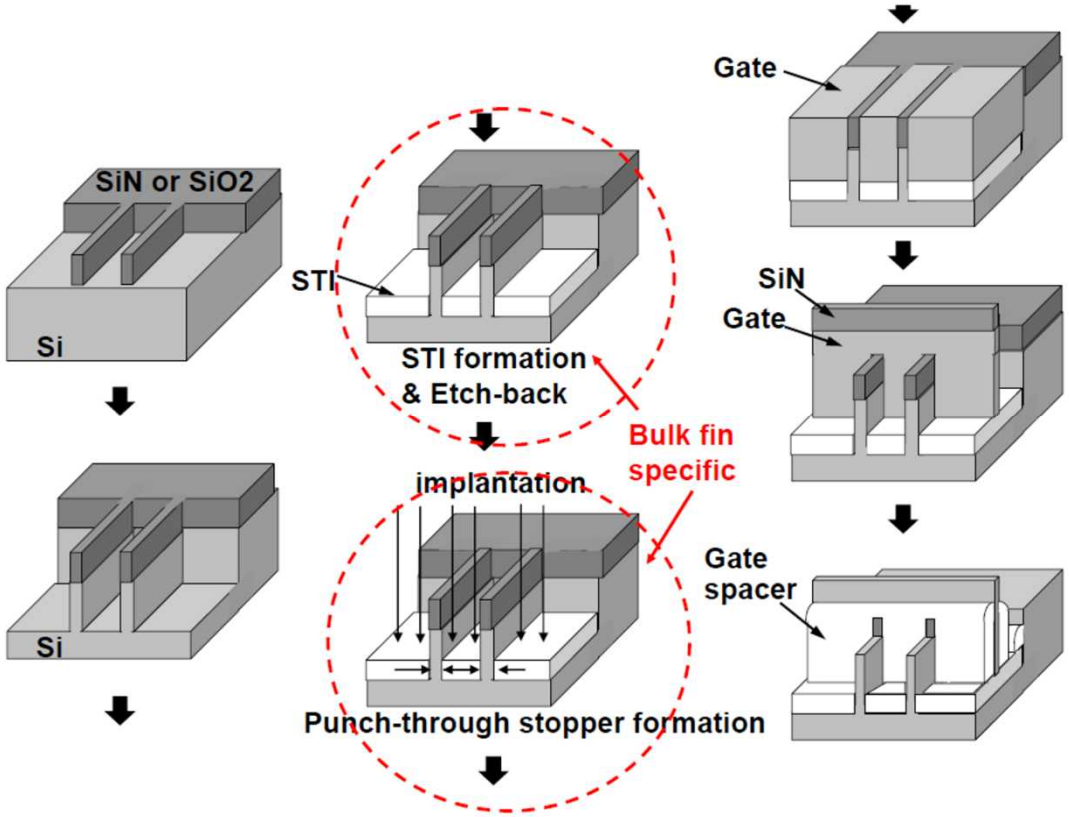
Path to FinFET Technology



www.tweaktown.com

Bulk FinFET Processing Technology

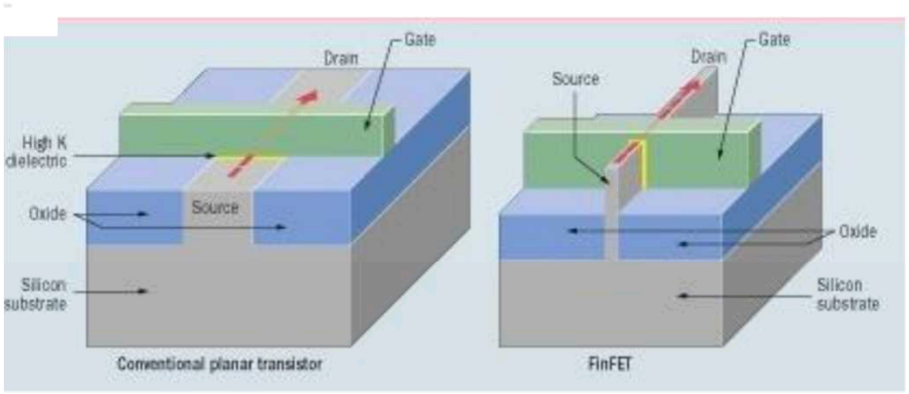
- Increasing processing complexity
- More challenging lithography
  - Quad patterning
- Line edge roughness
- Isolation steps
  - STI
  - CSD/SSRW

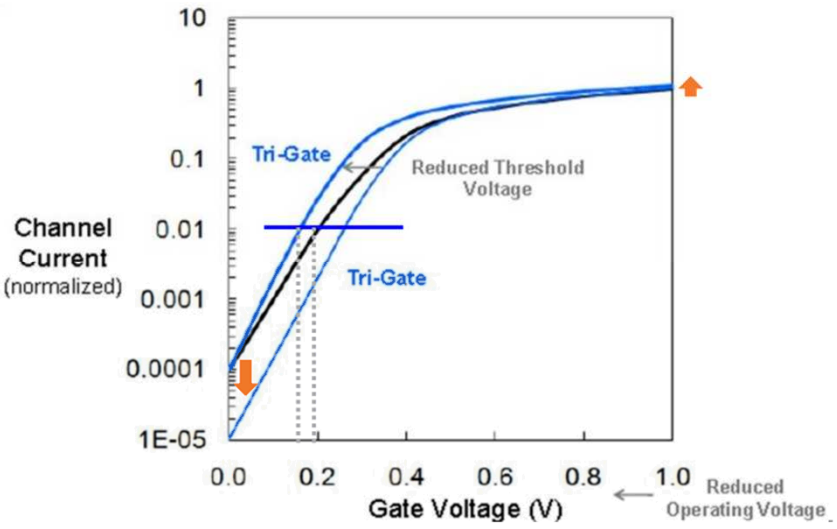


A. Yagishita (Toshiba), SOI Short Course (2009)

Breakthrough Performance / Power

Sandia National Laboratories



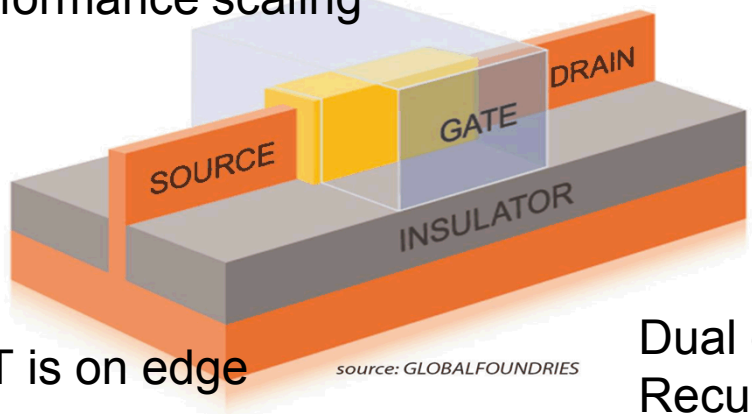


Advantages	Challenges
Better gate control	Higher parasitics than planar
Low power operation	Fixed height, discrete number of Fins
Higher drive current	Challenging process technology
Lower leakage	
Better reliability?	

Uppal (GF), *IIRW* (2016)

Advantages / Challenges

Gate length shrink
Performance scaling



FET is on edge

Dual gate
Recuces I_{off}

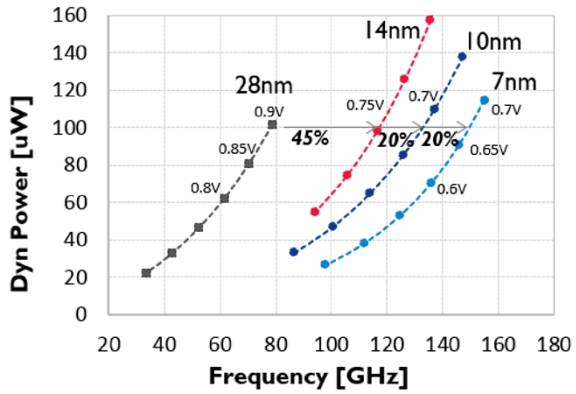
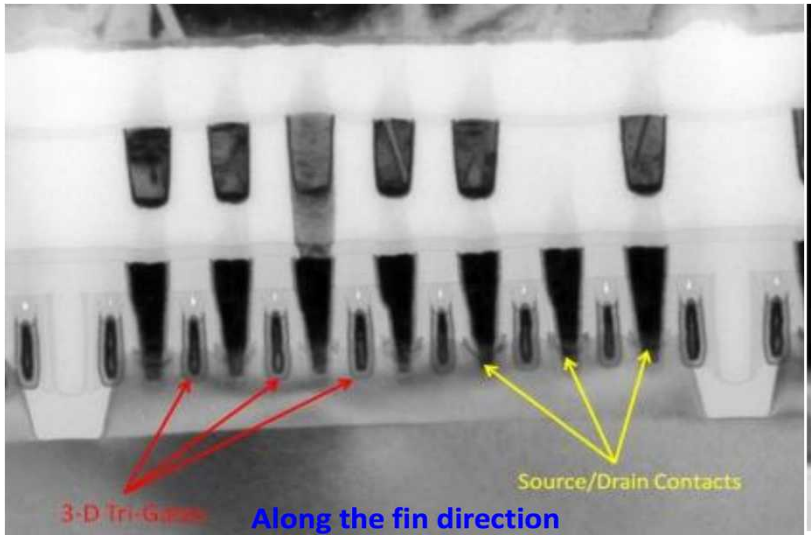
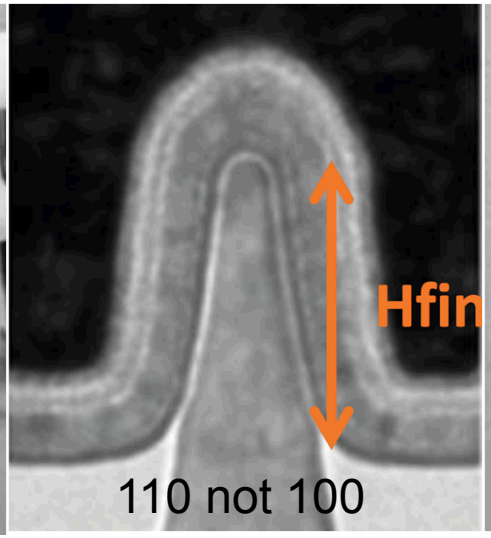
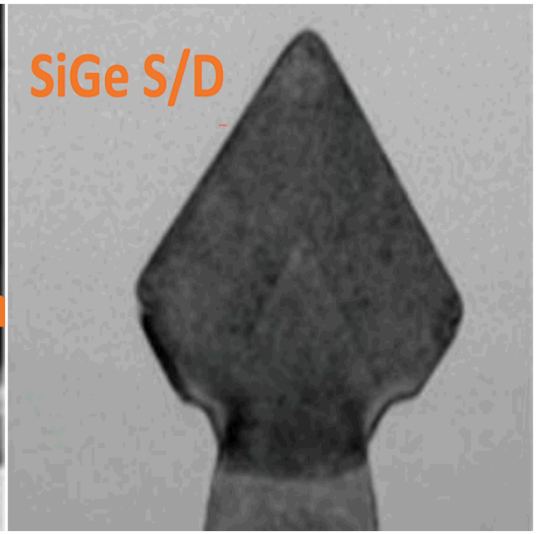


Fig. 2. Expected speed improvement from 28nm planar to FinFETs 14nm, 10nm, 7nm, at constant dynamic power and leakage power for High performance devices (Ioff≈15nA per device) on Ring oscillators of inverters with Fan-Out 3, 9Tracks library, no BEOL load.

M. G. Bardon (IMEC) *ICICDT* (2015)







Uppal (GF), *IIRW* (2016)

Reliability Outlook

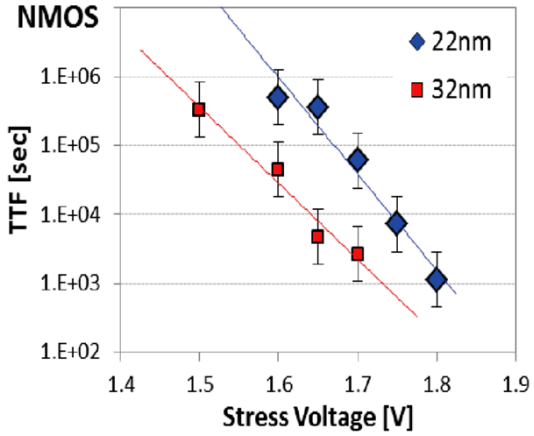


Fig. 2. NMOS TDDB in the 22nm technology is improved over 32nm [2] and indicates the intrinsic robustness of the tri-gate architecture.

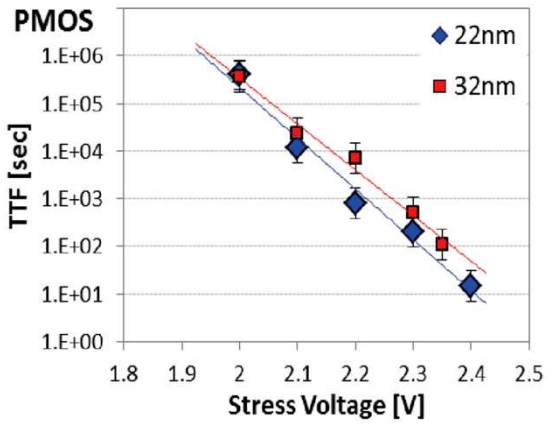


Fig. 4. PMOS TDDB has a slightly higher VAF from oxide scaling, resulting in matched behavior to 32nm at operating voltages.

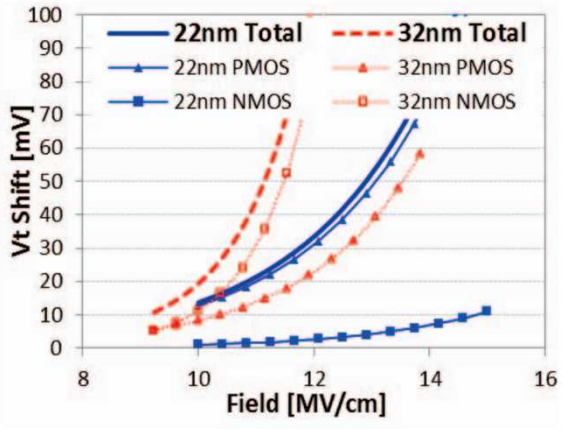


Fig. 6. 22nm BTI is comparable to 32nm. NMOS is significantly improved due to gate optimization, oxide scaling, and WF tuning.

- nMOS/pMOSFET TDDB shows some improvement over planar at 22 nm, expected to get better with continued gate scaling
- pMOSFET NBTI did show some regression, overall BTI improved
- Trends expected to continue at 14-nm
- Self-heating a significant issue

Ramey (Intel) IRPS (2013)

Review – Soft Error Studies

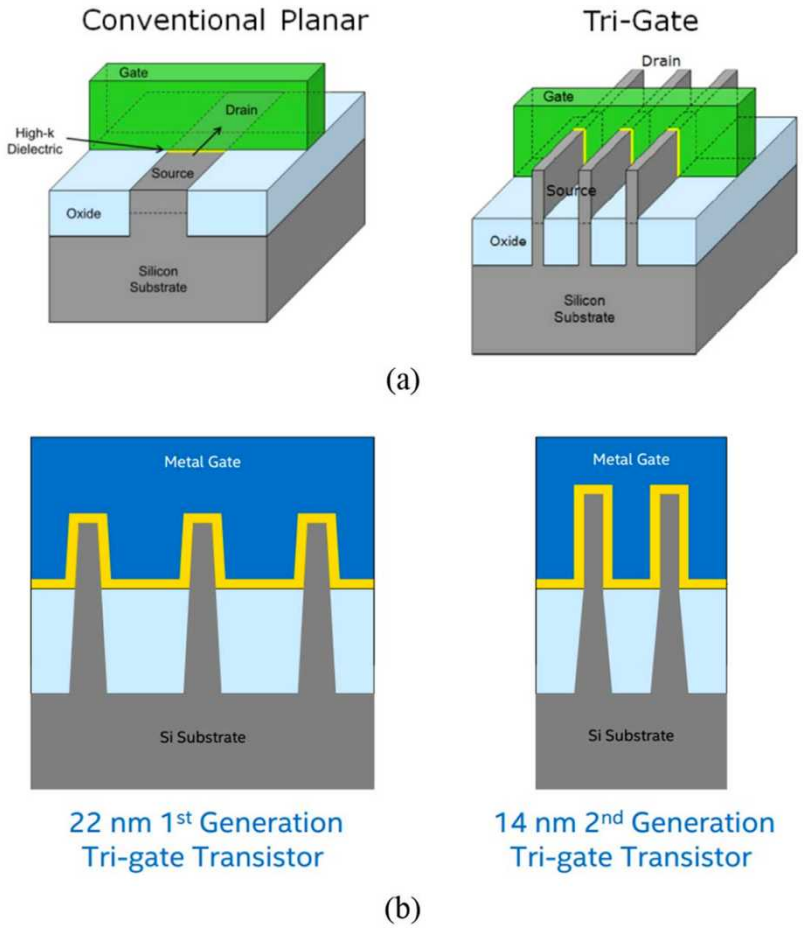


Fig. 1. Reduction in sensitive charge collection volume (a) from planar to tri-gate transistor and (b) from 22-nm tri-gate to 14-nm tri-gate transistor. 14-nm fins have smaller footprints and higher drive strengths due to taller fins, enabling an aggressive scaling of the number of fins and effective sensitive volume per cell.

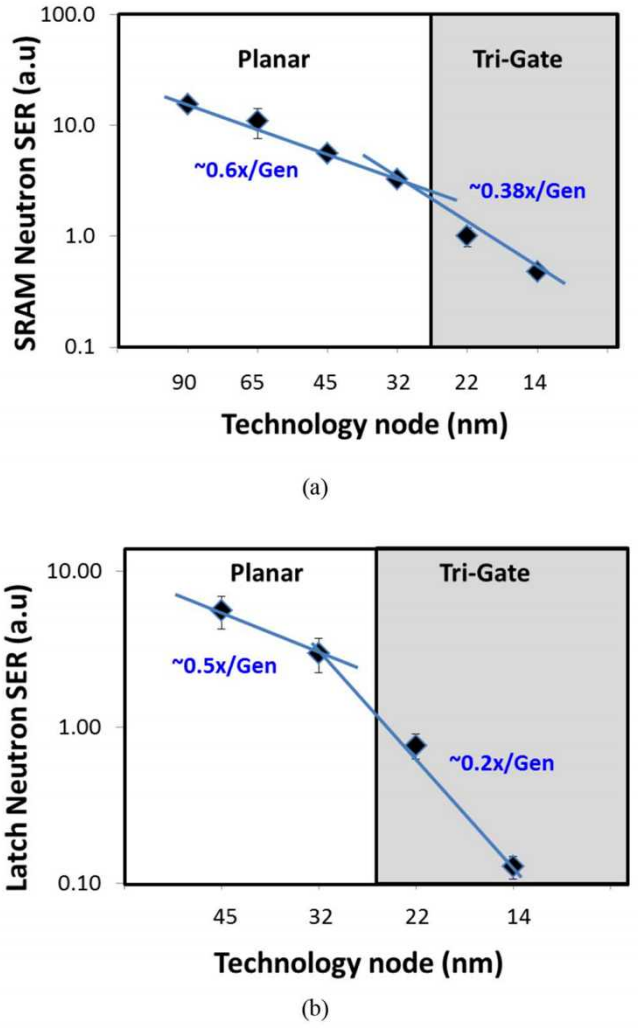


Fig. 6. Change in high-energy neutron SER with technology scaling in (a) SRAM and (b) latch at 0.7 V. Lines serve as a guide to the eye and are not fitting lines.

Seifert (Intel) IEEE TNS (2015)

Review – TID Work

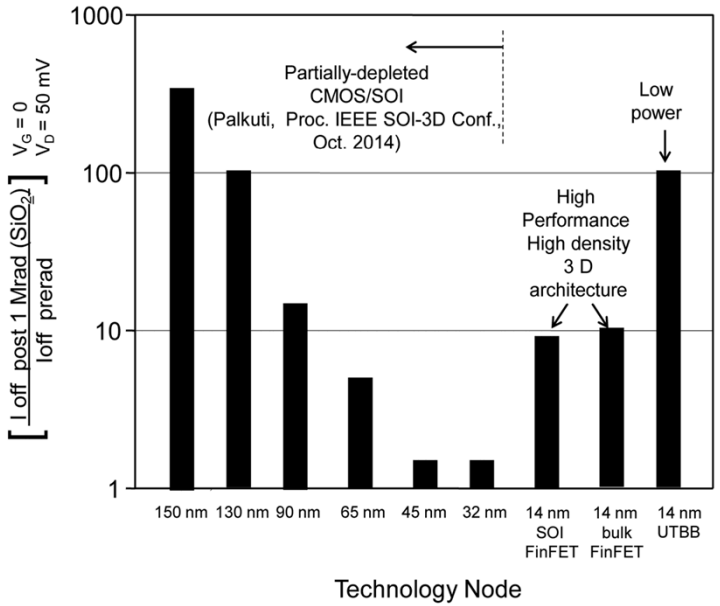


Fig. 1. Commercial Technology TID response of off-state current for a dose of 1 Mrad (SiO_2) versus technology scaling showing vulnerability turnaround after 32 nm.

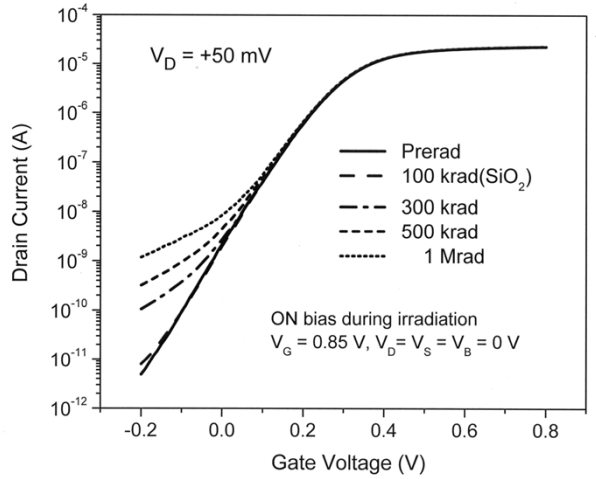


Fig. 6. Current-voltage characteristics versus 10 keV X-ray dose (517 rad(SiO_2)/s) for 14 nm bulk nFinFETs in the linear region (V_D = +50 mV). ON bias during irradiation.

- Initial assessment of bulk vs SOI 14-nm FinFETS
- $I_{ds,off}$ vs feature size scaling trends

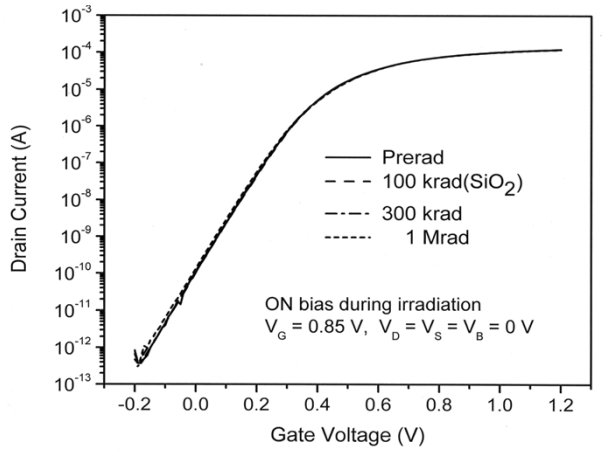


Fig. 2. Current-voltage characteristics versus 10 keV X-ray dose (517 rad(SiO_2)/s) for 14 nm SOI nFinFETs (V_D = +50 mV). ON bias during irradiation.

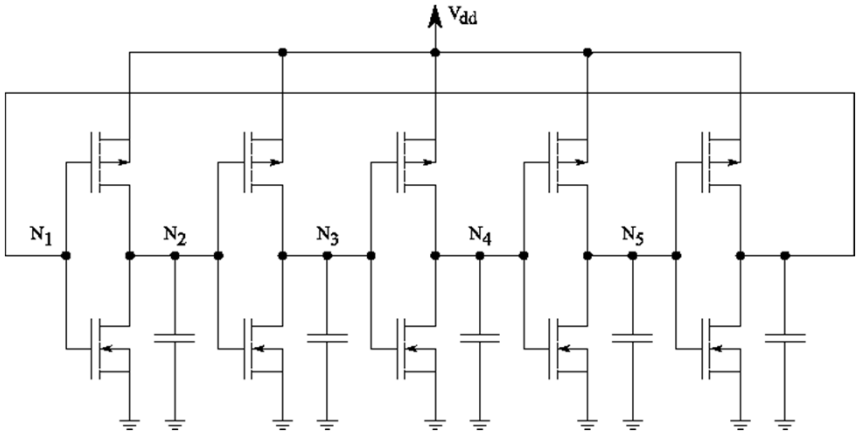
Hughes (NRL) REDW NSREC (2015)

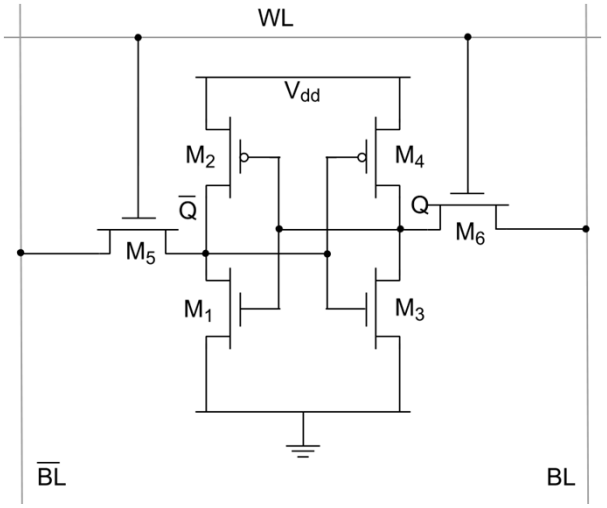
Sandia National Laboratories

The Deep Dive

IN-DEPTH STUDY OF TID IN 14-NM FINFETS

Description of Test Structures





- Single logic and IO transistors in all V_{th} flavors
- Special Structures
  - Ring oscillator (RO) (RF) transistors
  - Static random access memory (SRAM) transistors

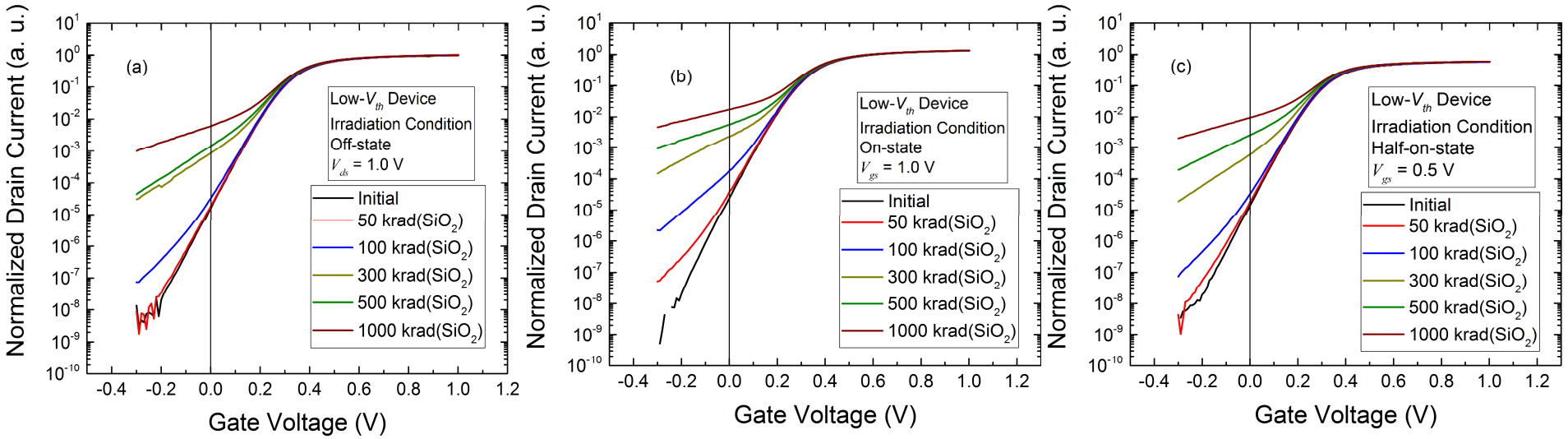
Experimental Methods

- Information extracted from I_{ds}-V_{gs} curves
  - V_{th} – linear region approximation
  - $g_m = dI_{ds}/dV_{gs}$
  - $I_{ds,on} = I_{ds}$ @ $V_{gs} = 0$ V, $V_{ds} = 50$ mV
  - $I_{ds,off} = I_{ds}$ @ $V_{gs} = 0$ V, $V_{ds} = 50$ mV
- Bias Conditions
  - Off-state: $V_d = 1.0$ V, $V_g = V_s = V_b = 0$ V
  - On-state: $V_g = 1.0$ V, $V_d = V_s = V_b = 0$ V
  - Half-on-state: $V_g = 0.5$ V, $V_d = V_s = V_b = 0$ V

Sandia National Laboratories

TID DEPENDENCE ON IRRADIATION BIAS CONDITION

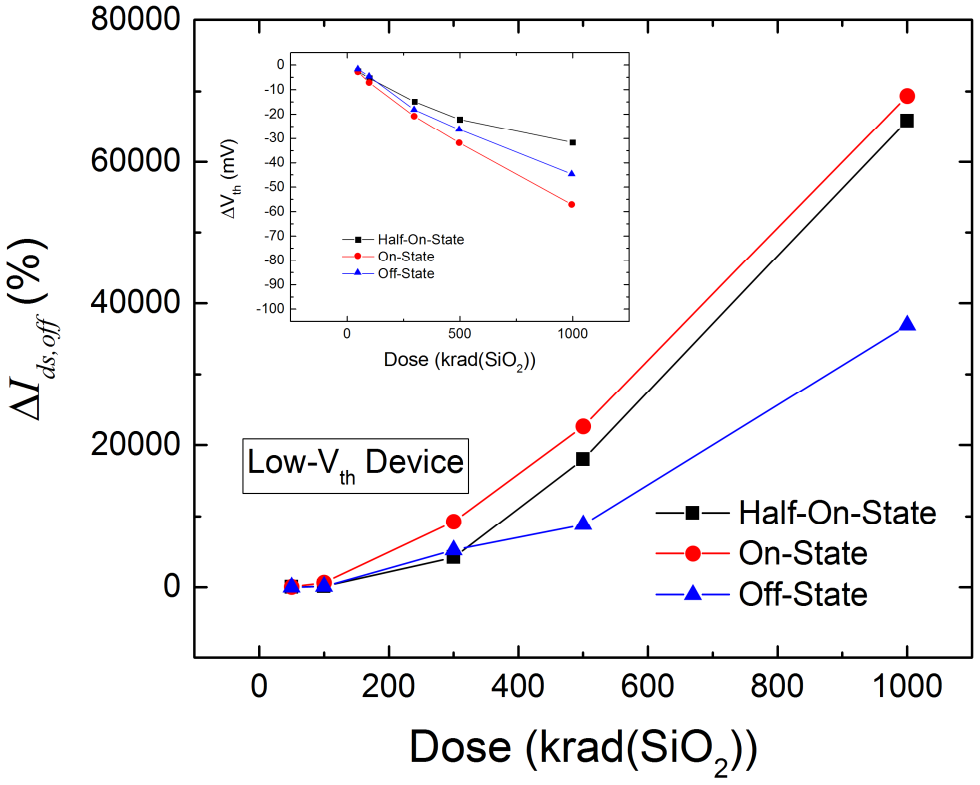
Low-V_{th} Device Bias Dependence



- Large changes in $I_{ds,off}$
- Gate-controlled leakage component
- *On*-state condition gives largest degradation
- Minimal change in V_{th}

TID Irradiation Bias Dependence

- $\Delta I_{ds,off}$ shows most degradation for on-state condition
- ΔV_{th} fairly similar for all bias conditions (and small)
- Lower operating voltage (half-on-state) shows marginal improvement in $\Delta I_{ds,off}$ and ΔV_{th} compared to full on-state



Degradation Mechanisms

- Gate degradation from interface traps and positive charge trapping in oxide bulk
- Leakage current (and gate control component) from charge trapping in STI

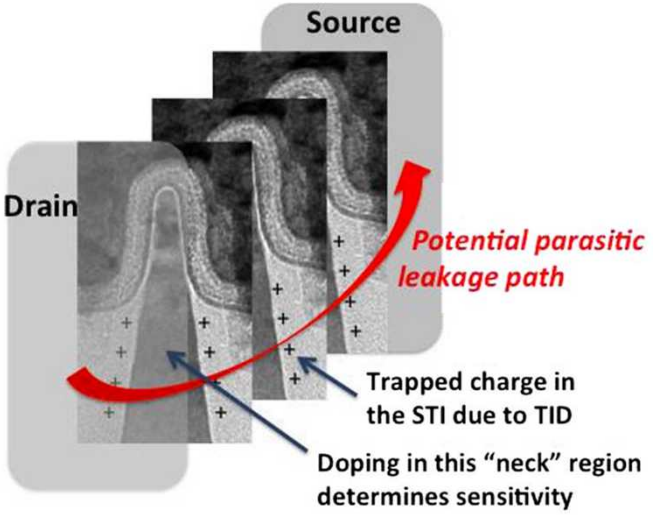
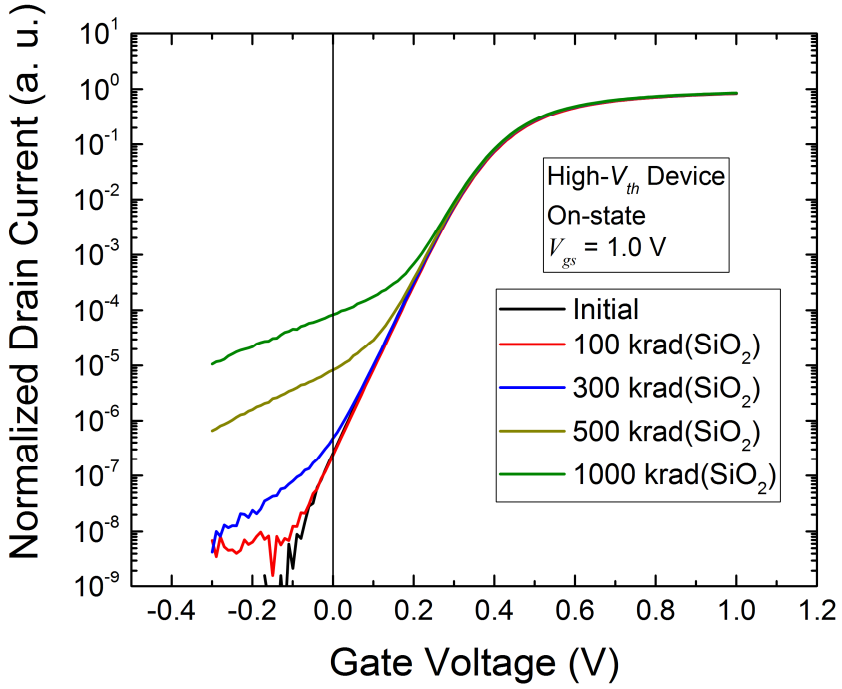
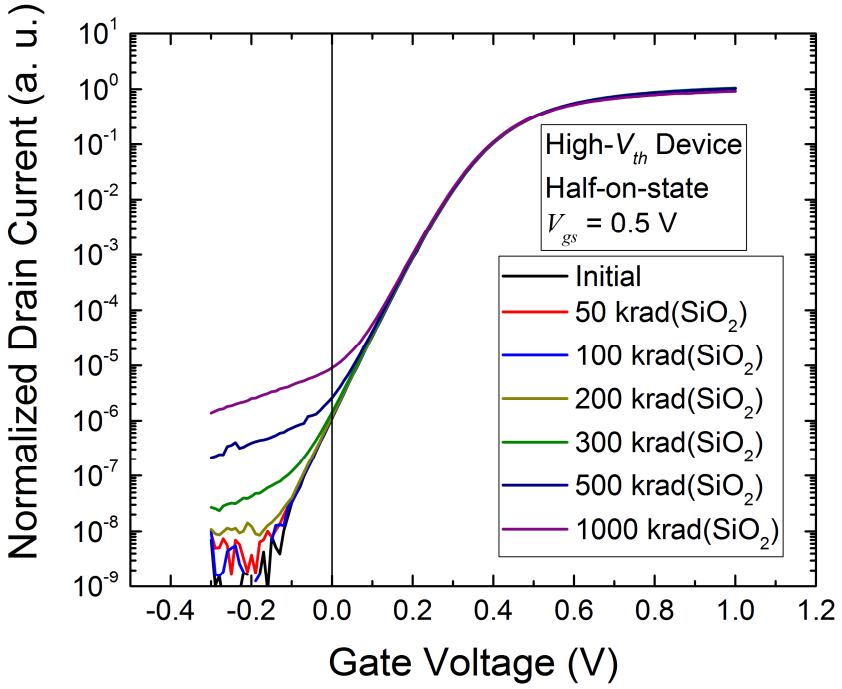


Fig. 4. Schematic showing the trapped charges in the isolation oxide in a multi-fin FET (representative figure only, not to scale). [20].

Chatterjee IEEE TNS (2013)

High-V_{th} Device



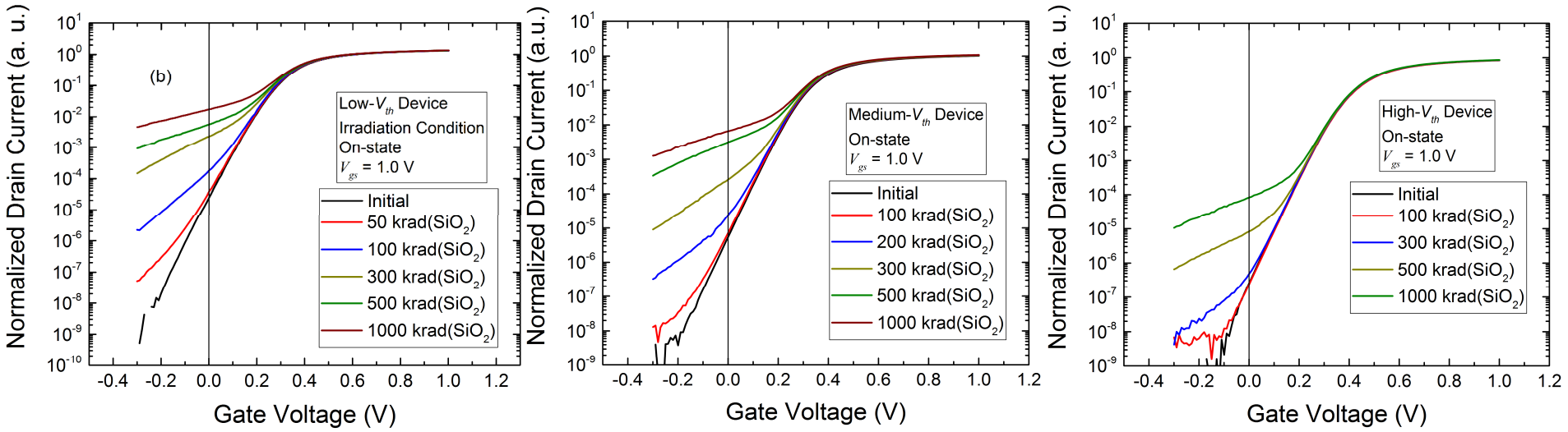


- Apparently less off-state leakage compared to low-V_{th} device
- Reduced operating voltage has a greater impact on TID degradation for higher V_{th}device

Sandia National Laboratories

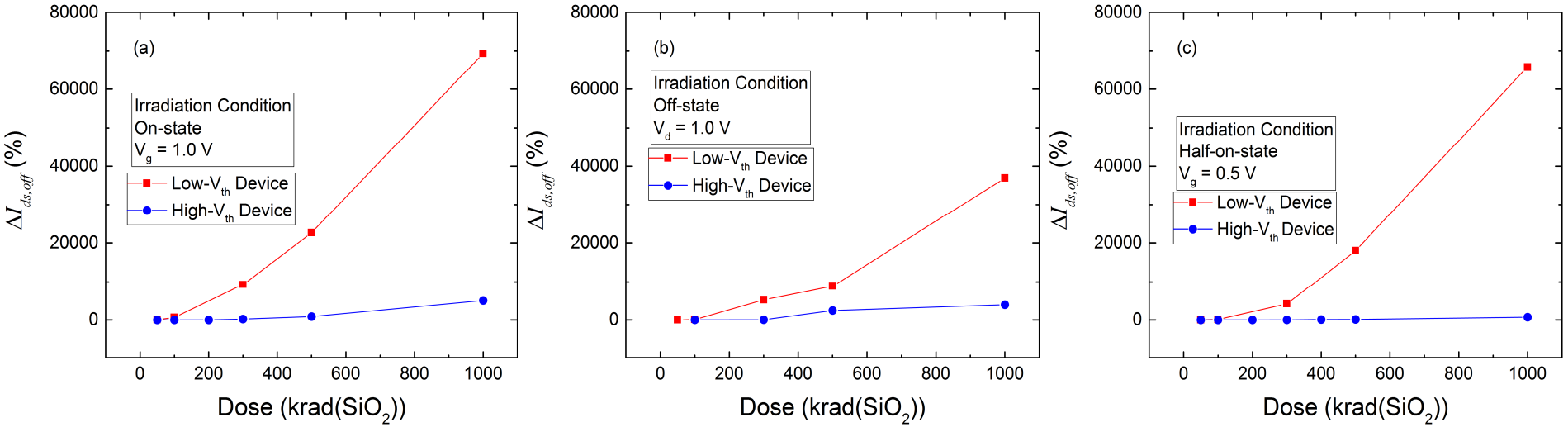
TID DEPENDENCE ON DUT V_{TH}

Different V_{th} Devices – On-State



- Increasing V_{th} shows less $I_{ds,off}$ degradation for equivalent dose
- Process level decisions will clearly impact TID impact on devices, circuits, and Ics

Comparison of TID Variability for Different V_{th}

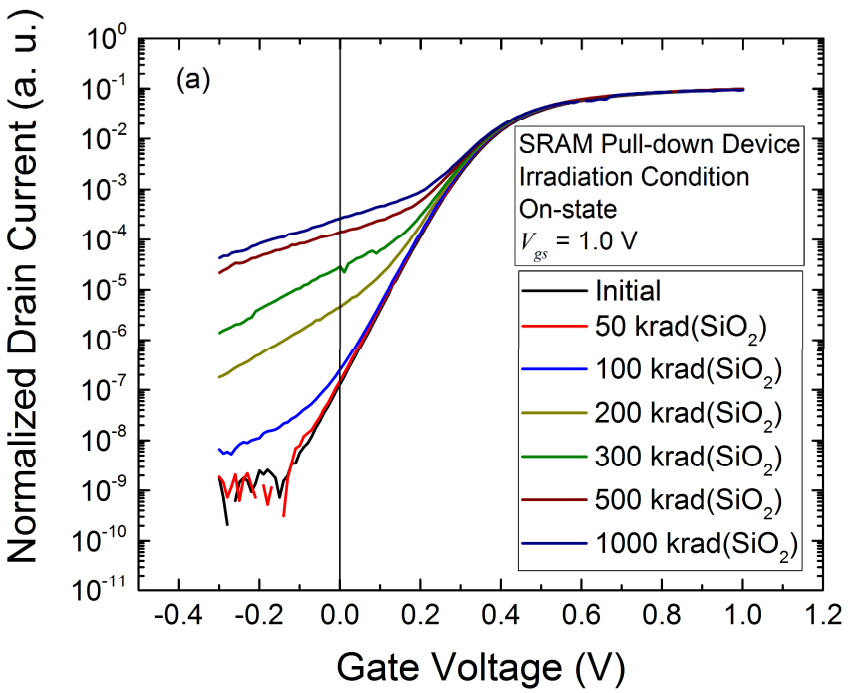


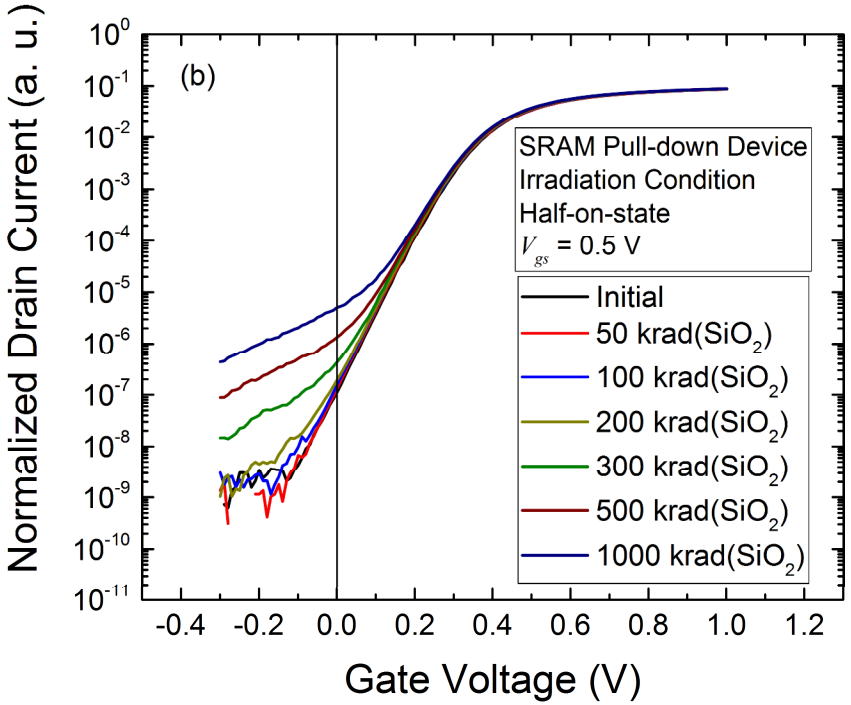
- High-V_{th} device shows less $\Delta I_{ds,off}$ compared to Low-V_{th} devices
- On-state appears to be the worst case for device leakage response

Sandia National Laboratories

TID RESULTS FOR SRAM PASS GATE AND PULL DOWN DEVICES

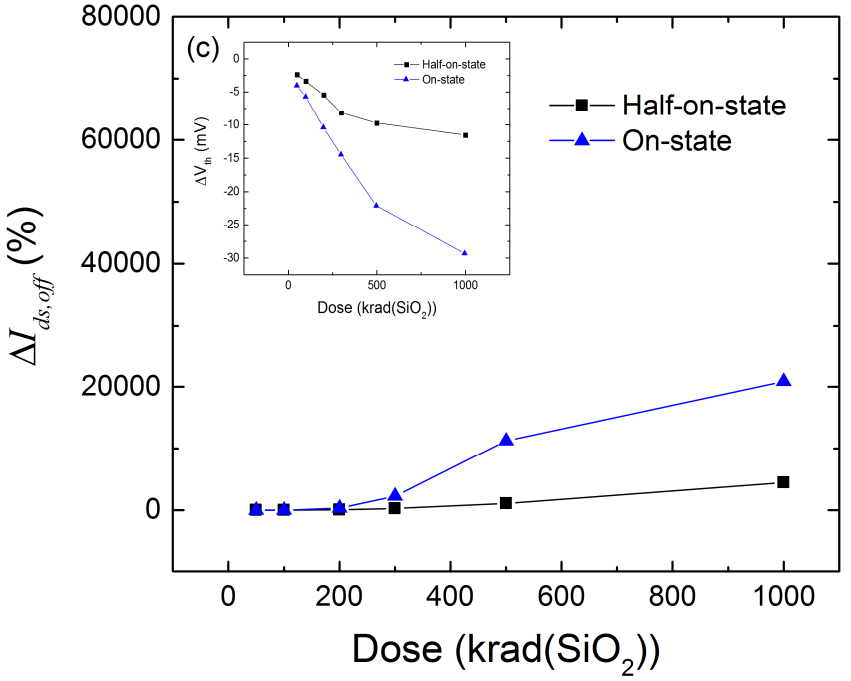
I_{ds}-V_{gs} curves for SRAM Pull Down Device





Summary of SRAM Pull Down Parametrics

- ΔV_{th} ~ 10-50 mV consistent with previous results on single transistor devices
- Large reduction in $I_{ds,off}$ for reduced operating voltage conditions



Conclusions

- High-V_{th} devices give a lower post-irradiation $I_{ds,off}$ than Low-V_{th} devices
- On-state bias condition appears to be the worst case for $I_{ds,off}$ for all the transistor variations evaluated in this work
- Lower voltage operating conditions (half-on-state) (near-threshold computing/dynamic voltage frequency scaling/low power applications) remain of interest as a means to reduce TID degradation of FinFET devices