Final Report

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Executive Summary

The DISTINCT project research objective is to develop an innovative N-port power converter for a utility-scale PV system that is modular, compact and cost-effective and that will enable the integration of a high-frequency, high-voltage solid-state transformer. The novelty of the proposed research is the electrical power conversion architecture using an N-port converter system that replaces the output 60Hz transformer with an integrated high-frequency low-weight solid-state transformer reducing power electronics and BOS costs to meet SunShot goals through modularity and direct high-voltage interconnection. A challenge in direct integration with a 13.8kV line is the high voltage handling capacity of the converters combined with high efficiency operation. The front-end converter for each port is a Neutral-Point Clamped (NPC) Multi-Level dc-dc Dual-Active Bridge (ML-DAB) which allows Maximum Power Point Tracking (MPPT). The integrated high frequency transformer provides the galvanic isolation between the PV and grid side and also steps up the low dc voltage from PV source. Following the ML-DAB stage, in each port, is an inverter with H-bridge configuration or NPC configuration. *N* number of NPC inverters' outputs are cascaded to attain the per-phase line-to-neutral voltage to connect directly to the distribution grid (i.e. 13.8 kV). The cascaded inverters have the inherent advantage of using lower rated devices, smaller filters and low Total Harmonic Distortion (THD) required for PV grid interconnection.

Our analysis and simulation results show improved performance on cost, efficiency, service life with zero downtime and THD. A comprehensive control scheme is presented to ensure the maximum power from each port and each phase are sent to the grid. A functional prototype of a 2-port converter with ML-DAB and cascaded H-bridges has been designed, built, and tested in a laboratory setup to verify the target technical metrics. The N-port converter system due to its modular structure with individual control per port can be easily adapted to integrate functionalities that go well beyond the conventional grid support functions and mitigates impacts of forecasted fast ramp downs or ramp ups and single-fault conditions by automatic reconfiguration of the output.

An integral part of this effort is to increase the diversity of students pursuing solar research, to enhance and expand the solar classroom experience and to provide extensive opportunities for solar research and internships with an expansive network of strategic partners locally, regionally and nationally. The University of Texas at San Antonio is in a unique position as it serves a broad and diverse student body and a San Antonio community committed to large-scale solar deployments exceeding 400MW. These attributes coupled with solar research capabilities to address SunShot goals can prepare student leaders to transform our energy future. Assessments and target metrics on the various activities associated with the education task are presented which are based on the student participation, diversity, new solar content in courses, research opportunities, publications, student jobs and internships.

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Background

The DISTINCT project is focused on the concept design and development of innovative N-port power electronic converter architecture with integrated high-frequency high-voltage solid-state transformer. The concept reduces power electronics and BOS costs through modularity and direct high-voltage interconnection without the need of heavy, low-frequency 60Hz transformers. In this section, key peer-reviewed literature on the latest developments in the field of power converters for utility-scale PV systems, are discussed. This discussion places the DISTINCT project in living context alongside the current state-of-the-art.

In [1], a 3-phase modular cascaded H-bridge multilevel inverter has been proposed for grid-connected PV systems. The cascaded full-bridge inverters are connected directly to the PV panels. The topology effectively uses the individual H-bridges to interface with PV with appropriate control. The proposed system still needs a 60Hz transformer to step-up the voltage to the distribution level. Various types of isolated and non-isolated dc-dc converter for PV front end have been discussed in [2]. In [3] a cascaded modular multilevel converter for grid-connected PV systems is proposed where cascading has been used both in DAB output dc-stage and after the inverter module to achieve higher voltages for direct interconnection with the three-phase grid. The authors in [3] discuss the challenges involved in difference in PV power for each stage and propose a decoupled active and reactive power control strategy to overcome the challenges. The same challenges are valid for the proposed N-port converter and can be fully leveraged to enhance the performance of the N-port converter. The authors in [4] propose a multi-port multi-level topology for PV application where the dc-ac stage uses 4-quadrant switches instead of dc-dc and dc-ac separate stages. Multiple ports of inverters are then cascaded to reach the utility scale voltage level. In terms of the number of semiconductor switches used in dc-ac converter, this is the same as separate dc-dc and dc-ac converters. The DISTINCT project effort is different from [4] in terms of two stages of conversion that provide additional flexibility in control and reconfiguration in the case of fast ramps or faults.

In [5-6], NCSU FREEDM center has proposed a dc-dc DAB converter that uses 15kV IGBTs instead of cascading to reach higher voltage. The primary side has three-level three-leg bridge with Y-connection and the secondary side has two-level three-leg bridge having Delta-connection across the HF transformer. A 100kW, 22kV/800V, 10kHz dc-dc converter design is shown in the paper. The work on 15kV SiC by FREEDM center introduces a non-cascaded approach to realize high voltages but the high voltage in itself pose several challenges in handling the parasitic at high frequencies. The FREEDM center work uses a NPC DAB to suggest methods for Zero Voltage Switching to reduce switching losses. In the DISTINCT project a DAB NPC is used in every port and even when 15kV SiC devices come into production, the NPC will offer ZVS advantages to improve efficiency. In addition, the DISTINCT project can leverage SiC Mosfets by cascading them to exceed technical target metrics on THD and efficiency. Hence the current DISTINCT effort remains important and significant. On the advances in DAB, [7] proposes a semi-dual active bridge (S-DAB) dc-dc converter for

unidirectional power flow (e.g. PV application) where the load-side bridge has two switches and two diodes instead of four active switches as in a conventional DAB. Operating principles and characteristic advantages are similar to a conventional DAB. Here the primary bridge produces a two level and secondary bridge produces a three level voltage waveform. Analysis for soft-switching operation are also presented. But the S-DAB lacks an NPC stage especially for high-voltage applications. In [8], a high-frequency-link-based grid-tied PV system is proposed. The innovations are in the small dc bus link capacitor thereby improving the reliability of the system replacing electrolytic with film capacitors. The results are proven in a 5kW prototype converter. DISTINCT project used this paper and all the references [1-8] to develop technical target metrics to meet and exceed the state-of-the-art.

Introduction

Significance and Innovation

The project continues to be significant as compared to the state-of-the-art in the following:

1. The N-port converter effectively eliminates the need of line frequency 60Hz step-up transformers in each inverter station and hence can contribute to significant reduction in BOS costs such as shipping, installation and labor for MW inverter stations.
2. The modularity and automatic re-configurability in the DISTINCT converter configuration enables zero downtime i.e., as one port is getting replaced, the N-1 ports continue to deliver the power to the grid and hence better serviceability.
3. While advances in SiC IGBT 15kV semiconductor technology is likely to become a reality in the next few years, the multi-level NPC DAB topology remains innovative as it provides the methodology for soft-switching operation (ZVS) to reduce switching losses at very high voltages and at the same time reduces the high dv/dt associated with high voltage switching.
4. The proposed architecture can be easily reconfigured for single-fault conditions when compared to any other existing architecture.
5. The architecture is platform-agnostic to either PV or storage or both and hence in the future, when PV systems use energy storage for ramp control, N-port architecture provides a modular structure with reduced power electronics costs.
6. The University of Texas at San Antonio is in a unique position as it serves a broad and diverse student body and a San Antonio community committed to large-scale solar deployments exceeding 400 MW. These attributes coupled with the solar research capabilities to address SunShot goals are preparing student leaders to transform our energy future.

Summary of SOPO tasks

A summary of SOPO tasks for this project is given below:

Task 1 (T-1) Analyze, Design and Develop N-port converter

This research task includes formulating design and performance requirements, analyzing in detail the N-port converter and designing and building a laboratory proof-of-concept N-port converter. *Milestone M(T-1)*: Build and test an N-port converter functional laboratory prototype that meets the design and performance requirements for dc-dc and dc-ac conversion

Task 2 (T-2): Ramp Forecasting Functionality Integration with Control Electronics

This task develops control algorithms for N-port converter that will allow reconfiguration to limit the slope of the ramps. *Milestone M(T-2):* Demonstrate short-term embedded ramp forecasting functionality

Task 3 (T-3): Design for Automatic and Remote Configurability

This task focuses on the design parameters of the N-port converter that allow for configuration changes in response to failures in one of the strings, the dc-dc converter or the inverter. *Milestone M(T-3):* Demonstrate automatic and remote configurability function of N-port converter in laboratory prototype such that the converter maintains the voltage output to the specified value for a single-fault condition.

Task 4 (T-4): Enhance Student Diversity in Solar Research and Education

This task actively recruits students in the DISTINCT program, creates a solar curriculum, creates a research experience program and conducts surveys for assessment. *Milestone M(T-4):* Perform Summative Assessment through documentation of the number and type of new solar course modules and solar classroom training opportunities, the number of students participating in solar related courses and solar research to achieve goals of workforce preparedness for minority students.

Task 5 (T-5): Implement Systems Level Integration and Testing

This task will implement systems level testing in a controlled laboratory environment. The cost effectiveness of the proposed architecture is evaluated at the systems level. Table 1 provides the target metrics for the N-port converter as compared to prior arts [1-3]. Prior arts [1] and [2] have published results for the entire system. Prior art [3] has results only on the DAB with solid-state transformer. Table 1 also indicates the associated SOPO sub-task and Milestones for each metric.

Task 6 (T-6): Evaluate Effectiveness of the Education Plan

This task will focus on evaluating the effectiveness of the education efforts in the DISTINCT program. This task includes the following milestones.

Table: 1 Target Technical Metrics for Proposed N-port Converter

Metric #	Technical Metric	UTSA target	SOPO Task/Milestone	Prior Art #1 [a]	Prior Art #2 [b]	Prior Art #3 [c]
1	Cost	<$0.1/W	ST-5.6	Not given	Not given	Not given
2	Efficiency	>97%	M (ST-5.3)	Not given	Not given	98.5% (DAB, simulated)
3	Service Life	>25 years (Modularity)	M (ST-5.5)	Not calculated	Not calculated	Not given
4	Size and Weight	66% reduction compared to central inverter	M (ST-5.3)	No size reduction	Not given	Not given
5	Control	Ramp control, Reconfiguration for N-1 failure, Power mismatch control	M (ST-5.5)	Power mismatch control only	Power mismatch control only	Not applicable
6	Power Rating	Prototype (P): 10kW Application (A): >1MW	M (ST-5.2)	P: 1.5kW A: >1MW	P: 10kW A: >3MW	P: 7.4kW
7	Grid Performance & Reliability	V-THD: <5% I-THD: <3%	M (ST-5.3)	V-THD: <5% I-THD: 4.6%	V-THD: 4.0% I-THD: 2.5%	Not applicable
8	Others	Reduced Installation, O&M costs compared to central inverter	M (T-5)	Not calculated	Not calculated	Not applicable
9	TRL	4	M (T-5)	3	3	2
10	Commercialization	Cost benefits analysis, Pathway to commercialization	ST-5.6	None	None	None

[a] Xiao, Bailu; Hang, Lijun; Riley, Cameron; Tolbert, Leon M.; Ozpineci, Burak, "Three-phase modular cascaded H-bridge multilevel inverter with individual MPPT for grid-connected photovoltaic systems," *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*, pp.468,474, 17-21 March 2013

[b] L. Liu, H. Li, Y. Xue and W. Liu, "Decoupled Active and Reactive Power Control for Large-Scale Grid-Connected Photovoltaic Systems Using Cascaded Modular Multilevel Converters," IEEE Transactions on Power Electronics, vol. 30, no. 1, pp. 176-187, 2015

[c] A. Tripathi, K. Hatua, K. Mainali, D. Patel, A. Kadavelugu, S. Hazra and S. Bhattacharya, "Design Considerations of a 15kV SiC IGBT Based Medium-Voltage High-Frequency Isolated DC-DC Converter," IEEE Transactions on Industry Applications, 2015

Milestone (Subtask 6.1): A formal mechanism in place to track student jobs/internships, to collect surveys from research partners and to update the solar research experience program at UTSA. The minimum target for number of student jobs/internships is 8.

Milestone (Subtask 6.2): A formal recruitment program that will ensure steady pipeline of students for the solar and sustainable energy research program at UTSA. The target for number of students recruited on solar research is estimated to reach 20 students.

Milestone (Subtask 6.3): Solar curriculum assessed by experts in academia and industry for content and research experience. Target is a minimum of 5 solar-based courses with solar content higher than 20%.

Milestone (Task 6): Perform formative evaluation through documentation of student solar preparedness Milestone (ST-6.3), the success of the student research experiences Milestone (ST-6.1), number of peer-reviewed publications (Target: 8), expected number of students Milestone (ST-6.2) and number of solar job placements Milestone (ST-6.1).

Project Results and Discussion

Task 1 (T-1) Analyze, Design and Develop N-port converter

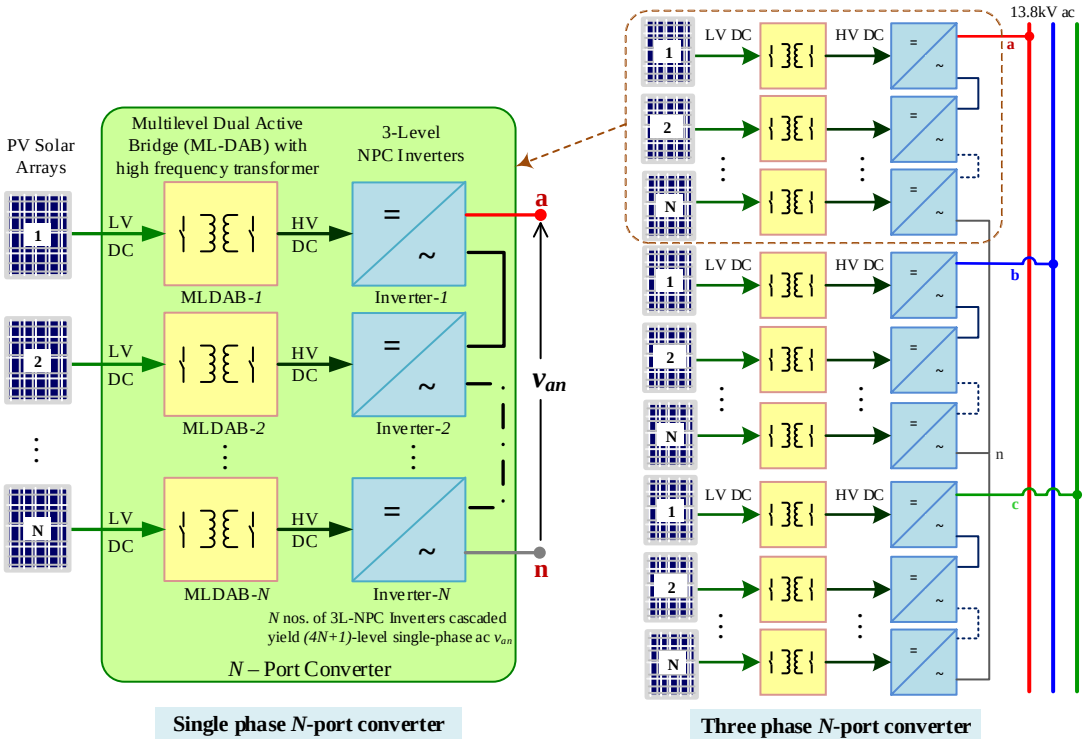


Fig. 1. Block-diagram of proposed *N*-port converter for grid-connected PV system.

The proposed *N*-port converter architecture is shown in Fig. 1. The *N*-port converter consists of *N* numbers of modular dc-dc and dc-ac power conversion stages in between PV and grid interface. Each port includes a dc-dc multilevel dual active bridge (ML-DAB) converter followed by a neutral point diode clamped (NPC) inverter. The high voltage bridge of the dc-dc ML-DAB has a three-level NPC configuration which is connected in a back-to-back manner with the NPC inverter having the common neutral point "*o*" as shown in Fig. 2. The PV dc voltage is stepped up in two stages, first in the dc-dc ML-DAB stage and then in the NPC inverter stage by cascading which yields the overall voltage up to 13.8 kV three-phase line-to-line rms. Each ML-DAB supplies a three-level

NPC-bridge inverter and all the *N* inverters are cascaded to produce a single-phase line-to-neutral voltage of 7.96kV (Fig. 2). The following sub-sections describe the building blocks of this *N*-port converter in detail.

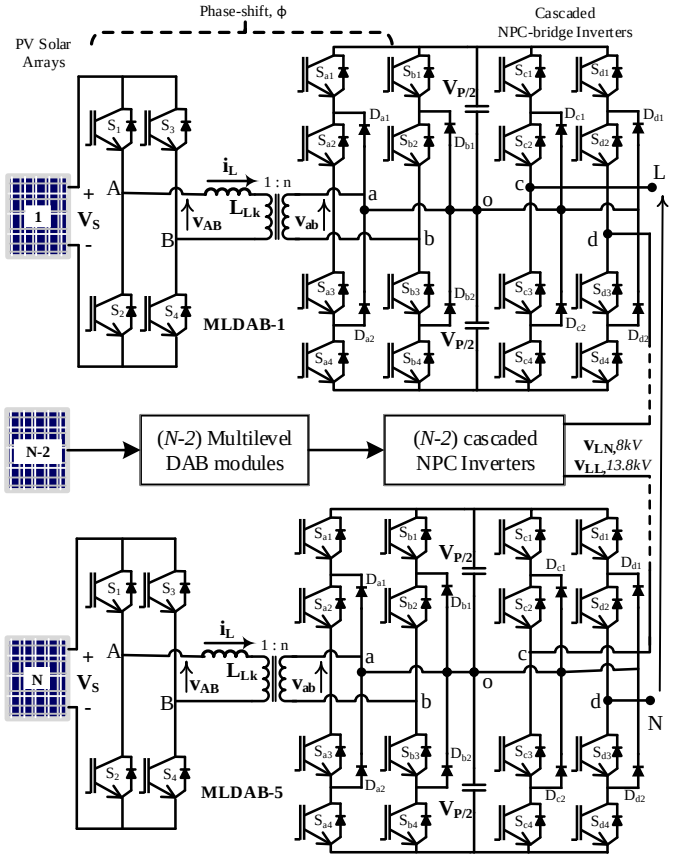


Fig. 2. Schematic of the proposed single-phase *N*-port PV

DC-DC Power Conversion Stage

In the proposed topology, a multilevel DAB (ML-DAB) is the first power conversion stage that boosts up the dc voltage obtained from the PV array and also provides isolation between PV and the grid. The concept of DAB was initially proposed in 1991. Since then DAB is being used for transformer isolated dc-dc conversion in medium and high power applications. In the conventional two-level DAB, two active bridges across a high frequency transformer produce two square waves which are phase-shifted to control the power flow. On the advances in DAB, [8] proposes a semi-dual active bridge (S-DAB) dc-dc converter for unidirectional power flow (e.g. PV application) where the load-side bridge has two switches and two diodes instead of four active switches used in conventional DAB. Operating principle and characteristic advantages are similar to conventional DAB but the S-DAB lacks a multilevel topology (e.g. a NPC stage) suitable for medium or high-voltage applications. The proposed ML-DAB topology for the *N*-port converter (Fig. 2) consists of the PV side primary bridge (switches S_1 to S_4) which

produces a two-level square wave v_{AB} and the secondary bridge which is composed of two 3-level (3L) neutral point clamped (NPC) legs produces a leg-to-leg 5-level (5L) v_{ab} staircase waveform as shown in Fig. 3. Conventionally, NPC legs are used in multi-level inverter applications. In the proposed ML-DAB application, each of the switches in the NPC bridge (S_{a1} to S_{a4} and S_{b1} to S_{b4}) is subjected to a maximum voltage stress of $V_P/2$, while the five-level voltage v_{ab} across the transformer has maximum peak voltage V_P.

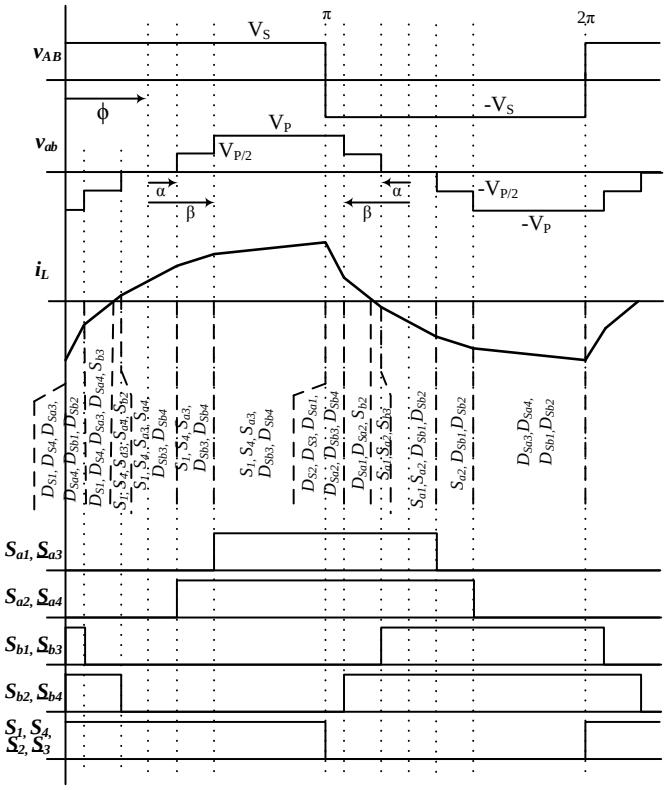


Fig. 3**.** Switch pulses and corresponding voltage waveforms and primary current in a 2L-5L DAB boost topology.

In order to synthesize the 5L voltage v_{ab}, the switching pulses and resulting voltage waveforms are defined with respect to angular distances (i.e. α, β) instead of the duty cycle. These angles α, β are measured symmetrically at zero, π and 2π within a switching period (Fig. 3). The zero and π are considered at the mid-point of the zero voltage level of the 5L voltage v_{ab}. Defining v_{ab} in such a symmetrical way is advantageous in terms of the minimum number of parameters (α, β) required. This provides a straightforward method for derivation of a simple mathematical expression for power flow in the ML-DAB [P-3]. Parameters α and β shape the multilevel voltage waveform and are used in voltage balancing of the clamping capacitors. The phase-shift angle ϕ is independent of α, β and acts as the control parameter to control the power flow in the ML-DAB.

The novelty of such an NPC based ML-DAB is that it can handle a higher output dc voltage (V_P) due to the multilevel topology which reduces both the voltage stress on switches and the dv/dt. The 5L voltage waveform (v_{ab}) across the high frequency transformer also reduces the THD in comparison to conventional 2L DAB. On the other hand, a higher dc voltage (V_P) is achieved in one ML-DAB module (1-port in Fig. 2) using one single-phase transformer, whereas doing the same with two cascaded 2L DABs would require at least two high-frequency transformers and more semiconductor switches.

Power Flow through the DC-DC ML-DAB

Power flow from the PV dc bus to the high voltage dc bus is based on the phase-shift between two active bridges. The phase-shift ϕ is defined based on the phase difference between the fundamental of the primary side 2L v_{AB} and NPC bridge output 5L v_{ab} as shown in Fig. 3.

In this topology, 3L NPC diode clamped legs form the high voltage side multilevel (5L) bridge. Sector-wise inductor current (i_{DAB}) $\mathrm{i_{DAB}}(\theta)$ at all different switching transitions has been analyzed in terms of α, β and ϕ in order to find the power-flow expression. From the fundamental relation of inductor voltage and current we get,

$$v_L = L\frac{di_L}{dt} \tag{1}$$

Here, $i_L = i_{DAB} =$ current through transformer's leakage inductance

$$i_L(\theta) = \frac{1}{\omega L}\int_{\theta_1}^{\theta_2} v_L.d\theta\ ; \qquad \text{where } \theta = \omega t \tag{2}$$

Now writing this $i_L(\theta)$ equation for each segment of $i_L(i.e.\ i_{DAB})$ from 0 to π and equating $i_L(\pi) = -i_L(0)$ as shown in Fig.3 we get,

$$i_L(0) = \frac{V_P}{n\omega L}.\left(\frac{\pi}{2} - \phi\right) - \frac{V_s}{\omega L}.\left(\frac{\pi}{2}\right) \tag{3}$$

The average power flow equation from primary bridge to secondary bridge through the leakage inductance can be written as follows,

$$P_o = \frac{1}{\pi}\int_0^{\pi} v_{AB}(\theta).i_L(\theta).d\theta \tag{4}$$

Putting the expression of $i_L(0)$ in $i_L(\theta)$ at different segment (Fig. 3) we get the power flow equation for the condition of $\beta < \phi < \frac{\pi}{2}$ as,

$$P_o = \frac{V_P V_s}{n\omega L}.\left(\phi - \frac{\phi^2}{\pi} - \frac{\alpha^2}{2\pi} - \frac{\beta^2}{2\pi}\right) \tag{5}$$

$$P_o = m\frac{V_s^2}{\omega L}\left(\phi - \frac{\phi^2}{\pi} - \frac{\alpha^2}{2\pi} - \frac{\beta^2}{2\pi}\right) \quad (6)$$

In the above equations (5, 6), P_0 is the transferred power through the high frequency transformer, V_s is the PV side dc voltage, V_P is the inverter side dc voltage, $\omega = 2\pi f_s$ where f_s is the switching frequency, n is the transformer turns ratio, m is the voltage conversion ratio defined as $m = \frac{V_P}{nV_s}$ and $L\ (= L_{Lk})$ is the primary referred leakage inductance used at the high frequency link.

Soft-Switching operation of ML-DAB

The conventional two level DAB topology can achieve zero voltage switching (ZVS) for all switches in the entire power range when m is equal to unity. The switching pulses for the 2L-to-5L DAB switches are shown in Fig. 3. It is possible to achieve the same in the primary bridge (S_1 to S_4) with the condition of $i_L(0) < 0$. ZVS happens in the switches S_{a1}, S_{a4}, S_{b1}, S_{b4} of the NPC bridge during turn-on at $m = 1$.The rest of the switches (S_{a2}, S_{a3}, S_{b2}, S_{b3}) are also turned on when the current through the switch is already zero. S_{a1} and S_{a4} are to be turned-on at ZVS when $i_L(\phi + \beta) > 0$. S_{b1} and S_{b4} are to be turned-on at ZVS when $i_L(\phi - \alpha) \geq 0$. In order to avoid the short circuit condition between D_{a1}, D_{a2} (7) and D_{b1}, D_{b2} (8) zero crossing of i_L should be avoided in the following regions:

$$(\pi + \phi + \alpha) \leq \theta \leq (\pi + \phi + \beta)\ \&\ (\phi + \alpha) \leq \theta \leq (\phi + \beta) \quad (7)$$

$$(\phi - \beta) \leq \theta \leq (\phi - \alpha)\ \&\ (\pi + \phi - \beta) \leq \theta \leq (\pi + \phi - \alpha) \quad (8)$$

By choosing an optimum range of α, β, ϕ ZVS turn-ON can be achieved in eight out of twelve switches. The above analysis of soft-switching operation in ML-DAB becomes important if the IGBTs are replaced by SiC Mosfets operating at higher switching frequencies. Recent development in silicon carbide (SiC) Mosfets, at the voltage level of 1200 V or higher, offer significantly lower switching loss - as much as 90% compared with silicon IGBTs, due to the absence of tail current and fast recovery characteristics of the body diode. Using SiC based switching devices the switching frequency can be in the order of hundred kHz, which in turn reduces the size of reactive components used in the converter.

Transformer design

The medium / high frequency transformer is used within the dc-dc ML-DAB stage which isolates the PV side from the grid. The transformer frequency is essentially same as the switching frequency used for the 12 switches used in the primary and secondary bridges in the ML-DAB. Higher switching frequency provides lower inductor size. But there is a trade-off while selecting the switching frequency, as higher frequency provides higher switching loss and also higher transformer core loss. Considering the operating frequency and loss profile, various core materials, such as silicon steel, amorphous alloy and nano-crystalline, are used as the transformer core. For frequencies

less than 10 kHz, the amorphous metglas material shows better performance. Based on the prototype voltage and power level a switching frequency of 5 kHz has been chosen as the Metglas Amorphous alloy core is suitable for even higher operating frequencies. Also the IGBTs (Infineon® FF100R12YT3, dual) chosen for the ML-DAB also shows a good switching loss profile at that frequency range. Amorphous metglas alloy 2605SA1 material has also shows high permeability, low core losses, high saturation flux density and narrow hysteresis curve. The design of a 3.4-kVA transformer core and winding wires has been calculated using the area-product method as shown below. The transformer core area product is defined as,

$$A_p = A_{core}A_{window} = \frac{k_{conv}\left(V_1 I_{1_{rms}} + V_2 I_{2_{rms}}\right)}{k_w B_{mx} J_{mx} f_s} \quad (9)$$

where $V_1 \approx V_s = 292\ V, V_2 \approx V_P = 1{,}667\ V$, switching frequency $f_s = 5\ kHz$,

$I_{1_{rms}} = 16.2\ A, I_{2_{rms}} = 2.9\ A$ (RMS values calculated from simulation results),

$k_{conv} = 0.5$ (this factor value is chosen based on the converter topology),

$k_w = 0.4$ (this is the fill-factor having values usually within range of 0.3 to 0.6),

$B_{mx} = 1\ T$ (chosen based on the maximum saturation flux density being 1.56 T),

$J_{mx} = 6\ A/mm^2$ (peak current density with the use of litz wire).

From Equation (9), we get $A_p = 398{,}650\ mm^4$. By using metglass 2605SA1 AMCC-50 core specification, we get, $A_p = 462{,}000\ mm^4, A_{core} = 330\ mm^2, A_w = 1{,}400\ mm^2$.

The conductor cross-section can be found as $A_{cond_1} = \frac{I_{1rms}}{J_{mx}} = 2.7\ mm^2, and\ A_{cond_2} = 0.48\ mm^2$. The number of turns in the transformer is calculated as,

$N_1 = \frac{k_{conv}V_1}{A_{core}f_s B_{mx}} = 89\ turns$, and similarly $N_2 = 509\ turns$. AWG 12 259/36 and AWG 20 38/30 Type 2 litz wire have been chosen for transformer primary and secondary windings, respectively. Fig. 4 shows a transformer and its components used in the 3.34 kVA ML-DAB.

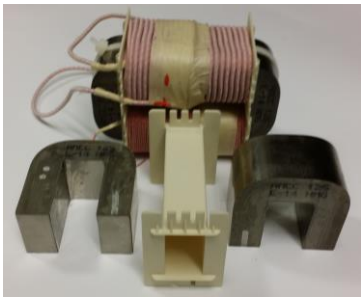
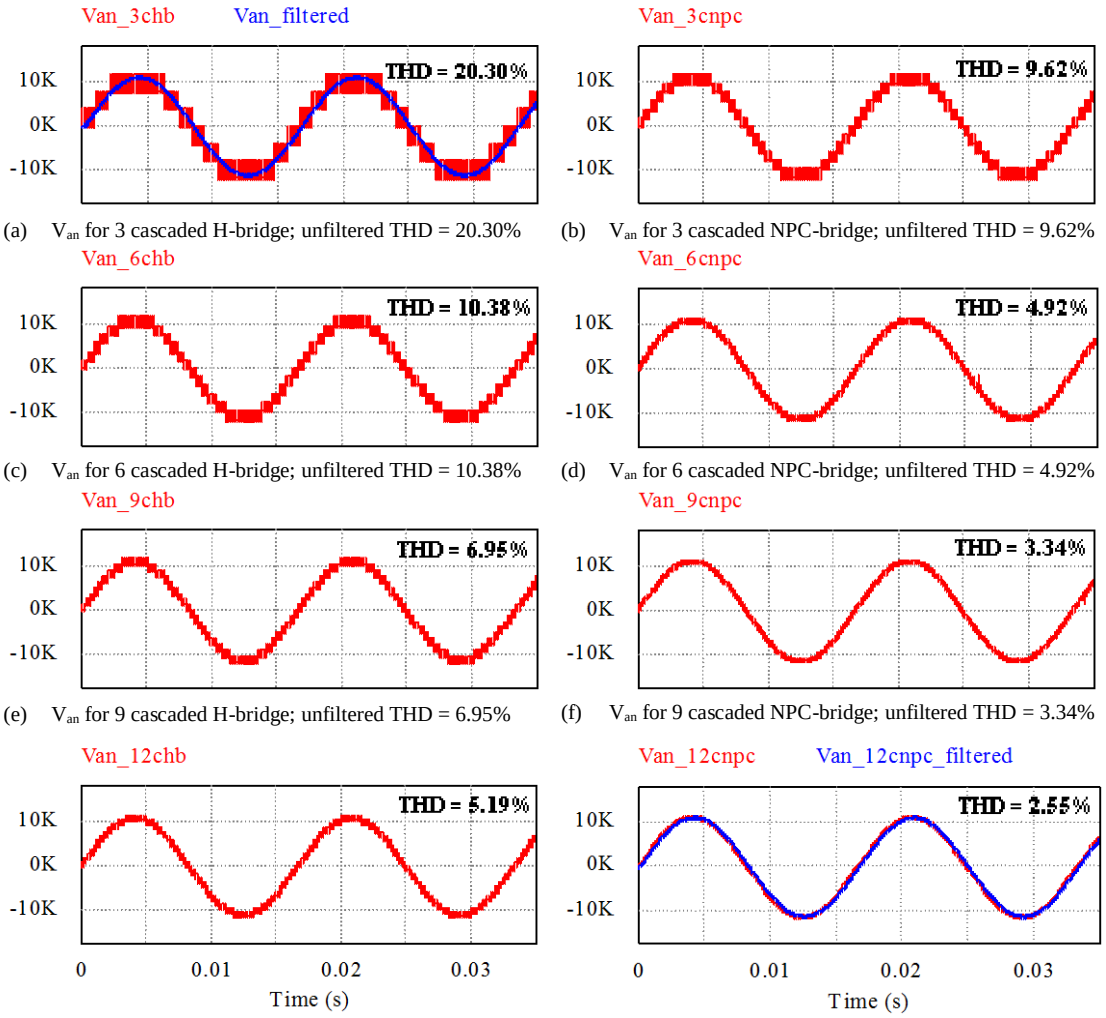


Fig. 4. A 3.34 kVA HF Transformer and its components used in the ML-DAB

Three-level NPC Bridge Inverter

Each port of the cascaded NPC (CNPC) inverter (Fig. 2) is switched to provide a leg-to-leg 5-level ac output (i.e. $V_P, \frac{V_P}{2}, 0, -\frac{V_P}{2}, -V_P$). *N* number of CNPC inverters produce outputs that are phase-shifted from each other by an angle $\frac{180^0}{N}$ to yield a (4N+1) level ac output as discussed later in Section III. In CHB modulation, the number of levels for *N* cascaded H-bridges is (2*N*+1). So, CNPC provides lower THD than CHB because of having more levels in the cascaded output voltage waveform. Fig. 5 shows how the THD is improved with the increase in number of ports (*N*) and how the CNPC provides better THD than CHB for any number of cascaded ports. In comparison to cascaded H-bridge (CHB) inverter stage, the CNPC bridge uses double the number of switches with lower voltage rating. It is also advantageous in terms of low $\frac{dv}{dt}$ and less harmonic distortion inherent to the multilevel topology.



(a) V_{an} for 3 cascaded H-bridge; unfiltered THD = 20.30%
(b) V_{an} for 3 cascaded NPC-bridge; unfiltered THD = 9.62%
(c) V_{an} for 6 cascaded H-bridge; unfiltered THD = 10.38%
(d) V_{an} for 6 cascaded NPC-bridge; unfiltered THD = 4.92%
(e) V_{an} for 9 cascaded H-bridge; unfiltered THD = 6.95%
(f) V_{an} for 9 cascaded NPC-bridge; unfiltered THD = 3.34%
(g) V_{an} for 12 cascaded H-bridge; unfiltered THD = 5.19%
(h) V_{an} for 12 cascaded H-bridge; unfiltered THD = 2.55%

Fig. 5. Left and right columns show the THD values at the cascaded unfiltered voltage output for CHB and CNPC configurations respectively.
From top to bottom (a, b), (c, d), (e, f) and (g, h) - cascaded port number varies as *N* = 3, 6, 9, 12 respectively.

Fig. 6 shows how the gate signals are generated for one leg (i.e. leg-*c* in Fig. 2). The signal generation is done by comparing two level-shifted triangular carriers with a sinusoidal modulating waveform. The other NPC leg (i.e. leg-*d*) has also similar pattern of gate pulses where the modulating signal is shifted by 180^0. The carrier frequency has been chosen as 1.5 kHz for easy visualization, though the simulation and hardware experiments have been performed using higher switching frequency. The simulation and hardware output waveforms are shown under sections V and VI.

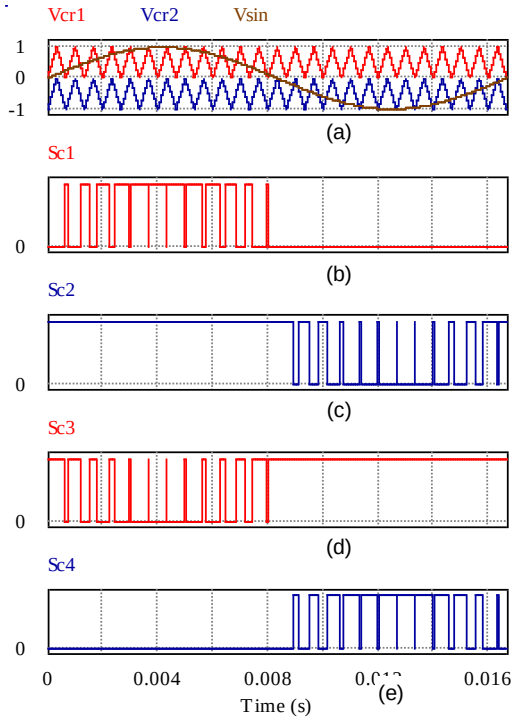


Fig. 6. (from top to bottom): (a) Level-shifted carriers (1.5 kHz) and modulating sine waveform (60 Hz), (b) to (e) gate signals for $S_{c1}, S_{c2}, S_{c3}, S_{c4}$ switches respectively in NPC inverter leg-c as shown in Fig. 2.

Calculation of Power Stage Parameters

In order to validate the control and power flow in the proposed converter configuration, a 500 $kW_{3\text{-}ph}$ converter has been chosen for design purpose. In that case, the per-phase power output should be,

$$P_{1\phi} = \frac{500kW}{3} = 166.67kW \tag{10}$$

Assuming the converter having *N* ports in each phase, each port should process,

$$P_{1port} = \frac{166.67}{N} kW \tag{11}$$

The 500 kW 3-phase (i.e. 166.67 kW 1-phase) converter is considered to be connected to the 3-phase utility grid at the 13.8 kV ($V_{l-l\,rms}$) voltage level. The voltage level of the converter at every point has been calculated based on 13.8 kV grid voltage

and the per-phase line-to-neutral peak voltage at grid interface for one phase (i.e. phase-*a*) is,

$$\hat{V}_{a\mathrm{N}} = \frac{13.8\ kV}{\sqrt{3}}.\sqrt{2} = 11.27\ kV \tag{12}$$

Assuming a 4% reserve the nominal dc voltage at the input of *N* inverter ports should be,

$$V_{dc_{Nport}} \geq 1.04 * \hat{V}_{a\mathrm{N}} = 11.72\ kV \tag{13}$$

For a *N*-port design of the overall single-phase converter (Fig. 2), the input voltage at each inverter port is,

$$V_P = \frac{V_{dc_{Nport}}}{N}\,kV \tag{14}$$

This dc voltage is the output from the 1-port ML-DAB. For example, if *N* = 9 the dc-link voltage $V_P = \frac{11.72\ kV}{9} = 1.3\ kV$. Due to the NPC configuration, the switches on the output side bridge of ML-DAB will withstand half of this voltage, i.e. $V_{c1} = V_{c2} = \left(\frac{V_P}{2}\right) = 650\ V$ as shown in Fig. 2.

The primary bridge dc voltage of the ML-DAB is actually the output voltage from the PV array. Large-scale PV installations usually generate PV power at a voltage level up to 600 V or 1000 V dc. This maximum PV voltage is usually constrained by the PV panel characteristics. Considering the SunPower® E20-435 (435 W, 72.9 V, 5.97 A) solar panel, 45 panels are required at each port for *N*=9. So, 9 series connected panels should make one string with $(72.9 \times 9) = 656\ V$ output. Five such strings should be connected in parallel to make a 19 kW array of 45 PV panels. In this case PV array voltage is,

$$V_s = V_{PV} = 72.9\ V\ \times\ 9\ panels\ in\ series = 656\ V \tag{15}$$

Selection of Semiconductor Switches

Choosing Semiconductor Switches for the NPC Inverter

In comparison to CHB inverter stage, the CNPC bridge uses double the number of switches with half the voltage rating (e.g. 1700 V rated IGBTs instead of 3300 V). It is also advantageous in terms of low $\frac{dv}{dt}$ inherent to the multilevel topology. In the kV voltage levels, typically lower the voltage rating cheaper the semiconductor switches cost. For example, an Infineon 1.7 kV, 340 A dual IGBT module (Part #FF225R17ME3) costs $124.58 each and from the same manufacturer Infineon, a 3.3 kV, 330 A dual IGBT module (Part #FF200R33KF2C) costs $648.56 (Mouser.com). At higher voltage and higher current level this price difference gets more and it becomes a key factor while choosing semiconductor switches for a cost-effective converter design.

In early 1900 it has been discovered that cosmic rays cause random failure of high voltage semiconductor devices, which depends on the blocking voltage of the device, junction temperature and altitude. In order to select the proper switching devices (e.g. IGBT, Diode) in the kV range the cosmic ray effect on device failure must be considered for reliable operation. For IGBT modules with voltage rating higher than 1700V, a DC Stability voltage ($V_{CE\ D}$ for Infineon®) or device commutation voltage ($V_{com@100FIT}$) is mentioned in the manufacturer datasheet. 100-FIT means 100 failures within 10^9 hours of time. This failure is influenced by the device blocking voltage, junction temperature and altitude although the effect of junction temperature and altitude is negligible at room temperature and sea level [10]. As per (16) the dc stability voltage at 100 FIT has been calculated for 1.7 kV, 2.5 kV, 3.3 kV, 4.5 kV and 6.5 kV IGBTs.

$$V_{CE@100FIT} = C_1 - C_2 / \ln\left(\frac{100FIT}{C_3}\right) \tag{16}$$

Here C1, C2, C3 are parameter values found from [9]. Based on this $V_{CE@100FIT}$ voltage value, another metric named “device voltage utilization factor (DVUF)” can be defined to choose an IGBT for cost-efficient design [10]. DVUF is defined as,

$$DVUF = \frac{V_{CES_{rated}}}{V_{CE@100FIT}} \tag{17}$$

Here, $V_{CESrated}$ is the maximum rated voltage mentioned in the IGBT manufacturer datasheet. In order to choose an IGBT module higher DVUF percentage is preferred for an optimum design of the converter. This factor not only optimizes the device utilization efficiency it also reduces the cost of IGBTs in most of the cases. Following Table I summarizes the required IGBT voltage rating for both CHB and CNPC inverters for *N* = 3 to 12.

TABLE I
IGBT SELECTION FOR CHB AND CNPC INVERTERS FOR *N* = 3 TO 12

	Assuming *N*-nos. of CHB modules per phase				Assuming *N*-nos. of CNPC modules per phase			
No. of Modules per phase (N)	V_{dc} at each port of CHB Inverter (V)	Required IGBT $V_{CESrated}$ (kV)	$V_{CE@100FIT}$ (V)	DVUF (%)	$V_{dc/2}$ at each port of CNPC Inverter (V)	Required IGBT $V_{CESrated}$ (kV)	$V_{CE@100FIT}$ (V)	DVUF (%)
3	3906	> 6.5	-	-	1953	4.5	2899	67.37
4	2930	6.5	3865	75.81	1465	3.3	1794	81.66
5	2344	4.5	2899	80.86	1172	2.5	1289	90.92
6	1953	4.5	2899	67.37	977	1.7	1072	91.14
7	1674	3.3	1794	93.31	837	1.7	1072	78.08
8	1465	3.3	1794	81.66	733	1.7	1072	68.38
9	1302	3.3	1794	72.58	651	1.2	No FIT data available. Assuming 720 V (60% of V_{CES})	90.42
10	1172	2.5	1289	90.92	586	1.2		81.39
11	1065	1.7	1072	99.35	533	1.2		74.03
12	977	1.7	1072	91.14	489	1.2		67.92

Choosing Semiconductor Switches for the ML-DAB

For the ML-DAB dc-dc converter the NPC-bridge IGBTs have the same voltage rating as calculated for the NPC inverter in Table I. The primary bridge of the ML-DAB is a 2-level full-bridge. Usually the PV voltage lies within 1000 V dc limit. If the input voltage is within 720 V (assuming 60% of the V_{CES} of 1.2 kV IGBTs), 1200 V IGBTs can be chosen for primary ML-DAB full-bridge. For PV voltages in 720 V to 1000 V range, 1700 V IGBTs are a good choice for the same full-bridge. The parameter values obtained for designing a 3-phase 500 kW *N*-port (i.e. *N* = 3, 5, 8, 12) PV converter are summarized in Table II below. The PV output voltage (V_s) has been chosen based on the string combination of SunPower® E20-435 panels. Based on the power requirement more parallel strings can be combined to form a suitable PV array.

TABLE II
ML-DAB PARAMETER VALUES FOR A 500 KW 3-PHASE *N*-PORT CONVERTER

For a 500 kW 3-ph 13.8 kV Converter	*N* = 3 ports/phase	*N* = 5 ports/phase	*N* = 8 ports/phase	*N* = 12 ports/phase
Power rating of 1ML-DAB	55.6 kW	33.4 kW	20.8 kW	13.9 kW
PV output voltage, V_s (for 10 or more parallel strings)	947.7 V to 1000 V	583.2 to 1000 V	364.5 V to 1000 V	291.6 V to 1000 V
ML-DAB output voltage, V_P	6.67 kV	4 kV	2.5 kV	1.67 kV
HF transformer turns ratio, $n = V_P/V_s$	7.035 or less	6.858 or less	6.858 or less	5.716 or less
Leakage inductor, *L* (for minimum V_s & f_s=5kHz)	0.32 mH	0.20 mH	0.12 mH	0.122 mH
ML-DAB primary IGBTs V_{ce}	1700 V	1200 V	600 V	600 V
ML-DAB secondary IGBTs V_{ce}	4.5 kV	3.3 kV	1700 V	1200 V

In choosing the no. of ports for this *N*-port converter design, the required voltage levels have been considered based on commercially available medium voltage IGBTs (e.g. 1.2 kV, 1.7 kV, 2.5 kV, 3.3 kV, 4.5 kV and 6.5 kV). The diodes and capacitors used in the converter is rated as per the IGBT rating associated with those diodes and capacitors. Some high voltage silicon carbide (SiC) based IGBTs have been discussed in literature [11-13] which would be helpful in reducing number of ports and thus improving the power density of the overall converter.

In large scale PV solar system, MPPT is commonly implemented on the inverter stage. In this converter MPPT, using perturb and observe (P&O) method, is achieved by controlling the phase-shift (ϕ) between the two active bridges in each ML-DAB [58]. The MPPT has also been verified in Simulink® using the incremental conductance algorithm. Based on the variation of insolation, the PV strings generate different currents. To draw the maximum current achievable, thus the maximum power from PV panels, the PV voltage and current are sensed and the derived control signal is translated to desired phase-shift (ϕ). Fig. 7 shows the block diagram of the grid connected PV system with P&O algorithm implemented in NI myRIO-1900®.

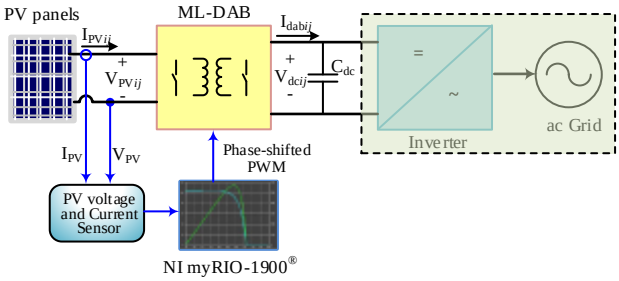


Fig. 7. MPPT control at each ML-DAB module using NI myRIO-1900®

Voltage and current sensors are used to sense the slope of PV power curve. A control voltage from the PI controller will accordingly vary the phase shift of ϕ (5). A P&O algorithm is implemented to achieve the MPPT control and implemented on LabVIEW® in real time. Phase shifted PWM pulses are generated in LabVIEW FPGA. Once the PV power output is connected to the MPPT circuit the open circuit voltage instantly drops to a new value which is dependent on the impedance of the load. The control algorithm implemented on the NI-myRIO sends corresponding switching pulses to the ML-DAB converter to move the new operating point to the maximum power point (MPP).

Milestone M(T-1): Build and test an N-port converter functional laboratory prototype

Each port (i.e. ML-DAB and NPC inverter) has been designed to process 3.34 kW of power for simulation and hardware experiments. Table I shows the voltage levels and parameter values for one port, which has been derived assuming the output of the cascaded NPC (CNPC) bridge is connected to the 13.8 kV utility grid. In order to realize the switching and conduction losses Infineon FF100R12YT3 dual IGBT module and IXYS DSEP 30-12AR clamping diodes are modeled in PSIM® thermal module simulation software. The same IGBTs and diodes are used in the hardware prototype also. The voltage conversion ratio m in the ML-DAB is chosen as unity resulting in the turns ratio $n = 5.7$. The switching frequency f_s is set at 5 kHz. Fig. 8 shows the simulated steady state voltage and current waveforms across the high frequency transformer in the ML-DAB where $V_s = 292V, V_P = 1668V, \alpha = 10^0, \beta = 30^0$.

A scaled down laboratory prototype of the proposed converter (ML-DAB and NPC inverter) has been built for validating the MPPT and power flow control and to observe the key waveforms at different stages of power conversion assuming open loop operation. Each ML-DAB and NPC inverter hardware has been designed to process a maximum 3.34 kW of power. The value of ϕ varies according the control signal received from the MPPT sub-circuit. Fig. 9 shows the experimental waveforms of the ML-DAB for $V_s = 125V, V_P = 650V, \alpha = 10^0, \beta = 30^0, \phi = 70^0$.

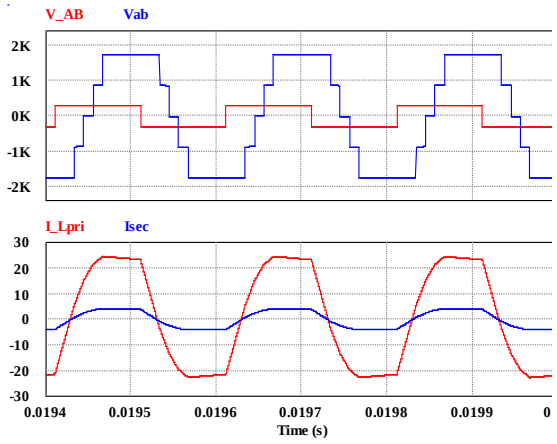


Fig. 8. (from top to bottom) – (a) PV-side bridge voltage, v_B, v_{ab} and (b) current i_{Lpri} and $i_{sec}$of 1-port ML-DAB

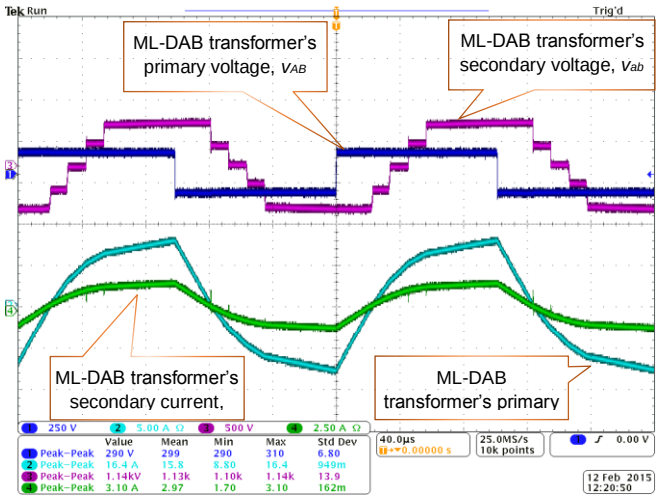


Fig. 9. Experimental output for ML-DAB 2-level voltage v_{AB}, 5-level voltage v_{ab} and currents through the transformers $i_{L_{pri}}, i_{L_{sec}}$; where $V_s = V_{PV} = 125\text{V}, V_P = V_{dc} = 650\text{V}, n = 5.71, \alpha = 10^0, \beta = 30^0$ and $\phi_{ini} = 70^0$.

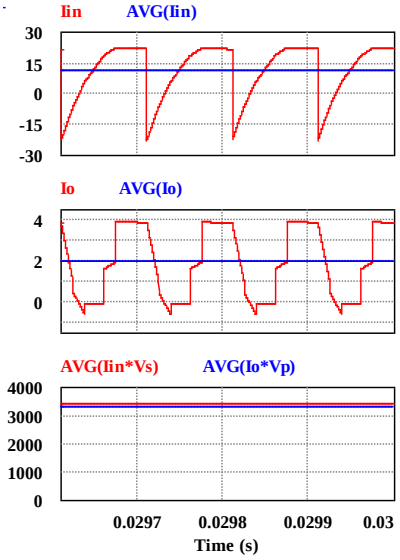


Fig. 10. (a) ML-DAB input current, (b) output current (c) Average input and output power; efficiency = 96.42% .

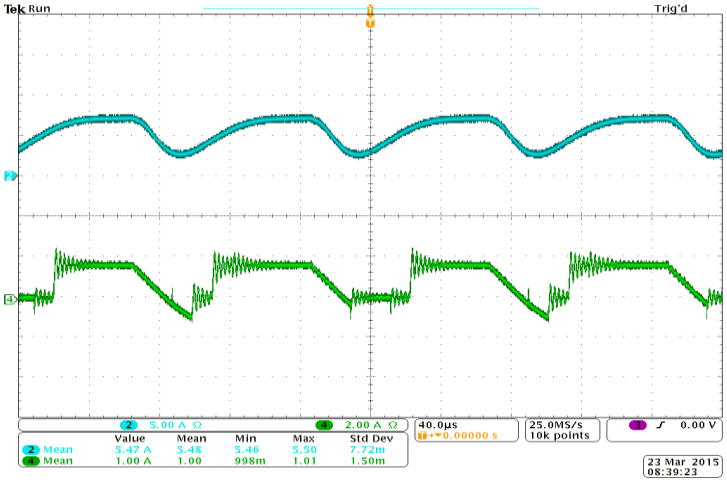


Fig. 11. Experimental output for ML-DAB input (top – blue) and output (bottom – green) dc currents respectively.

Figs. 10 and 11 show the simulated and experimental input-output currents at ML-DAB. MPPT control in ML-DAB adjusts the phase shift ϕ to obtain the maximum power available at the PV panels. The ML-DAB input voltage (V_s) is obtained from four PV panels in series. The PV parameters have been calculated based on the SunPower® E20-435W, 72.9V, 5.97A solar panel datasheet. Figs. 12 and 13 shows the effect of MPPT control and phase-shift modulation when PV current changes due to the change in solar irradiance for both Perturb and Observe (P&O) and Incremental Conductance algorithm.

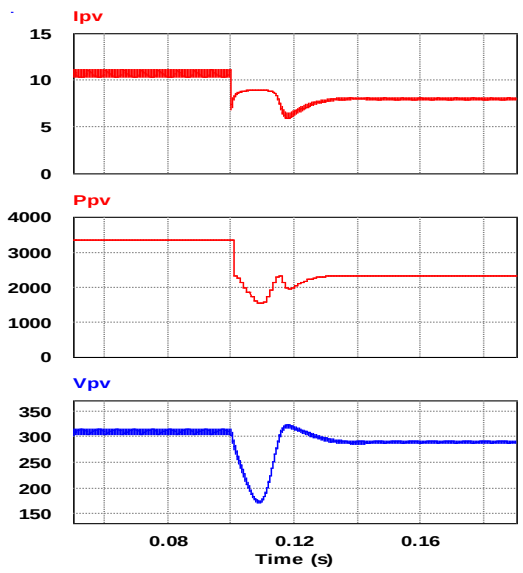


Fig. 12. MPPT, using P&O algorithm, controls the power flow when PV generation changes due to change in insolation from 1000 W/m^2 to 800 W/m^2 at t=0.1sec.

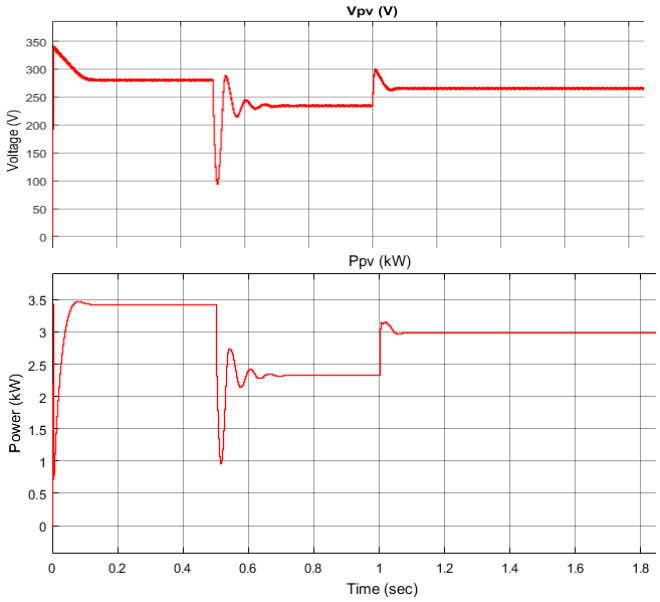


Fig. 13. MPPT, using Incremental Conductance algorithm, controls the power flow when PV generation changes due to change in insolation from 1000 W/m^2 to 800 W/m^2 to 900 W/ m^2 at t = 0.5 and 1sec.

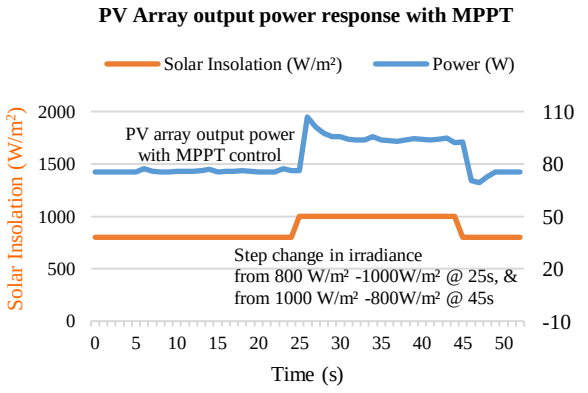


Fig. 14. The graph obtained from experimental data shows how the PV output power is controlled by the MPPT algorithm using MAGNA Power® XR200-10 PV source emulator and NI myRIO-1900®

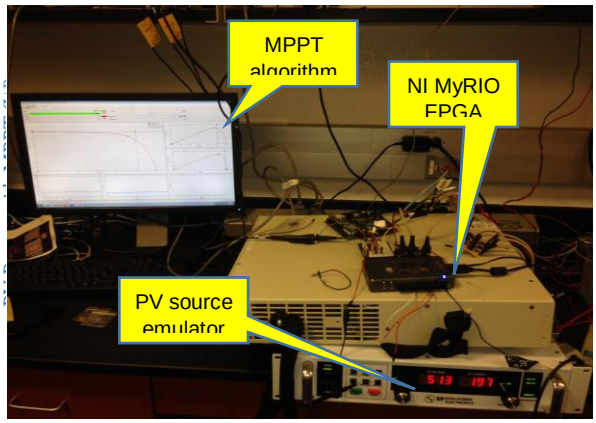


Fig. 15. Hardware setup for the MPPT control using MAGNA Power® XR200-10 PV source emulator and NI myRIO-1900® along with LabVIEW.

NI-myRIO® has been used to provide MPPT control signals for ML-DAB converter. The MPPT algorithm and the phase-shift PWM scheme is built, debugged and run with the help of LabVIEW development software. A voltage transducer (SCK-MU-1500V) has been used at the point where the PV module output is connected to the input of the DAB converter to measure the dc input voltage. A current transducer (CR5410-20) measures the PV generated current of the PV module on each operating point. Fig. 15 shows the experimental setup for MPPT. The MPPT algorithm provides the required phase-shift (ϕ) which gives the gate-pulse for the ML-DAB primary bridge switches. This

phase shift allows the required amount of power, generated from PV MPPT, to flow through the ML-DAB to the inverter and the load. Fig. 14 shows the MPPT results obtained from hardware using MAGNA Power® XR200-10 PV source emulator and NI myRIO-1900® FPGA (Fig. 7).

Task 2 (T-2): Ramp Forecasting Functionality Integration with Control Electronics

Solar forecasting has been extensively discussed at intra-hour and day-ahead time scales in the literature. At the intra-hour time scale, solar irradiance has been forecasted using a ground-based sky imager [14], where it is mentioned that major ramp events can be predicted using the sky-imager and forecasting algorithms. The use of solar forecasting in the control of PV inverters has not been discussed extensively in literature, particularly as it relates to controlling ramp slopes. In a utility-scale PV power plant with several inverters, it is possible to have a coordinated control of inverters to effectively use the PV under instances of curtailment, frequency regulation and high solar PV variability. Such advanced control in PV plants has been suggested in [15] to support grid stability and reliability. The proposed N-port converter can allow for integration of such advanced functionalities. Specifically, the DAB in every port can control the ramps by controlling the rate of rise/fall of the phase-shift ϕ. In the MPPT result shown in Fig. 14, the phase-shift ϕ is used to control the power flow and track the MPPT. By adding an additional control algorithm that receives the ramp forecasts and limits the rate of this control variable, it is possible to control ramp events. Further it is possible to operate each port under a reduced power reference instead of the MPP which is especially useful in curtailing power at the port level during frequency disturbances. The systems level integration and results of the Task T-2 are given in Task T-4 discussion.

Task 3 (T-3): Design for automatic and remote configurability

If 1 port goes OFF (N_{new}=11): $V_{P_{(N-1)}} = \frac{1667*12}{11} = 1820V$; $\frac{V_P}{2} = \frac{1820}{2} = 910V$; $\frac{910}{1200} = 75.83\%$

$$V_{s_{N-1}} = 292V\ (same\ as\ before\ with\ N\ ports);$$

$$\beta < \phi \leq \frac{\pi}{2};\ P_{o_{1port}} = \frac{V_p V_s}{n\omega L}\left(\phi - \frac{\phi^2}{\pi} - \frac{\alpha^2}{2\pi} - \frac{\beta^2}{2\pi}\right) \quad (18)$$

The total power (i.e. $N \times P_{o_{1port}}$) at the inverter output will be reduced to (($N-1$) $\times P_{o_{1port}}$)) due to 1-port failure. Actually, the current through the cascade bridges at the inverter output stage will be reduced to comply with this reduction in total power. Power from every single ML-DAB port should remain same as this power is obtained from PV MPPT control. $V_{s_{N-1}}$ (for 1-port) should also remain same as before since V_s ($= V_{PV}$) is controlled by the MPPT controller to achieve maximum available power from the PV panels. Only $V_{P_{N-1}}$will go high to maintain constant grid voltage. The turns ratio n

and leakage inductance L of the high frequency transformer will also remain the same as this is a parameter value obtained from hardware design. The switching frequency f_s is also kept constant (e.g. 5kHz).

According to the above constraint for $(N-1)$ redundancy, we have three controllable parameters (α, β, ϕ) left to compensate for the additional voltage $V_{P_{N-1}}$. Since ϕ is used to control the power flow using the MPPT circuit, we've only two more variables α & β to use. Numerically both α & β has equal effect in compensating V_P as shown in (18). But in terms of THD and soft-switching constraints, β is a better choice as a control variable to compensate the change in V_P. Table 3 shows the details of the calculations.

Table 3
For a 3.34kW Prototype (N=12) design with all 1200 IGBTs

For 12-port (N=12)	For 1 port (for N=**12**)	For 1 port (for N-1=**11**)
Power Rating of 1 single DAB module $\boldsymbol{P_o}$	3.34 kW	3.34 kW
$\boldsymbol{V_{dc(in)@DAB} = V_s}$	291.6 V	291.6 V
$\boldsymbol{V_{dc(out)@DAB} = V_P}$	1667 V	**1820 V**
DAB high frequency transformer's turns ratio, $\boldsymbol{n = \frac{V_P}{V_s}}$	5.716	5.716
$\boldsymbol{I_{DAB_{In}}}$	11.43 A	11.43 A
$\boldsymbol{I_{DAB_{out}}}$	2 A	1.835 A
Leakage Inductor for DAB high-frequency transformer, $\boldsymbol{L}$	0.5 mH	0.5 mH
2-level PV side bridge IGBT's $\boldsymbol{V_{CE}}$	292V (V_s is 25% of V_{CE})	292V (V_s is 25% of V_{CE})
3-level NPC bridge IGBT's $\boldsymbol{V_{CE}}$	1667V ($V_{P/2}$ is 70% of V_{CE})	1667V ($V_{P/2}$ is **76% of V_{CE}**)

Task 4 (T-4): Enhance Student Diversity in Solar Research and Education

This is the main education task for the Phase I of this project. Following paragraphs explain the accomplishments in the four sub-tasks associated with this T-4.

Sub-Task ST-4.1 Actively recruit students into the DISTINCT program

A total of 12 students have been supported as part of the research tasks on N-port converter in Phase I. In Phase II, 9 students have been added. A complete list of the students, degree program, graduation status and some key notes are given in detail later in Task 6.

Significant achievements in this sub-task are summarized below

1. Four undergraduate students were supported in this project, two of them have graduated.

2. One Undergraduate student transferred from a community college, completed BS degree in Electrical Engineering and moved on to the graduate program. This student continues to work on the DISTINCT project.
3. The DISTINCT research supported 3 PhD students.
4. Out of the 12 students, 5 are from traditionally underrepresented groups in Engineering and 1 student is a Navy veteran.
5. A sub-contract was signed with St.Philip's Community College (SPC) in Phase I and students have been recruited at SPC to participate in research activities and possibly transfer to UTSA undergraduate program as part of the 2+2 transfer agreement.

Sub-Task ST-4.2 Create a solar curriculum that gives students comprehensive knowledge on solar

A table of the courses in which solar content has been increased is shown in Table 4 along with notes on the exact content increase. A significant achievement is student enrollment in each of the courses. Course feedback results, from students averaged 4.6 out of 5.0. All the students who are supported by DISTINCT research, enrolled in these courses and these have been recommended for all students who are interested in pursuing a career in solar. Although these new content was introduced during years 2014 and 2015, the courses have continually implemented the modified content and will continue to do so. Table 4 also satisfies Task 6 technical metric of minimum of 5 courses with greater than 20% solar content in new curriculum.

Table 4
List of courses in DISTINCT solar curriculum

Dept.	Course title	Enroll-ment	Semester	Notes
EE	Power Electronics	46	Spring '14	Added 1 week discussion on PV inverters
ME	Sustainable Energy Systems	19	Spring '14 Spring '15	Added solar plant tours, 3 weeks on solar
ES	Renewable Energy	14	Spring '14	2 weeks of solar discussion
EE	Analysis of Power systems	35	Fall '14	Discussed high penetration of solar effects
EE	Power Converters for solar/wind	22	Spring '15	Half of the course discusses power electronics for solar
EE	Power Engineering Laboratory	11	Spring '15	Final project for the lab will be in PV inverters

EE – Electrical Engineering; ME – Mechanical Engineering; ES – Environmental Science

Sub-Task ST-4.3 Create a research experience program

Several outreach events have been conducted at UTSA to create an awareness of solar energy research and to encourage students to pursue a career in solar. These events include tech-talks by prominent experts in this field, campus career events and guest lectures in various departments and colleges. At the end of each of these events, a survey was given to document student feedback. The results of these surveys are

presented under ST-4.4. Table 5 lists the events and their details. Many of the students who are currently supported by DISTINCT for N-port converter research were previously participants in these events which helped them become a part of the research team. To expand participation of students in other programs funded by SunShot, UTSA is an affiliate university in the GRIDED project led by EPRI since Fall 2014. Students will now be able to participate in EPRI programs which will give them another research experience opportunity. In fact, two students are continually part of the student innovation board encouraged by GRIDED. PhD students also presented posters during the GEARED workshop. Finally, students were given opportunities to hone their soft skills through conference attendance and presentation to visitors from our network.

Table 5

List of outreach events to provide research opportunities in solar

Event name	Date	Notes
Texas Renewbale Energy Industry Associations Conference	Nov '13	Research and Networking experience for DISTINCT research students
Tech talk by Dr. Mooney, NREL	Mar '14	Technical talk on Solar PV opportunities and challenges
NREL job/internship information Session	Mar '14	An introduction to NREL job/internship opportunities for DISTINCT students
Guest lectures in 4 UTSA courses	Spring '14	Guest lectures by PI in various courses across Colleges to create awareness of solar and solar research at UTSA
Sandia National Lab Career Info Session	Sept '14	An introduction to Sandia job/internship opportunities for UTSA students
Guest lectures in Freshman Scientific Composition Class	Fall '14	Intro on solar generation to undeclared majors in Freshmen class

Sub-Task ST-4.4 Summative evaluation

Several student surveys have been collected at events, classes and guest lectures. A consistent message from the survey results is that the students are interested in pursuing a career in renewable and solar industry. Fig. 16 shows a survey result which had asked the students about their career choice. About 60% of the students, 120 out of 200 students, who attended these events are minorities, which is consistent with the diverse student body of UTSA.

Fig. 17 shows a graph of the student responses on the question of awareness of solar industry in United States before and after the guest lecture. These students were freshmen with most of them having undeclared majors. Figs. 16 and 17 are samples of the summative evaluation performed as part of this sub-task. These preliminary inputs from the students coupled with inputs from our research partners will serve as feedback to improve the solar program at UTSA and make it sustainable. Moreover the results of the jobs/internships students landed after graduation are given under Task -6.

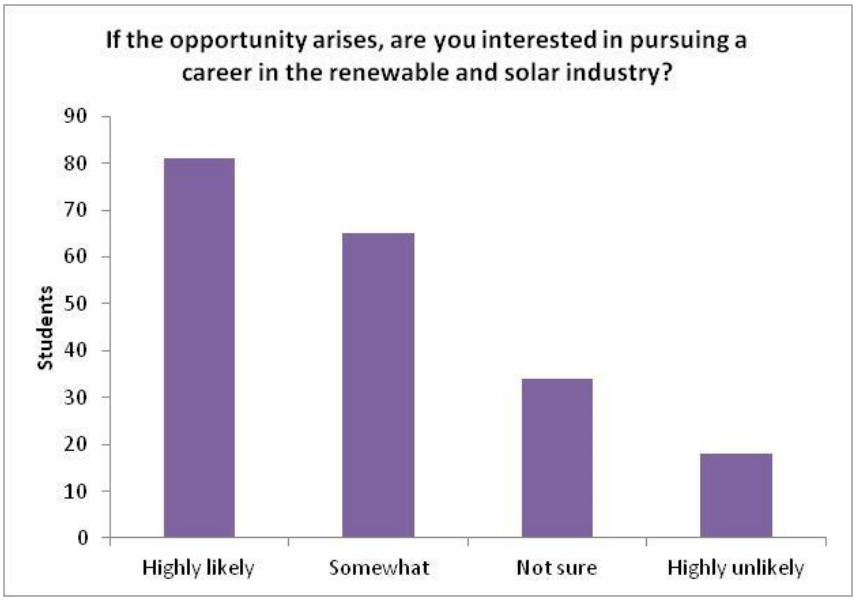


Fig. 16. Student Survey result on career choice

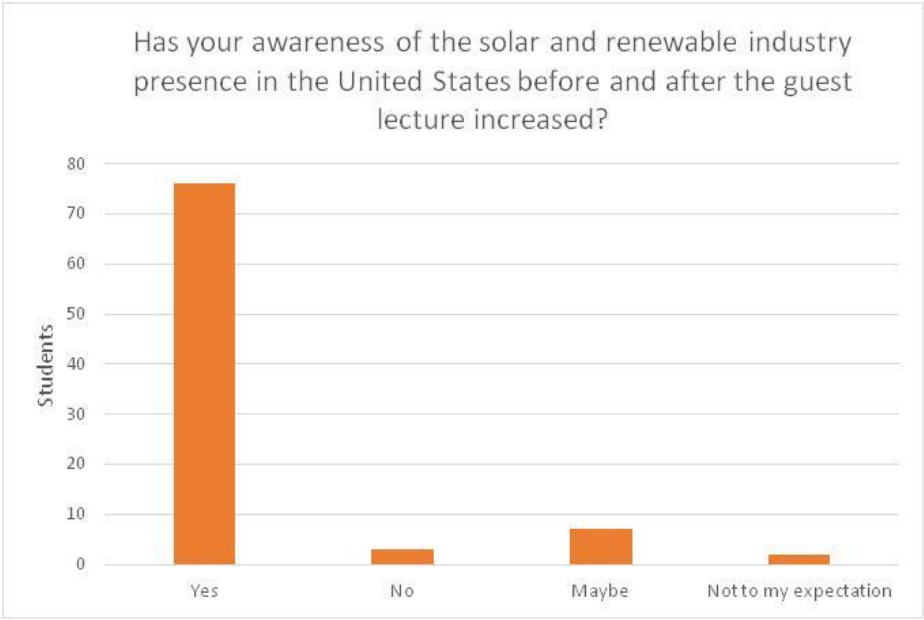


Fig. 17. Student Survey result on solar industry awareness after guest lecture

Task 5 (T-5): Implement Systems Level Integration and Testing

Capacitor voltage mismatch control at the ML-DAB

Ideally the ML-DAB should not experience any unbalance between V_{c1} & V_{c2}. Due to any load disturbance or converter non-ideality capacitor voltages become unbalanced i.e. $V_{c1} \neq V_{c2}$. During unbalanced condition a non-zero average neutral-point current i_{np} flows to/away from the neutral point "*o*" (Fig. 18).

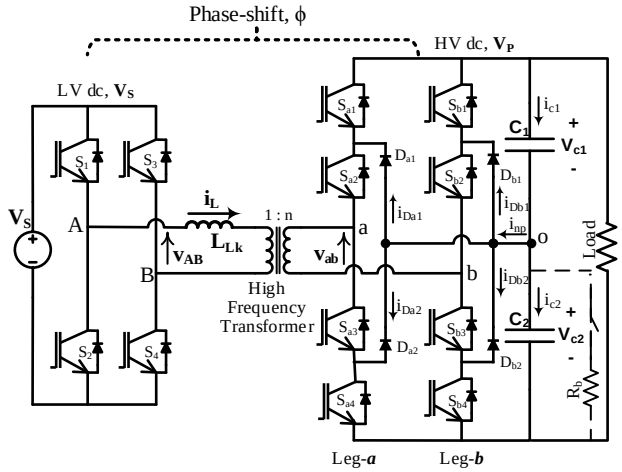


Fig. 18. Schematic of ML-DAB only showing NPC bridge currents.

From Fig. 18 we get the neutral point and clamping diode current relations as follows,

$$i_{np} = i_{c1} - i_2$$

$$i_{np} = i_{D_{a1}} - i_{D_{a2}} + i_{D_{b1}} - i_{D_{b2}} \tag{18}$$

In order to control the switching cycle average of i_{np}, the diode currents ($D_{a1} to\ D_{b2}$) can be controlled by changing the α & β , which modulates corresponding NPC switch gate pulses accordingly. For example, if during any unbalance $i_{c1} > i_{c2}$ then switching-cycle average of i_{c1} ($\overline{i_{c1}}$) should be reduced and $\overline{i_{c2}}$ should be increased. In order to implement this control, we need to delay $S_{a1}\& S_{b1}$ and start earlier $S_{a2}\& S_{b2}$ by an amount of $\Delta\theta$ as shown in Figs. 19 to 21 as the control output "*Theta_Control*". A similar capacitor voltage balancing control algorithm has been described in [16]. As shown in Fig. 19, an intentional imbalance between $V_{c1}\text{and } V_{c2}$ has been created bypassing a part of the i_{c2} through R_b (Fig. 19) at t = 0.02.

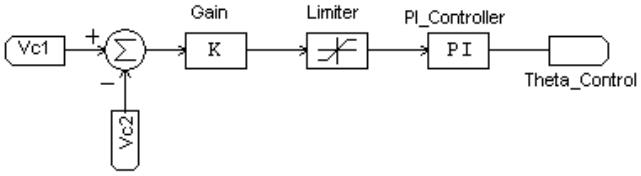


Fig. 19. Block diagram showing the capacitor voltage imbalance control.

Power Mismatch Control

Voltage imbalance and power mismatch among the different ports are control challenges for a multi-port cascaded converter topology. Various control strategies have been described in literature in order to regulate such unbalance for cascaded inverters in solid state transformer (SST) applications [17-18]. The overall control structure has been designed, in this paper, based on the input PV power mismatch among the various ports in all three phases. Maximum power point current I_{mpp} and corresponding voltage V_{mpp} can be obtained from the MPPT control. The product of V_{mpp} and I_{mpp} is

the output power P_{PV} from the solar PV panels which is fed into the dc-dc ML-DAB converter. Assuming η_{dab} as the efficiency for ML-DAB dc-dc stage conversion, we get,

$$P_{dab_{ij}} = \eta_{dab}.P_{PV_{ij}} \text{ ; where } i = 1,2,\dots,N \text{ ports and } j = a,b,c \text{ three phases} \quad (19)$$

For *N* numbers of ports per phase, the total power to be processed in three phases should be,

$$\sum P_{dab_{ij}} = P_{dab_{1a}} + P_{dab_{2a}} + \cdots + P_{dab_{Na}} + P_{dab_{1b}} + \cdots + P_{dab_{Nb}} + P_{dab_{1c}} + \cdots + P_{dab_{Nc}}$$
$$= \eta_{dab} * \left(P_{PV_{1a}} + P_{PV_{2a}} + \cdots + P_{PV_{Na}} + P_{PV_{2b}} + \cdots + P_{PV_{Nb}} + P_{PV_{1c}} + \cdots + P_{PV_{Nc}}\right) \quad (20)$$

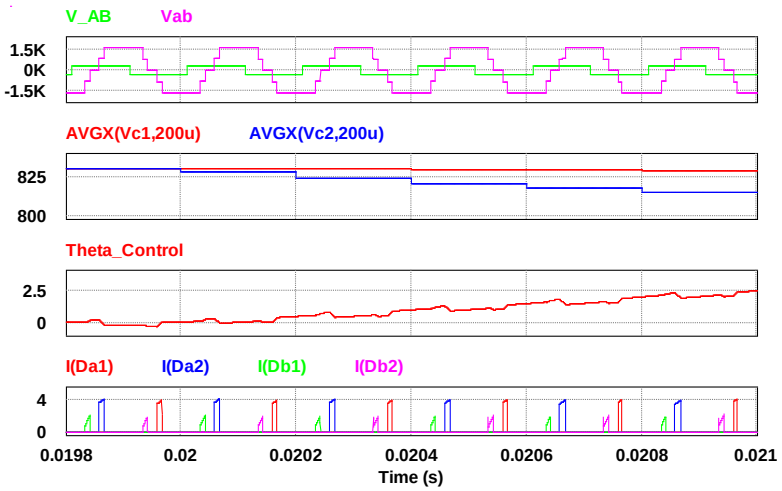


Fig. 20. After t=0.02s, $V_{c1} \neq V_{c2}$ and the control signal "*Theta_Control*"starts compensating the imbalance by modulating diode currents ON-time duration ($I_{D_{a1}} to\ I_{D_{b2}}$).

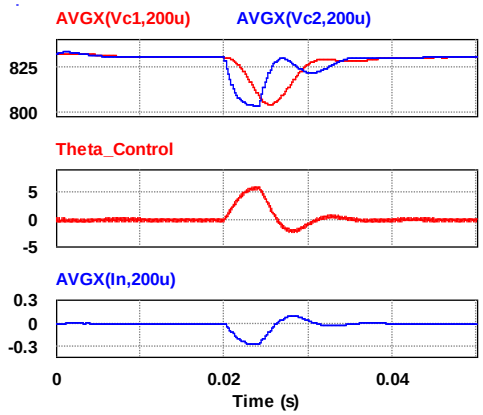


Fig. 21. Capacitor voltage balancing using a PI controller ($I_n = i_{np}$).

The dc-dc ML-DAB power equation for one port is as follows. Here α, β are assumed to be constant and ϕ varies according to MPPT control (Fig. 3).

$$P_{dab_{ij}} = \frac{V^*_{dc_{ij}} . V_{PV_{ij}}}{n\omega L} . \left(\phi_{ij} - \frac{\phi^2_{ij}}{\pi} - \frac{\alpha^2}{2\pi} - \frac{\beta^2}{2\pi} \right)$$

$$= \eta V_{PV_{ij}} I_{PV_{ij}} = V^*_{dc_{ij}} I_{dab_{ij}} \quad (21)$$

ML-DAB output current $\left(I_{dab_{ij}} \right)$ can be obtained by using the variables such as ϕ, α, β, *n, w, L* and V_{PV} as follows,

$$I_{dab_{ij}} = \frac{V_{PV_{ij}}}{n\omega L} . \left(\phi_{ij} - \frac{\phi^2_{ij}}{\pi} - \frac{\alpha^2}{2\pi} - \frac{\beta^2}{2\pi} \right) \quad (22)$$

As there will be difference in power from the PV panels connected to different ports, it is necessary to find the ratio (r_{ij}) of the individual port's PV power to the total PV power.

$$r_{ij} = \frac{P_{dab_{ij}}}{\sum_{\substack{i=1,..N; \\ j=a,b,c}} P_{dab_{ij}}} \quad (23)$$

The respective ratio of the individual ports is multiplied by *d*-axis grid current i^*_d and *d*-axis grid voltage v^*_d, obtained from $abc - dq$ transformation, to calculate the inverter input power for the respective port of the *N*-port converter (Figs. 22, 23).

$$P_{g_{ij}} = r_{ij} . V^*_d . i^*_d \quad (24)$$

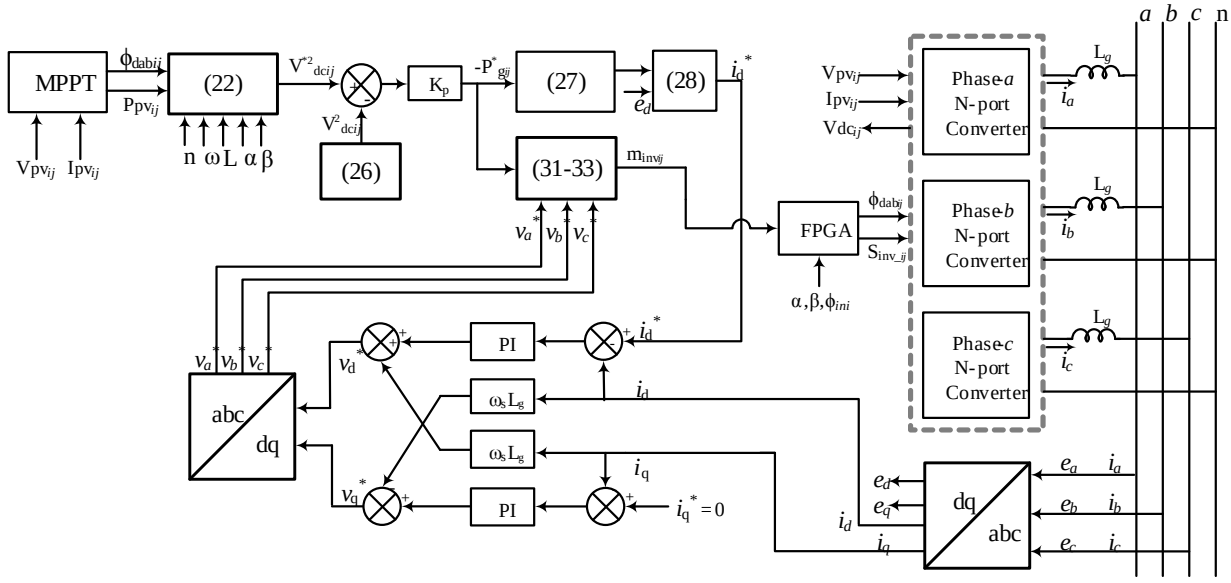


Fig. 22. Block diagram showing the control of the *N*-port three-phase grid-connected PV converter

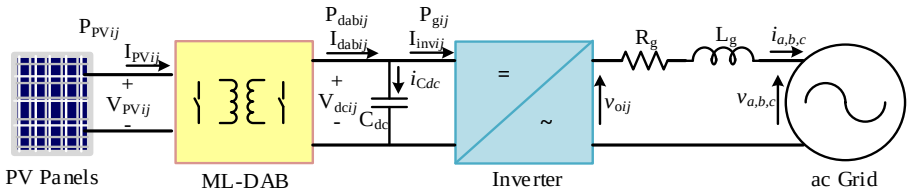


Fig. 23. Block diagram showing key parameters and power flow from PV panels to the grid

An approach to control the dc-link voltage has been described in [19] for a doubly fed induction generator (DFIG). This can be modified in the proposed *N*-port converter for balancing the power mismatch among different ports. The energy stored in a small time period dt in the dc-link capacitor C_{dc} can be expressed as the power difference between $P_{dab_{ij}}$ and $P_{g_{ij}}$ at any instant (Fig.23). The reference DC bus voltage ($V_{dc_{ij}}$) can be obtained from (26).

$$\frac{1}{2}C_{dc}\frac{d}{dt}\left(V_{dc_{ij}}^2\right) = P_{dab_{ij}} - P_{g_{ij}} \tag{25}$$

Considering $v_{dc_{ij}}^2$ as the control variable and assuming $P_{dab_{ij}}$ as constant (i.e. perturbation in $P_{dab_{ij}}$ to be zero), the small signal model can be derived from (26), as shown in (27).

$$\frac{V_{dc_{ij}}^2(s)}{-P_{g_{ij}}(s)} = 2\frac{1}{sC_{dc}} \tag{26}$$

The controller parameters can be found from (27). The square of measured dc-link voltage $v_{dc_{ij}}^2$ is compared with the reference $V_{dc_{ij}}^{*2}$ obtained from (22) to regulate the dc-link voltage. This yields the active power reference $P_{g_{ij}}^*$ (Fig. 12). This power gives the reference for i_d^* as shown in (28), where e_d is the d-axis component of grid voltage and $\sum P_{g_{ij}}^*$ is calculated from (29)-(30).

$$i_d^* = -\frac{\sum_{\substack{i=1,..,N \\ j=a,b,c}} P_{g_{ij}}^*}{e_d} \tag{27}$$

$$\left.\begin{aligned} \sum_{i=1,\dots,N} P_{g_{ia}}^* &= P_{g_{1a}}^* + P_{g_{2a}}^* + \cdots + P_{g_{Na}}^* \\ \sum_{i=1,\dots,N} P_{g_{ib}}^* &= P_{g_{1b}}^* + P_{g_{2b}}^* + \cdots + P_{g_{Nb}}^* \\ \sum_{i=1,\dots,N} P_{g_{ic}}^* &= P_{g_{1c}}^* + P_{g_{2c}}^* + \cdots + P_{g_{Nc}}^* \end{aligned}\right\} \tag{28}$$

$$\sum_{\substack{i=1,..,N \\ j=a,b,c}} P^*_{g_{ij}} = \sum_{i=1,...,N} P^*_{g_{ia}} + \sum_{i=1,...,N} P^*_{g_{ib}} + \sum_{i=1,...,N} P^*_{g_{ic}} \tag{29}$$

The ac output voltage from every single inverter port can be obtained by multiplying the reference grid phase voltage (e.g. v_a^*) with the respective negative power reference ($-P^*_{g_{ia}}$) ratio as shown in (31).

$$v_{o_{ia}} = v_a^* . \frac{P^*_{g_{ia}}}{\sum P^*_{g_{ia}}} \tag{30}$$

Similarly, the ac output from all other ports can be obtained for phases b and c as shown below,

$$v_{o_{ib}} = v_b^* . \frac{P^*_{g_{ib}}}{\sum P^*_{g_{ib}}} \tag{31}$$

$$v_{o_{ic}} = v_c^* . \frac{P^*_{g_{ic}}}{\sum P^*_{g_{ic}}} \tag{32}$$

The sum of the output voltages from each of *N*-port inverters appears across the respective phase of the grid (i.e.v_{an}, v_{bn}, v_{cn})

$$\left.\begin{aligned} v_{an} &= \sum_{i=1,..,N} v_{o_{ia}} = v_{o_{1a}} + v_{o_{2a}} + \cdots + v_{o_{Na}} \\ v_{bn} &= \sum_{i=1,..,N} v_{o_{ib}} = v_{o_{1b}} + v_{o_{2b}} + \cdots + v_{o_{Nb}} \\ v_{cn} &= \sum_{i=1,..,N} v_{o_{ic}} = v_{o_{1c}} + v_{o_{2c}} + \cdots + v_{o_{Nc}} \end{aligned}\right\} \tag{33}$$

The current flowing towards the grid (i_a, i_b, i_c) can be found using (35) to (37), where e_a, e_b are respective grid voltages and R_g, L_g are the lumped resistance and inductance respectively at the grid interface.

$$v_{an} = i_a . R_g \ + \ L_g . \frac{di_a}{dt} + \ e_a \tag{34}$$

$$v_{bn} = i_b . R_g \ + \ L_g . \frac{di_b}{dt} + \ e_b \tag{35}$$

Assuming balanced grid currents, the sum grid currents i_a, i_b, i_c is zero.

$$i_c = \ -(i_a + i_b) \tag{36}$$

Using $abc - dq$ transformation, grid currents i_a, i_b, i_c are transformed into i_d and i_q (Fig. 12). Current i_d is compared with the corresponding reference current i_d^*, and i_q is assumed to be zero. The output of the d-phase PI controller is summed up with the product of ω_s , L_g and i_q current and the resultant is the d-phase reference voltage v_d^*. v_q^* can be obtained similarly as shown in Fig. 12. After the $dq - abc$ transformation reference voltages v_a^*, v_b^*, v_c^* can be obtained. These reference voltages are used as the modulating signal for the level-shifted PWM to generate the corresponding gate pulses ($S_{inv_{ij}}$) for the IGBTs used in the NPC inverters. The phase-shift control parameter

($\phi_{dab_{ij}}$) has been derived independently from the MPPT control, which generates the gate pulses for the ML-DAB primary bridge switches ($S_{1_{ij}}$ to $S_{4_{ij}}$) corresponding to the required phase-shift ($\phi_{dab_{ij}}$) between two bridges.

(N-1) Redundancy

The following paragraphs explain the work done on automatic reconfigurability - fault-tolerant control for the N-port converter.

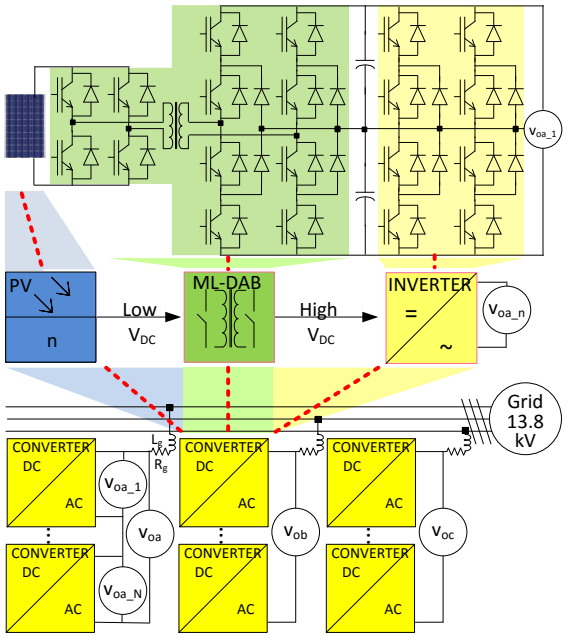


Fig. 24 N-Port Converter to illustrate automatic reconfigurability control [P-6,P-7]

A multi-port converter consists of several stages as shown in Fig. 24. An array of PV panels feed power to a multi-level dual active bridge (ML-DAB). This stage performs a high-power transformation utilizing a high frequency AC-AC step-up transformer. Two capacitors handle the high voltage charge by the ML-DAB and share them with a neutral point clamped (NPC) inverter. The NPC inverter synthesizes a near sinusoidal voltage, which is controlled by a new control algorithm. Cascading and synchronizing the ports create an output to the voltage grid. Each port contains a high number of semiconductor devices as compared to two level DAB and H-Bridge inverter configurations. These devices can fail and are limited by their individual lifetimes. Reliability of converters has been analyzed before, illustrating a mean time between failures at around 50,000 hours of operation. The NPC inverter, converting DC into AC, utilizes carrier based sine wave pulse width modulation (SPWM). Triangular carrier waveforms are compared to sinusoidal waveforms, generating PWM signals for each switch. The triangular waveform is phase shifted between the cascaded ports, establishing a level shifted multi-carrier modulation. The number of ports determines the shift angle (180 / n-ports) and the created amount of levels (4n+1). Sinusoidal waveforms are shifted by 120 degrees for the phase shifted multi-carrier modulation.

The waveforms depend on the input of a phase-locked loop, an abc-dq controller, and a separate voltage and current control loop. In order to keep the converter control loops stable, the feasibility of the system has to be evaluated. Fault resolution occurs by the manipulation of the SPWM and is described in following sections.

Voltage and Current Analysis

As a utility size converter feeding a line-to-line 13.8kV transmission voltage system, economic requirements dictate the use of commercially available electronic components. Cost-competitive medium voltage IGBT's need to be incorporated. The above described configuration utilizes two shared capacitors at the NPC inverter input side, reducing the DC voltage seen across the capacitors and the semiconductor devices in half of the total DC output voltage. Additionally, the power output has to be considered. A minimum size of 50kW is delivered by 3 phases, each producing 16.7kW and evenly distributed across n-ports of the multi-port configuration. Incorporating the output of solar panels and the step up transformation of the ML-DAB the following numerical requirements are needed to achieve the desired power levels. Sun Power Panels SPR-435 are selected, rated at V_{mpp}=72.9VDC, I_{mpp}=5.97A, and P_{nom}=435W. The ML-DAB is evaluated an assumed transformer ratio of 5.716. Ultimately, the desired outcome is achieved, having four panels in series and 12 ports per phase. Therefore, the required one phase line-to-neutral cascaded NPC inverter AC output should be

$$V_{peak,L\text{-}N1\varphi,1\ port} = \frac{13.8\text{kV}*\sqrt{2}}{\sqrt{3}*\text{n}-\text{ports}} = \frac{11.27\text{kV}_{ac}}{12} = 939\ \text{Vac}.$$

This results in a needed DC input voltage of

$$V_{DC,1port} = \frac{V_{peak,L-N1\varphi,1port}*2}{\sqrt{3}} = \frac{939V_{ac}*2}{\sqrt{3}} = 1084\ V_{DC}.$$

The ML-DAB output with the SPR-435 under ideal conditions, defining also the NPC inverter input, equals

$V_{DC,ML\text{-}DAB(out)}$ = 4 $SPR\text{-}435_{in\ series}$ * V_{mpp} * ML-DAB $_{Transformer\ Ratio}$ = 4 * 72.9V_{DC} * 5.716 = 1.67kV_{DC}.

This inverter input, divided in half due to the system design, allows for the use of cost-competitive IGBT's rated smaller than 1200V. The current for each port with the given transformer ratio is 1.04A (I_{mpp} / 5.716), creating a power output of 1.74kW ($V_{DC,ML\text{-}DAB(out)}$*1.04A). Ignoring losses in the NPC inverter, this power output exceeds the required output of

$$P_{1port} = \frac{\text{Power plant requirement}}{3*\text{n}-\text{ports}} = \frac{50\text{kW}}{3*12} = 1.39\text{kW}.$$

Creating a fault in one port, the following voltage, current and power calculations can be done:

$V_{DC,1port} = \frac{13.8kV * \sqrt{2} * 2}{\sqrt{3} * n-ports * \sqrt{3}} = \frac{13.8kV * \sqrt{2} * 2}{3 * 11}$ = 1183 V_{DC}; $P_{1port} = \frac{50kW}{3 * 11}$ = 1.52kW; $I_{DAB,Out} = I_{Inv,In} = \frac{1.52kW}{5.716 * 292V}$ = 0.90A.

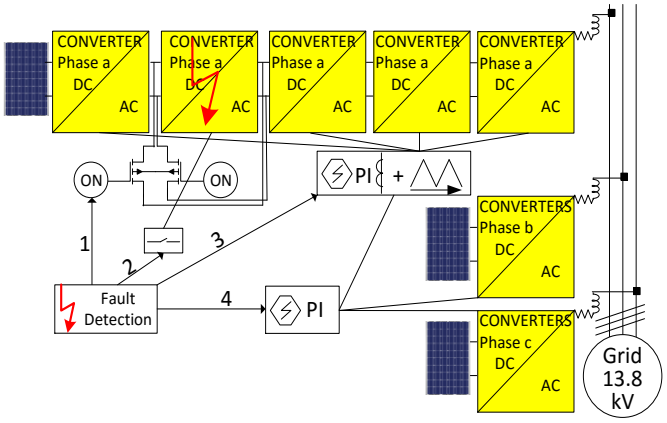


Fig. 25. Fault Process

In comparison to the required power plant numbers, this configuration incorporates a buffer for failures. Continuing the calculation with subsequent faults demonstrate that a maximum of two ports per phase can fail while still achieving the required power output of 50kW. A control logic is implemented to guarantee uninterrupted generation of electricity.

Fault Detection, Identification and Resolution

A continuous operation can be ensured by applying a fault detection and resolution control to the system. Faulty semiconductor parts can be identified by the circuit driver IC. IGBT's, diodes, DC and AC output voltages are constantly monitored. When a fault is detected, or voltages drop below a predefined state, a signal is send to the control logic, starting a resolution process. The resolution process involves several steps as depicted on Fig. 26. Bypasses for each module consist of high performance IGBT switches. The control sends a high signal to the switch, enabling an in series circuit around the faulty module. The carrier wave is set to zero and the IGBT's of the ML-DAB H-Bridge are turned off, disconnecting the PV from the converter. The levels for the multi carrier modulation have to be shifted according the converter sequence. This will smoothen the sinusoidal output waveform and therefore improve THD. The three phase voltages are unequal and require a balance. This is achieved by a PI control algorithm comparing the average cascaded output voltages, and modifying the modulation index (*m*) of each single inverter stage. Principally, *m* is the main control for the multi-port converter, but can only be varied to a limited extend defined by the number of cascaded ports.

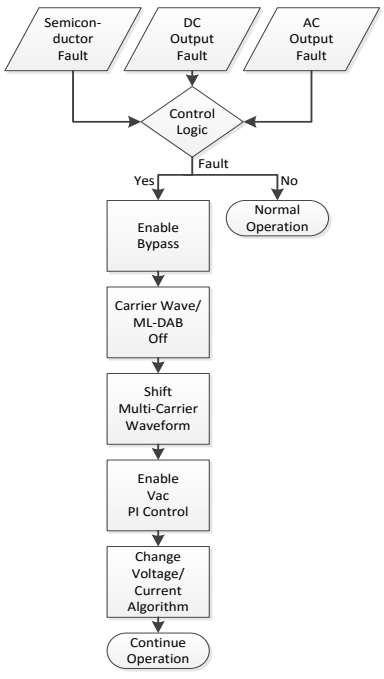


Fig. 26. Fault Resolution Process

The characteristic of using SPWM inhibits a large reduction of m, since losses of voltage levels will occur creating an increase in THD. An overmodulation (*m*>1.0) will result in a distortion of the current sinusoidal output. A basic rating of *m*=0.9 is selected, allowing for a modulation range in both directions. The optimum efficiency is achieved setting *m* close to 1; however, this

will prevent a voltage and current balancing algorithm among the multi-ports for each phase, which performs the adjustments for the required compensation of a missing module.

Simulation Results

A multi-port converter is incorporated in MATLAB/SIMULINK to simulate a single modular failure. The ML-DAB is simulated by a DC voltage source feeding two shared capacitors. Calculations are done for 12 ports per phase and a 13.8kV transmission voltage. Due to the high part count causing simulation constraints, only 5 ports are simulated for one phase and two for the other two, setting the grid voltage to 1.88kV$_{ac}$. All ports are concurrently simulated; resistors and inductors are embedded creating a grid reactance, while solar irradiance is set at average intensity of 800 W/m^2. The capacitor voltage is

$$V_{DC,Capacitor} = \frac{V_{DC,ML-DAB(out)} * \text{Solar Irradiance}}{2\ \text{Capacitors}} = \frac{1.67\ \text{kV} * 800}{2 * 1000} = 667\ V_{DC,2ports} = \frac{667\ V_{DC,2ports} * 2}{5} = 267\ V_{DC,5ports}.$$

At 80 msec. the second port of phase “a” is faulted, reducing the output voltage, disturbing the modulation sequence and the output current. The control logic is initiated, shown on Fig. 26, enabling a bypass, turning the triangular carrier wave off, shifting the carrier wave modulation sequence to 4 ports, enabling the V_{ac} PI controller, and changing the balancing algorithm. Fig. 27 illustrates the output currents and voltages. The grid voltage remains undisturbed during the fault. The fault is recovered after about 150 msec. All PI controllers stabilize the current and voltage imbalances, constituting a robust system.

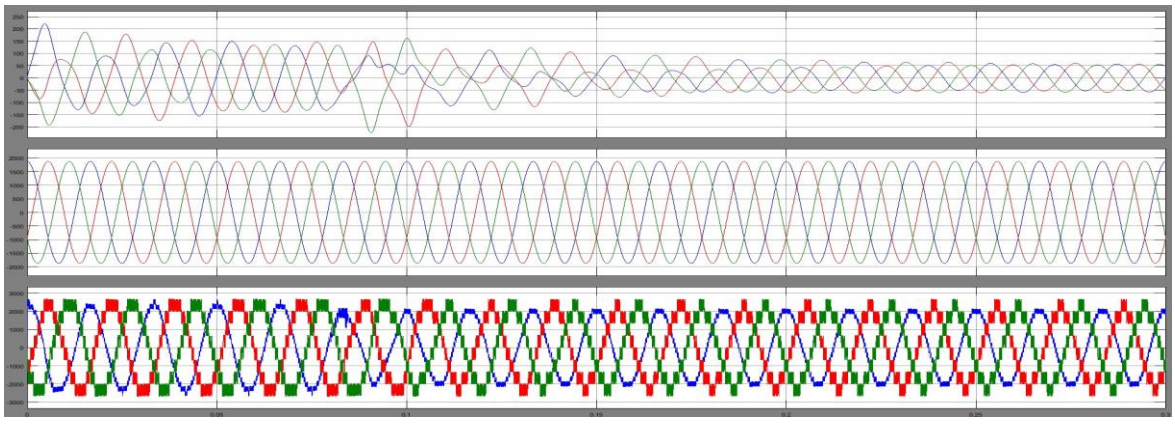


Fig. 27. (a) 3φ Current (50A/div.), (b) 3φ Grid Voltage (500V/div.), (c) 3φ Output Voltage (1000V/div.), horizontal: 50msec/div

The peak output voltage for each inverter phase varies due to a PI control using averaged levels, but stays higher than the grid voltage. The unfiltered waveforms show 21 levels for the 5 port cascade and 9 for the 2 port. The failure causes a reduction from 21 to 17 levels confirming the possible loss of a converter without losing voltage levels. THD remains reduced due to the near sinusoidal output power. Due to the need of

balancing of all converters, the output current will be reduced compared to a non-faulty system, reducing the output power. Fig. 28 depicts a working abc-dq control with the disturbance. The leading angle shows a continuous current feed into the grid.

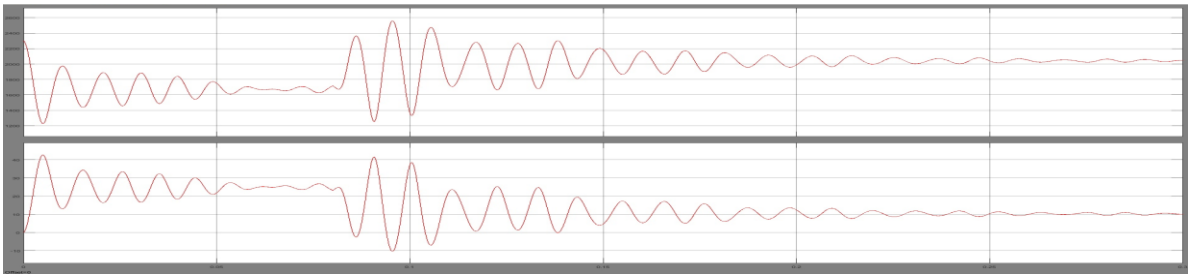


Fig. 28. abc-dq PI-Control Output: (a) v_{di} (200V/div.) and (b) v_{qi} (10V/div.), horizontal: 50msec/div.

Technical Metrics Discussions

Metric #1 Cost

*Since this section contains $ numbers we obtained from A Solar Company in partnership with St. Philip's college, we request this section alone be confidential marked with *[…]*.*

***[**Based on the proposed design of the N-port converter and a 3.34 kW hardware prototype, an effort has been made with the help of St. Philip's College, Alamo Community College District, to estimate the proposed converter cost and compare it with a commercially available utility-scale overall PV system. In order to prepare a cost comparison with a conventional 1 MW PV system, authors got the support from faculty and students at the St. Philip's college which gives an Associate degree in power generation. Due to more number of ports per phase the proposed *N*-port converter is likely to be costlier than the central inverter considering power electronics cost alone. However, the conventional transformer cost is not there in the proposed converter since it eliminates the line frequency transformer with smaller high frequency transformers integrated in dc-dc stage. Still, the converter alone is not cheaper than the combination of central inverter and transformer. Most of the cost in the proposed converter comes from the HF transformer and electronics. But, the overall gain can be achieved from balance of systems (BOS) cost.

Due to internal higher voltages the corresponding current carried by each port and each interconnection box gets much lower in comparison to the central inverters. This lower current saves money by saving a good amount of copper cable, conduit and switchgear. A comparative summary, with some key components in a 1 MW PV system, has been shown in Table 6. The comparison has been made based on the standard PV system with central inverter solution. It appears that the proposed *N*-port converter can be $0.13/watt cheaper than a conventional central inverter in the 1 MW scale. All the item costs have been estimated based on present market price which may vary as per design, place, manufacturer and other market conditions.

TABLE 6
COST COMPARISON OF THE PROPOSED N-PORT CONVERTER WITH A CENTRAL INVERTER BASED 1 MW PV SYSTEM

	Central Inverter	Proposed N-port Inverter
Inverters	$ 0.0526	$ 0.2000
Transformers	$ 0.1070	Included in Inverter Cost
Copper Cable	$ 0.0320	$ 0.0252
PVC conduit	$ 0.0034	$ 0.0085
AC switchgear	$ 0.0835	$ 0.0337
Combiners	$ 0.0140	$ 0.0060
Concrete	$ 0.0070	$ 0.0059
key items above:	*$ 0.2995*	*$ 0.2000*
Assuming rest of the project cost is same for both Central and N-port Modular PV Inverter		
Overall $/watt	$ 1.85	$ 1.72

]*

Metric #2 Efficiency

Efficiency for the centralized inverter is conventionally measured as the ratio of output power vs the input power. The transformer efficiency is not taken into account in considering the overall efficiency of power conversion. Since the DISTINCT project integrates the transformer in each port, the target metric is the product of the efficiencies of the state-of-the-art inverter and conventional transformer which is 97% *99% = 96%. In addition, the metric determination also takes into account the progress made in the literature on solid-state transformer.

In the DISTINCT N-port power converter configuration, all ports are in parallel with each other, with each port delivering maximum power. Hence it is sufficient to calculate and verify efficiency for one port. Extensive tests have been conducted on one port. Due to limitations in hardware, simulation results have been used to supplement in a way that the initial hardware and simulation results match well (see Fig. 29) and the simulation results are then scaled up. Fig. 29 shows the plot of efficiency vs the input voltage at the PV side. Due to limitations in handling high voltage >1kV at the ML-DAB stage in a laboratory environment, the hardware results were produced power greater than 1kW. The scale up simulation results at 3.5kW per port is 94%. The efficiency is still lower than the target of 96%. We used an amorphous metglass core which contributed to increase core and copper losses. It is possible to optimize the design of the transformer with ferrite or nanocrystalline cores to improve the efficiency. Also, about 3% loss in efficiency is due to the front-end converter conduction losses. With new advances in SiC Mosfets it is possible to cut these losses by half but it would impact the cost. A trade-off between efficiency and costs based on magnetic cores and semiconductor devices is needed in the final design to meet or even exceed current efficiency.

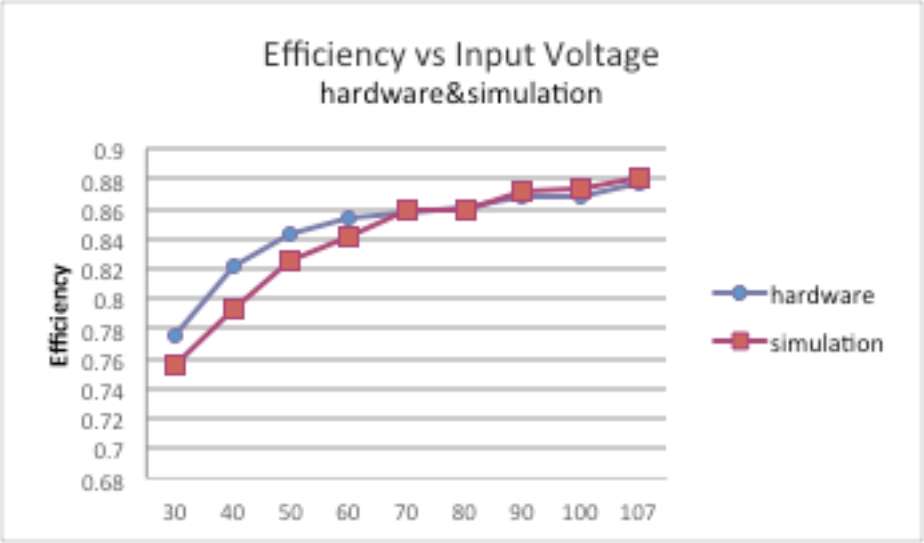


Fig. 29 Simulation and Experiment results on Efficiency

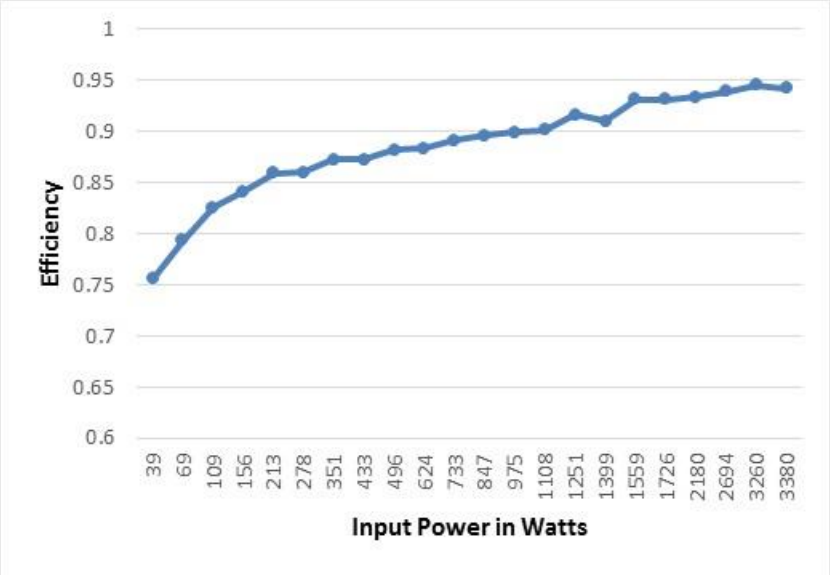


Fig. 30 Efficiency vs input power for the scaled-up simulation model

Metric #3 Service Life

The N-port converter system is modular. It has been proved in Task 6 that the converter can continue to function even with one port failure. This means that there is zero downtime when one port fails and the converter continues to deliver power with the remaining N-1 ports. Hence for the service person, it is easy to replace each port with no impact on overall system function. The cost of each port is also much lesser compared to a central inverter replacement cost. Combined with modularity, fault-tolerance and automatic reconfigurability, the serviceability of the N-port converter system can easily extend beyond 25 years.

Metric #4 Size and Weight

To determine the footprint occupied by a N-port converter, a 500kW sample design is used and compared with a 500kW conventional central inverter. Figure 31 shows a one-line diagram with 9 ports per phase, corresponding interconnection boxes and switchgear. The current ratings are also shown. It was observed that the proposed N-port converter has more than 40% lower footprint in comparison to the combination of central inverter and line frequency transformer especially. The parts used in arriving at the footprint are listed in Table 8.

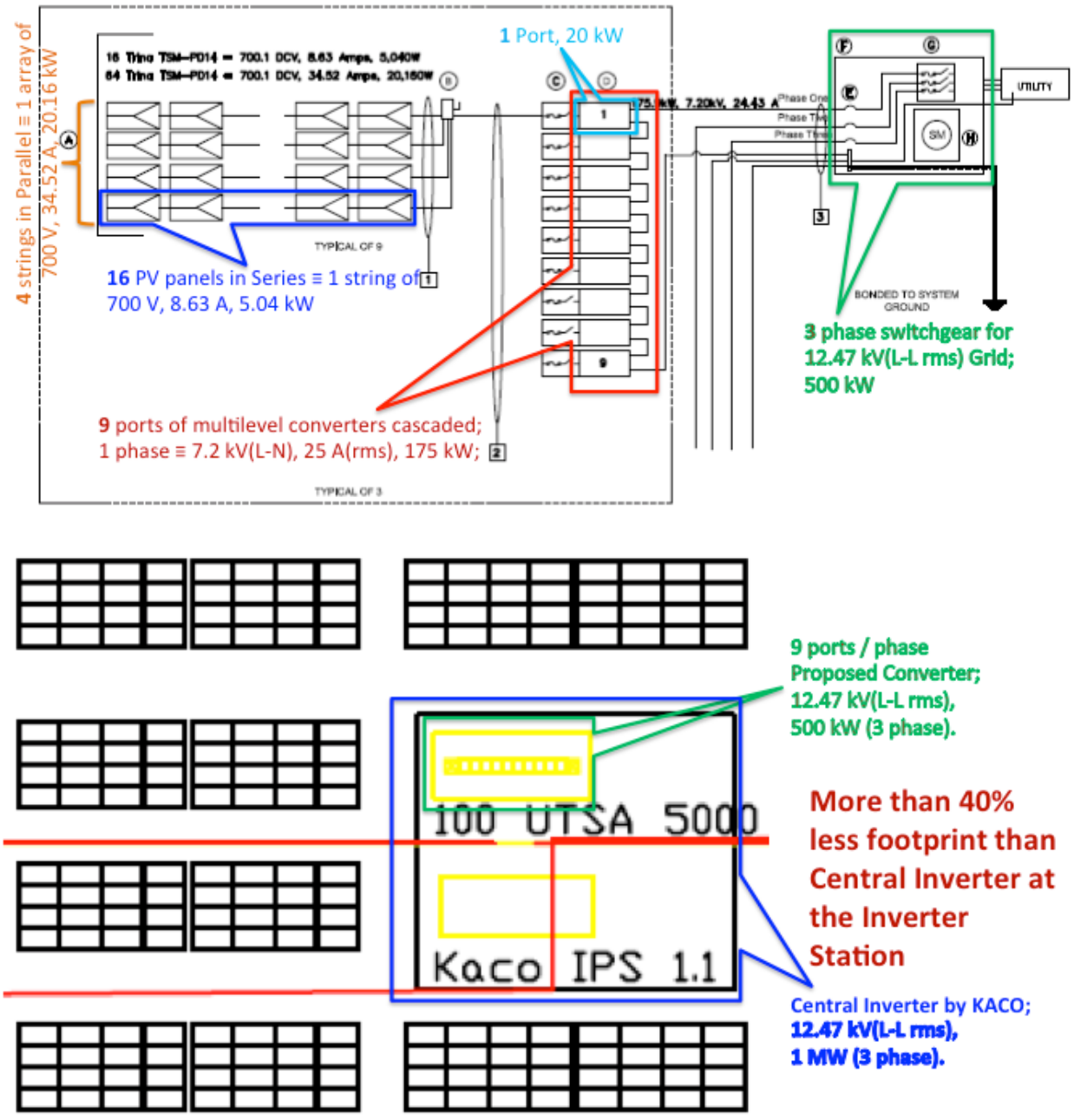


Fig. 31 One-Line diagram of 500kW N-port Converter design vs conventional central inverter design

Metric #5 Control

Port power imbalance control, capacitor voltage imbalance control and fault-tolerant control have been explained in detail under Task 6. DISTINCT students have published peer-reviewed papers on these control methods listed under publications [P-6], [P-7], [P-8] and [P-9].

Metric #6 Power Rating

Due to constraints in the laboratory in terms of handling high voltage >1kV, the power rating was limited to 1kW/port. However, all simulation results are presented at high power with the models used in simulation matching with the low power hardware results.

Metric #7 Grid Performance

Grid performance in terms of THD is discussed under Task 1. Each port of the cascaded NPC (CNPC) inverter (Fig. 2) is switched to provide a leg-to-leg 5-level ac output (i.e. $V_P, \frac{V_P}{2}, 0, -\frac{V_P}{2}, -V_P$). *N* number of CNPC inverters produce outputs that are phase-shifted from each other by an angle $\frac{180^0}{N}$ to yield a (4N+1) level ac output. In CHB modulation, the number of levels for *N* cascaded H-bridges is (2*N*+1). So, CNPC provides lower THD than CHB because of having more levels in the cascaded output voltage waveform. Fig. 5 shows how the THD is improved with the increase in number of ports (*N*) and how the CNPC provides better THD than CHB for any number of cascaded ports. In comparison to cascaded H-bridge (CHB) inverter stage, the CNPC bridge uses double the number of switches with lower voltage rating. It is also advantageous in terms of low $\frac{dv}{dt}$ and less harmonic distortion inherent to the multilevel topology. The THD under CNPC is 2.55% meeting the target metric in Table 1.

Task 6 (T-6): Evaluate Effectiveness of the Education Plan

One of the target metrics under this tasks is to have a minimum of 8 student jobs/internships. For monitoring and tracking, students who are “directly” and “indirectly” benefitting from the DOE DISTANCE grant are included such as:

1. Graduate and Undergraduate Research Assistants who work on N-port Converter Research
2. Students advised by PI on solar energy related research
3. Students enrolled in courses that have enhanced solar content as a result of DISTANCE grant

4. Students enrolled in our partner institution, St. Philip's College, Alamo Community Colleges

Table 7 summarizes the student jobs/internships. Met minimum target of 8.

Table: 7 Student Jobs/Internships

Name	BS/MS/PHD	Graduation	Current Position/Company
Student 1	PhD	Summer 16	Post-Doc at Sandia National Labs
Student 2	BS	Fall 16	UG internship with electric utility company in Brownsville, Texas
Student 3	MS	Spring 16	Actively looking for opportunities
Student 4	MS	Spring 16	Actively looking for opportunities
Student 5	MS	Fall 15	PowerFin, Solar Company
Student 6	BS	Spring 15	Engineering Consultant
Student 7	MS	Spring 15	EcoJiva, Solar Company
Student 8	BS	Spring 15	CPS Energy
Student 9	MS	Spring 15	Zachry Group
Student 10	MS	Spring 15	ERCOT
Student 11	BS	Fall 14	Zachry Group

Another target metric for this task is to meet a minimum of 20 students directly and indirectly supported through the DISTINCT project. Table 8 gives a list of 21 students. The total number of current/past students supported through this grant stands at 21, with a target metric of 20. The student from UT El Paso, Student 17, who joined the group for summer 2015 research experience, was supported through NSF fellowship, but still contributed to the DOE project as part of student's undergraduate research experience. If this student is also counted, the total number is 22. Details are given in Table 8.

Table: 8 Students in DISTINCT Project

Name	MS / Ph.D	Graduated (Defense Date)	Current Position	Type of Support Direct vs Indirect and corresponding details
Student 1	MS	4/15/14	PhD Student	Direct - Research Assistantship
Student 2	MS	4/17/14	PhD Student	Direct - Research Assistantship
Student 3	BS	12/31/14	MS student	Direct - Research Assistantship
Student 4	BS	5/31/15	Engineering Consulting Company	Direct - Research Assistantship - Undergraduate

Student 5	BS	5/31/15	Engineer, Zachry Group	Direct - Research Assistantship - Undergraduate
Student 6	MS	5/31/15	Engineer, Zachry Group	Direct - Research Assistantship
Student 7	MS	5/31/15	Engineer, ERCOT	Indirect - PI is thesis advisor - Student supported through another project. But thesis focuses on solar forecasting
Student 8	PhD	4/30/16	Engineering Consulting Company	Direct - Research Assistantship
Student 9	PhD	7/29/16	Post-Doc Sandia National Labs	Direct - Research Assistantship
Student 10	PhD		PhD Student	Direct - Research Assistantship
Student 11	MS	4/30/16	Looking for opportunity	Direct - Research Assistantship - Undergraduate and Graduate
Student 12	MS	4/30/16	Looking for opportunity	Direct - Research Assistantship
Student 13	BS	12/31/15	Engineering Firm	Direct - Research Assistantship - Undergraduate
Student 14	BS	5/31/16	Caterpillar Inc	Direct - Research Assistantship
Student 15	MS	11/15/16	Solar company - start-up in San Antonio	Indirect - PI is thesis advisor - Student did a project on Soft costs with local solar company
Student 16	BS		UG student	Direct - Student wanted to work in PI's lab to understand solar research - Got an internship position at an utility company before giving UG research assistantship
Student 17	BS		UG student at UT El Paso	Indirect - Student came in from UT El Paso through NSF LSAMP program/fellowship and completed a LabView related project on N-port Converter
Student 18	AAS			Direct - Student assistantship
Student 19	AAS	Spring 2016	Sea World - Energy Efficiency program	Direct - Student assistantship
Student 20	AAS	Spring 2016	UTSA undergrad student	Direct - Student assistantship
Student 21	AAS			Direct - Student assistantship

The target technical metric on number of courses with solar content has been discussed under Task 4. The last target technical metric is the number of peer-reviewed publications (Target 8), which are listed below. The ones that are currently under peer review are also listed.

Project Publications

[P-1] M.A. Moonem; H. Krishnaswami; “Control and Configuration of Three-Level Dual-Active Bridge DC-DC Converter as a Front-End Interface for Photovoltaic System,” Applied Power Electronics Conference (APEC 2014), March 16-20, 2014, Dallas, TX

[P-2] M.A. Moonem; T. Duman; H. Krishnaswami; “Power converter configuration with integrated high-frequency transformer for high-voltage grid-connected large-scale photovoltaic system,” IEEE Photovoltaics Specialists Conference (PVSC-40), June 2014

[P-3] Moonem, M.A.; Pechacek, C.L.; Hernandez, R.; Krishnaswami, H. “Analysis of a Multilevel Dual Active Bridge (ML-DAB) DC-DC Converter Using Symmetric Modulation”. *Electronics* **2015**, *4*, 239-260.

[P-4] M A Moonem; R. Hernandez; T. Duman; and H. Krishnaswami; “Capacitor Voltage balancing in a Neutral-point Clamped Multilevel dc-dc Dual Active Bridge Converter,” DOE GEARED Workshop, NAPS 2015, Oct 4-6, 2015.

[P-5] S. Marti; M A Moonem; R. Hernandez; and H. Krishnaswami; “Implementation of Maximum Power Point Tracking Control Using NI myRIO-1900 for Multi-Level Dual-Active Bridge DC-DC Converter” DOE GEARED Workshop, NAPS 2015, Oct 4-6, 2015.

[P-6] T. Janssen and H. Krishnaswami; “Fault-Tolerant Control for a Modular Cascaded NPC Inverter Configuration,” Accepted for IEEE Workshop on Control and Modeling for Power Electronics, IEEE COMPEL 2016, 27-30 June 2016.

[P-7] T. Janssen and H. Krishnaswami; “Voltage and Current Control of a Multi-port NPC Inverter Configuration for a Grid-Connected Photovoltaic System,” Accepted for IEEE Workshop on Control and Modeling for Power Electronics, IEEE COMPEL 2016, 27-30 June 2016

Under Peer Review

[P-8] M.A. Moonem; S. Marti; A. Rifath and H. Krishnaswami, “A Modular Multilevel Converter with Power Mismatch Control for Grid-connected Photovoltaic System,” IEEE Transactions on Power Electronics.

[P-9] S. Marti and H. Krishnaswami, “Novel Control Algorithm for two-stage, N-port, String-Connected Modular Multilevel Cascaded Inverters,” Submitted for Texas Power and Energy Conference in 2017.

[P-10] T. Duman; M.A. Moonem and H. Krishnaswami, “Capacitor Voltage balancing in a Neutral-point Clamped Multilevel dc-dc Dual Active Bridge Converter,” Submitted for IEEE Power Electronics for Distributed Generation Conference in 2017.

Conclusions

The DISTINCT project research objective is to develop an innovative N-port power converter for a utility-scale PV system that is modular, compact and cost-effective and that will enable the integration of a high-frequency, high-voltage solid-state transformer. The novelty of the proposed research is the electrical power conversion architecture

using an N-port converter system that replaces the output 60Hz transformer with an integrated high-frequency low-weight solid-state transformer reducing power electronics and BOS costs to meet SunShot goals through modularity and direct high-voltage interconnection. The key results include modularity, grid performance, direct high voltage interconnection with no impact on THD, controller for handling port level power imbalance, automatic re-configurability, fault tolerance: N-1 redundancy, serviceability >25 years, 40% reduction in footprint and $0.13/W cheaper than conventional inverter. The functionalities and metrics have been validated in a low power laboratory prototype. The converter when scaled up to high power coupled with high efficiency magnetic materials and SiC Mosfets has the potential to exceed conventional inverter efficiency.

An integral part of this effort is to increase the diversity of students pursuing solar research, to enhance and expand the solar classroom experience and to provide extensive opportunities for solar research and internships with an expansive network of strategic partners locally, regionally and nationally. The project meets and exceeds assessments and target metrics on the various activities associated with the education task such as student participation, diversity, new solar content in courses, research opportunities, publications, student jobs and internships. Milestones and go/no-go decision points have been continuously monitored with quarterly conference calls with DOE and have been successfully met.

Budget and Schedule

The approved amount for Budget Period 1 is $372,135 and Budget Period 2 is $377,865. A total of $672,760 has been spent which is equivalent to approximately 90%. This is attributed to low spending in one category, contractual. The contractual agreement with St. Philip’s college was formally signed in Q4 2014 and there was a delay from SPC in recruiting and providing assistantships to students. However, this did not impact a lot on the schedule, since the main deliverables from SPC were student participation and cost calculations. At the end of the project, one student has transferred to UTSA undergraduate program and this project has now established a pipeline from community college to 4-year college, which will be leveraged in future. There has been little to no schedule slips in our program.

Path Forward

The DISTINCT project has established a solar curriculum at the College of Engineering with multiple courses and a research experience partnership network for student jobs/internships. Many students will continue to go through curriculum and some of those students undergraduate and graduate will pursue research in solar energy and renewable energy in general. Having established a pipeline of students from community college to 4-year college to graduate school, the DISTINCT efforts will continue to make

a significant impact on students. UTSA research lab is acquiring a powerful Real-time simulator OP 5600 along with power amplifier for PHIL testing. The N-port converter and the system level controller will continue to be validated “at scale” in a PHIL platform. This will provide significant results at scale to pursue technology transfer and commercialization. The N-port converter research will be expanded for other platforms such as microgrids and DOD forward deployment applications.

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