Low temperature spalling of silicon: A crack propagation study

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ABSTRACT — **Spalling is a promising kerfless method for cutting thin silicon wafers while doubling the yield of a silicon ingot. The main obstacle in this technology is the high total thickness variation of the spalled wafers, often as high as 100% of the wafer thickness. It has been suggested before that a strong correlation exists between low crack velocities and a smooth surface, but this correlation has never been shown during a spalling process in silicon. The reason lies in the challenge associated to measuring such velocities. In this contribution, we present a new approach to assess, in real time, the crack velocity as it propagates during a low temperature spalling process. Understanding the relationship between crack velocity and surface roughness during spalling can pave the way to attain full control on the surface quality of the spalled wafer.**

***Index Terms* — Spalling, silicon, kerfless, wafering, crack velocity**

I. INTRODUCTION

The goal of kerfless technologies is to develop new methods for cutting silicon that eliminates slurry and wires while doubling the yield of a silicon ingot. One of the challenges is to do so repeatedly through the ingot without losses in lifetime. Spalling has been shown to be a promising technology, which capitalizes on the crystalline and mechanical properties of silicon. However, previous implementations of this technology, especially those using high temperature with metal foils, carry several challenges for PV application [1]. In some cases, the substrate needs to be heated to temperatures higher than 600˚C in order to sufficiently activate the spalling mechanism that kicks in upon the subsequent cooling [2], [3]. This range of temperatures combined with the presence of metals from the stressor layers substantially degrades the electronic properties of the substrate.

The only way to avoid this degradation is to perform the spalling at lower temperatures (<150˚C) but even experiments performed at these temperatures show poor wafer performance [4]. The main cause for this low performance is that the surface of the cleaved wafers is not smooth enough and often present a total thickness variation as high as 100% of the wafer thickness [5].

The root cause of this issue relies on the velocity at which the crack propagates during spalling. At high velocities, typical of spontaneous spalling, the crack becomes unstable. This instability leads to critical variations in the crack trajectory with a consequent branching and corrugation of the surface [6].

The high velocities add another problem; when the crack propagates above a certain range of velocities, it emits a wave [7]. This emitted wave then reaches the edges of the sample and reflects back into the material, interfering with the crack tip, causing substantial ripples on the surface [8]. This process can drastically change the velocity and the direction of the propagating crack and, thus, the uniformity of the cleaved surface.

A clear correlation between surface roughness and crack velocity was presented by Arakawa during a study on brittle polymers [9]. What is more, he demonstrated experimentally, that the roughness of a cleaved wafer depends on the product of the crack velocity and the stress state at the crack tip, also known as the stress intensity factor, *K*. This *K-value* depends mainly on the material, the sample geometry, and the applied load to the system.

By controlling the loading conditions, the roughness of the spalled wafer can be confined. In order to do so, a greater understanding of the crack velocity and dynamics must be achieved. However, while crack velocities have been measured during traditional tension tests, no reliable method to measure the crack propagation velocity for spalling of silicon substrates has ever been presented. In the following paper, we report on a novel method to measure in real time the velocity of a dynamic crack during spalling of silicon wafers.

II. BACKGROUND

In fracture mechanics, several measurement techniques have been developed to measure crack velocities for a range of materials during tension tests. In general, three different techniques have been implemented to obtain the valuable information of a crack's velocity:

(a) A common technique takes advantage of the interaction of the crack and its front waves after the crack has propagated fully through the material. This interaction locally induces a perturbation causing the crack front to curve, called Wallner lines. From a geometry analysis, the crack velocity can be calculated for different points in the material [10]. The complexity of observing and differentiating the crack front from the Wallner lines in rough surfaces, as those produced in spalling, makes this technique highly non-reliable.

(b) A second method is high-speed photography. As seen by Bellanger *et al*. this technique has several limitations on obtaining information about the crack tip during spalling [4]. The cameras cannot determine the exact initiation time of the crack propagation and cannot precisely provide information of the crack position with time, something crucial to establish a correlation with roughness.

(c) Finally, the potential drop technique has been a successful way used to calculate the crack velocity during tension tests in insulating and conductive materials [11]–[13]. A strip of a thin conductive layer is coated along the predicted crack path. After fracture initiation in a pre-made notch, a dynamic crack will break the resistive coating thereby varying the sample's resistance as shown in Fig. 1 redrawn based on Fineberg *et al.* [13]. The instantaneous resistance of the conductive layer is calculated by measuring the voltage drop across it.

With this system geometry, a nearly linear relation between the crack length and the resistance of the coated plate can be obtained. This method requires a conductive strip along the predicted crack path, and for current spalling methods this would be extremely complicated, as the strip and electrodes needed to measure the voltage drop would have to be applied on the side of the entire thin substrate (~700μm).

In this paper, we revolutionize the concept of the potential drop technique to facilitate the measurement during spalling of conductor substrates. The modification overcomes the difficulty associated with the geometric constraints of the low temperature spalling setup and it allows, for the first time, to track the position and velocity of a dynamic crack with high spatial and temporal resolution during initiation, propagation and arrest. We refer to this technique as "In-plane Crack Dynamics" (ICD).

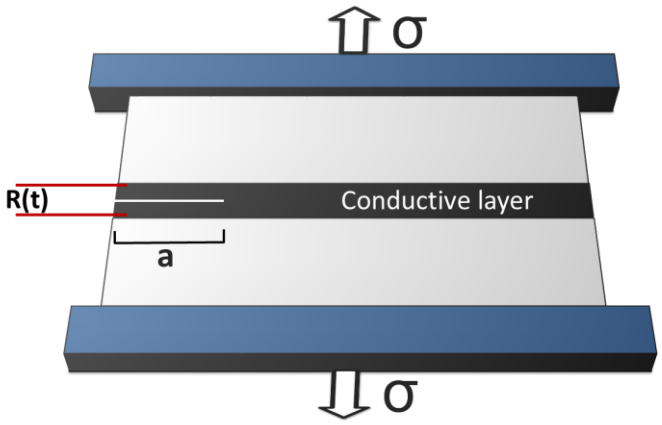

Figure 1. Schematic view of a traditional voltage drop technique system in a tension test with an applied load σ, crack length a, and the resistance of the material $R(t)$. Redrawn based on Fineberg *et al.*[13]

III. In-plane Crack Dynamics

The main characteristic in the traditional potential drop techniques is the conductor strip located at the top, bottom or side of the substrate that is ruptured during fracture. As the fracture advances, the resistance of the strip changes, and provides exact information on the position and speed of the crack. However, for any spalling technique in silicon or any other brittle material, a stressor layer is bonded to the bottom of a thin substrate through deposition or epoxy [14]–[16]. Thus, it is not possible to successfully use the bottom or side of the substrate to deposit the conductive strip. However, the benefit of using a semiconductor as silicon allows the implementation of a more advantageous configuration.

In this novel ICD technique, two electrode strips made of silver are deposited by thermal evaporation at 10^{-7} Torr on the surface of the silicon substrate, separated by 5mm, with a thickness of approximately 200nm. A low silver strip to substrate thickness ratio is important to assure that the silver strips do not affect the spalling process.

The silver strips are then connected to a Wheatstone bridge as shown in Fig.2. The Wheatstone bridge is powered by batteries for noise reduction in the measurements with a voltage V_{in} applied. The voltage output of the bridge (V_b) is digitized at a rate of 2 MHz by a PXIe 12-bit Analog to Digital converter from National Instruments. The resistance of the substrate between electrodes, R_x, is obtained by measuring V_b, and using the known values for the bridge resistors R_a, R_b, R_c and V_{in} following Eq. 1.

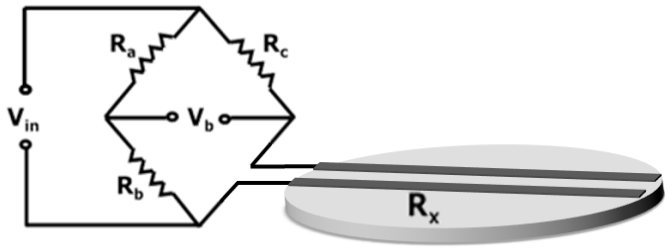

Figure 2. The diagram shows the system composed by the Wheatstone bridge and silicon substrate with two silver strips deposited on top as electrodes. It consists of three known resistors (R_a,R_b,R_c), a silicon substrate with resistance R_x, a battery (V_{in}) and the measured voltage output of the bridge (V_b).

$$R_x = \frac{\frac{R_b}{R_a + R_b} + \frac{V_b}{V_{in}}}{1 - \left(\frac{R_b}{R_a + R_b} + \frac{V_b}{V_{in}}\right)} \cdot R_c \qquad (1)$$

The resistance R_x is a function of the crack length and is sensitive to the geometry of the silver strips and the substrate. The relations are explained in the following:

The resistance, R_x, across the two metal strips depends on three factors, the resistivity of the substrate, ρ, the distance between both metal strips, d, and the cross sectional area, A,

$$R_x = \frac{\rho \cdot d}{A} = \frac{\rho \cdot d}{L \cdot T} \tag{2}$$

where A can be expressed as product of the length of the strips, L and the thickness of the wafer, T, as seen in Fig.3.

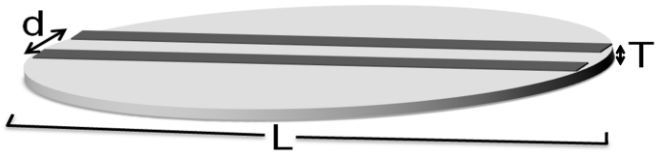

Figure 3. Schematic of the silicon substrate with the most relevant dimensions.

As the crack propagates from a pre-made notch on the side of the substrate, the thickness of the measured substrate varies as depicted in Fig. 4. When the crack is propagating, there are two distinct sections that contribute to the resistance between the strips; one related to the section that has been spalled and; one other section that has not been spalled yet. The spalled section of the substrate will have a thickness $t = T\text{-}w$, where T is the entire substrate thickness and w the thickness of the final spalled wafer. The length of the spalled section, $a(t)$, is time-dependent and defined by the position of the crack front.

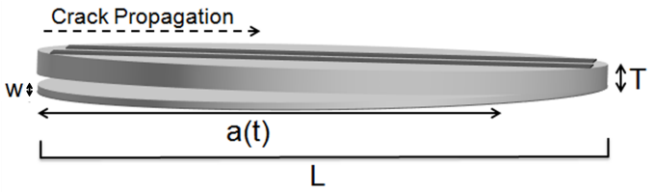

Figure 4. Schematics of system configuration as the crack propagates from left to right.

The un-spalled part of the substrate has a thickness, T, and a time-dependent length of $l(t) = L - a(t)$. Therefore, the resistance of the substrate changes with time following the equation:

$$R_x(t) = \rho d \left(\frac{1}{a(t)(T-w) + \big(L - a(t)\big)T} \right) \tag{3}$$

Rearranging this equation, the crack length is:

$$a(t) = \frac{1}{w}\left(LT - \frac{\rho d}{R_x(t)} \right) \tag{4}$$

Thus, by simply differentiating the crack position data for every point in time, the crack velocity can be calculated at any point in distance or time.

Using this methodology to investigate the crack propagation velocity we would typically observe that the velocity profile would start at zero as long as the stress field at the crack tip, K, is below a critical value, K_{IC} [17]. Once the crack starts propagating, the velocity will increase abruptly and, after that, the crack could keep accelerating, slow down or arrest if the stress field at the tip is below the critical value, K_{IC}. In Fig. 5 we show preliminary data of the crack position and velocity versus time using In-plane Crack Dynamics technique.

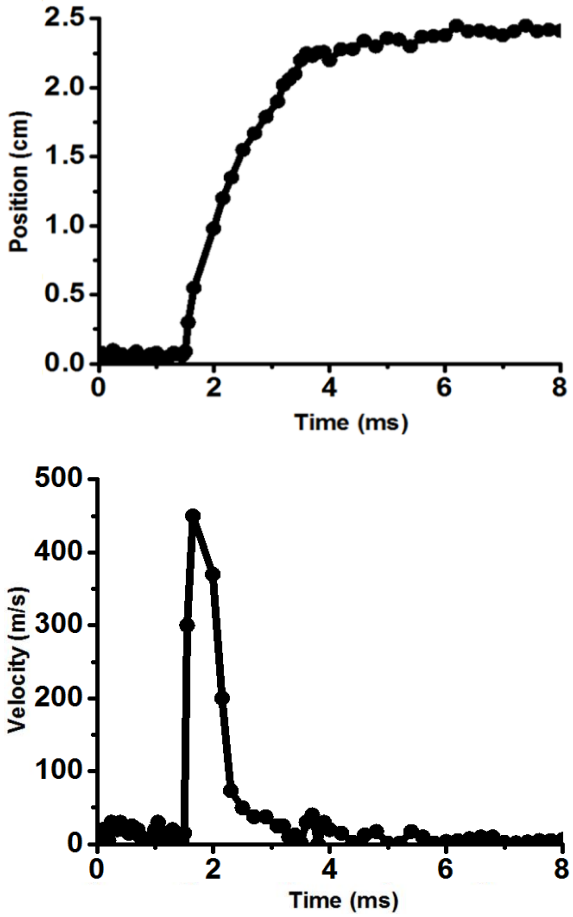

Figure 5. Illustration of position and velocity calculation for a crack during spalling. The graph ranges are approximate but representative for the measurement setup.

The correlation of this crack velocity to the stress applied to the system and to the surface roughness of the spalled wafer is ongoing work and will be presented in a future report. These new insights into the dynamics of propagating cracks are crucial for the further understanding of the relationship between surface quality and crack velocity, with the ultimate goal of being able to control crack motion to achieve a desired roughness.

IV. Conclusion

In this paper, we have introduced a new technique for measuring the velocity of a propagating crack during spalling denominated "In-plane Crack Dynamics" (ICD).

To the best of our knowledge, this technique is the first one capable to provide a direct measurement of crack velocity during the spalling of silicon wafers or any other semiconductor or conductor material. The developed technique grants full information on the entire fracture process, including initiation, spalling, and arrest with high spatial and temporal precision.

One of the main issues with spalling is the control of the crack propagation and the resulting poor surface quality of the spalled wafers. This new technique enables the collection of significantly more information collected about the crack velocity and in overcoming the main barrier of spalling, this new crack measurement technique plays a key role in gaining full control over the crack dynamics and surface roughness.

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