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# Tunable nitride Josephson junctions

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# Tunable Nitride Josephson Junctions

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## Abstract

We have developed an ambient temperature, $SiO_2$/Si wafer-scale process for Josephson junctions based on Nb electrodes and $Ta_xN$ barriers with tunable electronic properties. The films are fabricated by magnetron sputtering. The electronic properties of the $Ta_xN$ barriers are controlled by adjusting the nitrogen flow during sputtering. This technology offers a scalable alternative to the more traditional junctions based on $AlO_x$ barriers for low-power, high-performance computing.

## ACKNOWLEDGMENTS

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## FIGURES

## 1. INTRODUCTION

Recent interest in compact, high performance, low- power dissipation computing is driving a resurgence in superconducting electronics research [1]. Remarkable progress towards the development of a VLSI technology based on Nb/Al-AlOx/Nb Josephson junctions (JJs) has been made in the last few years [2,3]. The requirements for this technology to ultimately become viable include the ability to fabricate scalable, high-density logic circuits integrated with memory cells on large wafers, while maintaining precise control and reproducibility of individual component characteristics. Although extremely promising results have been demonstrated to date, the ability of the thin aluminum oxide barrier layer to continue to meet performance margins upon scaling to smaller node sizes and three-dimensional integration is unknown.

Junction technologies based on nitrides [4-22] may offer a promising alternative. The relative stability of nitrides at high temperatures and the ability to tune the electronic properties of barrier layers such as $Ta_xN$ [7, 8, 10-12, 14] in the formation of proximity SNS junctions may allow greater flexibility in fabrication and design constraints upon scaling. Although several groups have demonstrated high-quality SNS junctions, most have been grown at high temperatures and/or on MgO substrates. This work builds upon these previous studies to develop the technology needed for large wafer-scale junctions with $Ta_xN$ barriers grown at ambient temperatures on $SiO_2$/Si substrates.

## 2. APPROACH

Film growth was optimized in order to obtain high critical temperature (for the superconducting electrodes), single phase, and minimum surface roughness using both dc magnetron sputtering (MS) and pulsed laser deposition (PLD). Initially, NbN films for the superconducting electrodes were investigated in order to achieve all-nitride JJs. Variation in the $N_2$ gas flow during growth allowed the electronic properties of the $Ta_xN$ films to be tuned from superconducting to insulating at low temperatures. Oxidation of the NbN surface upon exposure to air showed oxygen ingress beyond a passive surface layer, consistent with the presence of voids. Further details are available in references [22,23]. Subsequent cross-sectional images of MS NbN/$Ta_xN$/NbN junctions by scanning transmission electron microscopy (STEM) revealed the presence of porous, columnar NbN grains with peak to valley roughness of 10 nm. Since the $Ta_xN$ junction barrier thickness is of this same order, smoother MS Nb electrodes were employed in place of NbN.

Microfabrication processes were developed to enable junction fabrication by MS on 150 mm $SiO_2$/Si substrates. Nb/$Ta_xN$/Nb trilayers were grown on the ambient temperature substrate without breaking vacuum, where deposition conditions for Nb have been previously described [24] and Ta was sputtered in a gas mixture of 15 sccm Ar, with $N_2$ flow varying from 4 to 16 sccm, in order to vary the Ta:N ratio and control the JJ electronic properties. In order to further control the coupling between superconducting electrodes, the $Ta_xN$ thickness was varied from 10 to 40 nm. Standard photolithography was used to define the junction area and wiring layers. The trilayer was etched to define the lower electrode wiring layer and individual JJ mesa structures using an inductively coupled plasma reactive ion etch in a 15 mTorr gas mixture of $SF_6$, $C_4F_8$, and Ar. An $SiO_2$ dielectric for electrical isolation of the top wiring layer was then deposited by plasma enhanced chemical vapor deposition at 250°C. Chemical mechanical polishing

allowed planarization of the entire wafer. Electrical contact to the top electrode was achieved by removing any oxide residue at the top of the mesa using a capactively coupled Ar ion etch. Nb was then deposited and etched to define the wiring to the top electrode. Ti/Au contact pads were evaporated and patterned by lift-off.

Characterization of the junction electrical properties was performed by probing four-point contacts across the entire wafer at room temperature. Low-temperature measurements were obtained by wire-bonding to individual die and either dipping into liquid helium on a probe with an integrated magnet or cooling in a temperature controlled cryostat.

## 3. RESULTS

Four-point, ambient temperature measurements of the junction resistance were uniform for devices within the central 75 mm of a wafer, with higher values at the edges. This result would be expected when using a 3 in. sputtering target, where N incorporation into the film will depend upon the local concentration of $N_2$ ions. Die for low-temperature characterization were therefore selected near the center of the wafer so that a clear dependence of properties on $N_2$ flow during growth and $Ta_xN$ thickness could be compared from wafer to wafer.

Early results from low temperature, four-point measurements on serpentine structures indicated a varying and reduced critical current of the lower Nb wiring layer. This was hypothesized to result from non-uniform reactive ion etching of that layer. A thin Al etch-stop layer [25], several nm below the surface of the lower Nb base electrode/wiring layer, was incorporated during the trilayer growth, resulting in significantly higher and more uniform critical currents.

Junctions grown with thin $Ta_xN$ barriers using low $N_2$ flow rates did not show Josephson behavior, but simply switched to the the normal state, indicating that the $Ta_xN$ barrier was superconducting, and the switch occurred upon reaching the $Ta_xN$ critical current. Josephson behavior was observed for 15 nm $Ta_xN$ barriers, grown with $N_2$ flow rates of of 12-14 sccm, as shown in Figure 1a for a 4 $\mu$m diameter junction. The critical current is reduced as the $N_2$ flow increases, indicating reduced proximity coupling for higher $N_2$ content $Ta_xN$. The critical current ($I_c$) and resistance ($R_n$) were observed to scale with junction area as shown in Figure 2, where red data points correspond to $I_c$ (left axis) and blue data points correspond to $R_n$ (right axis) for junctions with a 15 nm $Ta_xN$ barrier grown with a 13 sccm $N_2$ flow. The inset of Figure 1b shows the $I_cR_n$ product as a function of junction area, where values between 180-280 $\mu$V are observed. As is evident from this plot, where the $I_cR_n$ product should be independent of area, outliers are observed. Modulation of the junction critical current in an applied magnetic field is shown in Figure 3 for the 10 $\mu$m diameter junction discussed in Figure 2. Field modulation is clearly observed, although only the first lobe of the Fraunhoffer pattern is apparent.

The temperature dependence of the junction properties are shown in Figure 4 for a 12 $\mu$m diameter junction with a 15 nm thick $Ta_xN$ barrier grown with 12 sccm $N_2$ flow. Fig. 4a shows the current-voltage characteristics as a function of temperature and Fig. 4b shows the temperature dependence of the critical current. Above 8.7K, the critical temperature of the Nb electrodes, the junction critical current is zero. It rises up to a maximum of 0.68 mA with an apparent exponential dependence, although more data points would be needed for verification.

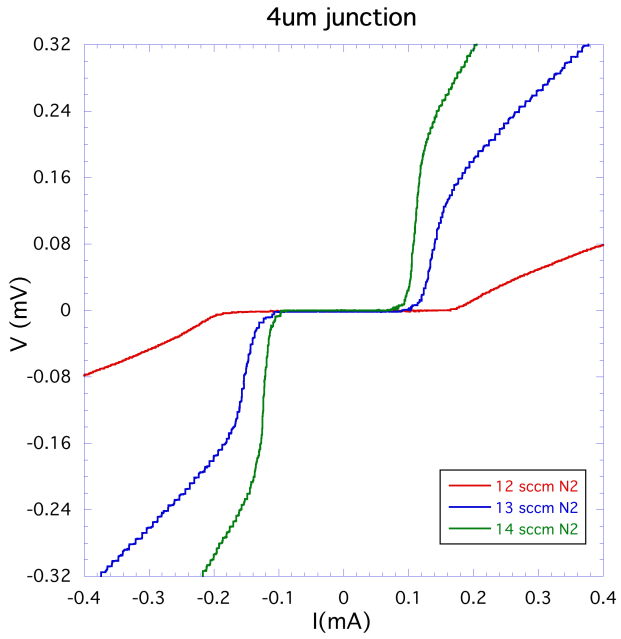


**Figure 1. Current-Voltage characteristics at 4K for 4 $\mu$m junctions as a function of nitrogen flow during 15 nm $Ta_xN$ barrier growth: 12 sccm red, 13 sccm blue, 14 sccm green.**

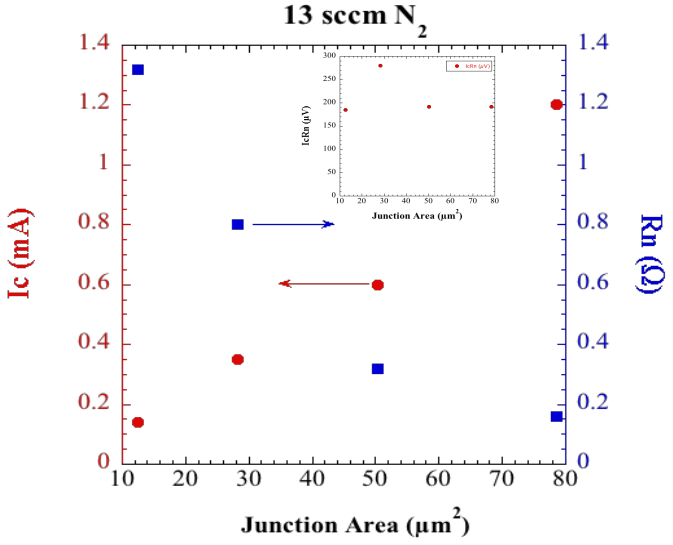


**Figure 2. Critical current (red circles, left axis) and normal resistance (blue squares, right axis) for 15 nm $Ta_xN$ junctions at 4K as a function of junction area for junctions grown with a nitrogen flow of 13 sccm. Inset shows $I_cR_n$ product as a function of area.**

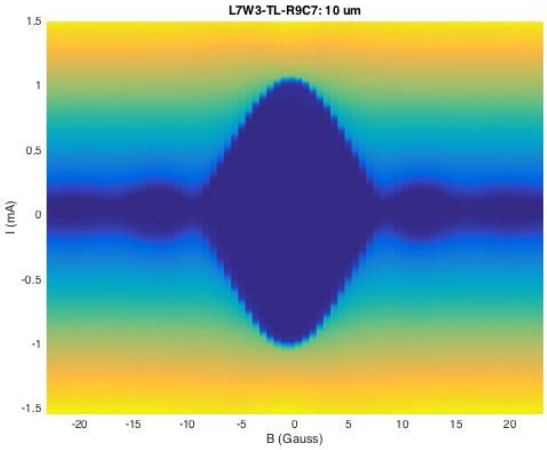


**Figure 3. Critical current at 4K as a function of applied magnetic field for a 10 $\mu$m diameter junction grown with a 15 nm $Ta_xN$ barrier with nitrogen flow of 13 sccm.**

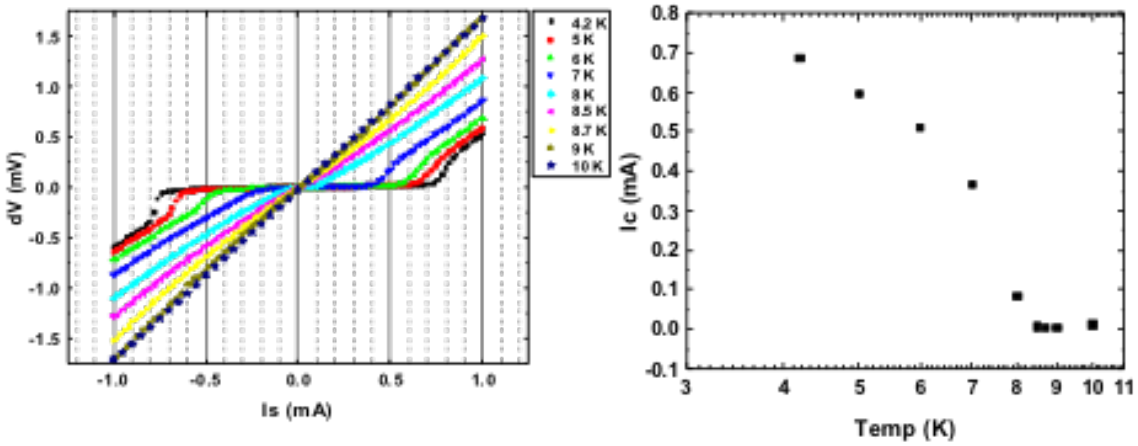


**Figure 4. Current-Voltage characteristics (left) and critical current as a function of temperature for a 12 $\mu$m diameter junction grown with a 15 nm $Ta_xN$ barrier with nitrogen flow of 12 sccm.**

## 4. CONCLUSIONS

These results demonstrate an alternative, scalable route for superconducting electronics technology. For the first time, a planarized, Nb/$Ta_xN$/Nb junction technology that employs ambient temperature growth on 150 mm $SiO_2$ wafers was developed. The ability to tune the junction properties by controlling the $N_2$ gas flow during $Ta_xN$ barrier deposition allows optimization for a variety of circuit applications. Future work will

explore routes to higher $I_cR_n$ products and improving the uniformity of junction properties.

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