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All-optical lithography process for contacting nanometer precision donor devices

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We describe an all-optical lithography process that can make electrical contact to nanometer-precision donor devices fabricated in silicon using scanning tunneling microscopy (STM). This is accomplished by implementing a cleaning procedure in the STM that allows the integration of metal alignment marks and ion-implanted contacts at the wafer level. Low-temperature transport measurements of a patterned device establish the viability of the process.

Keywords: Methods of micro- and nanofabrication and processing

The ability to fabricate devices with atomic precision holds promise for revealing the key physics underlying everything from quantum bits[1,2] to ultra-scaled digital circuits[3–7]. A known atomic-precision fabrication pathway uses a scanning tunneling microscope (STM) to create lithographic patterns on a hydrogen-passivated Si(100) surface[8]. Phosphine gas introduced into the vacuum system selectively adsorbs on sites where Si dangling bonds have been re-exposed by patterning[9], yielding atomically precise, planar structures made of P donors. Unlike electron beam lithography (EBL), which can pattern hydrogen with a resolution of around 100 nm and is unable to image the pattern[10], the STM is an ideal instrument for this process because it can both pattern and image the hydrogen resist with atomic precision[11]. However, STMs are typically only capable of patterning devices up to 10 μm by 10 μm in size, which is too small to directly contact. A post-patterning microfabrication process, consisting of etching via holes in an encapsulating Si overlayer and then depositing metal in direct contact with the planar donor layer, is used to make electrical contact to the devices. Even the largest features made with the STM are small enough that this contacting process relies on EBL for patterning and 200 nm- scale processing. At this scale, making good electrical contact between a deposited metal and an atomically-thin one-dimensional line of donors at the edge of an etched hole is challenging, and even successful EBL process flows in this application are rate-limiting.

In this paper, we detail an all-optical lithography contacting process that reduces the time of fabricating donor devices with the STM by an order of magnitude. This is made possible by the integration of both ion-implanted contacts and metal alignment marks in the starting material, which bridge the scale between the largest regions accessible by STM and the smallest length scale accessible by low-cost photolithography. Specifically, the ion-implanted contacts neck down to a small enough area that the STM can place the donor device in direct contact with them, and extend out to a region large enough that multiple photolithography steps done to a precision of 2 μm can connect the donor device to 200 μm sized metal pads. Directly fabricating donor structures on top of ion implanted Si simplifies the burden on microfabrication to that of making contact between deposited metal and an ion implanted region, which can be done with near perfect yield. Moreover, this entire contacting process can be executed in a single day using tools available in most clean-rooms, and can be run on multiple chips in parallel. Moving forward, the increased throughput of our reliable all-optical contacting process promises to dramatically reduce the cost of making new discoveries with the STM-based fabrication pathway.

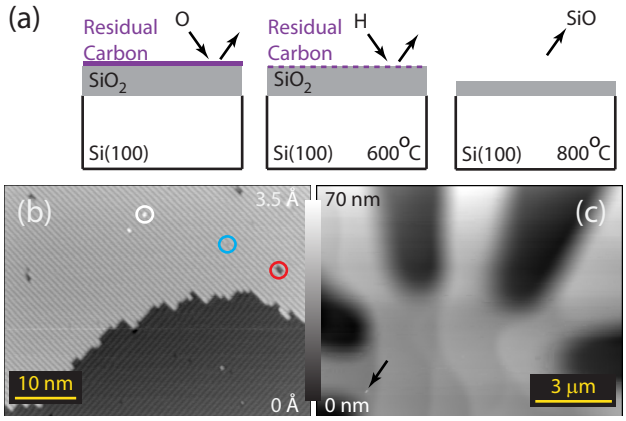

FIG. 1. (a) STM sample cleaning procedure, including oxygen plasma clean (left), atomic hydrogen clean (center), and oxide removal anneal (right). (b and c) STM topographs of a sample produced using the procedure in Fig. 2a, using this sample cleaning procedure in (a) followed by a hydrogen surface termination. These were taken at a sample bias of -2.5 V and junction setpoint of 200 pA. The atomic-scale image in (b) was taken approximately in the middle of the large-scale image in (c), a few hundred nm away from the trenches c. In (b), the white circle marks an unterminated silicon dimer, the blue circle a c-type defect, and the red circle a missing pair of dimers. In (c), the black arrow a SiC defect structure.

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The standard process for cleaning Si(100) samples for STM patterning[12] precludes the integration of metal alignment marks and ion implanted contacts, since the caustic chemical pre-cleaning *ex situ* and *in vacuo* annealing to 1200˚C would destroy them. As illustrated in Figure 1a, we have adopted a modified cleaning procedure and applied it to STM fabrication. All the Si(100) samples used in this work were first cleaned *ex situ* in an ultrasonic bath of acetone and isopropyl alcohol to remove remnant photoresist. An oxygen plasma clean at 100 W of power for 20 minutes removes most of the remaining hydrocarbon debris from the surface. After inserting the samples into the STM vacuum chamber, we degas the samples by heating them successively to 450˚C for 20 minutes and then 600˚C for 40 minutes. Subsequently exposing the samples to atomic hydrogen removes the remaining trace carbon on the surface, based on the process described in Ref. 13. In our implementation, a tungsten filament at 1700˚C in a background pressure of $5\text{x}10^{-6}$ torr hydrogen gas generates atomic hydrogen while the sample is heated to 600˚C for 20 minutes. We then heat the sample to a modest 800˚C to remove the surface oxide. Finally, we terminate the surface with atomic hydrogen by using the same tungsten filament, but with a pressure of $2\text{x}10^{-6}$ torr hydrogen gas, while holding the sample between 225-325˚C (we quote a range of temperatures because our thermometery is inaccurate, although highly reproducible, below 450˚C). The resultant surfaces are atomically clean on small length scales and show no contamination on larger length scales (Figures 1b,c).

This cleaning procedure enables the integration of ion-implanted contacts and metal alignment marks in the starting material, at the wafer level, as illustrated in Figure 2a. Alignment marks are first etched in the material, a p-type Si(100) wafer having a volume resistivity of 10-20 Ω cm and covered in 10 nm of sacrificial oxide (not shown). These etched alignment marks are used to align all photolithography steps prior to loading a chip in the STM. A photoresist mask is then used to perform a selective implant of As ions at 40 keV and an areal density of $3\text{x}10^{15}$ ions/cm^2. These ion-implanted contacts start from a 40 μm by 40 μm field, large enough for aligning subsequent photolithography steps, and neck down to an 8 μm by 8 μm field, small enough for the STM to contact directly. The resist is then stripped and the sacrificial oxide removed using HF, exposing a pristine surface. Following RCA1, RCA2 , and HF cleans[14], a 10 nm steam oxide is grown at 850˚C to protect the sample. Due to damage from the ion implantation, oxide grows at roughly 6 times the rate in implanted regions compared to pristine ones. The oxidation process is followed by a 15 minute anneal at 850˚C in nitrogen. A final photoresist mask is used to deposit tungsten alignment markers (Figure 2b). Unlike the etched alignment markers used up to this point, the tungsten alignment markers survive the thermal steps of the STM sample preperation proces. Critically for STM, this process produces atomically

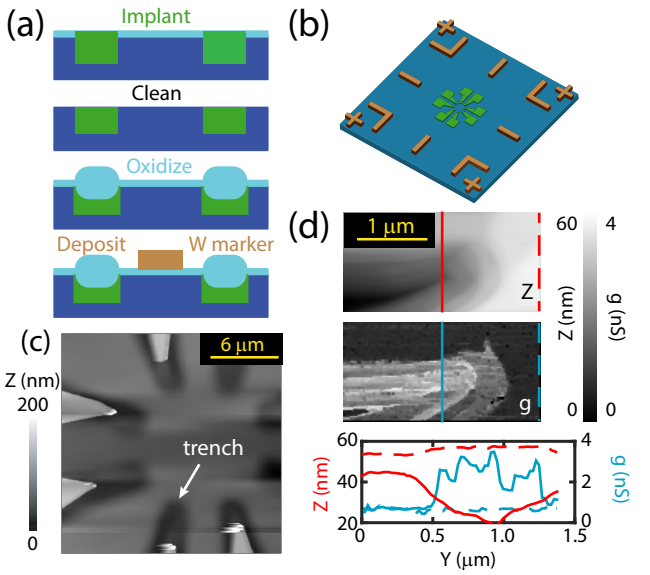

FIG. 2. (a) Side view of the process flow for integrating ion-implanted contacts and metal marks into the starting wafer. Here, Si is shown in blue, oxide in teal, implanted regions in green, and metal markers in brown. (b) Illustration of device fabrication process covering the 170 x 170 μm device area of the die, including the ion-implanted region (green) and the high contrast tungsten alignment markers (brown). (c) Atomic force microscope (AFM) topographic image of the implanted region of a chip after the sample preparation routine outlined in Figure 1, and a shorter 15 minute flash that only partially remove the thick oxide over the implants. The arrow points at the 30-60 nm trench that forms from the removal of the oxide. AFM imaging was performed *ex situ*, and is not part of the device fabrication workflow. (d) STM height (Z) and differential conductivity (g) data of the tip of a single ion implanted contact after a longer 30 minute flash that removes the thick oxide completely, producing a trench. Topographic data (Z) was taken with a sample bias of -1.5 V and tunnel junction setpoint of 800 pA. The differential conductivity (g) of the tunnel junction was recorded simultaneously using a lockin-amplifier at a frequency of 511 Hz and an ac excitation of 50 mV. The speckled areas are a noise artifact- they do not appear in both the forward-scanned and backward-scanned frames of the data (not shown). The bottom panel shows line cuts of the height (red) and differential conductivity (blue) through the middle of (solid) and outside of (dashed) the implanted region.

clean surfaces once the resultant chips are subjected to the sample clean outlined above (Figure 1b,c). By avoiding any acid-based cleaning, metal alignment marks are not damaged. Limiting the flash to 800˚C prevents any significant diffusion of the ion-implanted contacts. While ion-implanted contacts have been implemented before[15], the process flow relied on interdigitated implanted contacts across large regions of the chip, and is thus limited to simple two-terminal devices. No such limitations exist for the process flow we have implemented.

Flashing the sample to 800˚C for 5 minutes is sufficient to remove the 10 nm of surface oxide, but leaves

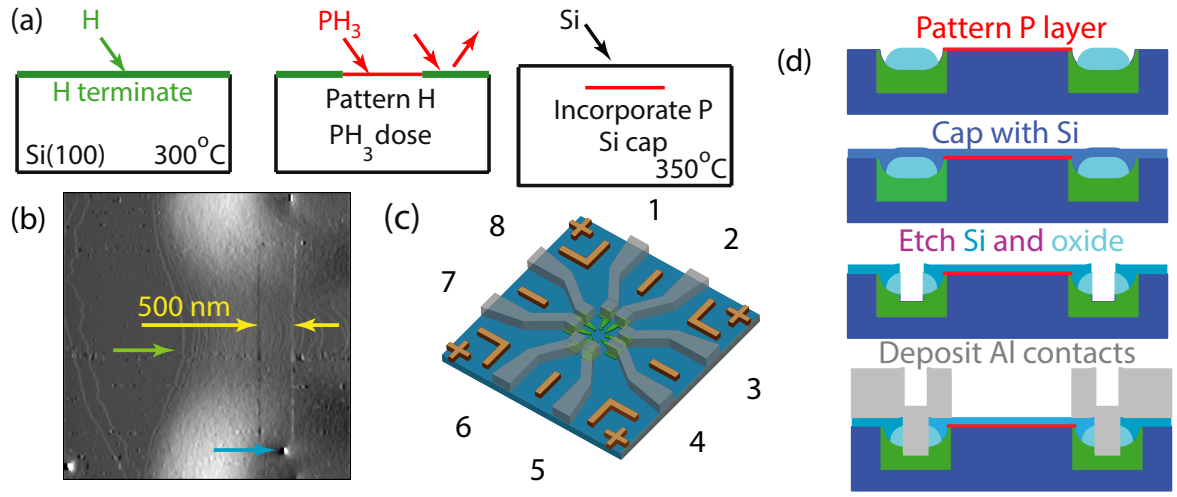

FIG. 3. (a) STM process flow, including hydrogen termination (green), phosphine exposure (red) and silicon capping. (b) STM image, taken with a sample bias of -3 V and tunnel junction setpoint of 200 pA, of a ∼2000 nm by 500 nm depassivated region. A Sobel filter has been used to enhance edge contrast. The green arrow points to a step edge, yellow arrows point out the depassivated region connecting contacts 3 and 4 (right-side, top and bottom in c), and the blue arrow to one of two SiC defects in the field of view. (c and d) Plan and cross-sectional view of the process used to make contact to the donor device. Here, Si is shown in blue, oxide in teal, implanted regions in green, metal markers in brown, the P donor device in red, and aluminum contacts in grey. We wire bond directly to the aluminum contacts.

the implanted contacts buried in oxide. Since STM cannot tunnel into a thick insulator, the sample must be flashed longer to remove the oxide over the implanted region, exposing the implanted silicon. Figure 2c shows a topographic image of a sample after it is flashed to 800°C for 15 minutes. Rather than a uniform reduction of all the thick oxide in the implanted region, the partial removal of the thick oxide proceeds from the edge of the implanted region. This leaves a 30-60 nm deep trench (arrow) that is easily identified by STM (Fig. 1c). Samples are typically flashed for 30 minutes to ensure that the oxide has retreated to the square pads far away from the region accessible to the STM, although it will still need to be accounted for during the electrical contacting process. Using only the high contrast metal markers and a high-resolution optical camera, we can align the tip precisely to the implanted contacts with sub 2 μm precision, with a single 10 μm STM topograph required after the optical alignment to locate all 8 implants. To determine whether the implanted dopants diffuse out of the implanted region, we have simultaneously acquired topographic and spectroscopic data using the STM in Figure 2d. This data indicates that there is a region inside the trench that has an enhanced tunneling density of states, corresponding to a high concentration of activated donors[16]. Moreover, this enhanced density of states is confined to the trench, indicating that As dopants have not diffused out from the implant region.

The STM tip can be aligned to the high contrast metal marks. Following this, hydrogen lithography can be used to make direct contact to the implanted contacts, which neck into a square that is 8 μm on a side. The samples are first terminated with atomic hydrogen, which serves as the monolayer resist for this process (Figure 3a). This hydrogen resist can both be imaged by STM at low junction biases (1-3 V), or removed at higher junction biases with either atomic precision (∼3-5 V, 10 nm/s tip speed) or more coarsely (∼7-10 V, 200 nm/s tip speed)[8,11,17]. In Figure 3b, we have patterned a 500 nm wide wire between two implanted contacts. The resultant exposed dangling bonds selectively adsorb phosphine when it is introduced into the chamber[9]. We apply a total dose of 15 L at a chamber pressure of $2\text{x}10^{-8}$ torr. A thermally activated surface decomposition reaction of the phosphine, at a temperature that leaves the hydrogen resist intact, results in P donors incorporated into the lattice at a density ranging between 17%[18] for the smallest windows (1 donor in a 3 dimer window) and 25% for large areas[19]. We perform the thermal incoporation of the P donors nominally at 250-350°C for 10 minutes, where the range comes from an uncertainty in thermometery, and not lack of reproducibility. This will result in a P nanowire connecting the two As implanted regions. To preserve the donor-based device, it is then encapsulated in Si deposited at a rate of 1 nm/s to a thickness of 30 nm, while continuing to hold the sample at the same temeprature. From sample preparation to encapsulation, fabricating a donor device that fans out to contact pads in a roughly 8 μm by 8 μm region takes about 12 hours, with the two most time-intensive parts being the initial STM scan to locate the implants (4 hours), and patterning of the coarse features (4 hours), which has been computer-automated[20]. This time is comparable to that taken by the EBL based process flow up to this point, but with an *in situ* STM

device-positioning scan replacing *ex situ* scanned probe methods of locating the already-patterned device[21–23].

The process of making electrical connection to the donor device now requires only optical lithography and standard clean-room microfabrication to put metal in direct contact with the eight ion-implanted contacts in a 40 μm by 40 μm area (Figure 3d). Etching down to the implanted Si is complicated by the material stack in that part of the sample, which starts with the Si capping layer, followed by oxide which was incompletely removed during the sample flashing process, and finally by the doped Si. Contacts are made by patterning 2 μm diameter vias with optical lithography followed by a reactive ion etch of the Si capping layer using CF_4 at 25°C. Next, the leads are patterned for a lift-off metal deposition. Immediately before metal deposition a relatively long, 90 s etch in 1:6 BOE (buffered oxide etch) is used to remove the remaining oxide in the vias over the ion-implanted regions. After depositing 150 nm of Al, by electron beam deposition, a standard metal lift-off process is used to complete the eight contacts that fan out into bond pads, shown schematically in Figure 3c. This process is simpler than the typical EBL-based process used to make electrical contacts because the only part of the device that is different chip-to-chip (the STM-patterned part) is now divorced from the contact-making process, which is identical chip-to-chip. In addition to increased efficiency from not needing a specialized tool (EBL), and not needing to make per-chip adjustments (new CAD patterns), this reduces the time for processing half a dozen chips in parallel to scarcely more than that required for processing one.

Electrical transport data on the simple nanowire device shown in Figure 3b establishes the validity of this approach to making donor devices (Figure 4). These measurements must be carried out below ∼50 K to freeze out the carriers in the substrate. At 4 K the only resistive elements in the path of the current are cables, the contacts to the 2D device layer, and the donor nanowire itself. The DC transport through the nanowire is Ohmic down to tens of micro-Volts, and gives a resistance of 5.6 kΩ. We also examine, in Figure 4b, the transport between contacts that are not connected by a patterned donor structure. These show less than 0.1 nA of leakage current between isolated contact pairs at 2 V of bias. Two control samples, one which saw the same thermal processing as our donor device but no phosphine dose, and a second one which was not subjected to any thermal processing, show similar levels of leakage current to one another. This indicates that the thermal budget of our process does not lead to enough As implant diffusion to be measurable. This also suggests that the additional leakage current between isolated contacts in the patterned sample originates largely from phosphine adsorbing through imperfections in the hydrogen resist. Both the Ohmic conduction through the nanowire, and the small leakage between unconnected pairs of contacts, compare well to an earlier effort which realized metal silicide contacts, but reported nonlinear I-V curves through

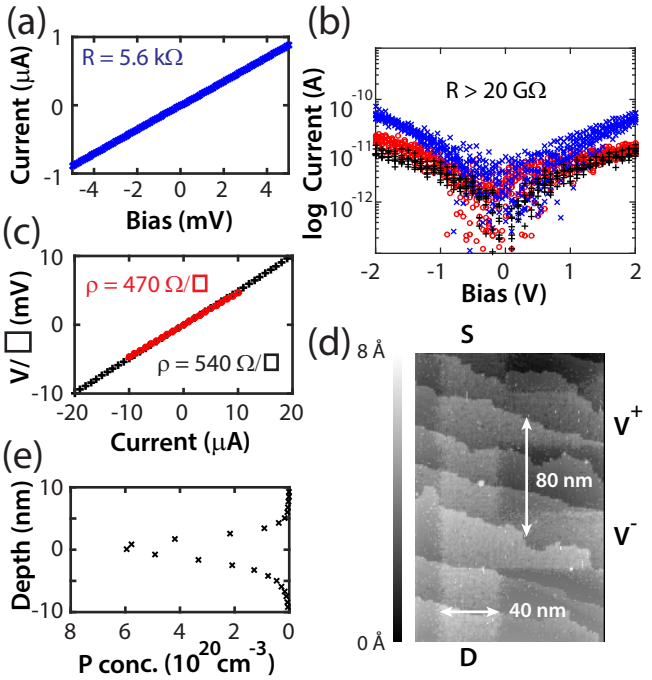

FIG. 4. (a) Current-voltage curve taken of the nanowire patterned in Figure 3b between contacts 3 and 4. (b) Current-voltage curves taken between all other contact pairs on the same chip (blue), which had no P nanostructure connecting them. Also shown are current-voltage curves from a chip processed in the same way, but not dosed with phosphine (red), and a third chip that was not subjected to any in-vacuum processing at all (black). All data were taken at 4 K by biasing a single contact and collecting the current on a neighboring contact while leaving the other contacts electrically floated. The absolute value of the current is plotted for negative biases. (c) Current-voltage curve taken of an etch-defined Hall bar fabricated on a delta-doped blank chip (red), and of an STM-patterned four-terminal nanowire (black), showing the four-terminal resistivity per square of the two structures. (d) STM topograph of just the active area of a four-terminal nanowire with a 40 nm wide source-drain channel and voltage contacts seperated by 80 nm. Topograph was taken with a sample bias of -2.5 V and tunnel junction setpoint of 200 pA. (e) A SIMS depth profile of the phosphorus concentration in a delta-doped blank chip capped with 50 nm of silicon; in this data, the sample's surface is located at +50 nm.

an Ag nanowire with much larger leakage between unconnected contacts.[24]

A key characteristic of our all-optical contacting scheme is that it reliably produces low-resistance contacts. To determine the resistance of the contacts themselves, we must subtract out the resistance of the phosphorus wire connecting the implants, itself the product of the resistivity of the phosphorus doped material and the number of squares connecting the implants (four). To determine the resistivity of the donor-doped material, we have fabricated an etch-defined Hall Bar having an 80 μm by 400 μm active area into a delta-doped sheet fabricated on a blank chip. A four-terminal measurement yields an

areal resistivity of 470Ω/□ (Fig. 4c), implying a contact resistance of 2 kΩ per contact for the device in Figure 3, which includes the metal-implant interface, the resistivity of the implanted region itself, and the implant-P interface. This method has produced a high yield of successful contacts; 12 contacts across five different chips have all shown comparably low contact resistances. The high yield can be attributed to two advantages of the scheme presented here. First, implanted contacts present an extended surface that deposited metal can come into contact with, including the bottom surface of the via holes, while in the EBL-based process flow, the metal needs to make a line contact to the two-dimensional phosphorus layer itself. Second, the size of the implanted region is large, permitting conventional microns-wide vias which are ten times wider than they are deep. Process stability plateaus are noticeably narrower with the high-aspect-ratio vias required by the EBL-based process flow, typically 100 - 200 nm wide and 50 - 100 nm deep.

Finally, we demonstrate that this process flow can be used to fabricate nanometer-scale structures. In Figure 4d, we have patterned a 40 nm wide, 80 nm long four-terminal nanowire using the STM in coarse-patterning mode (sample bias of 8.5 V, junction setpoint of 0.75 nA, tip speed of 175 nm/s). The electrical transport data from this STM-patterned nanowire, made on a chip with implanted contacts and metal markers, gives a resistivity of 540Ω/□ (Fig. 4c), which is comparable to that measured for the etch defined Hall bar made on a delta-doped chip with no implants or marks. Given the three orders of magnitude difference in wire size, and different scattering mechanisms that are relevant at these different length scales, this level of agreement is quite reasonable. Further, this process flow is compatible with making truly atomic precision devices. The silicon in the central region between the implants has defect densities comparable to pristine Si(100) (Fig. 1b). The STM could be used to perform hydrogen lithography more carefully, in atomic precision mode. Lastly, an advanced so-called locking layer method could be used for dopant incorporation and silicon capping in order to yield the sharpest dopant profiles in the vertical dimension[23,25], as opposed to the slightly broader profiles produced by the single-temperature capping approach we used here (Fig. 4e).

In conclusion, we have presented a new all-optical method for contacting nanometer-precision donor devices that takes a single day to execute, easily allows multiple chips to be processed in parallel, and achieves a high yield of successful contacts. This was made possible by adopting a process for cleaning Si(100) in an STM that is sufficiently low-temperature to allow for the integration of tungsten metal alignment markers and ion implanted contacts in the starting material. The fast processing time and high yield are expected to dramatically reduce the costs of developing new innovations with STM fabricated donor devices. In closing, we note that the entire process, with the notable exception of the STM-based parts, is CMOS compatible. While the process itself currently has no application impact without the STM-based parts, it opens the door to integration of some aspects of the STM pathway in the future.

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